

June 1994

Monolithic CMOS Analog Switches

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- ON-Resistance $<35\Omega$
- Low Power Consumption ($P_D <35\mu W$)
- Fast Switching Action
 - $t_{ON} <150ns$
 - $t_{OFF} <100ns$
- Low Charge Injection
- DG401/883 Dual SPST; Replaces HI-5041/883
- DG403/883 Dual SPDT; Replaces DG190/883B, IH5043/883B, IH5151/883B, HI-5051/883, HI-5043/883B
- DG405/883 Dual DPST; Replaces DG184/883B, HI-5045/883, IH5145/883B
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems

Description

The DG401/883, DG403/883 and DG405/883 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance ($<35\Omega$) and fast switch time ($t_{ON} <150ns$). Low charge injection simplifies sample and hold applications.

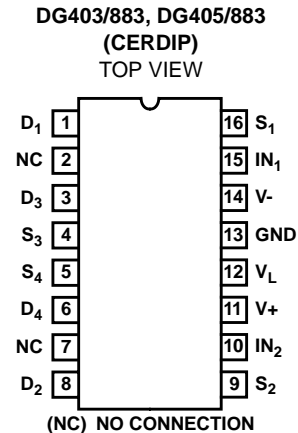
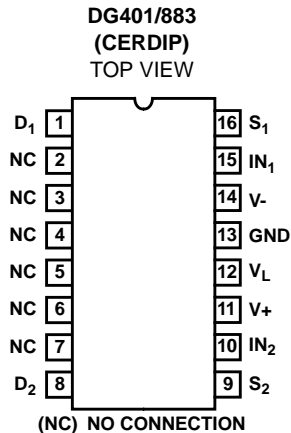
The improvements in the DG401/403/405/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from $\pm 5V$ to $\pm 17V$.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a $\pm 15V$ analog input range. The three different devices provide the equivalent of two SPST (DG401/883), two SPDT (DG403/883) or two DPST (DG405/883) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

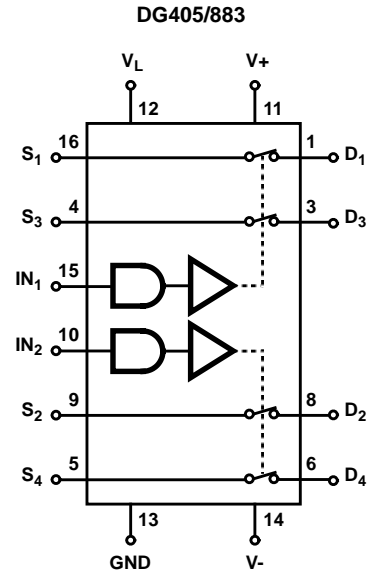
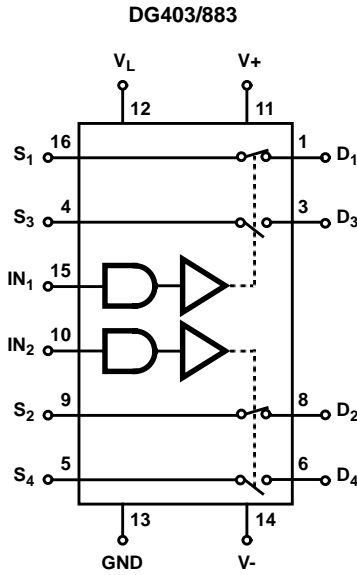
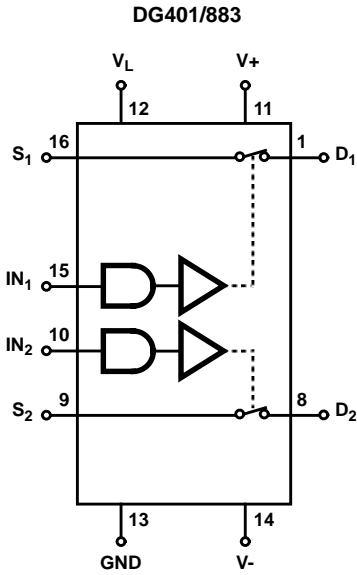
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG401AK/883	-55°C to +125°C	16 Lead CERDIP
DG403AK/883	-55°C to +125°C	16 Lead CERDIP
DG405AK/883	-55°C to +125°C	16 Lead CERDIP

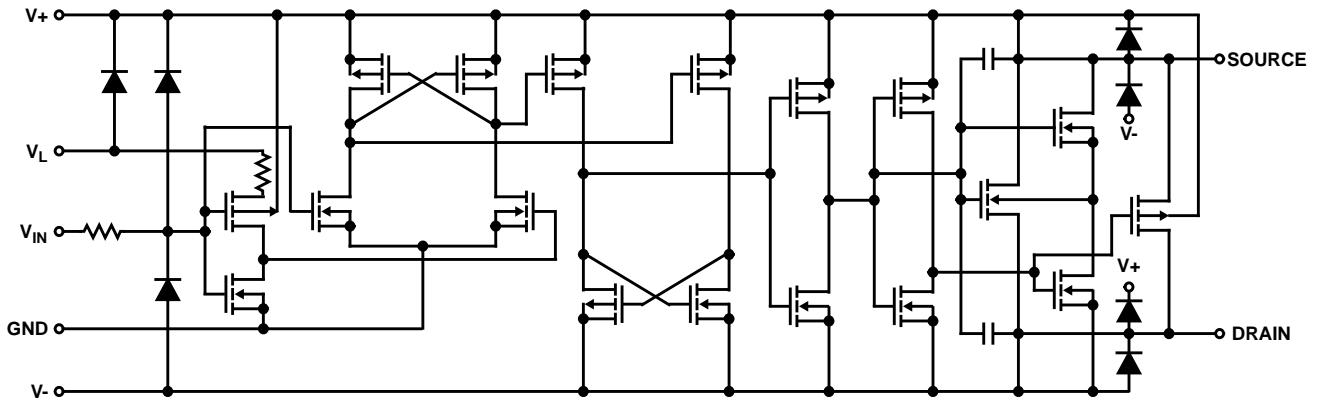
Pinouts



Functional Diagrams



Schematic Diagram



Truth Table

LOGIC	DG401/883	DG403/883		DG405/883
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" ≤ 0.8V. Logic "1" ≥ 2.4V.

Specifications DG401/883, DG403/883, DG405/883

Absolute Maximum Ratings

V+ to V-+44.0V
GND to V- 25V
V _L (GND - 0.3V) to (VC+) +0.3V
Digital Inputs (Note 1), V _S , V _D (V-) -2V to (V+) +2V or 30mA, Whichever Occurs First
Continuous (Any Terminal) Current, (Note 1)±30mA
Peak Current, S or D (Note 1)±100mA (Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (A Suffix) -65°C to +125°C
Lead Temperature (Soldering 10s) +300°C

Reliability Information

Thermal Resistance (Max)	θ_{JC}	θ_{JA}
CERDIP Package	18°C/W	75°C/W
Operating Temperature (A Suffix)-55°C to +125°C	
Junction Temperature (CerDIP) +175°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range±20V Max	Input High Voltage 2.4V Min
Operating Temperature Range -55°C to +125°C	Input Rise and Fall Time 20ns
Input Low Voltage 0.8V Max		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V, V- = -15V, V_L = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Drain-to-Source ON Resistance	R _{DS(ON)}	V+ = +13.5V, V- = -13.5V, I _S = -10mA, V _D = ±10V	1	+25°C	-	35	Ω
			2, 3	+125°C, -55°C	-	45	Ω
Delta Drain-to-Source ON Resistance	Delta R _{DS(ON)}	V+ = +16.5V, V- = -16.5V, I _S = -10mA, V _D = +5V, 0V, -5V	1	+25°C	-	3	Ω
			2, 3	+125°C, -55°C	-	5	Ω
Source OFF Leakage Current	I _{S(OFF)}	V+ = +16.5V, V- = -16.5V, V _S = -15.5V, V _D = +15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
		V+ = +16.5V, V- = -16.5V, V _S = +15.5V, V _D = -15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
Drain OFF Leakage Current	I _{D(OFF)}	V+ = +16.5V, V- = -16.5V, V _S = -15.5V, V _D = +15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
		V+ = +16.5V, V- = -16.5V, V _S = +15.5V, V _D = -15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
Channel ON Leakage Current	I _{D(ON)} + I _{S(ON)}	V+ = +16.5V, V- = -16.5V, V _S = V _D = ±15.5V	1	+25°C	-	±0.4	nA
			2	+125°C	-	±40	nA
Low Level Input Current	I _{IL}	V _{IN} Under Test = 0.8V, All Others = 2.4V	1, 2	+25°C, +125°C	-	±1.0	μA
High Level Input Current	I _{IH}	V _{IN} Under Test = 2.4V, All Others = 0.8V	1, 2	+25°C, +125°C	-	±1.0	μA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5V, V _{IN} = 0V or 5.0V	1	+25°C	-	+1.0	μA
			2, 3	+125°C, -55°C	-	+5.0	μA
Negative Supply Current	I-	V+ = +16.5V, V- = -16.5V, V _{IN} = 0V or 5.0V	1	+25°C	-	-1.0	μA
			2, 3	+125°C, -55°C	-	-5.0	μA
Logic Supply Current	I _L	V+ = +16.5V, V- = -16.5V, V _{IN} 0V or 5V	1	+25°C	-	+1.0	μA
			2, 3	+125°C, -55°C	-	+5.0	μA
Ground Current	I _{GND}	V+ = +16.5V, V- = -16.5V, V _{IN} 0V or 5V	1	+25°C	-	-1.0	μA
			2, 3	+125°C, -55°C	-	-5.0	μA

Specifications DG401/883, DG403/883, DG405/883

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn On Time	t_{ON}	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	-	150	ns
			10, 11	+125°C, -55°C	-	275	ns
Turn Off Time	t_{OFF}	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	-	100	ns
			10	+125°C	-	250	ns
			11	-55°C	-	175	ns
Break-Before-Make Time Delay (DG403 Only)	t_D	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	10	150	ns

NOTE:

1. Signals on S_X , D_X , or IN_X exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 3 Intentionally Left Blank.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

2150 μ m x 1720 μ m x 485 \pm 25 μ m

METALLIZATION:

Type: Si - Al

Thickness: 12k \AA \pm 1k \AA

GLASSIVATION:

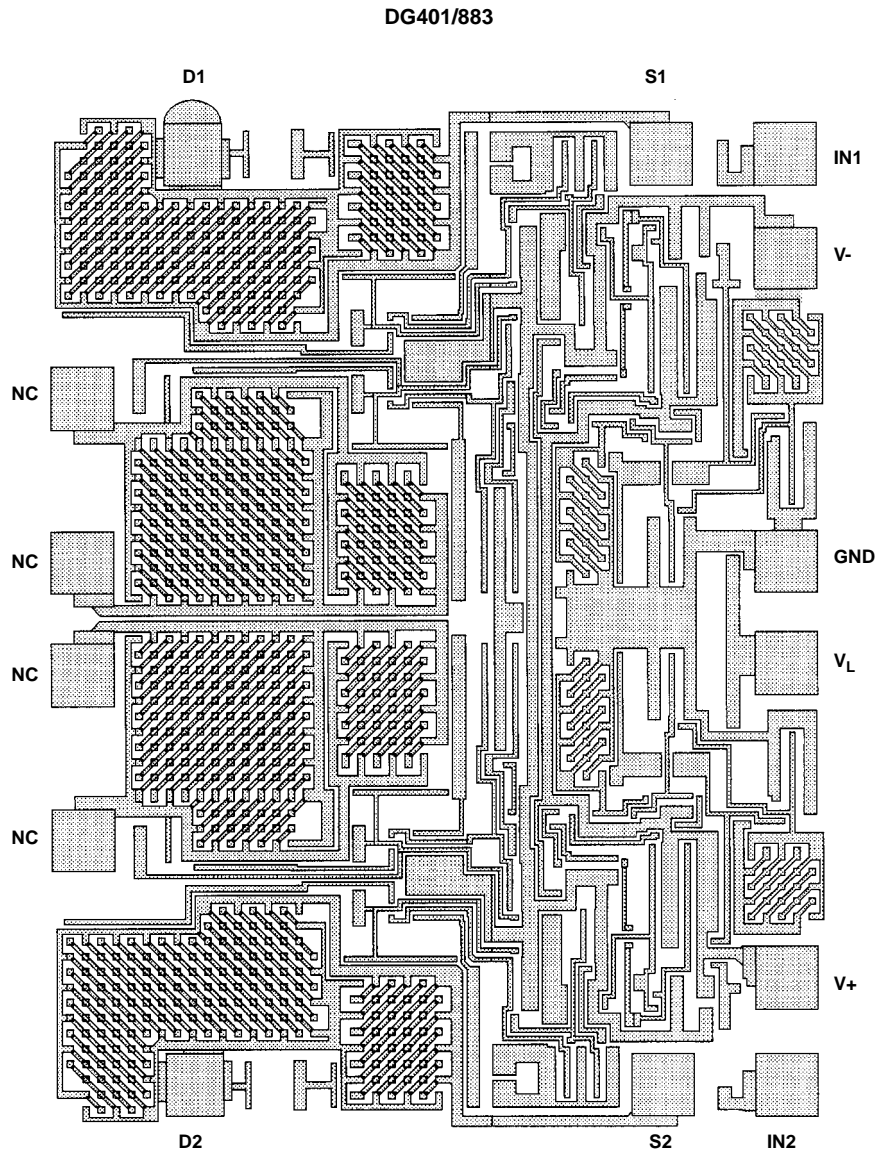
Type: Nitride

Thickness: 8k \AA \pm 1k \AA

WORST CASE CURRENT DENSITY:

1.5 x 10⁵A/cm²

Metallization Mask Layout



Die Characteristics

DIE DIMENSIONS:

2150 μ m x 1720 μ m x 485 \pm 25 μ m

METALLIZATION:

Type: Si - Al

Thickness: 12k \AA \pm 1k \AA

GLASSIVATION:

Type: Nitride

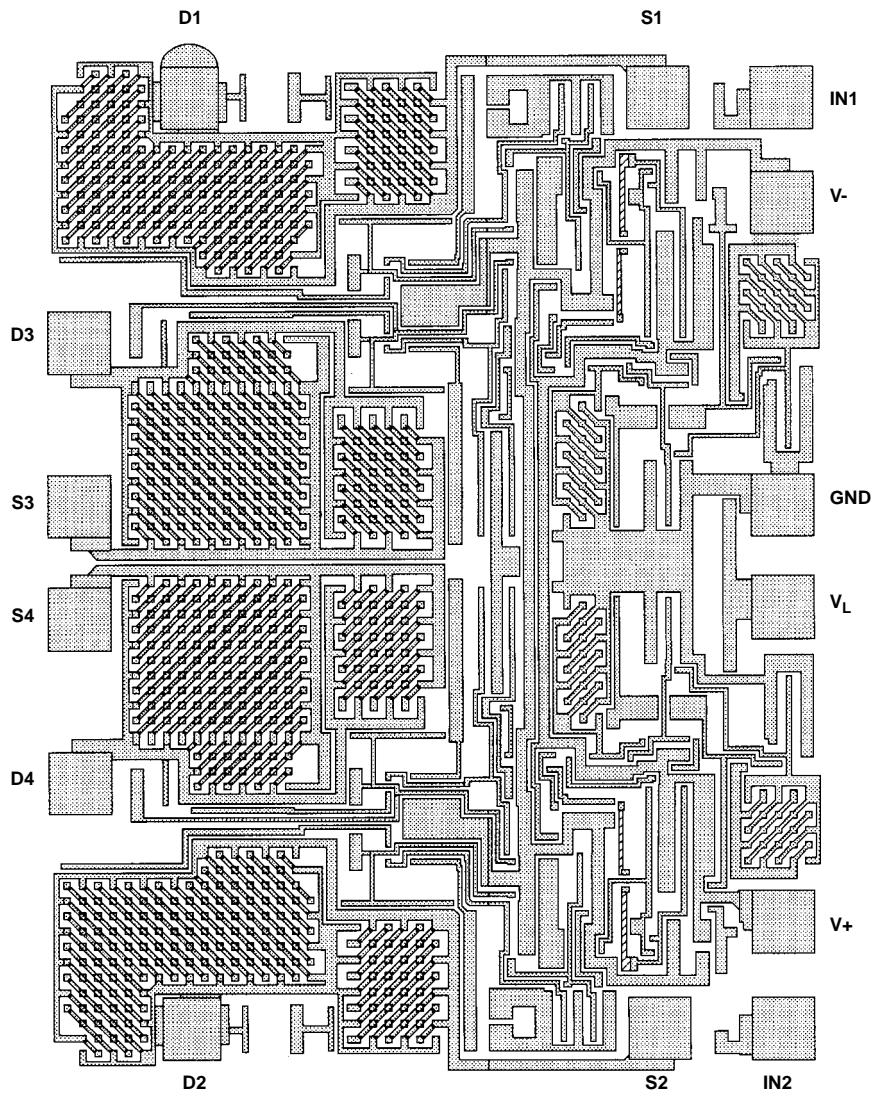
Thickness: 8k \AA \pm 1k \AA

WORST CASE CURRENT DENSITY:

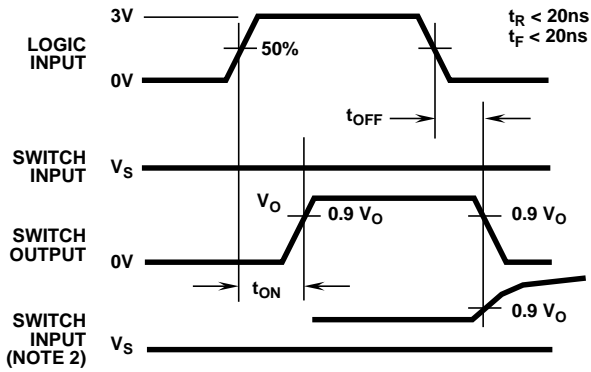
1.5 x 10⁵A/cm²

Metallization Mask Layout

DG403/883, DG405/883



Test Circuits



NOTES:

1. Logic input waveform is inverted for switches that have the opposite logic sense.
2. $V_S = 10V$ for t_{ON} , $V_S = -10V$ for t_{OFF} .

FIGURE 1A.

FIGURE 1. SWITCHING TIME

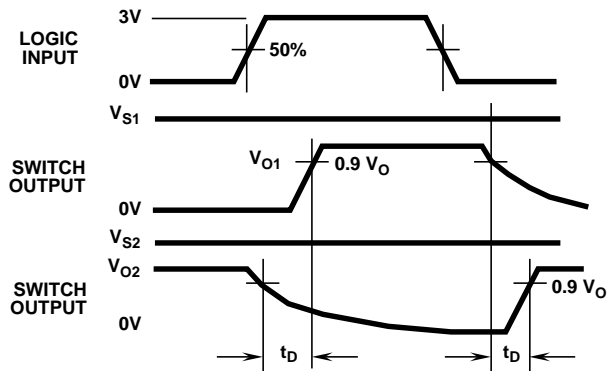
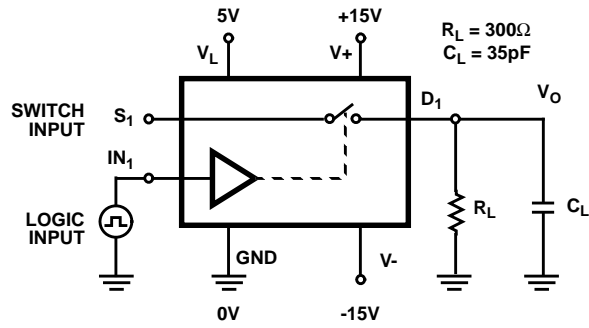


FIGURE 2A.

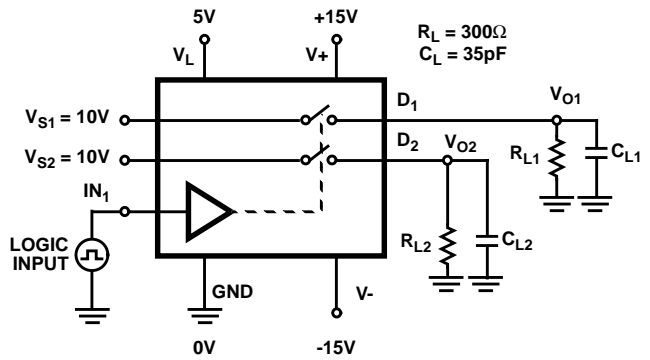
FIGURE 2. BREAK-BEFORE-MAKE



Repeat test for IN_2 and S_2
For load conditions, see Specifications. C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B.

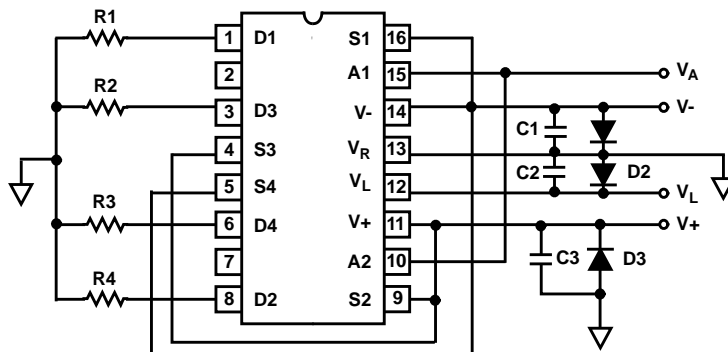


C_L (includes fixture and stray capacitance)

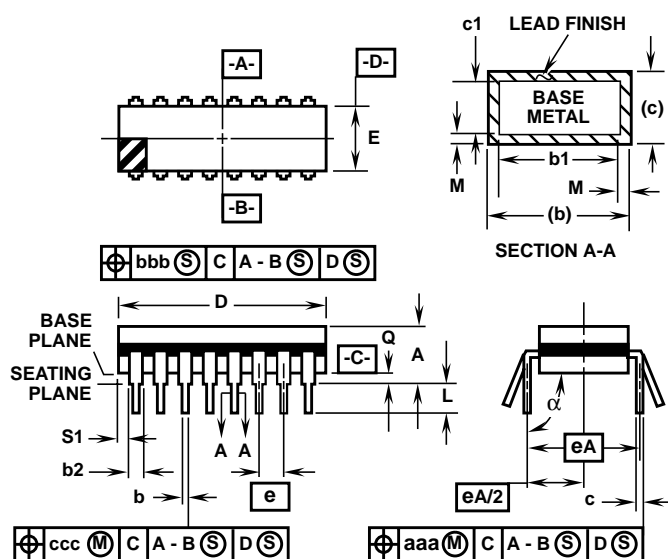
FIGURE 2B.

Burn-In Circuit

DG401/883, DG403/883, DG405/883



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



**F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.
11. Materials: Compliant to MIL-I-38535.

Rev. 0 4/94

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

DESIGN INFORMATION

Monolithic CMOS Analog Switches

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

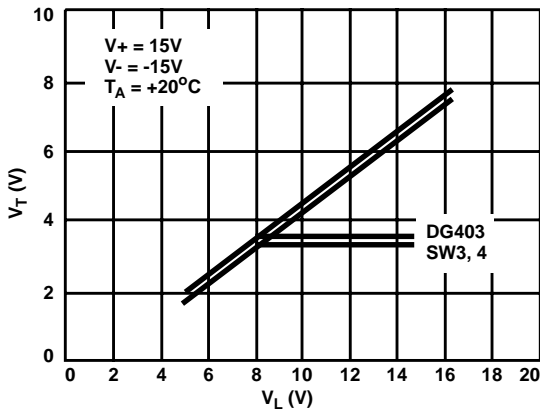


FIGURE 3. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

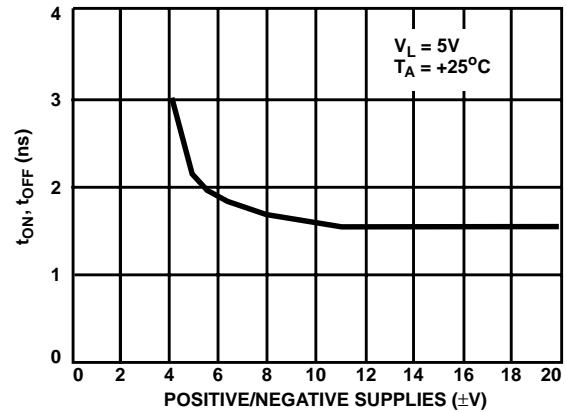


FIGURE 4. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

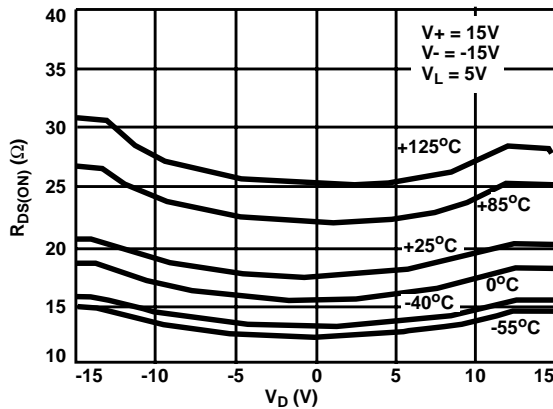


FIGURE 5. R_DS(ON) vs V_D AND TEMPERATURE

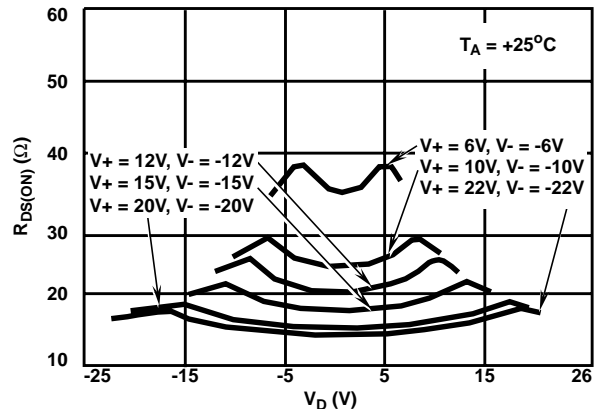


FIGURE 6. R_DS(ON) vs V_D AND POWER SUPPLY VOLTAGE

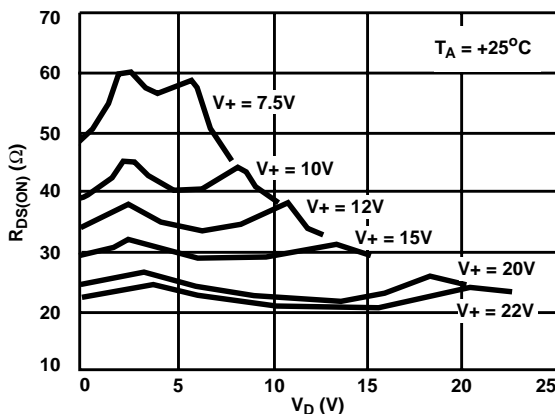


FIGURE 7. R_DS(ON) vs V_D AND POWER SUPPLY VOLTAGE, V- = 0V

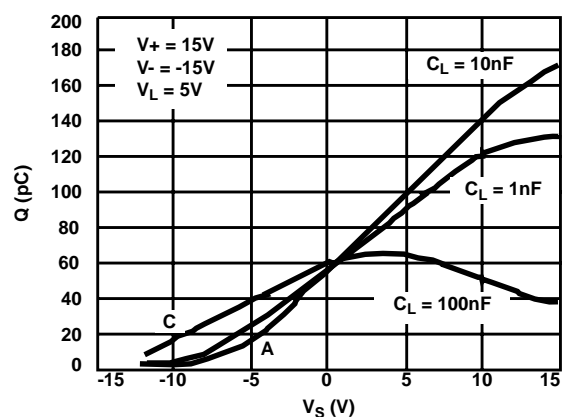


FIGURE 8. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

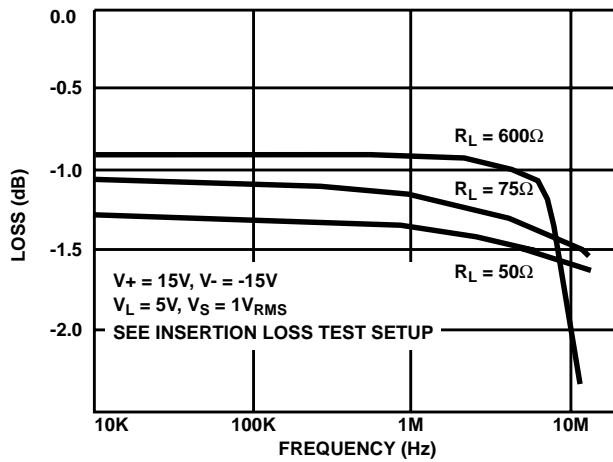


FIGURE 9. INSERTION LOSS vs FREQUENCY

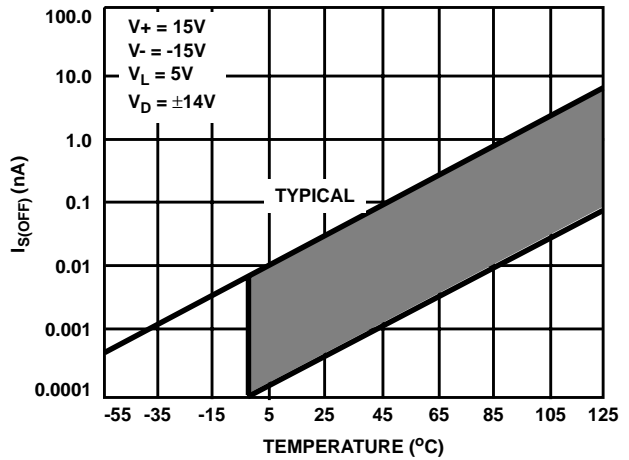


FIGURE 10. $I_{S(OFF)}$ vs TEMPERATURE

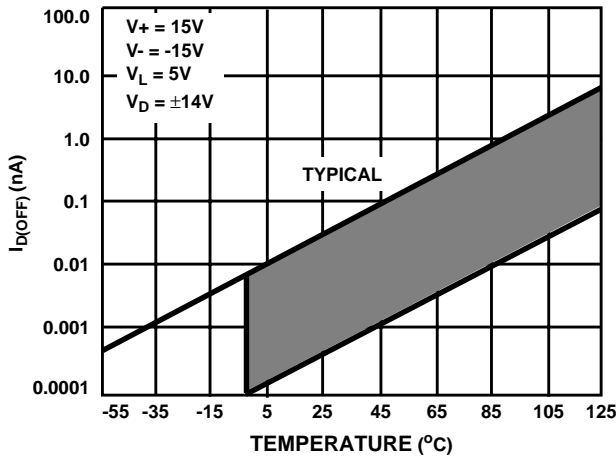


FIGURE 11. $I_{D(OFF)}$ vs TEMPERATURE

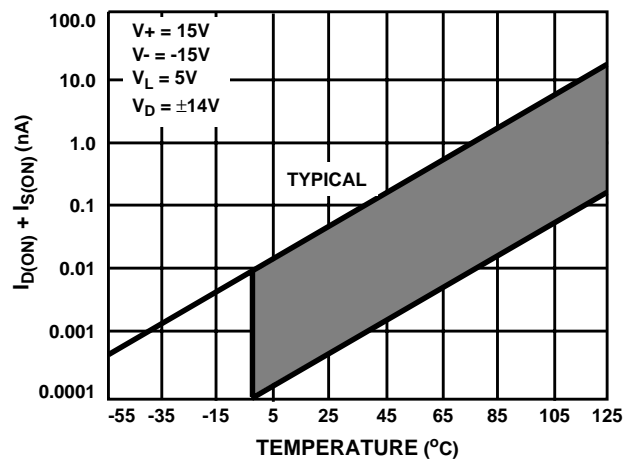


FIGURE 12. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

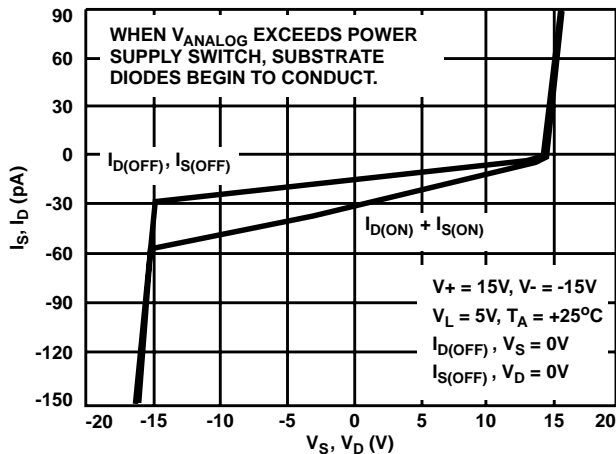


FIGURE 13. LEAKAGE CURRENT vs ANALOG VOLTAGE

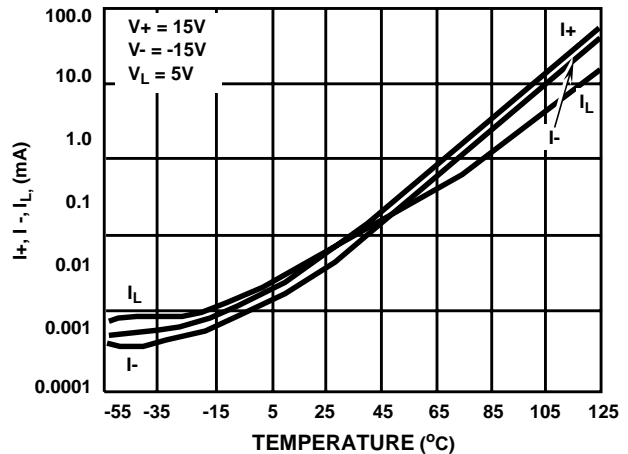


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

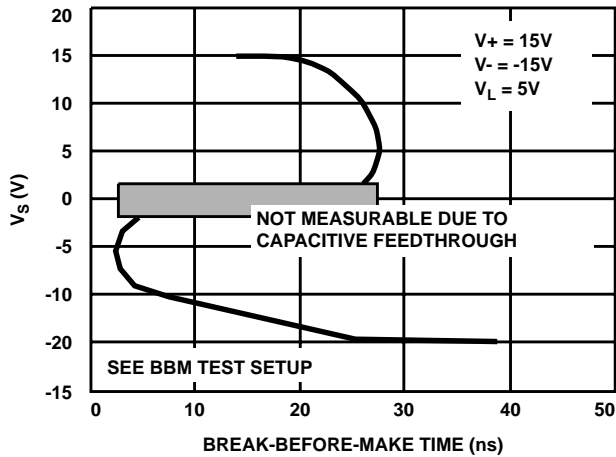


FIGURE 15. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

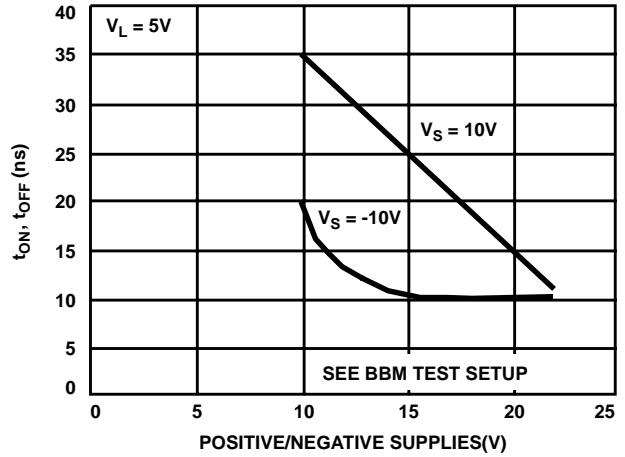


FIGURE 16. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

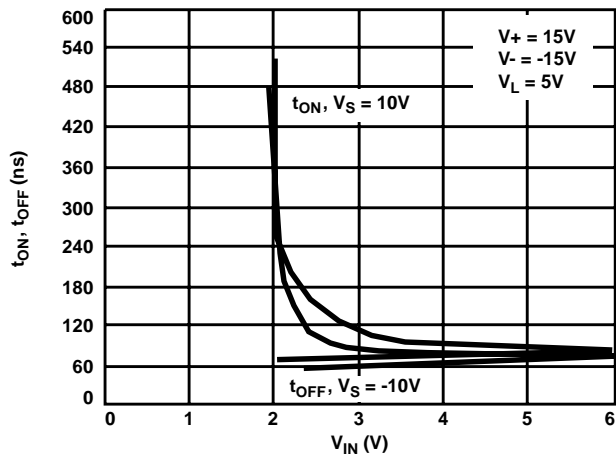


FIGURE 17. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) REFER TO FIGURE 1 FOR TEST CONDITIONS.

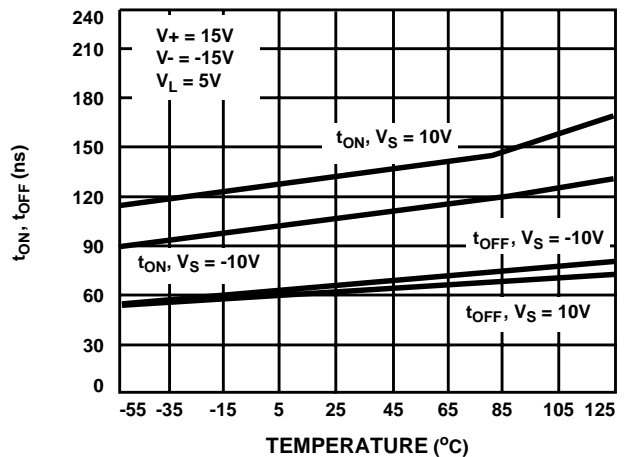


FIGURE 18. SWITCHING TIME vs TEMPERATURE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

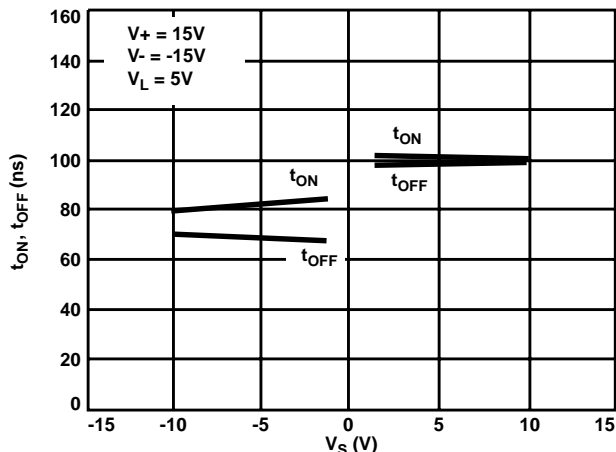


FIGURE 19. SWITCHING TIME vs ANALOG VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

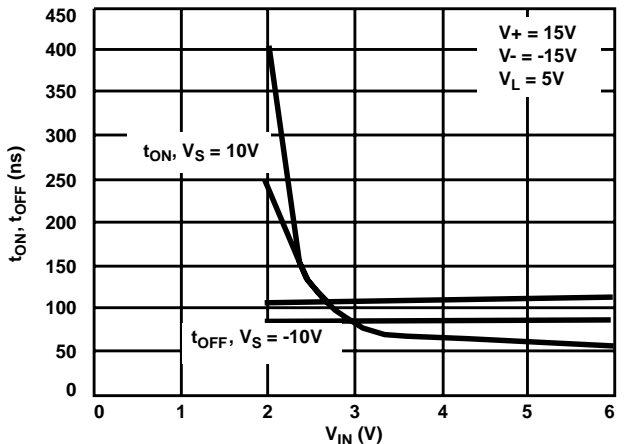


FIGURE 20. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}), REFER TO FIGURE 1 FOR TEST CONDITIONS.

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Intersil Corporation and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves (Continued)

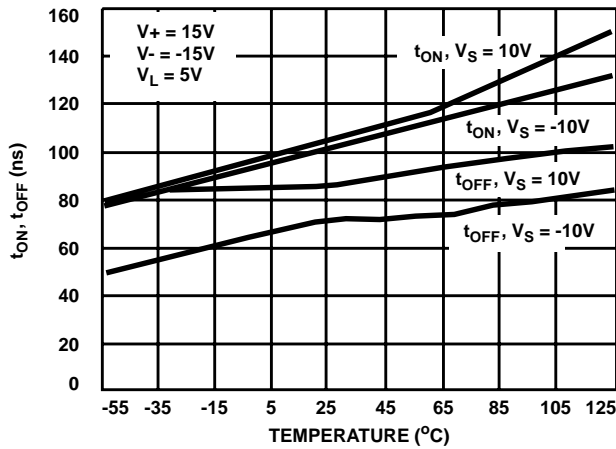


FIGURE 21. SWITCHING TIME vs TEMPERATURE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

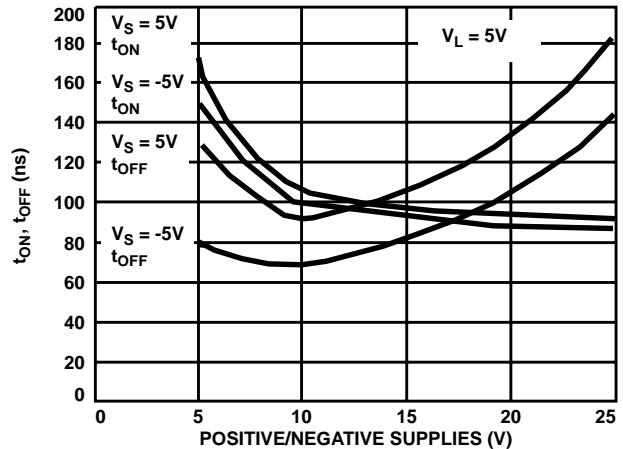


FIGURE 22. SWITCHING TIME vs POWER SUPPLY VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

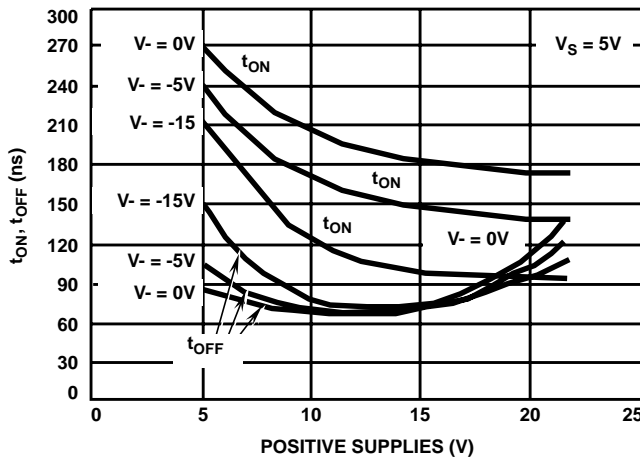


FIGURE 23. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

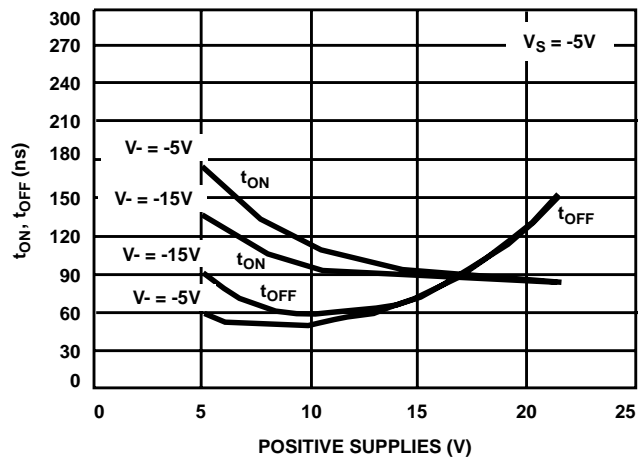


FIGURE 24. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

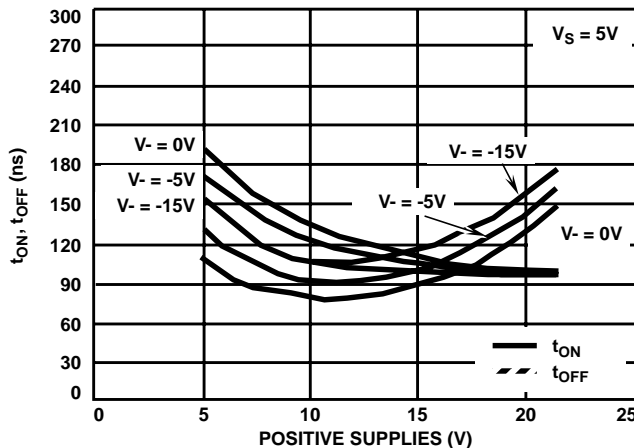


FIGURE 25. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.

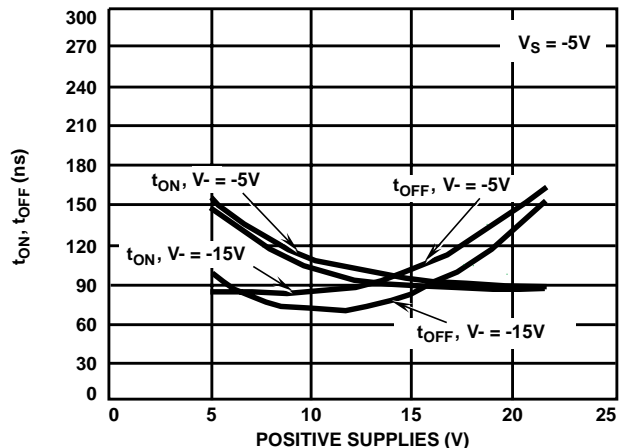


FIGURE 26. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, REFER TO FIGURE 1 FOR TEST CONDITIONS.