32MB – 4Mx64 SDRAM, UNBUFFERED

FEATURES

- PC100 and PC133 compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 144 Pin SO-DIMM JEDEC
  - D1: 27.94 (1.10")

DESCRIPTION

The WED3DG644V is a 4Mx64 synchronous DRAM module which consists of four 4Mx16 SDRAM components in TSOP II package, and one 2Kb EEPROM in an 8 pin TSOP package for Serial Presence Detect which are mounted on a 144 pin SO-DIMM multilayer FR4 Substrate.

* This product is subject to change without notice.

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

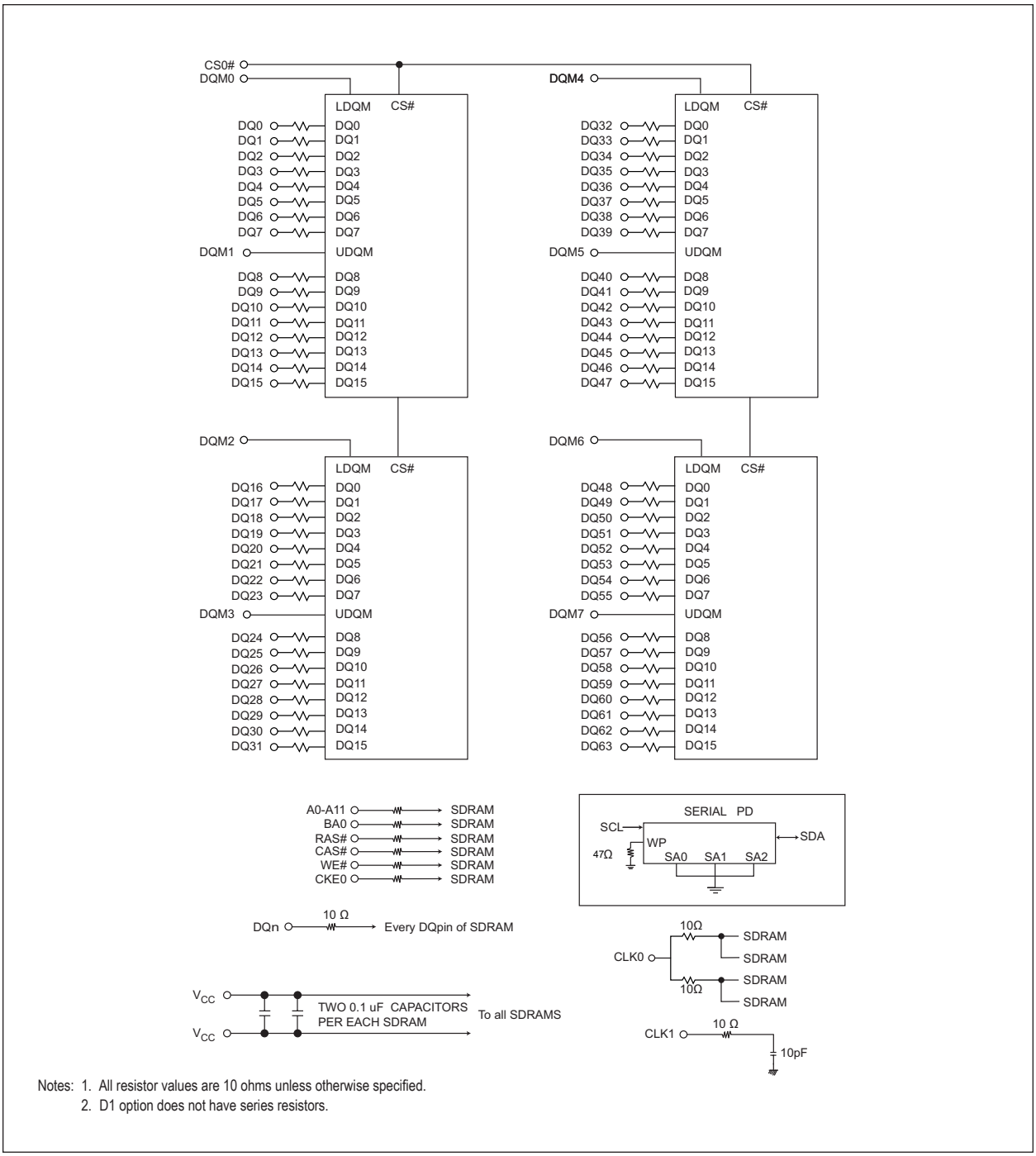
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	2	V_{SS}	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	V_{SS}	56	V_{SSv}	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	V_{CC}	102	V_{CC}
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	V_{CC}	12	V_{CC}	VOLTAGE KEY				105	A8	106	BA0
13	DQ4	14	DQ36					107	V_{SS}	108	V_{SS}
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	V_{CC}	64	V_{CC}	113	V_{CC}	114	V_{CC}
21	V_{SS}	22	V_{SS}	65	RAS#	66	CAS#	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE#	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0#	70	*A12	119	V_{SS}	120	VSS
27	V_{CC}	28	V_{CC}	71	*CS1#	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DNU	74	*CK1	123	DQ25	124	DQ57
31	A1	32	A4	75	V_{SS}	76	V_{SS}	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	V_{SS}	36	V_{SS}	79	NC	80	NC	129	V_{CC}	130	V_{CC}
37	DQ8	38	DQ40	81	V_{CC}	82	V_{CC}	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	V_{CC}	46	V_{CC}	89	DQ19	90	DQ51	139	V_{SS}	140	V_{SS}
47	DQ12	48	DQ44	91	V_{SS}	92	V_{SS}	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	V_{CC}	144	V_{CC}

PIN NAMES

A0 – A11	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock input
CKE0	Clock Enable input
CS0#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground
*V_{REF}	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



Notes: 1. All resistor values are 10 ohms unless otherwise specified.
2. D1 option does not have series resistors.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	4	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	$V_{CCQ+0.3}$	V	1
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	2
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-10	—	10	µA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	25	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	25	pF
Input Capacitance (CKE0)	C_{IN3}	25	pF
Input Capacitance (CLK0)	C_{IN4}	19	pF
Input Capacitance (CS0#)	C_{IN5}	25	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	8	pF
Input Capacitance (BA0-BA1)	C_{IN7}	25	pF
Data Input/Output Capacitance (DQ0-DQ63)	C_{OUT}	10	pF

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 0°C to +70°C)

			Version		
Parameter	Symbol	Conditions	133/100	Units	Note
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \leq t_{RC}$(min) I_{OL} = 0mA	300	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	4	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	4		
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), tcc =10ns Input signals are charged one time during 20	48	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≥V_{IL}(max), t_{CC} = ∞ Input signals are stable	24		
Active Standby Current in Power-Down Mode	I_{CC3P}	CKE ≥ V_{IL}(max), t_{CC} = 10ns	8	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8		
Active Standby Current in Non-Power Down Mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns	80	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable	40	mA	
Operating Current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CLK	460	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	360	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	4	mA	

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS

V_{CC} = 3.3V ± 0.3V, 0 ≤ T_A ≤ 70°C

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t_R/t_F = 1/1	ns
Output timing measurement reference level	1.4	V

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version	Unit	Note
			7.5, 10		
Row active to row active delay		t_{RRD} (min)	15	ns	1
RAS# to CAS# delay		t_{RCD} (min)	20	ns	1
Row precharge time		t_{RP} (min)	20	ns	1
Row active time		t_{RAS} (min)	45	ns	1
		t_{RAS} (max)	100	us	
Row cycle time		t_{RC} (min)	65	ns	1
Last data in to row precharge		t_{RDL} (min)	2	CLK	2
Last data in to Active delay		t_{DAL} (min)	2 CLK + t_{RP}	—	
Last data in to new col. address delay		t_{CDL} (min)	1	CLK	2
Last data in to burst stop		t_{BDL} (min)	1	CLK	2
Col. address to col. address delay		t_{CCD} (min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

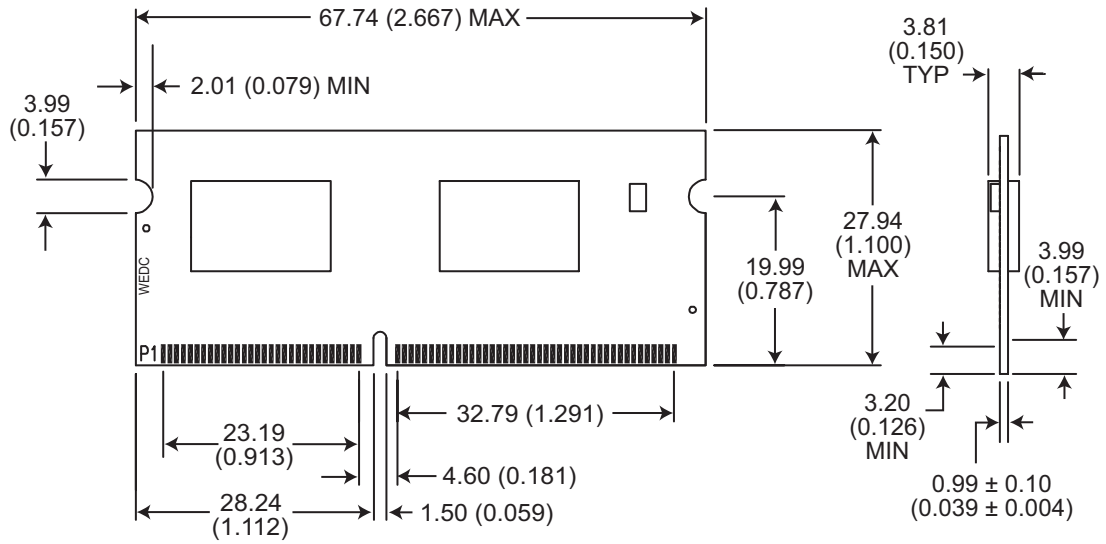
ORDERING INFORMATION FOR D1

Part Number	Clock Speed	CAS Latency	Height*
WED3DG644V10D1x-xx	100MHz	CL=2	27.94 (1.100")
WED3DG644V7D1x-xx	133MHz	CL=2	27.94 (1.100")
WED3DG644V75D1x-xx	133MHz	CL=3	27.94 (1.100")

NOTES:

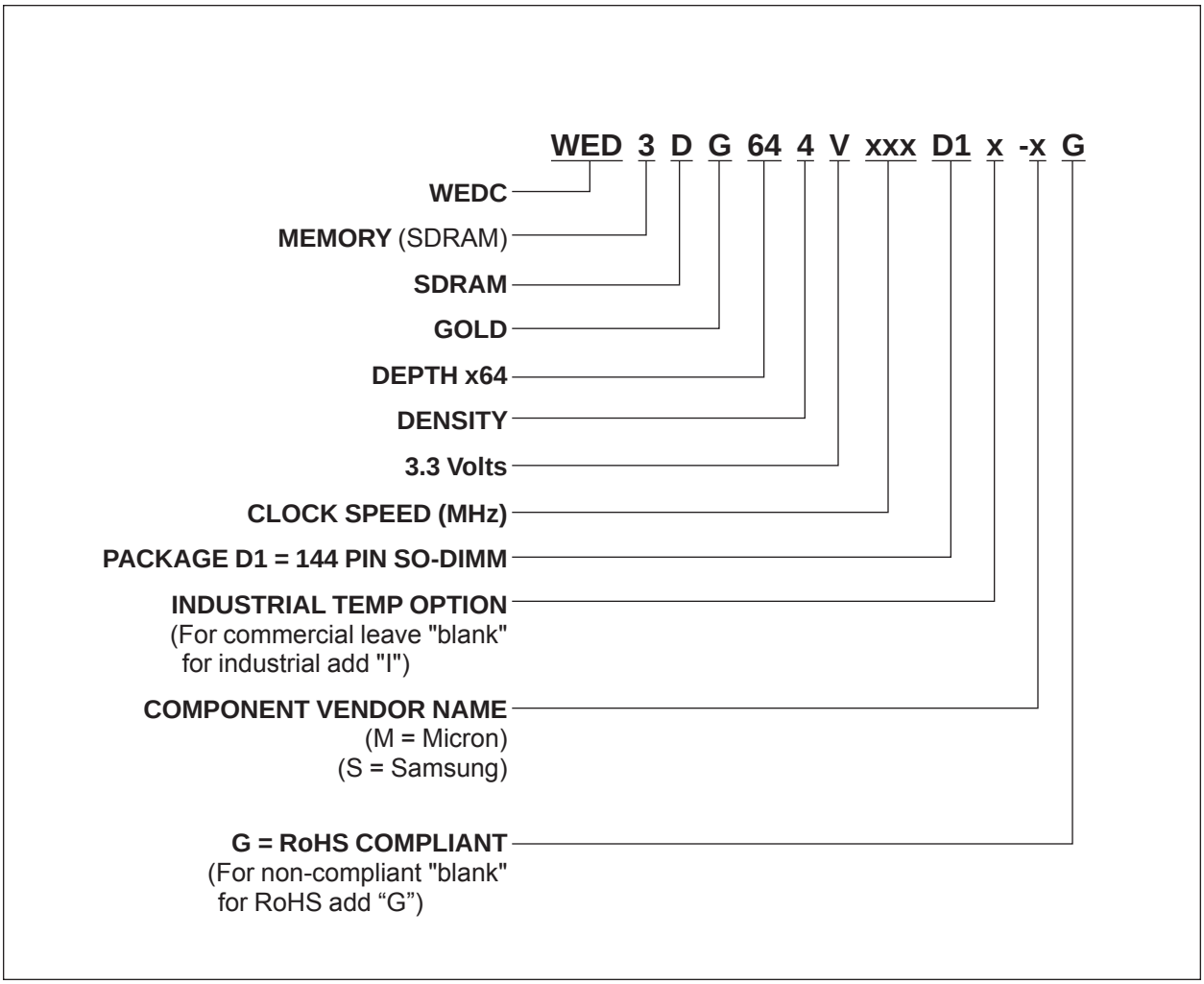
- Consult Factory for availability of RoHS products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "-x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D1



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

PART NUMBERING GUIDE



Document Title

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DRAM DIE OPTIONS:

- SAMSUNG: K-Die
- MICRON: Y14W:G

Revision History

Rev #	History	Release Date	Status
Rev A	Created	11-15-01	Advanced
Rev 0	Changed from Advanced to Final	9-6-02	Final
Rev 1	Updated CAP and I_{DD} specs	6-04	Final
Rev 2	2.1 Added RoHS and lead-free notes 2.2 Added vendor source and industrial tem notes 2.3 Added part number matrix	1-06	Final
Rev 3	3.1 Updated part number guide 3.2 Updated “ordering information” part number 3.3 Added DRAM die options	6-06	Final