

## DESCRIPTION

The M5M532R16 is a family of 32768-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controled either togethe or separately by /LB and /UB.

## FEATURES

- Fast access time M5M532R16J,TP-10 --- 10ns(max)  
 M5M532R16J,TP-12 --- 12ns(max)  
 M5M532R16J,TP-15 --- 15ns(max)
- Low power dissipation Active ----- 500mW(typ)  
 Stand by ----- 15mW(typ)
- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by /S
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs
- Separate control of lower and upper bytes by /LB and /UB

## APPLICATION

High-speed memory system

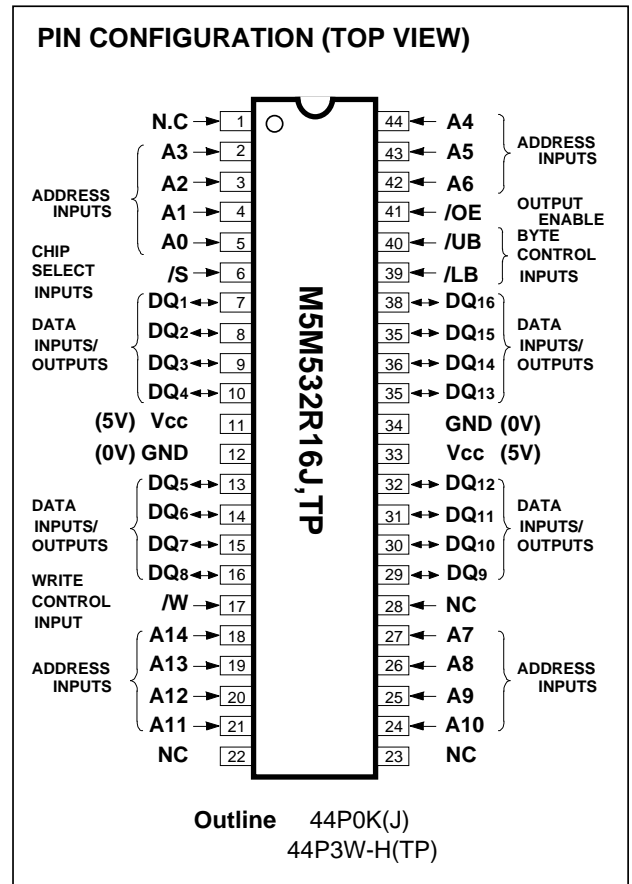
## FUNCTION

The operation mode of the M5M532R16 is determined by a combination of the device control inputs /S, /W, /OE, /LB, and /UB. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with low level /LB and/or low level /UB and low level /S. The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of /W, /LB, /UB or /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting W at a high level and /OE at a low level while /LB and/or /UB and /S are in an active state. (/LB and/or /UB=L, /S=L)



## PACKAGE

M5M532R16J : 44pin 400mil SOJ  
 M5M532R16VP: 44pin 400mil TSOP(II)

When setting /LB at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting /UB at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

When setting /LB and /UB at a high level or /S at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /LB, /UB and /S.

Signal-/S controls the power-down feature. When /S goes high, power dissipation is reduced extremely. The access time from /S is equivalent to the address access time.

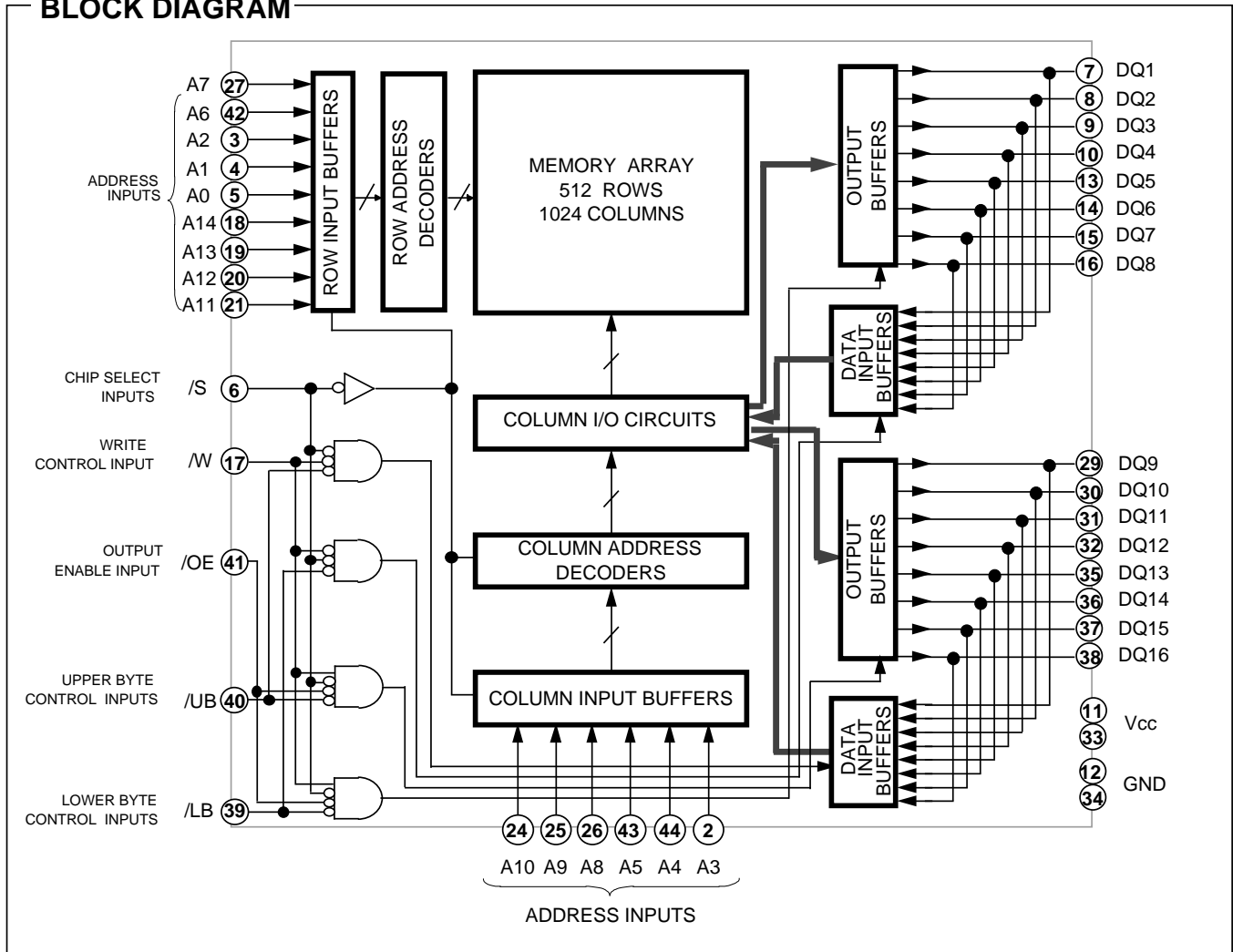
# MITSUBISHI LSIs M5M532R16J,TP-10,-12,-15

524288-BIT (32768-WORD BY 16-BIT) CMOS STATIC RAM

## FUNCTION TABLE

/S	/W	/OE	/LB	/UB	Mode	DQ1 - 8	DQ9 - 16	Icc
L	H	L	L	L	Read cycle All Bytes	D OUT	D OUT	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D OUT	Active
L	H	L	L	H	Read cycle Lower Bytes	D OUT	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D IN	D IN	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D IN	Active
L	L	X	L	H	Write cycle Lower Bytes	D IN	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage		-3.5* ~ 7	V
V <sub>I</sub>	Input voltage	With respect to GND	-3.5* ~ V <sub>cc</sub> +0.3	V
V <sub>O</sub>	Output voltage		-3.5* ~ V <sub>cc</sub> +0.3	V
P <sub>d</sub>	Power dissipation		T <sub>a</sub> =25°C	1000
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg(bias)</sub>	Storage temperature(bias)		-10 ~ 85	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

\* Pulse width ≤ 20ns, In case of DC: - 0.5V

## DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>cc</sub>=5V±10% , unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>cc</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3*		0.8	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 4mA	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8mA			0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> = 0 ~ V <sub>cc</sub>			2	μA
I <sub>OZ</sub>	Output current in off-state	V <sub>I</sub> (/S)= V <sub>IH</sub> V <sub>O</sub> = 0 ~ V <sub>cc</sub>			10	μA
I <sub>CC1</sub>	Active supply current (TTL level)	V <sub>I</sub> (/S)= V <sub>IL</sub> other inputs V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	AC(10ns cycle)		170	mA
			AC(12ns cycle)		150	
			AC(15ns cycle)		130	
			DC	100	110	
I <sub>CC2</sub>	Stand-by supply current (TTL level)	V <sub>I</sub> (/S)= V <sub>IH</sub>	AC(10ns cycle)		70	mA
			AC(12ns cycle)		65	
			AC(15ns cycle)		60	
			DC		50	
I <sub>CC3</sub>	Stand-by current (MOS level)	V <sub>I</sub> (/S)= V <sub>cc</sub> ≥ 0.2V other inputs V <sub>I</sub> ≤ 0.2V or V <sub>I</sub> ≥ V <sub>cc</sub> - 0.2V			5	mA

\* Pulse width ≤ 20ns, in case of AC : - 3.0V

## CAPACITANCE (T<sub>a</sub>=0 ~ 70°C, V<sub>cc</sub>=5V±10% , unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>i</sub> =25mVrms, f=1MHz			6	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>o</sub> =25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V<sub>cc</sub>=5V, T<sub>a</sub>=25°C

3: C<sub>I</sub>, C<sub>O</sub> are periodically sampled and are not 100% tested.

## AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>cc</sub>=5V±10% , unless otherwise noted)

### (1) MEASUREMENT CONDITION

Input pulse levels ----- V<sub>IH</sub> =3.0V, V<sub>IL</sub> =0.0V

Input rise and fall time ----- 3ns

Input timing reference levels ----- V<sub>IH</sub> =1.5V, V<sub>IL</sub> =1.5V

Output timing reference levels ----- V<sub>OH</sub> =1.5V, V<sub>OL</sub> =1.5V

Output loads ----- Fig1, Fig2

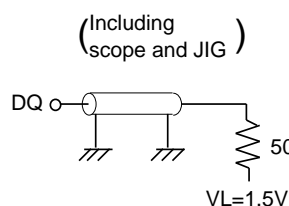


Fig.1 Output load

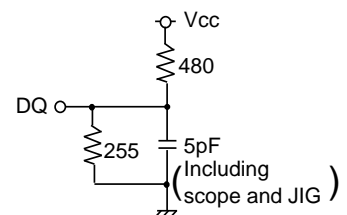


Fig.2 Output load for ten , tdis

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### READ CYCLE

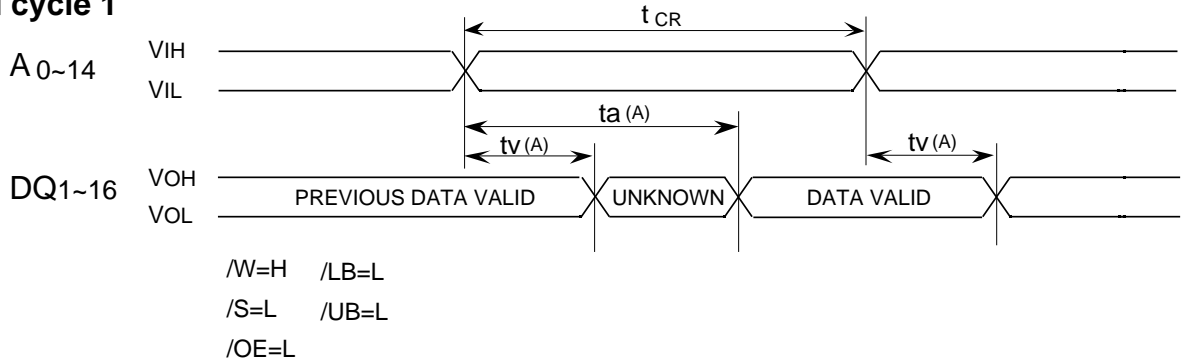
Symbol	Parameter	Limits						Unit
		M5M532R16 -10		M5M532R16 -12		M5M532R16 -15		
		Min	Max	Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	10		12		15		ns
t <sub>a (A)</sub>	Address access time		10		12		15	ns
t <sub>a (S)</sub>	Chip select access time		10		12		15	ns
t <sub>a (OE)</sub>	Output enable access time		5		6		7	ns
t <sub>a (B)</sub>	/LB,/UB access time		5		6		7	ns
t <sub>dis (S)</sub>	Output disable time after /S high	0	5	0	6	0	7	ns
t <sub>dis (OE)</sub>	Output disable time after /OE high	0	5	0	6	0	7	ns
t <sub>dis (B)</sub>	Output disable time after /LB,/UB high	0	5	0	6	0	7	ns
t <sub>en (S)</sub>	Output enable time after /S low	4		4		4		ns
t <sub>en (OE)</sub>	Output enable time after /OE low	3		3		3		ns
t <sub>en (B)</sub>	Output enable time after /LB,/UB low	3		3		3		ns
t <sub>v (A)</sub>	Data valid time after address change		4		4		4	ns
t <sub>PU</sub>	Power-up time after chip selection	0		0		0		ns
t <sub>PD</sub>	Power down time after chip selection		10		12		15	ns

### Write cycle

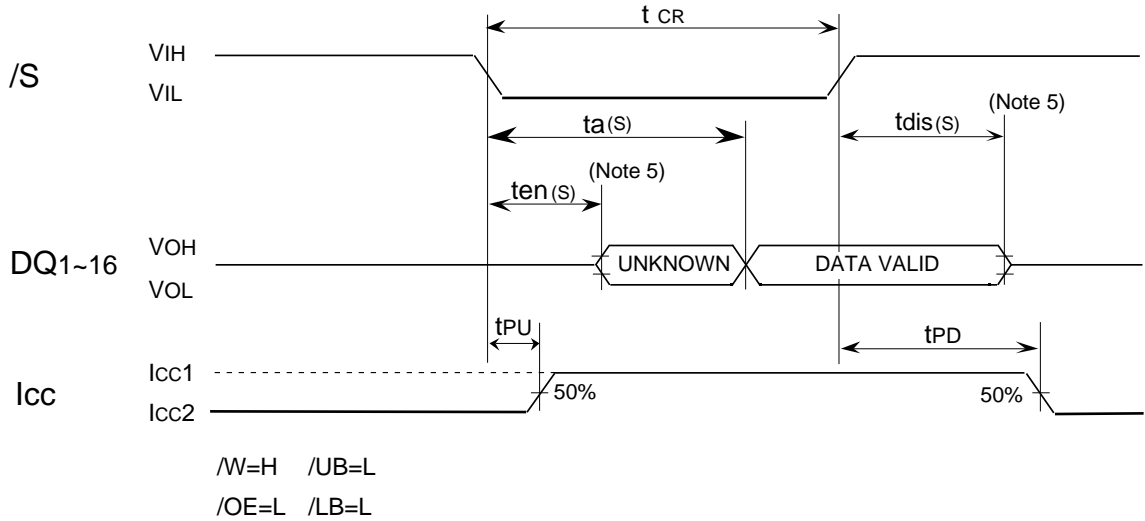
Symbol	Parameter	Limits						Unit
		M5M532R16 -10		M5M532R16 -12		M5M532R16 -15		
		Min	Max	Min	Max	Min	Max	
t <sub>cw</sub>	Write cycle time	10		12		15		ns
t <sub>w(W)</sub>	Write pulse width	9		10		12		ns
t <sub>su(B)</sub>	/LB,/UB setup time	9		10		12		ns
t <sub>su(A)1</sub>	Address setup time(/W)	0		0		0		ns
t <sub>su(A)2</sub>	Address setup time(/S)	0		0		0		ns
t <sub>su(S)</sub>	Chip select setup time	9		10		12		ns
t <sub>su(D)</sub>	Data setup time	5		6		7		ns
t <sub>h(D)</sub>	Data hold time	0		0		0		ns
t <sub>rec(W)</sub>	Write recovery time	0		0		0		ns
t <sub>dis (W)</sub>	Output disable time after /W low	0	5	0	6	0	7	ns
t <sub>dis (OE)</sub>	Output disable time after /OE high	0	5	0	6	0	7	ns
t <sub>en (W)</sub>	Output enable time after /W high	0		0		0		ns
t <sub>en (OE)</sub>	Output enable time after /OE low	0		0		0		ns
t <sub>en (B)</sub>	Output enable time after /LB,/UB low	0		0		0		ns
t <sub>su(A-WH)</sub>	Address to /W High	9		10		12		ns
t <sub>su(A-SH)</sub>	Address to /S High	9		10		12		ns
t <sub>su (A-BH)</sub>	Address to /LB,/UB High	9		10		12		ns

**(4)TIMING DIAGRAMS**

**Read cycle 1**



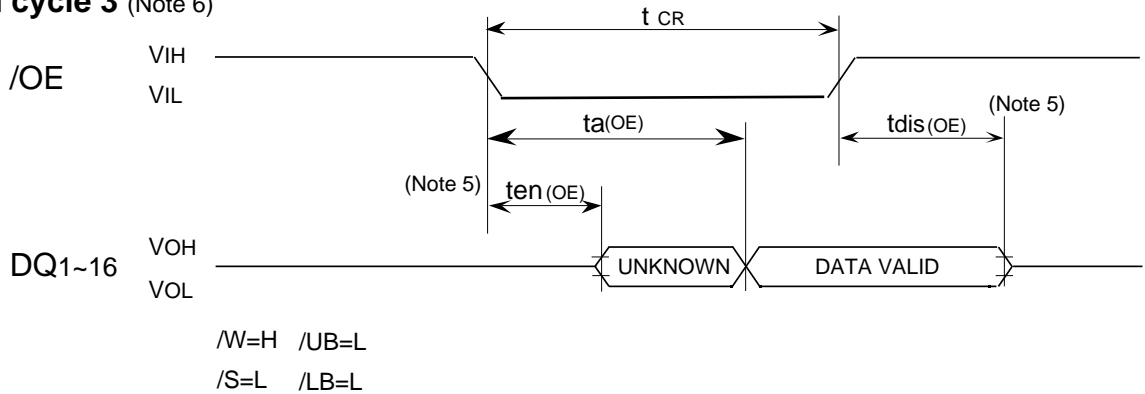
**Read cycle 2 (Note 4)**



Note 4. Addresses valid prior to or coincident with  $/S$  transition low.

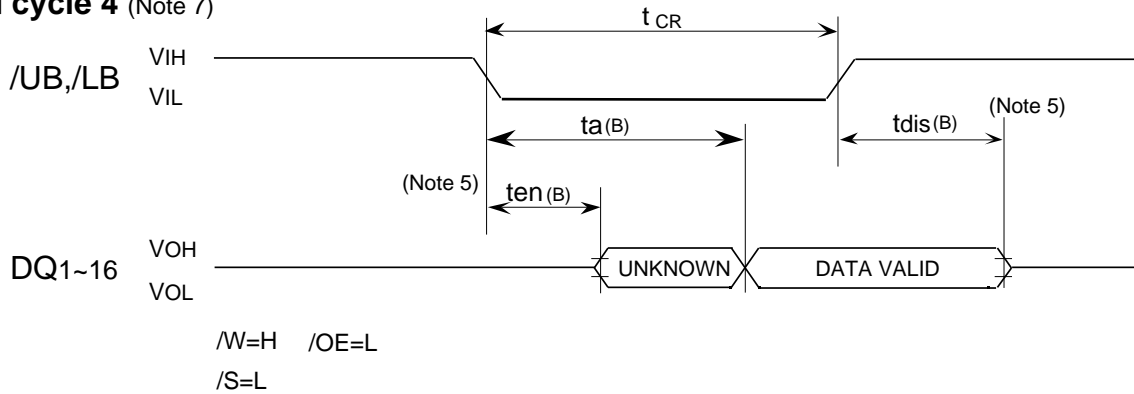
5. Transition is measured  $\pm 500\text{mv}$  from steady state voltage with specified loading in Figure 2.

**Read cycle 3 (Note 6)**



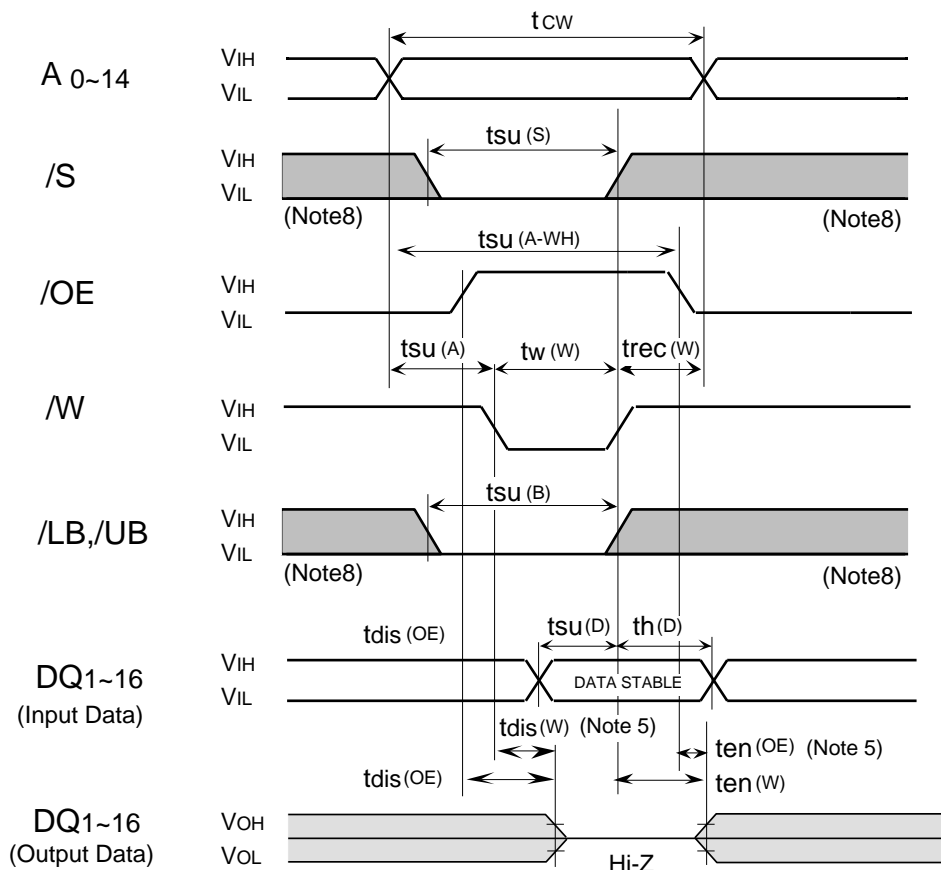
Note 6. Addresses and  $/S$  valid prior to  $/OE$  transition low by  $(t_a(A)-t_a(OE))$ ,  $(t_a(S)-t_a(OE))$

**Read cycle 4** (Note 7)



Note 7. Addresses  $\overline{S}$  and  $\overline{OE}$  valid prior to  $\overline{LB}, \overline{UB}$  transition low by  $(t_{a(A)}-t_{a(B)})$ ,  $(t_{a(S)}-t_{a(B)})$ ,  $(t_{a(OE)}-t_{a(B)})$ .

**Write cycle (/W control mode)**

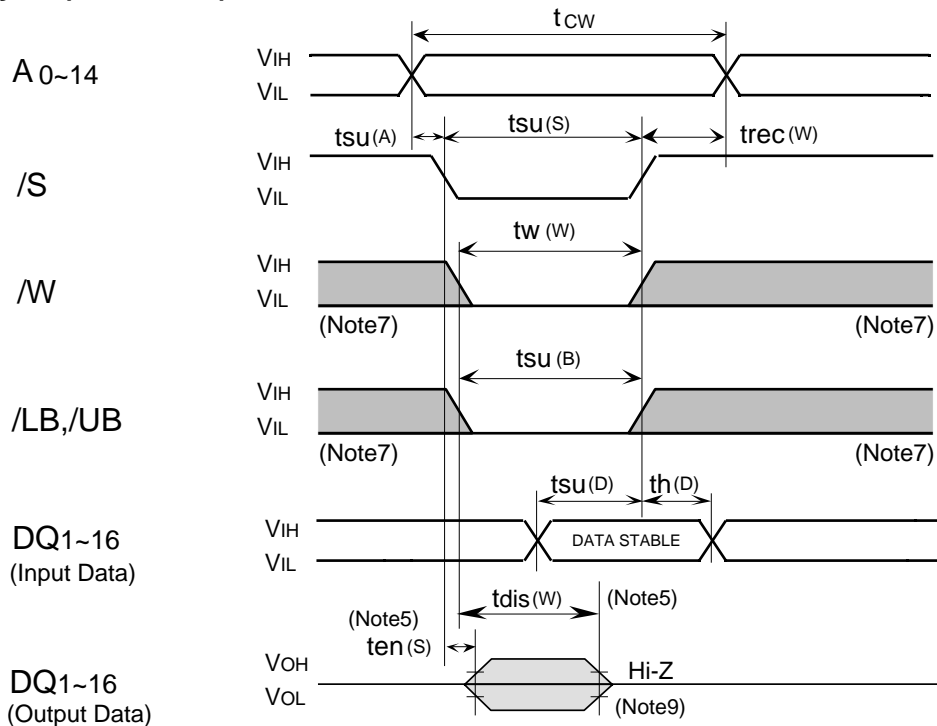


Note 8: Hatching indicates the state is don't care.

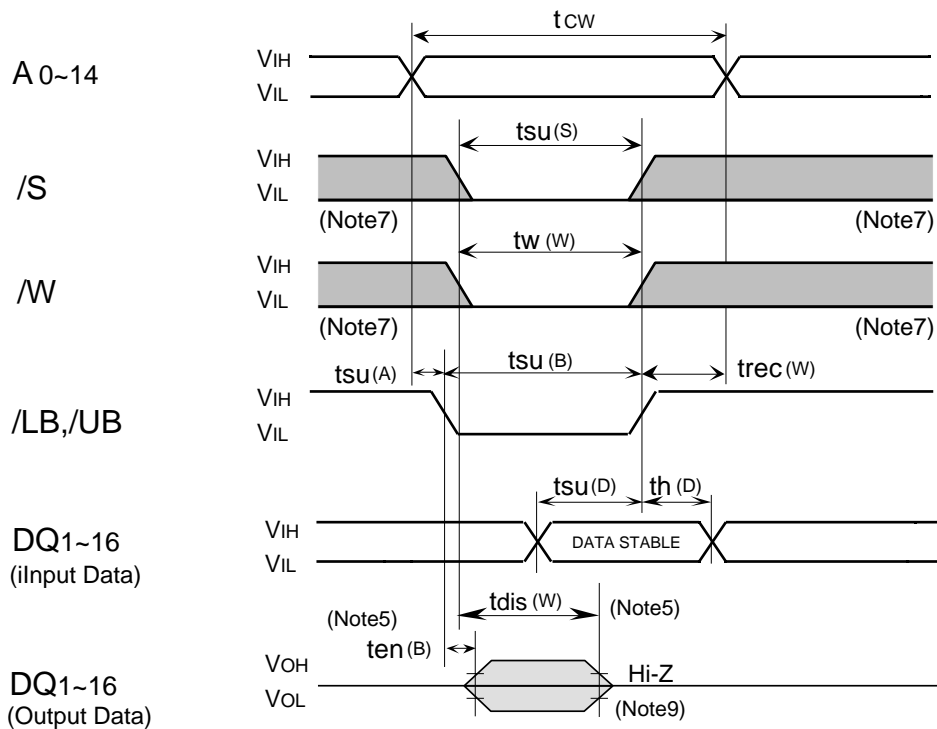
9: When the falling edge of  $\overline{W}$  is simultaneous or prior to the falling edge of  $\overline{S}$ , the output is maintained in the high impedance.

10:  $t_{en}, t_{dis}$  are periodically sampled and are not 100% tested.

**Write cycle(/S control)**



**Write cycle(/LB, /UB control)**



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'97.01.22 P3 Output loads=50

k.kubo