Current Sharing Controller for High Performance Processors

FEATURES

- Automatic True Current Sharing with Parallel Converters
- External SCR Drive for Fault Protection
- Over-Voltage Protection
- Programmable Over-Current Protection
- Voltage Mode Control
- Precision 1.3-V, ±1.6% Reference
- Drives N-Channel Switch and Rectifier
- 800-µA Quiescent Current (f_s = 200 kHz)
- 150-µA Standby Current
- Integrated “Power Good” Output
- Synchronization
- Under-Voltage Lockout

DESCRIPTION

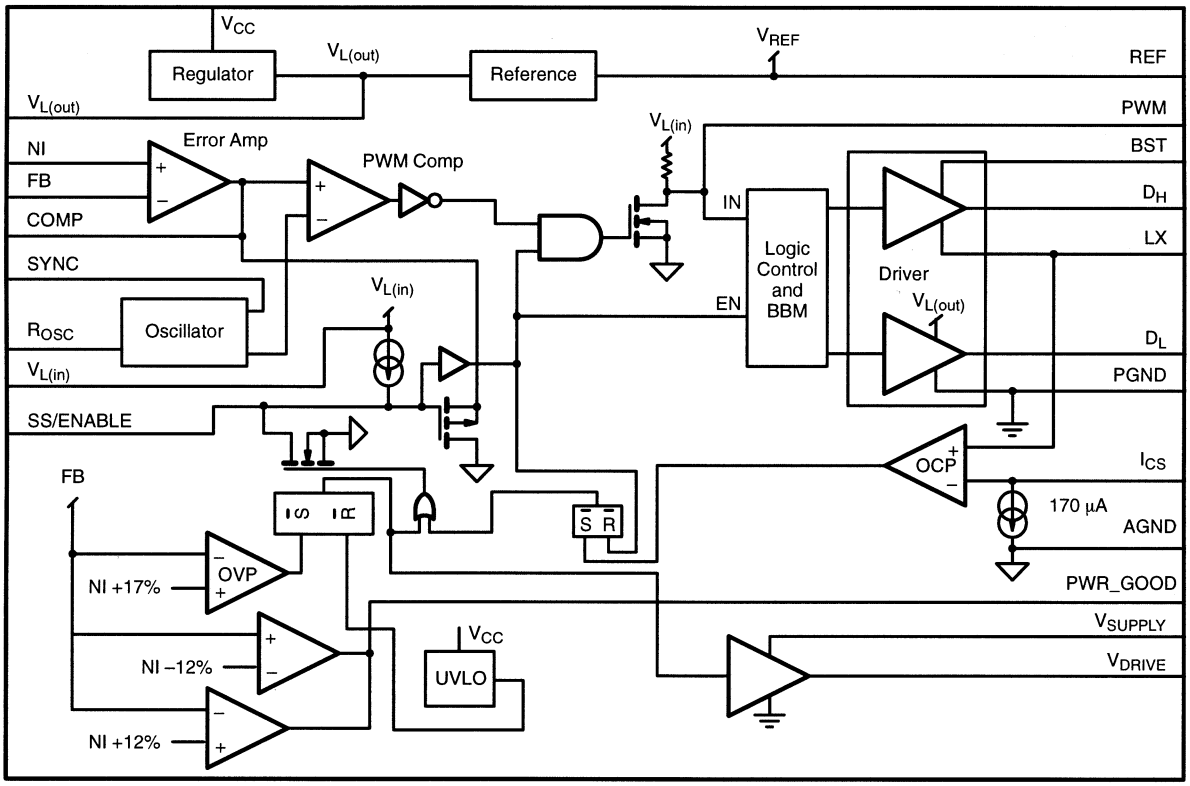
The voltage mode, synchronous buck controller is designed for point-of-use dc/dc conversion in high performance server and desktop computers. High efficiency is accomplished at full load by driving high- and low-side n-channel MOSFETs. The input voltage range has been designed for 4.75 V to 13.2 V to allow use of either 5 V or 12 V. The 1-MHz switching frequency combined with the 10-MHz error amplifier provides ultra-fast transient response necessary in a high performance microprocessor power supply.

Si9143 is designed to provide automatic true current sharing with parallel power supplies. True current sharing reduces stress on a single supply and increases system reliability. The system reliability is further increased by short circuit protection and external SCR drive signal to disconnect the power supply during fault conditions.

Si9143 is available in a wide-body 24-pin SSOP package and specified to operate over the commercial (0° to 70°C) temperature range.

A demo board, Si9143DB, is available.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to AGND

V_{SYNC_IN} . . . . . -0.3 to 7 V
V_{SYNC_OUT} . . . . . -0.3 to 7 V
V_{CC} . . . . . -0.3 to 15 V

Voltages Referenced to PGND

V_{BST} . . . . . -0.3 to 20 V
V_{PGND} to V_{AGND} . . . . . ±2 V
V_L Short to GND . . . . . Continuous
V_{REF} Short to GND . . . . . Continuous
V_{SUPPLY} . . . . . -0.3 to 15 V

Continuous Power Dissipation (T_A = 25°C)[a]
24-Pin SSOP[b] . . . . . 1.2 W
Operating Temperature Range . . . . . 0 to 70°C
Storage Temperature Range . . . . . -65 to 125°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
T_{JMAX} . . . . . 150°C
Θ_{JA} . . . . . 104°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.6 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

V_{CC} . . . . . 4.75 V to 13.2 V
V_{SUPPLY} . . . . . ≤13.2 V
R_{OSC} . . . . . 100 kΩ (100 kHz) to 10 kΩ (1 MHz)
$V_{L(out), (in)}$ Capacitance . . . . . 4.7 µF
$V_{L(out)}$ Load . . . . . ≤1 mA
V_{REF} Capacitance . . . . . 0.1 µF
V_{REF} Load . . . . . ≤1 mA
Analog and Digital Inputs . . . . . 0 to V_L

SPECIFICATIONS

Specifications	Test Conditions Unless Otherwise Specified V_{CC} = 4.75 V to 13.2 V		Limits T_A = 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Reference						
Output Voltage	I_{REF} = 0		1.30 -1.6%	1.30	1.30 +1.6%	V
Regulation	I_{REF} = 0 to 1 mA		-10		10	mV
Line Rejection	At 10 kHz			80		dB
Oscillator						
Operating Frequency	Sync = Open		100		1000	kHz
PWM Maximum Duty Cycle	f_{OSC} = 200 kHz			94		%
	f_{OSC} = 400 kHz			88		
PWM High	I_{OH} = -100 µA			0.7 V_L		V
PWM Low	I_{OL} = 500 µA			0.3 V_L		
SYNC High	I_{OH} = -100 µA			0.7 V_L		
SYNC Low	I_{OL} = 500 µA			0.3 V_L		
Output Drivers						
Source/Sink I (Peak)	BST - LX = 4.5 V	H Driver	500	1000		mA
	V_{CC} = 4.75 V	L Driver	500	1000		
Supply						
Quiescent Current PWM	f_{osc} = 200 kHz			800	1200	µA
Standby Current Shutdown	V_{CC} < 3.5 V			150	225	
V_L						
Output Voltage	I_{VL} = 0, V_{CC} = 5.7 to 13.2 V		4.95	5.5	6.05	V
	I_{VL} = 0, V_{CC} = 4.7 to 5.7 V			V_{IN} - 0.2 V		
Line Rejection	At 10 kHz			30		dB

SPECIFICATIONS

Specifications	Test Conditions Unless Otherwise Specified V_{CC} = 4.75 V to 13.2 V	Limits T_A = 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
SS/Enable					
Source Current		-2.5	-5	-7.5	µA
Fault Sink Current		20	35		mA
Logic Low				0.8	V
Logic High		2.4			
UVLO (V_L)					
Lockout Voltage	V_L Falling		3.6	3.8	V
Hysteresis			200		mV
Error Amplifier					
Unity-Gain BW Product	V_{CC} = 5 V		10		MHz
Input Bias Current	$V_{NI} = V_{REF}$, V_{FB} = 1.0 V	-1	0	1	µA
Offset Voltage	$V_{NI} = V_{REF}$	-15.0	0	15.0	mV
Output Current	Source (V_{FB} = 0.8 V, NI = V_{REF})			-1	mA
	Sink (V_{FB} = 2.4 V, NI = V_{REF})	0.8			
PWR_GOOD					
V_{PWR_GOOD} High	Typical Hysteresis = 1% $V_{NI} = V_{REF}$	V_{NI} + 7%	V_{NI} +12%	V_{NI} + 17%	V
V_{PWR_GOOD} Low		V_{NI} - 17%	V_{NI} -12%	V_{NI} - 7%	
Output Sink Current	$V_{DS} \le 1$ V	2			mA
OVP					
Threshold Voltage	$V_{NI} = V_{REF}$, BST - L_X = 4.5 V	V_{NI} + 12%	V_{NI} + 17%	V_{NI} + 22%	V
V_{DRIVE} Shutdown Delay			2.0	3.0	µS
OCP					
I_{CS} Sink Current	$4.75 \le V_{ICS} \le 13.2$ V	126	170	204	µA
External SCR Drive					
V_{SUPPLY} Quiescent Current	V_{SUPPLY} = 13.2 V		3		µA
V_{DRIVE} Source/Sink Current			10		mA
V_{DRIVE} High Voltage	I_{SOURCE} = -100 µA, $4.75 \le V_{SUPPLY} \le 13.2$ V	V_{SUPPLY} - 0.5			V
V_{DRIVE} Low Voltage	I_{SINK} = 100 µA, $4.75 \le V_{SUPPLY} \le 13.2$ V			0.4	

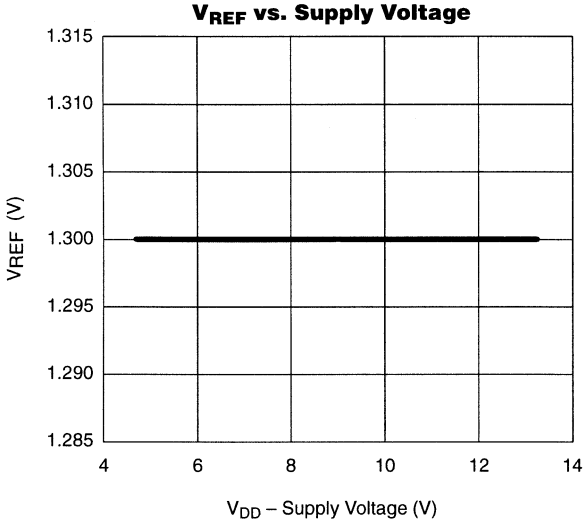
Notes

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

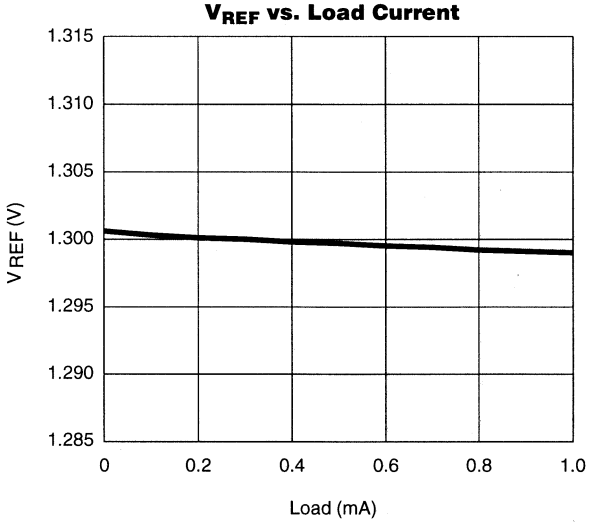
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

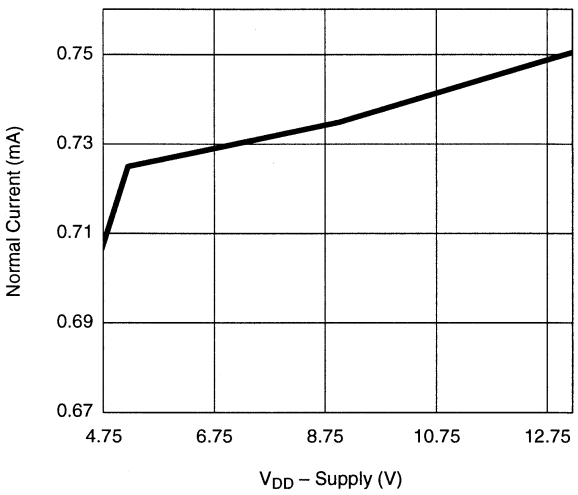
V_{REF} vs. Supply Voltage



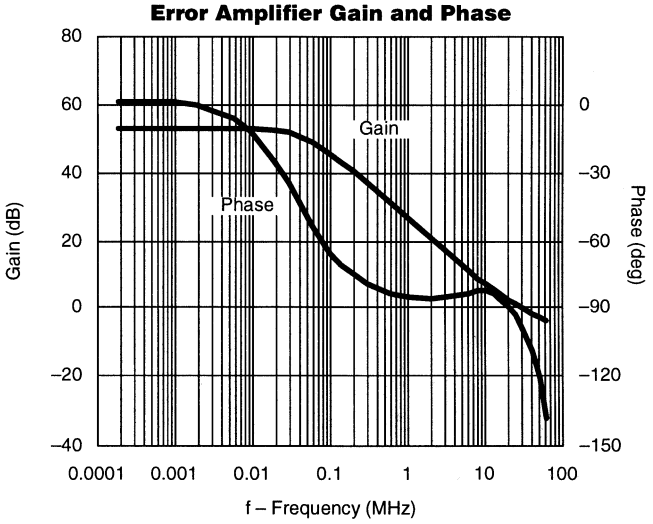
V_{REF} vs. Load Current



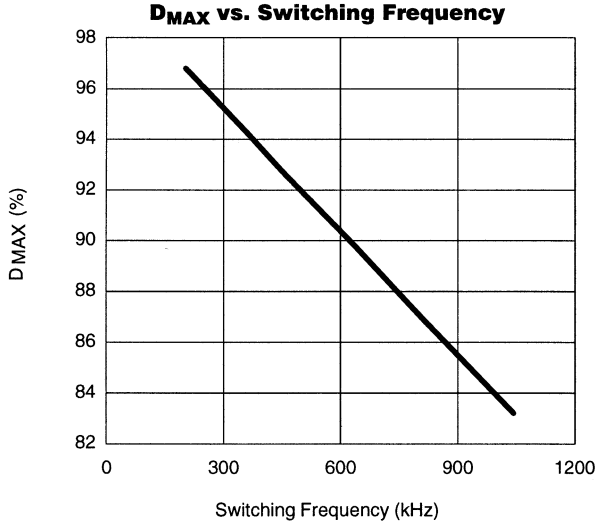
Supply Current vs. Supply Voltage



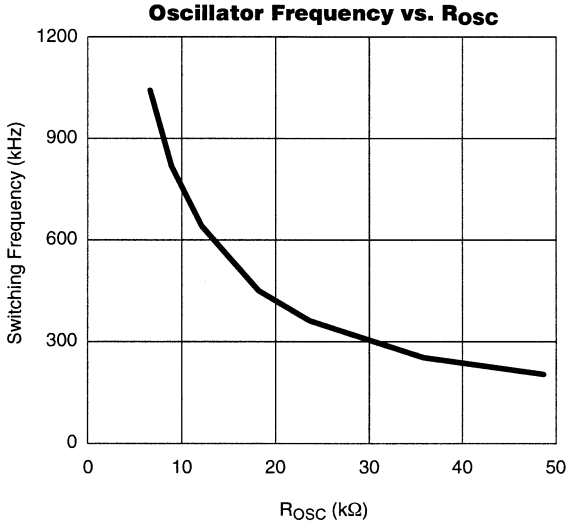
Error Amplifier Gain and Phase



D_{MAX} vs. Switching Frequency

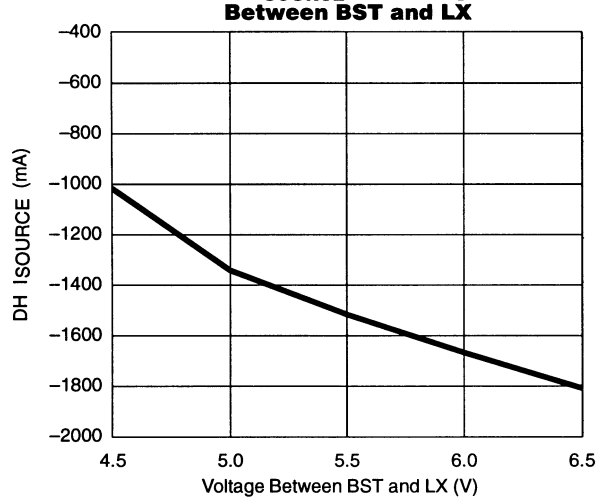


Oscillator Frequency vs. R_{OSC}

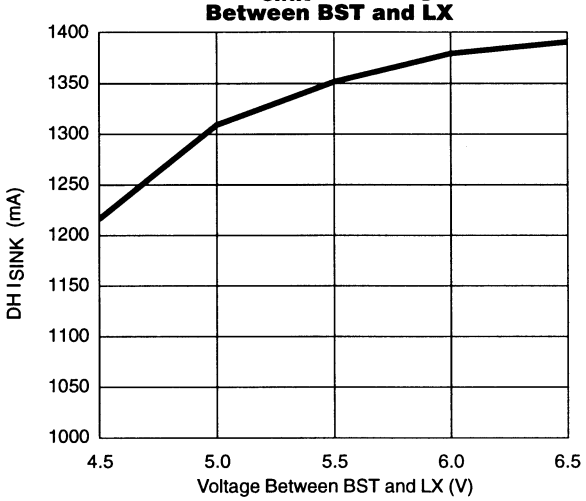


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

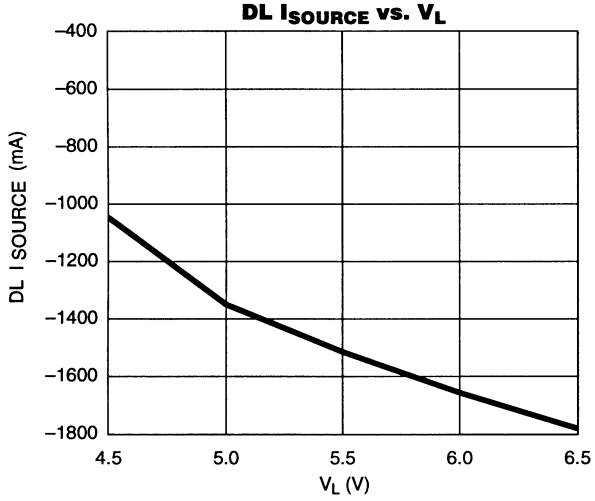
DH I_{SOURCE} vs. Voltage Between BST and LX



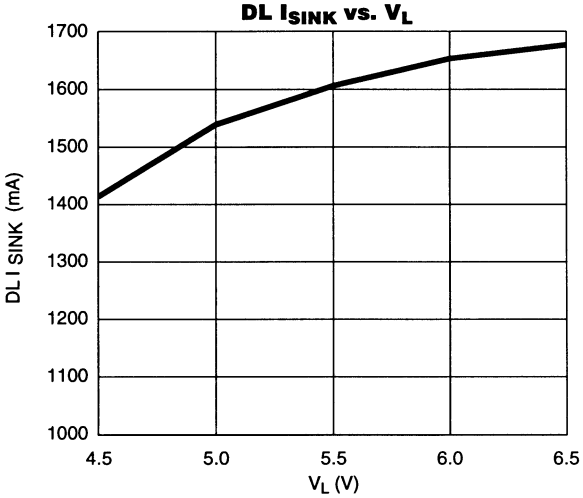
DH I_{SINK} vs. Voltage Between BST and LX



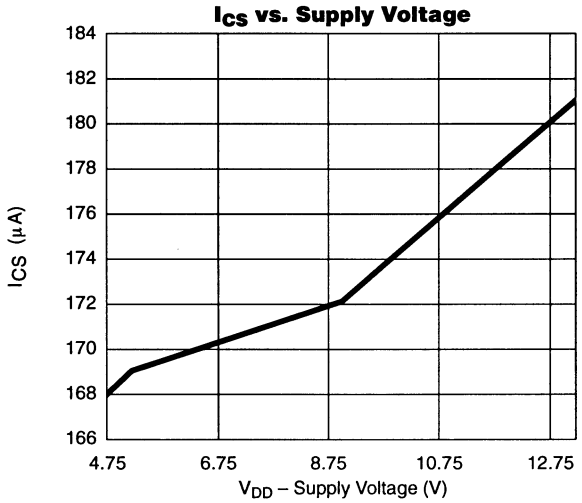
DL I_{SOURCE} vs. V_L



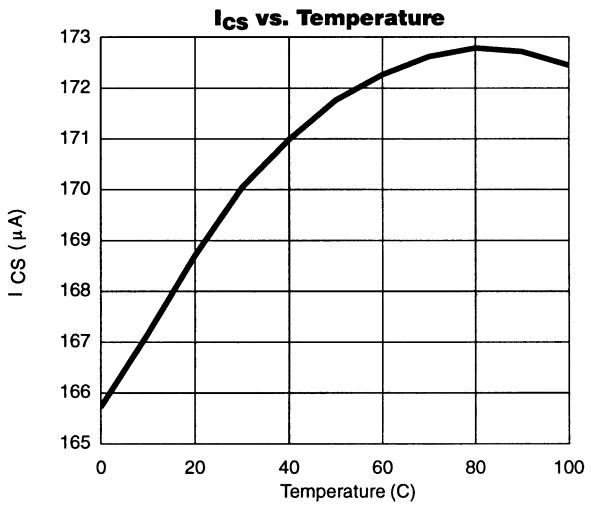
DL I_{SINK} vs. V_L



I_{CS} vs. Supply Voltage

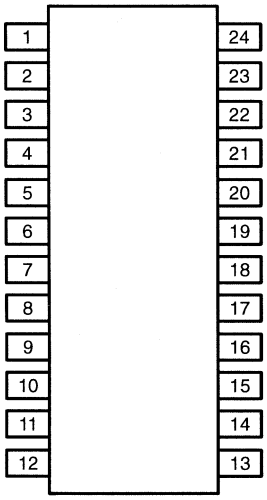


I_{CS} vs. Temperature



PIN CONFIGURATION

SSOP-24



Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Packaging**
Si9143CG	0 to 70°C	Bulk
Si9143CG-T1		Tape and Reel

Ev Kit	**Temperature Range**	**Board Type**
Si9143 DB	0 to 70°C	Surface Mount

PIN DESCRIPTION		
Pin Number	**Symbol**	**Description**
1	NIs	Error amplifier non-inverting input
2	SS/Enable	Soft-Start: Capacitor programmable or logic level controlled shutdown
3	FB	Feedback
4	COMP	Compensation node for the external feedback circuit
5, 6	V_{CC}	Input Voltage: 4.75 V to 13.2 V
7	V_{REF}	1.30 V precision reference
8	AGND	Ground: Connect to quiet ground.
9	R_{OSC}	External resistor to determine switching frequency
10	NC	Not internally connected
11	SYNC	Synchronizing Clock
12	V_{SUPPLY}	External supply voltage for SCR drive
13	V_{DRIVE}	External SCR drive voltage
14	PWR_GOOD	Power_Good window comparator output
15, 16	PGND	Power Ground
17	D_L	Low-side gate driver for the synchronous rectifier
18	$V_{L(out)}$	5.5-V reference for gate drive supply
19	$V_{L(in)}$	Reference input, connect to RC filter from $V_{L(out)}$
20	LX	Inductor connection node
21	D_H	High-side gate driver for the power switch
22	BST	Boost capacitor connection node to generate high-side gate drive
23	I_{CS}	Programmable over current limit
24	PWM	PWM output node for current sharing

TIMING DIAGRAMS

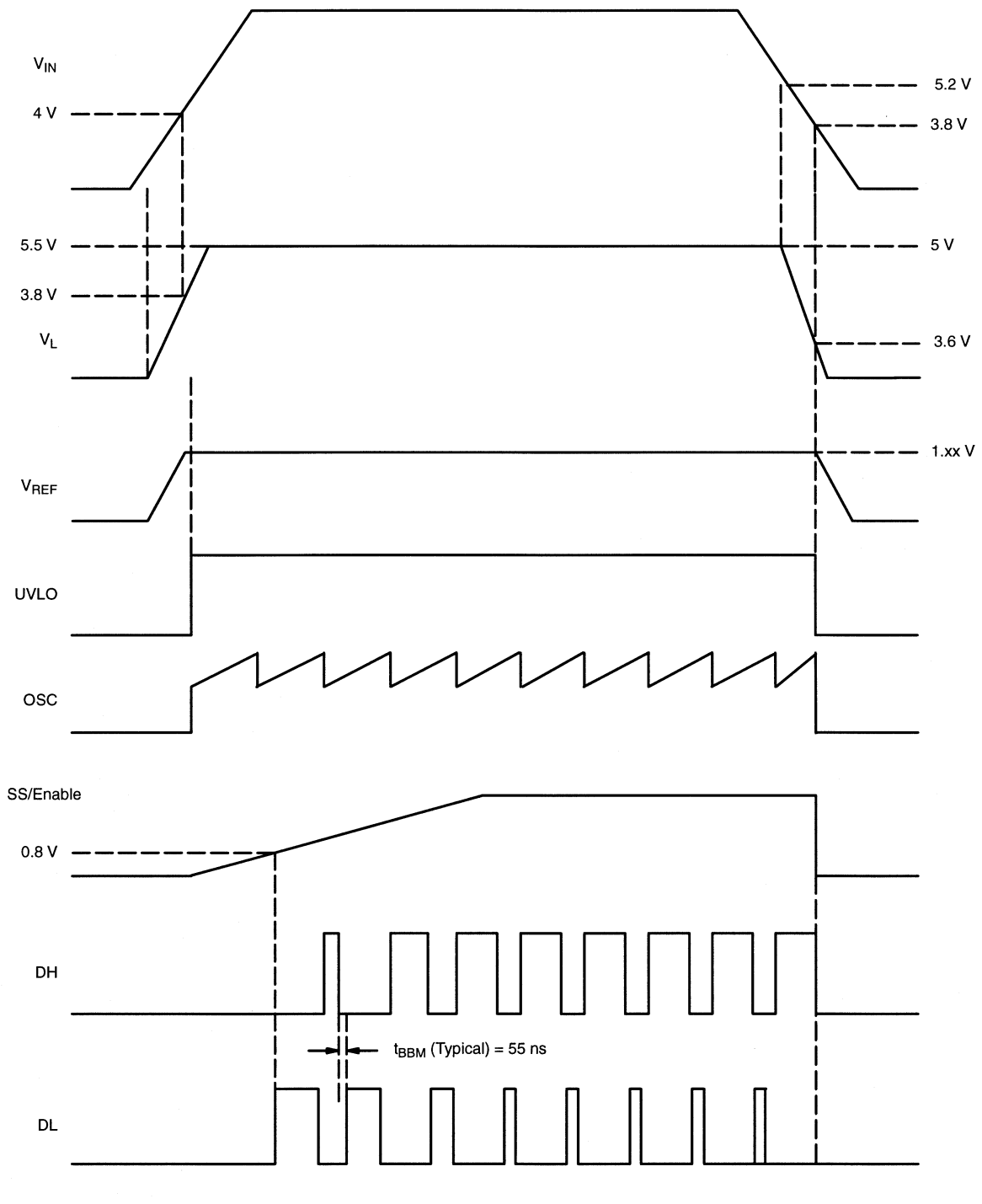


FIGURE 1. Start-up Timing Sequence

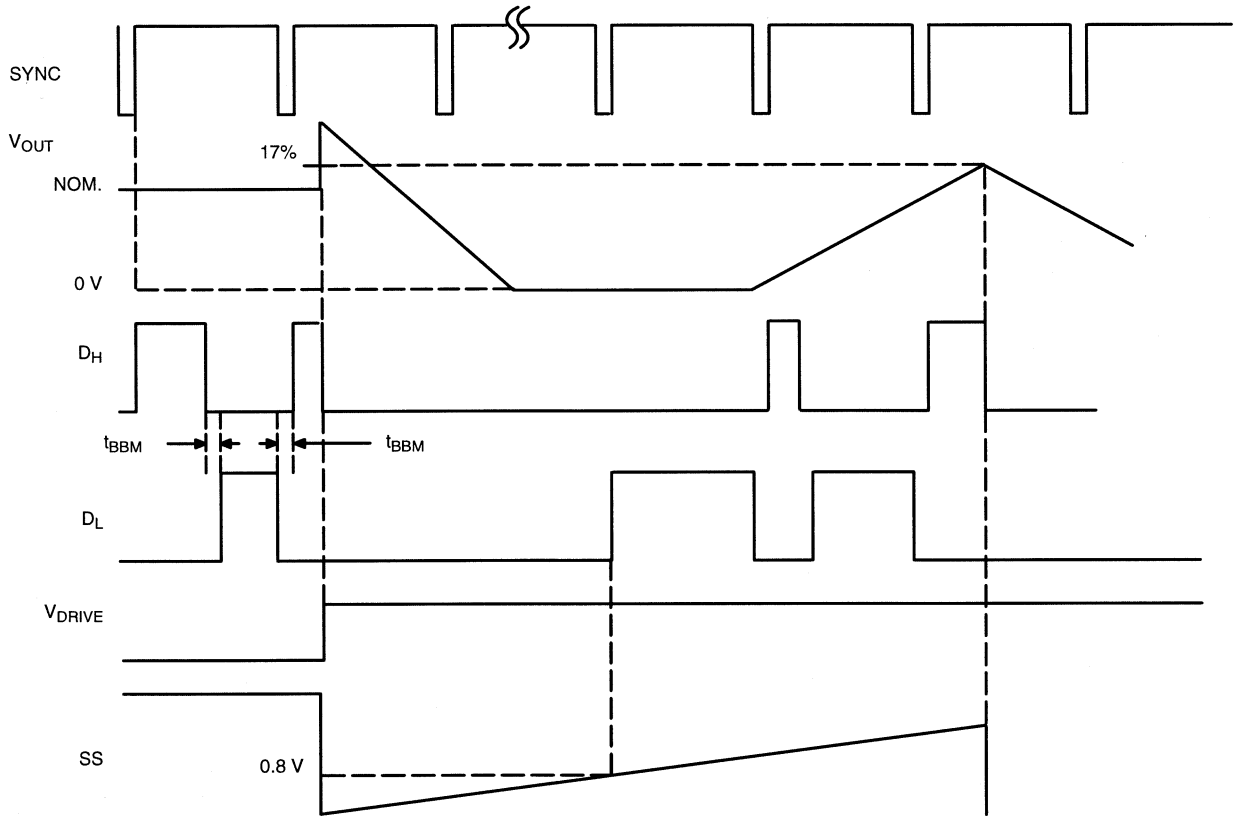


FIGURE 2. OVP Timing Diagrams

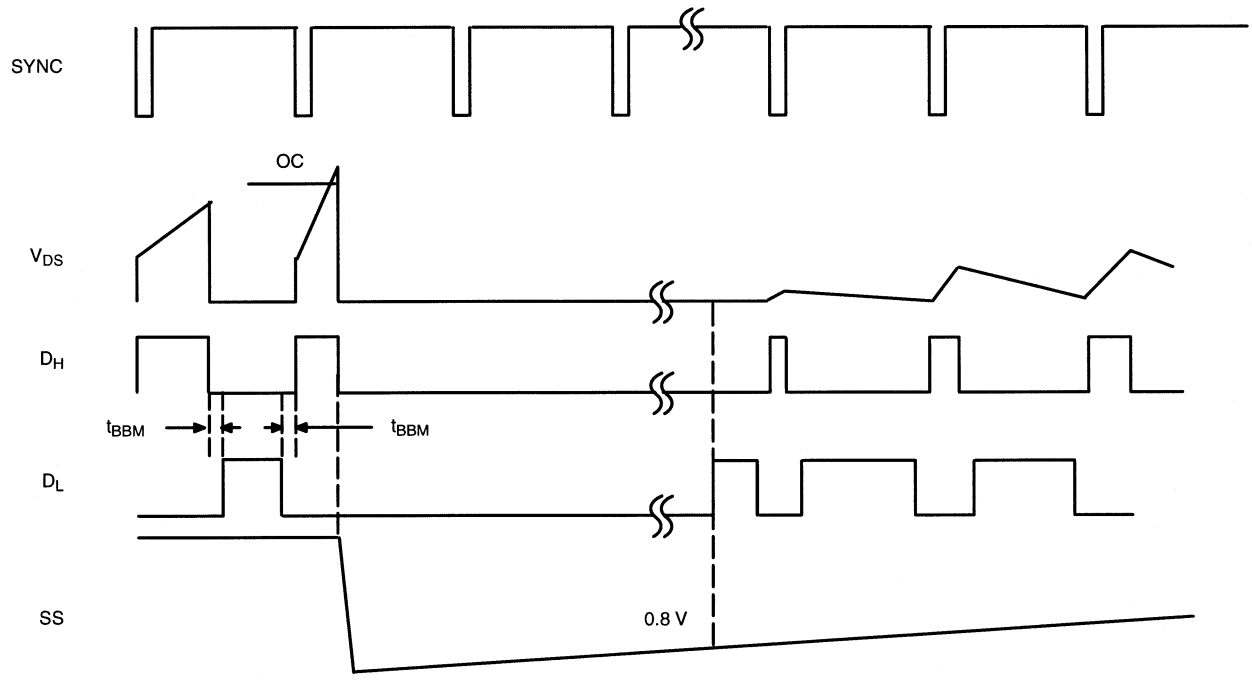


FIGURE 3. OCP Timing Diagrams

DESCRIPTION OF OPERATION

The Si9143 is a voltage mode synchronous buck controller designed to power a high performance microprocessor power supply. The voltage mode control provides efficiency and cost saving advantages over current mode control in high output current converters by eliminating the current sense resistor. The Si9143 provides ultra-fast (5-µsec) transient response time and all the necessary protection circuits demanded by microprocessor supply designers.

Pin 1. NI - Non-Inverting Input

NI is the non-inverting input of the error amplifier. For converter output voltages equal to or greater than 1.3 V, the NI pin can be connected directly to V_{REF}. For converter output voltages less than 1.3 V, the NI pin can be connected to V_{REF} through a voltage divider.

Pin 2. SS/Enable - Soft-Start/Enable

Soft-start is accomplished by connecting a capacitor from this pin to AGND. The soft-start functions as a constant current source into this capacitor. A logic low (v0.8 V) on this pin disables the output gate drives; the oscillator continues to function. A logic high (w2.4 V) enables the output gate drives, assuming the input voltage is above the UVLO threshold, and that no over-voltage or over-current condition exists.

Pins 3 and 4. FB and COMP - Error Amplifier

FB is the inverting input of the error amplifier. The voltage on this pin is also connected internally to the input terminals of the OVP and PWR_GOOD comparators for fault detection and protection. The error amplifier has 10-MHz gain-bandwidth when connected to a 20-pF load with 5-V input voltage. COMP is the output of the error amplifier. The output voltage is clamped at a maximum level to avoid long delays due to saturation during large transient conditions. The minimum COMP voltage is a diode drop below the 0% duty cycle voltage; the maximum voltage is a diode drop above the 94% duty cycle voltage.

Pins 5 and 6. V_{CC} - Input Voltage

Both V_{CC} pins should be connected to the input voltage for optimum performance. The input voltage range of the Si9143 is specified to operate with either +5 VDC or +12 VDC. In order to accommodate the tolerance of the +12 V, and the possibility of using this controller in 2-cell Li+ notebook applications with a battery charger, the input voltage is rated up to +15-V absolute maximum.

Pin 7. V_{REF} - Reference Voltage

The reference voltage is designed to produce 1.30 V ±1.6% over the line and temperature range, to produce equally tight output regulation of the converter. The reference should be decoupled with at least 100-nF capacitance. The reference is capable of driving 1mA of external load.

Pin 8. AGND - Analog Ground

AGND is the analog ground for the low power circuitry in the converter. This ground should be separated locally from PGND, and should have a separate run back to the input bypass capacitors.

Pin 9. R_{OSC} - Oscillator Timing Resistor

A resistor from this pin to AGND determines the internal switching frequency of the oscillator. The internal circuitry produces 10% frequency accuracy with a 1% timing resistor. The oscillator is capable of switching at up to 1 MHz.

Pin 11. SYNC - Synchronization

The SYNC signal is generated from the internal oscillator. When the oscillator is ramping positive, SYNC will be logic high; when the oscillator is ramping negative, SYNC will be logic low. The SYNC pin can be used to synchronize the Si9143 to an external clock. In particular, if several Si9143s have their SYNC pins shorted together, they will all switch at the same frequency and in phase, with the frequency being set by the fastest oscillator.

Pins 12 and 13. V_{SUPPLY} and V_{DRIVE} - External SCR Drive

V_{DRIVE} is intended to protect the converter's load from potentially damaging over-voltage. If the output voltage exceeds regulation by 17%, V_{DRIVE} goes high, driving an external SCR to blow a fuse. V_{SUPPLY} powers the V_{DRIVE} signal, and could be connected to a separate supply to ensure adequate gate drive.

Pin 14. PWR_GOOD - Open Collector Power Good Signal

This pin signals the status of the output voltage. The window comparator is set at ±12% of the voltage at the NI pin, with a tolerance of 5%. The PWR_GOOD signal is an open drain output capable of sinking 2 mA.

Pins 15 and 16. PGND - Power Ground

PGND is the power ground for the high power circuitry in the converter. This ground should be separated locally from AGND, and should have a separate plane run back to the input bypass capacitors.

Pins 17 and 21. D_H and D_L - High- and Low-Side Gate Drives

D_H is the high-side and D_L the low-side gate drive to the external MOSFETs. Both can source and sink 2.5-A peak with 4.5-V gate drives. The timing sequence of high- and low-side gate drives is shown in Figure 1. The internal break-before-make time interval (t_{BBM}) of 55 nsec prevents shoottthrough current in the external MOSFETs. The ringing from the gate drive output's trace inductance can produce negative voltages on D_H and D_L as much as 2-V negative with respect to PGND.

The gate drive circuit is capable of withstanding these negative voltages without any functional defects.

Pins 18 and 19. $V_{L(out)}$ and $V_{L(in)}$ - 5.5-V Linear Regulator

$V_{L(out)}$ produces a +5.5-V output used as the gate drive voltage for both the high- and low-side external MOSFETs. The gate drive voltage for the high-side MOSFET is bootstrapped ($V_{L(out)}$ - V_{DIODE}) above the input voltage. $V_{L(out)}$ should be bypassed with at least 4.7 µF of decoupling capacitance, and should not be used for any other external loads. $V_{L(in)}$ drives the internal circuitry. It should be connected through an RC filter to $V_{L(out)}$.

Pin 20. LX - Inductor Node

The LX node is used internally to float the high-side n-channel MOSFET gate drive. During the on-time of this MOSFET, the gate to source voltage will be ($V_{L(out)}$ - V_{DIODE}). The LX node is also used internally as the negative sense voltage for over-current protection.

Pin 22. BST - Bootstrap Voltage

The external high-side n-channel MOSFET gate drive voltage is derived by bootstrapping the $V_{L(out)}$ voltage on top of the input supply voltage. The external 100-nF capacitor connected across the BST and LX pins is charged to ($V_{L(out)}$ - V_{DIODE}) when the external low-side MOSFETs are on. Then, when the low-side MOSFETs are turned off, BST is internally connected to D_H in order to turn on the high-side MOSFET. D_L is turned on at startup to ensure initial charging of the BST capacitor.

Pin 23. ICS - Programmable Over-Current Protection

The over-current protection circuit senses the voltage across the external high-side n-channel MOSFET to determine the presence of an over-current condition. Current sensing occurs only during the on-time of this MOSFET. The trigger level of the over-current circuit is programmable by selecting the external resistor value connected from V_{CC} to I_{CS}. Once the over-current circuit has been triggered, it disables both output gate drives within 250 nsec. The circuit also discharges the soft-start capacitor as shown in the timing diagram in Figure 3.

Pin 24. PWM - PWM Comparator Output

The PWM signal is used to provide true current sharing when multiple Si9143s are used in a system; the PWM pins must all be shorted together to enable this feature. The PWM signal is internally configured as an open-drain output forming an AND gate to the logic section. Thus, all of the Si9143s will have precisely the same duty cycle, determined by the IC with the shortest duty cycle, permitting the true current sharing.

Under Voltage Lock-Out (UVLO)

The internal UVLO circuit is designed to prevent a converter from starting when insufficient input voltage is present. UVLO disables the oscillator, soft-start and output drives of the Si9143 until $V_{L(out)}$ reaches 3.8 V; see Figure 1. The UVLO circuit has 200-mV hysteresis to prevent turn-on and -off oscillations. When the oscillator is disabled, the Si9143 is in stand-by mode, and consumes only 150 µA of supply current.

Start-up Timing Sequence

Please refer to Figure 1 for this description. When V_{CC} reaches 4 V, $V_{L(out)}$ produces at least 3.8 V, and V_{REF} has stabilized and is regulating. The UVLO circuit enables the oscillator and the soft-start circuits. Once the soft-start voltage exceeds 1.5 V, the gate drive pulses begin, with the duty cycle of the high-side MOSFET beginning at 0% and gradually increasing until the output voltage is in regulation.

APPLICATIONS

Current Sharing

The Si9143 is designed to permit true load current sharing between multiple paralleled voltage-mode controllers. Traditional voltage-mode controllers do not support load sharing at all—the controller with the highest output voltage will attempt to provide all the load current. Even current-mode controllers do not properly share unless their error amps are tied together.

The Si9143 is a new concept in current sharing (Pat. Pend.) that works by forcing the duty cycles of multiple controllers to be identical. This is accomplished by tieing together the PWM and SYNCH pins of all the controllers. The SYNCH pins force each controller to start their duty cycle at the same time, which is to say that they all run at the same frequency and phase; the controller with the highest frequency controls all of the others. The PWM pins force each controller to finish their duty cycle at the same time, causing them to have exactly equal duty cycles; the controller with the smallest duty cycle controls all of the others.

The current that each converter delivers will thus be 1/N of the total current, if there are N total converters in parallel. Limitations to this scheme are dependent primarily on matching of the resistances in the converter: mismatch in resistance results in one converter delivering more current than another. However, this effect is minor for practical converter designs, and typical current sharing may be expected to be within 10%.

Paralleling and Redundancy

The Si9143 is specifically designed for paralleling converters, meaning that multiple converters run from the same power source and deliver power to the same output bus (see Figure 4). The typical reason for such an arrangement is a limitation in how much power a single converter is able to deliver. The limitations are often thermal, and arise for example from finite on-resistance of available MOSFETs, causing them to self-heat. More power cannot then be derived

from the single converter, as it would result in thermal runaway of the devices.

Although the Si9143 is not specifically designed for redundancy, it may still be usefully used in some such situations. Redundancy refers to a power system design in which the failure of a single converter does not interfere with the continuous delivery of power to a load, the current being sourced from other paralleled converters. Paralleled converters are thus necessary, but not sufficient, for a redundant system: A redundant system must also have some way of preventing a failed converter from affecting the other converters and the output power bus.

In a redundant power system utilizing the Si9143, isolation of shorted converters is accomplished by orring diodes (see Figure 5). If, for example, an output capacitor or low-side MOSFET on one of the supplies failed short, the diode prevents the other converters from sourcing current into it, and thus the output power bus remains up. If a converter fails by having its output go high, for example by having the high-side MOSFET fail shorted, the V_{DRIVE} pin goes high, firing an SCR that blows out an input fuse, disconnecting the power from the failed MOSFET.

Orring Diodes and Remote Sensing

In a typical paralleled converter application, outputs of multiple Si9143 converters can be simply attached together. Since the converters have true current sharing, orring diodes are unnecessary. This makes it possible to do remote sensing: the feedback node for the output voltage for the converters can be right at the load, eliminating voltage droop between the converter output and the load.
For a redundant system, orring diodes are necessary to isolate failed converters. Voltage feedback must be done inside the diode, so that each controller can determine if its own converter is causing an overvoltage condition. Although there will be some degradation of regulation due to the forward voltage of the diode and its temperature dependence, such degradation can be minimized by using a high performance Schottky, such as the Motorola MBRB2515L. This type of part has extremely low V_f, minimizing power loss, and very little variation of V_f with current or temperature.

Driving the SCR

The Si9143 provides a separate driver for driving the gate of an SCR in the event of an output overvoltage in a redundant system. The driver can source 1 mA, which is sufficient to drive a sensitive gate SCR. If a normal SCR is used, it is necessary to buffer the driver, which can be done as shown in Figure 6.

Setting the Current Limit

The current limit is set by comparing the voltage drop across the external high-side n-channel MOSFET with the voltage dropped across a sense resistor connected between V_{CC} and I_{CS}. The I_{CS} pin draws a constant current, and thus the equation governing the overcurrent threshold is:

$$170\ \mu A \times R = I_{Limit} \times R_{MOSFET}$$

Once the on-state resistance of the MOSFET is known, R can be selected to set the desired current limit. One caution is in order: since the MOSFET will normally be quite warm, the resistance used in the equation should be the maximum resistance at elevated temperatures, not typical resistance at 25°C. The designer should also leave adequate margin above the normal output current, both to account for tolerances and noise in the IC, as well as to permit any initial high currents while charging output capacitors.

The Boost Diode

The application circuit shows the use of a 1N4148 diode for the boost circuit. This provides a low-cost component for this application. However, it may be advantageous in some circuits to use a Schottky diode instead. The difference is that the Schottky has less forward drop than the regular rectifier, and this in turn means a somewhat greater gate drive voltage for the external high-side MOSFET. For MOSFETs with high gate threshold and/or low transconductance, the additional gate drive may prove very beneficial in terms of the heating of the MOSFET, and in turn the efficiency of the converter. A ½-A, 30-V Schottky works well in this application.

Grounding

The Si9143 is provided with both analog and power ground pins (AGND and PGND, respectively). Because of the high gate drive currents the Si9143 can source, it is essential that these two grounds be separated. PGND should be attached to the source of the external low-side MOSFET; AGND should be attached to the small-signal components of the circuit, such as the timing resistor and the feedback resistor. Each of these grounds should be run back independently to the input line capacitors, to avoid ground loops.

APPLICATIONS

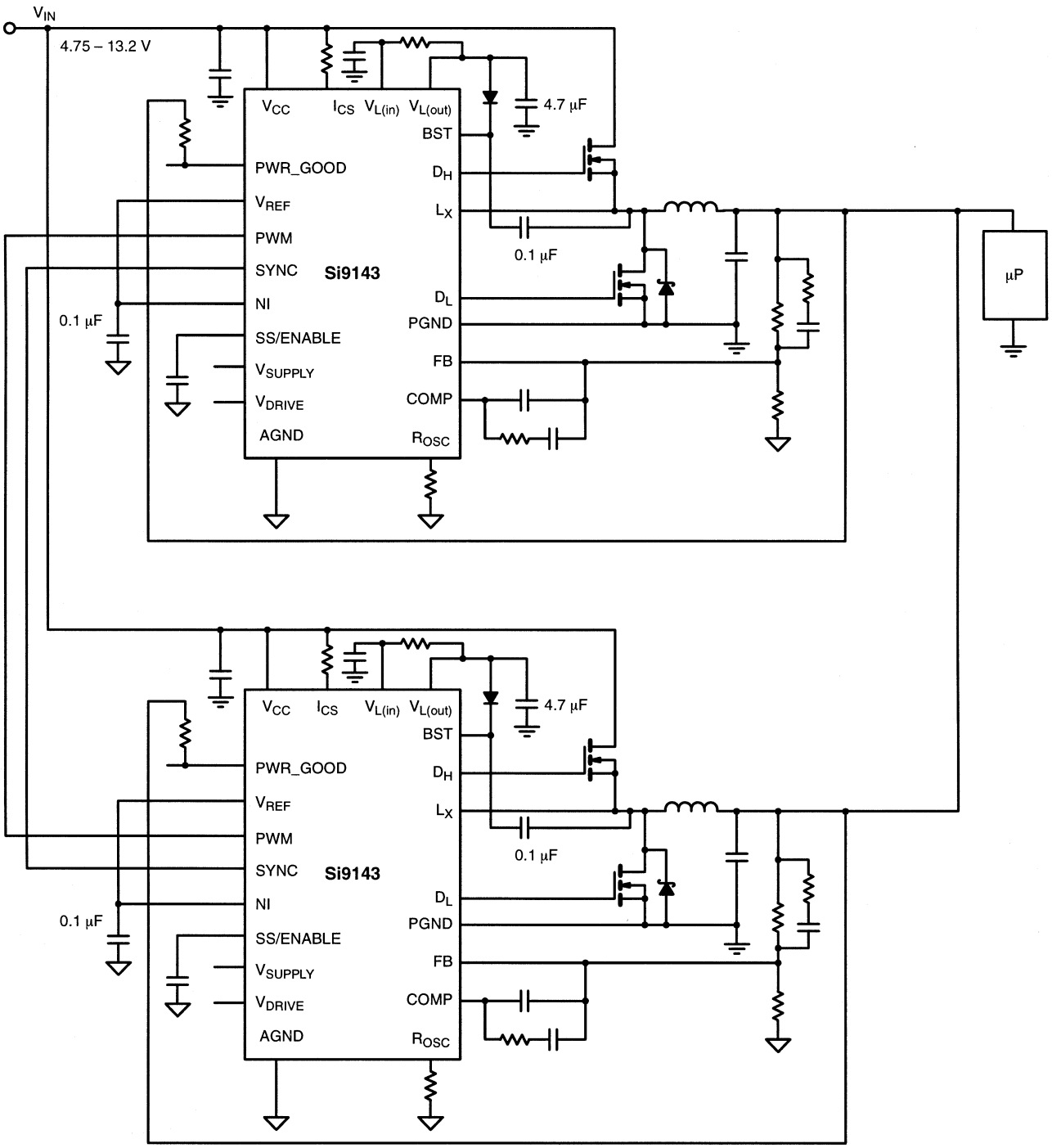


FIGURE 4. Paralleled Converters

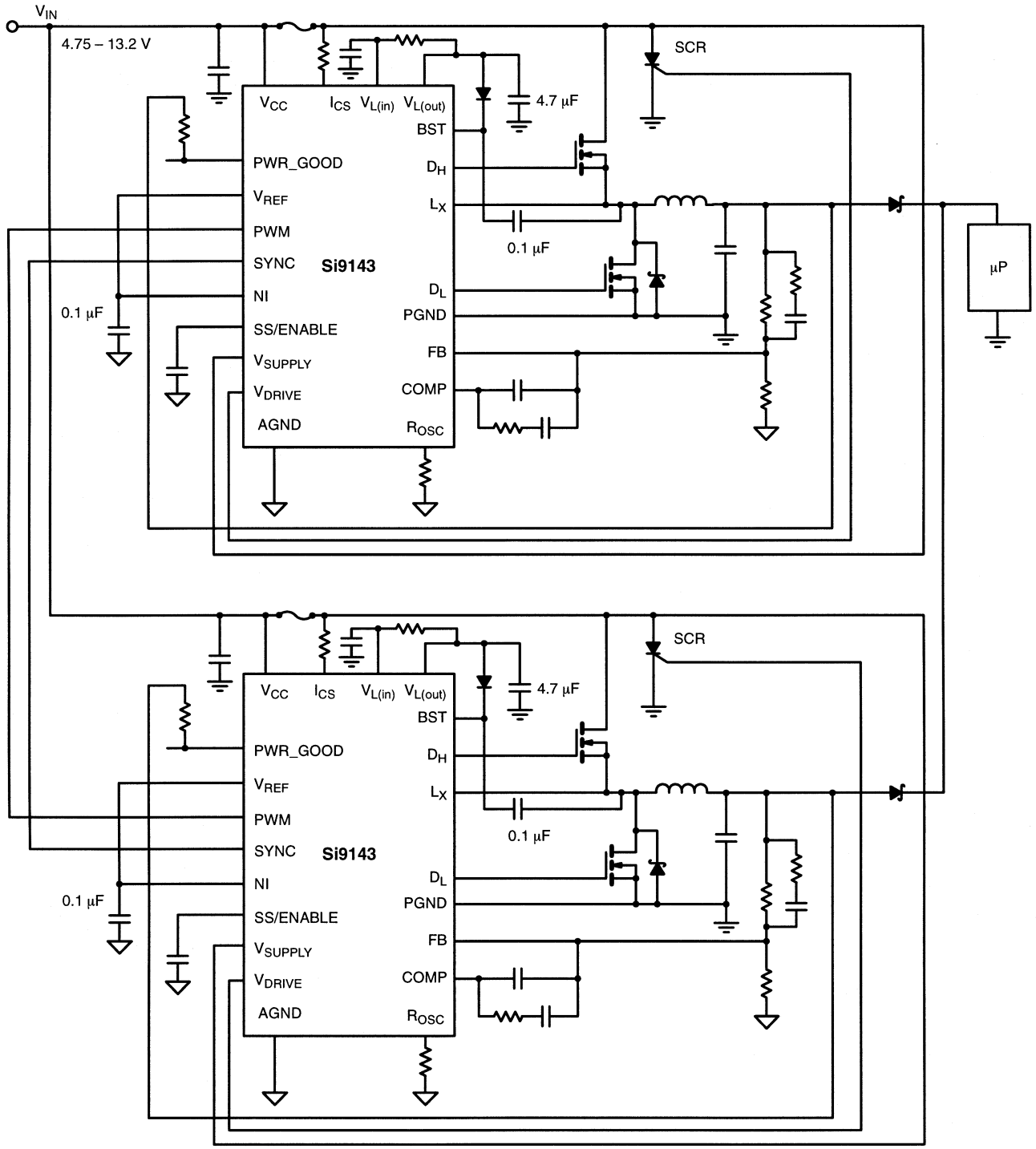


FIGURE 5. Paralleled Converters with Fault Protection

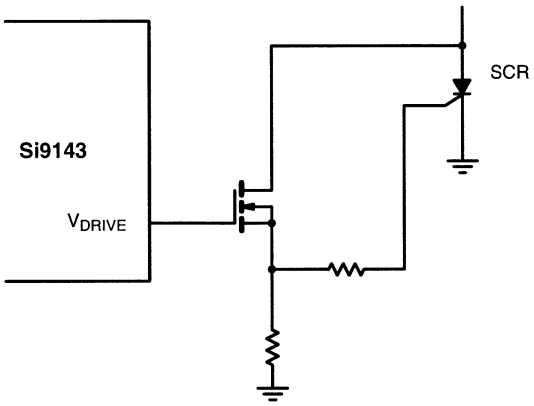


FIGURE 6. Driving a High-Current SCR Gate