

SANYO Semiconductors

DATA SHEET

LA6575H —

Monolithic Digital IC

Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

Overview

The LA6575H is a five-channel motor driver IC for MD and CD players with four BTL channels and one H bridge channel for the loading motor. It features a built-in 5 V regulator circuit.

Functions and Features

- Four power amplifier channels plus one H bridge channel
- I_O max: 700 mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- One muting circuit system (output on/off control): applies to the BTL amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 5 V regulator

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V _{CC} max		14	V	
Allews ble serves discinction	Independent IC		0.82	10/	
Allowable power dissipation	Pdmax	* Mounted on a board.	2.0	W	
Maximum output current	I _O max	Each channel for CH1 to CH5	0.7	Α	
Maximum input voltage	VINB		13	V	
MUTE pin voltage	VMUTE		13	V	
Operating temperature	Topr		-30 to +85	°C	
Storage temperature	Tstg		−55 to +150	°C	

Note *: Mounted on a board (76.1 × 114.3 × 1.6 mm) Material: glass epoxy

Recommended Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		5.6 to 13	V

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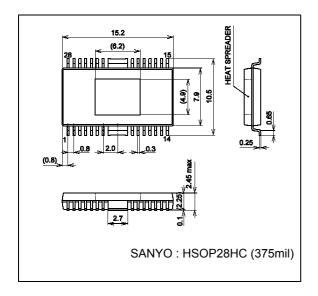
Electrical Characteristics (Unless specified otherwise, the conditions are Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8$ V, $V_{REF} = 1.65$ V)

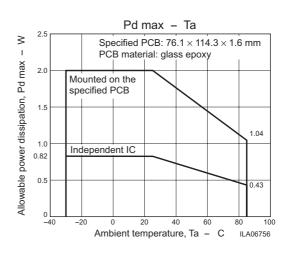
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Parameter	Symbol	Symbol Conditions		typ	max	Unit
[Overall Characteristics]						
No load current drain - ICC on	I _{CC} -ON	All outputs on, FWD = REV = 0 V *1		30	50	mA
No load current drain - ICC off	I _{CC} -OFF	All outputs off, FWD = REV = 0 V *1		10	20	mA
VREF input voltage range	VREF-IN		1		V _{CC} -1.5	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	BTL amplifiers, the voltage difference across each channel's output	-50		+50	mV
Input voltage range	V _{IN}	Input voltage range	0		V _{CC}	V
Output voltage	Vo	The voltage between each of the V _O +/V _O – pairs when R _L is 8 Ω . *2	4	5		V
Closed loop voltage gain	VG	Gain from input to output	3.5	4	4.5	Multi- plier
Slew rate	SR	With the amplifier operating independently, twice the value measured between outputs *4		0.5		V/μs
Mute on voltage	VMUTE-ON	Each Mute *3			0.5	V
Mute off voltage	VMUTE-OFF	Each Mute *3	2			V
[H Bridge Block]						
Output voltage	V _O -LOAD	The voltage between each of the V _O +/V _O - pairs when R _L is 8 Ω .	5.6	6		٧
Low-level input voltage	V _{IN} -L				1	٧
High-level input voltage	V _{IN} -H		2			V
[Regulator Block]						
Output voltage	Vreg	I _L = 100 mA	4.75	5	5.25	V
Load regulation	ΔVRL	I _L = 0 to 200 mA	-50	0	+10	mV
Line regulation	ΔVVCC	$V_{CC} = 6 \text{ to } 12 \text{ V}, I_L = 100 \text{ mA}$	-15	+21	+60	mV

- Note *1: The total current drain for $V_{\mbox{\footnotesize{CC}}}1$ and $V_{\mbox{\footnotesize{CC}}}2$ with no load.
 - *2: Voltage difference across the load (8 Ω). With the outputs in the saturated state.
 - *3: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off (high-impedance state).
 - *4: Design guarantee value

Package Dimensions

unit: mm 3234B





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Pin Functions

Pin No.	Symbol	Pin descriptions			
1	V _{CC} 2	Channel 5 power supply			
2	V _O 5–	Loading output (–)			
3	V _O 5+	Loading output (+)			
4	V _O 4+	Channel 4 output (+)			
5	V _O 4-	Channel 4 output (–)			
6	V _O 3+	Channel 3 output (+)			
7	V _O 3–	Channel 3 output (-)			
8	V _O 2+	Channel 2 output (+)			
9	V _O 2-	Channel 2 output (-)			
10	V _O 1+	Channel 1 output (+)			
11	V _O 1–	Channel 1 output (-)			
12	V _{CC} 1	Channels 1 to 0 4 (BTL) power supply (This pin must be shorted to V _{CC} -S)			
13	V _{IN} 1	Channel 1 input			
14	V _{IN} 1G	Channel 1 input (gain adjustment input)			
15	V _{IN} 2	Channel 2 input			
16	V _{IN} 2G	Channel 2 input (gain adjustment input)			
17	V _{IN} 3	Channel 3 input			
18	V _{IN} 3G	Channel 3 input (gain adjustment input)			
19	REG-IN	Regulator input (external pnp transistor base)			
20	REG-OUT	Regulator output (external pnp transistor collector)			
21	VREF-IN	Reference voltage input			
22	V _{CC} -S	Signal system power supply (This pin must be shorted to V _{CC} 1.)			
23	V _{IN} 4G	Channel 4 input (gain adjustment input)			
24	V _{IN} 4	Channel 4 input			
25	MUTE	Channels 1 to 4 (BTL amplifiers) output on/off control			
26	S-GND	Signal system ground			
27	FWD	Channel 5 (VLO) output switching (FWD); loading block logic input			
28	REV	Channel 5 (VLO) output switching (REV); loading block logic input			

Note: • The center frame (FR) is used as the power system ground. Along with the signal system ground (S-GND), this level must be the lowest potential in the system.

 $[\]bullet$ The three power supply pins V_{CC}–S, V_{CC}1, and V_{CC}2 must be shorted together externally.

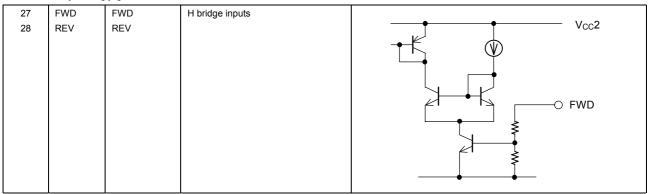
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Pin Functions

Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
13	V _{IN}	Inputs	Inputs	
14	V IIN	Inputo	mpate .	V _{IN} G O
15				V _{IN} GO
16				V _{CC} -S
17				
18				
23				
24				
				Vref
				\mathbb{V}
4	V _O	Outputs	Outputs	
5	VO	Outputs	Outputs	- Vcc1
6				\mathbb{V}
7				
8				▼ '
9				<u> </u>
10				OUT
11				
				<u> </u>
25	MUTE	Mute	ON/OFF each output	
			MUTE: H output ON	V S ()
			MUTE: L output OFF	Vcc-s O
				MUTE O S
				\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
				S-GND
2	V _O 5+ V _O 5-	V _O 5	H bridge outputs	V _{CC} ²
3	V _O 5–			
				√

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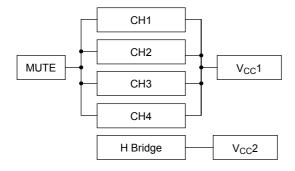


H Bridge Block

FWD	REV	V _O 5+	V _O 5-	Mode
L	L	OFF	OFF	Open *1
L	Н	Н	L	Forward
Н	L	L	Н	Reverse
Н	Н	L	L	Brake *2

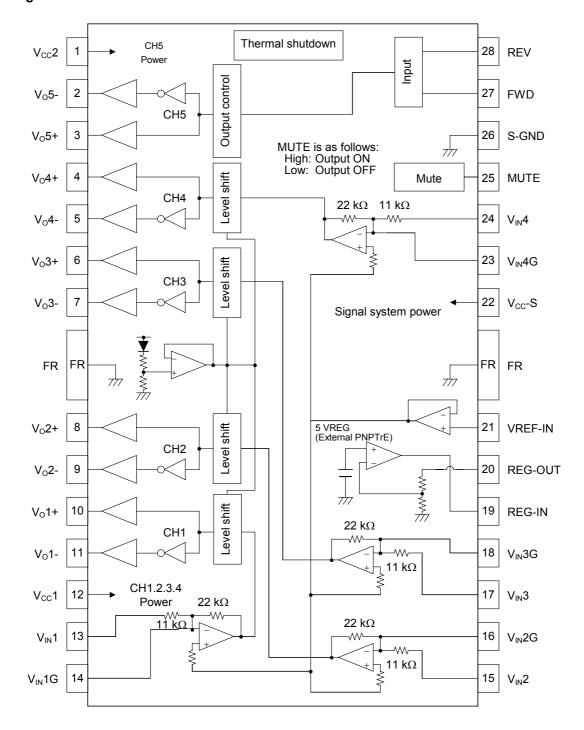
Note *1: The output are in the high-impedance state in this mode

Relationship between the MUTE pin and the power supplies (V_{CC}*)

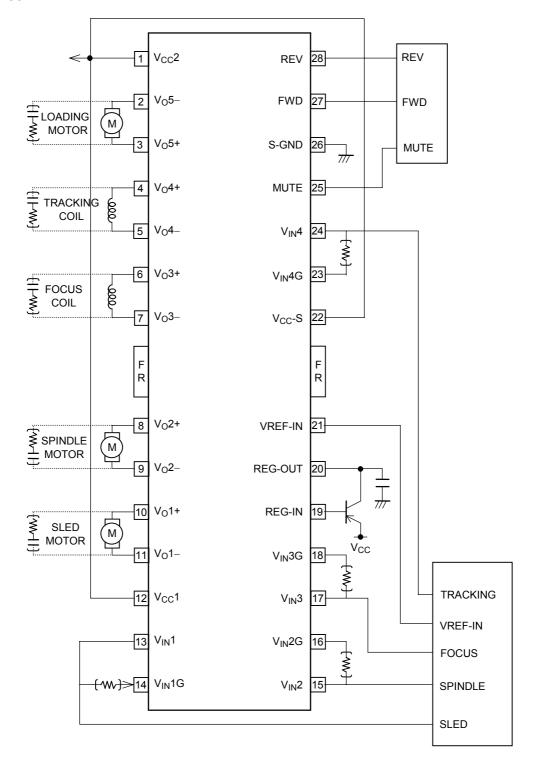


^{*2:} In brake mode, the sink side transistors are on (short-circuit braking). The VLO+ and VLO- levels go to a level essentially the same as the ground level.

Block Diagram



Sample Application Circuit



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