Integrated Circuit Systems, Inc.

ICS87946-01

LOW SKEW ÷1, ÷2 LVPECL-TO-LVCMOS/LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87946-01 is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87946-01 has one LVPECL clock input pair. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

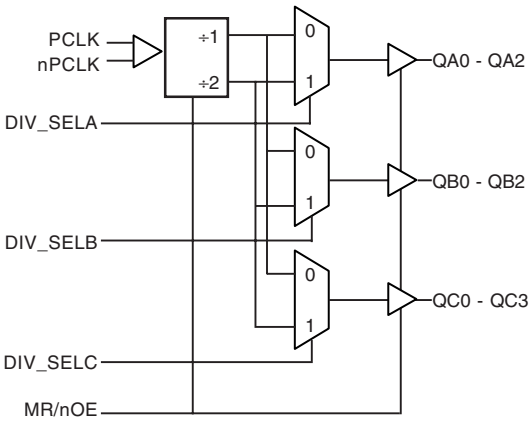
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87946-01 is characterized at 3.3V core/3.3V output and 3.3V core/2.5V output. Guaranteed bank, output and part-to-part skew characteristics make the ICS87946-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

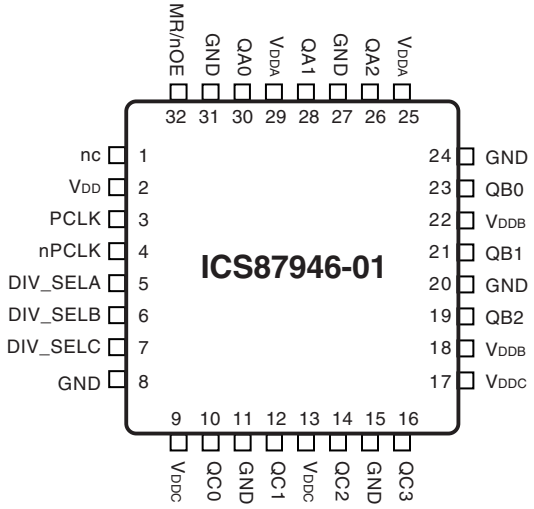
FEATURES

- 10 single ended LVCMOS outputs, 7Ω typical output impedance
- LVPECL clock input pair
- PCLK, nPCLK supports the following input levels: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 200ps (maximum)
- Part-to-part skew: 500ps (typical)
- Multiple frequency skew: 350ps (maximum)
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	nc	Unused		No connect.
2	V_{DD}	Power		Positive supply pins. Connect to 3.3V.
3	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground. Connect to ground.
9, 13, 17	V_{DDC}	Power		Positive supply pins for Bank C outputs. Connect to 3.3V or 2.5V.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Bank C outputs. LVCMOS interface levels. 7Ω typical output impedance.
18, 22	V_{DDB}	Power		Positive supply pins for Bank B outputs. Connect to 3.3V or 2.5V.
19, 21, 23	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS interface levels. 7Ω typical output impedance.
25, 29	V_{DDA}	Power		Positive supply pins for Bank A outputs. Connect to 3.3V or 2.5V.
26, 28, 30	QA2, QA1, QA02,	Output		Bank A outputs. LVCMOS interface levels. 7Ω typical output impedance.
32	MR/nOE	Input	Pulldown	Master reset and output enable. Resets outputs to tristate. Enables and disables all outputs. LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, *V_{DDx} = 3.465V		TBD		pF
R_{OUT}	Output Impedance			7		Ω

*NOTE: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.

TABLE 3. FUNCTION TABLE

Inputs				Outputs		
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	QA0 - QA2	QB0 - QB2	QC0 - QC3
1	X	X	X	Hi Z	Hi Z	Hi Z
0	0	X	X	fIN/1	Active	Active
0	1	X	X	fIN/2	Active	Active
0	X	0	X	Active	fIN/1	Active
0	X	1	X	Active	fIN/2	Active
0	X	X	0	Active	Active	fIN/1
0	X	X	1	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDx} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
*V_{DDx}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Core Supply Current			41		mA
**I_{DDx}	Output Supply Current			8		mA

*V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.
**I_{DDx} denotes I_{DDA}, I_{DDB}, I_{DDC}.

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, MR/nOE	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	V
I_{OZH}	Output Tristate Current High					TBD	V

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See page 7, Figure 1A, 3.3V Output Load Test Circuit.

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 250MHz		3.2		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 250MHz		3.2		ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDx}/2$			100	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDx}/2$			200	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDx}/2$			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDx}/2$		500		ps
t_R	Output Rise Time; NOTE 6	20% to 80%		700		ps
t_F	Output Fall Time; NOTE 6	20% to 80%		700		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz				ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz				ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDx}/2$.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDx}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
*V_{DDx}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Core Supply Current			41		mA
**I_{DDx}	Output Supply Current			8		mA

*V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.
**I_{DDx} denotes I_{DDA}, I_{DDB}, I_{DDC}.

TABLE 4E. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	V
I_{OZH}	Output Tristate Current High					TBD	V

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See page 7, Figure 1B, 3.3V/2.5V Output Load Test Circuit.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{DD} = V_{DDx} = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	V_{DD} = V_{IN} = 3.465V			150	µA
		nPCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 250MHz		3.2		ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f ≤ 250MHz		3.2		ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at V_{DDx}/2			100	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at V_{DDx}/2			200	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at V_{DDx}/2			350	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at V_{DDx}/2		500		ps
t_R	Output Rise Time; NOTE 6	20% to 80%		600		ps
t_F	Output Fall Time; NOTE 6	20% to 80%		600		ps
odc	Output Duty Cycle			50		%
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz				ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz				ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDx}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at V_{DDx}/2.
NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDx}/2.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

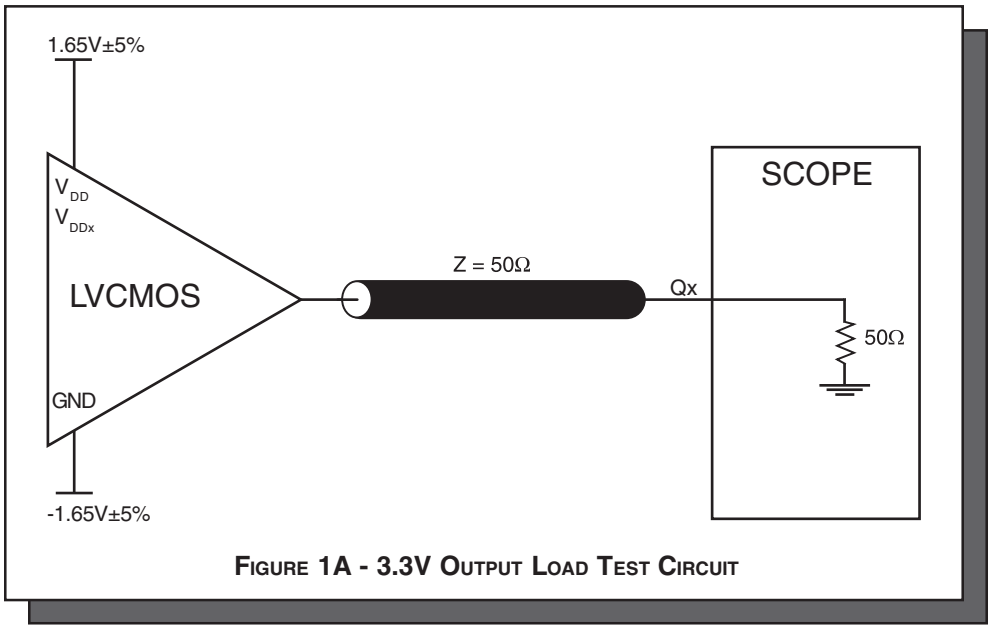


FIGURE 1A - 3.3V OUTPUT LOAD TEST CIRCUIT

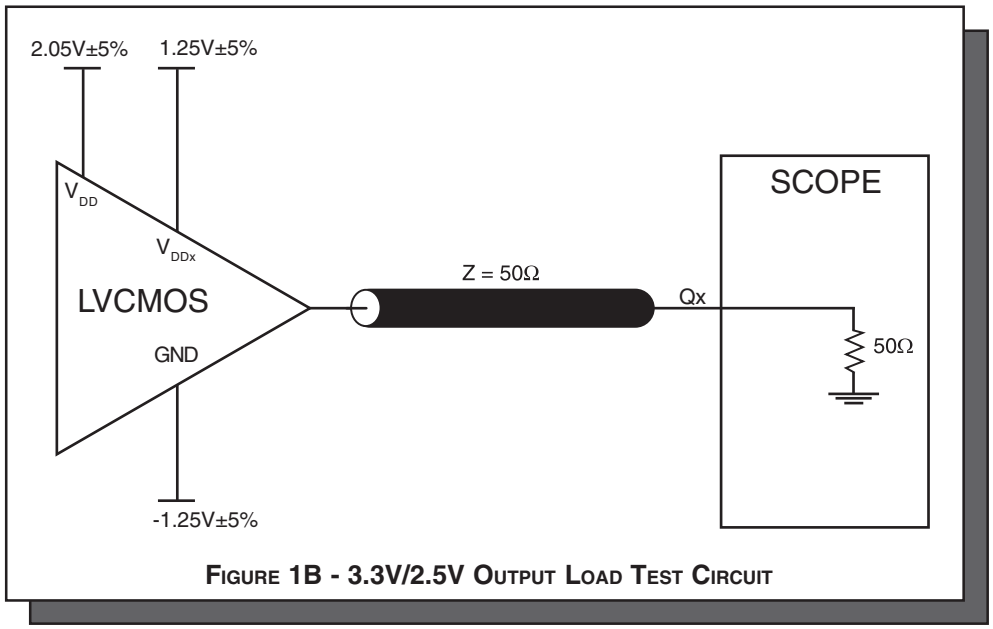


FIGURE 1B - 3.3V/2.5V OUTPUT LOAD TEST CIRCUIT

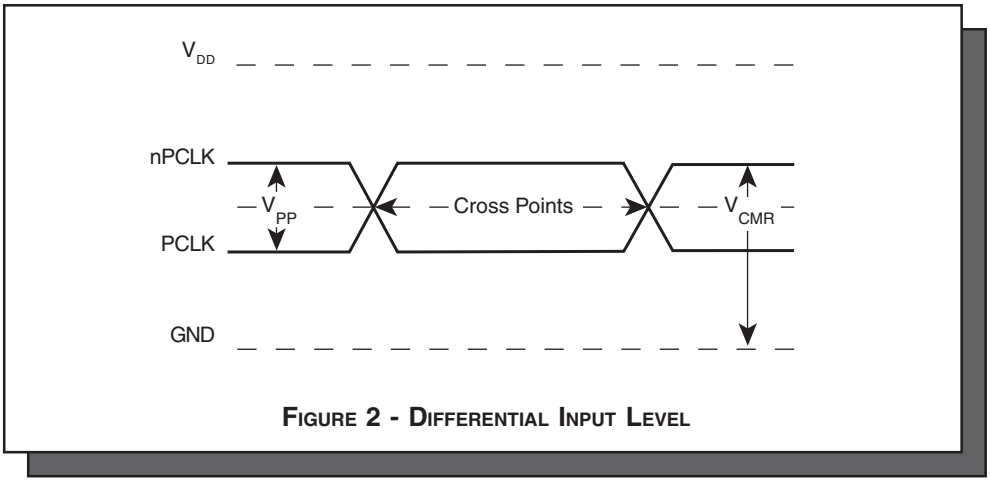


FIGURE 2 - DIFFERENTIAL INPUT LEVEL

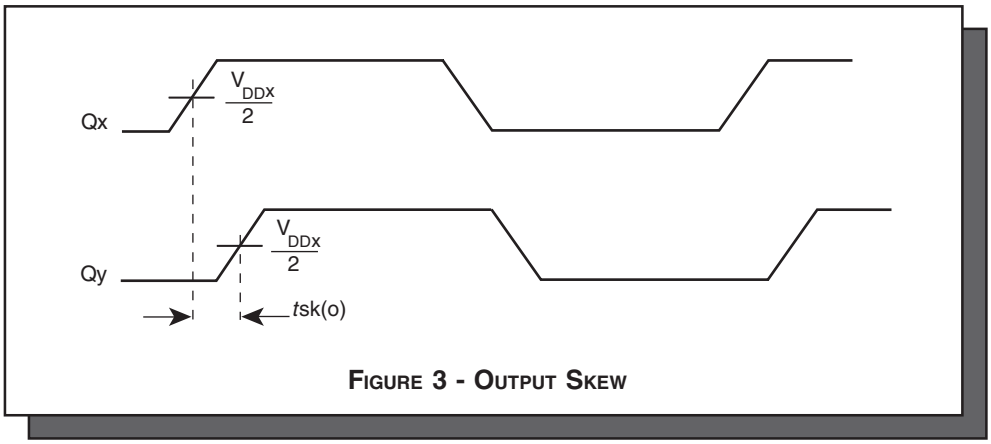


FIGURE 3 - OUTPUT SKEW

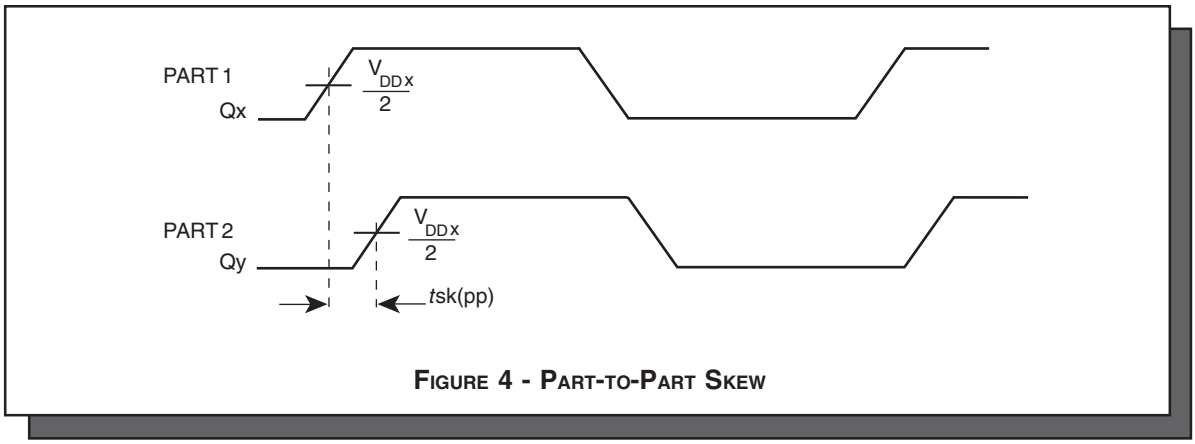


FIGURE 4 - PART-TO-PART SKEW

FIGURE 5 - INPUT AND OUTPUT RISE AND FALL TIME

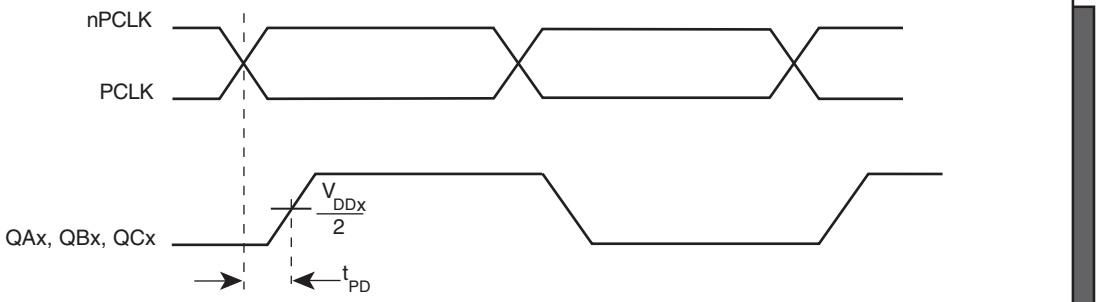


FIGURE 6 - PROPAGATION DELAY

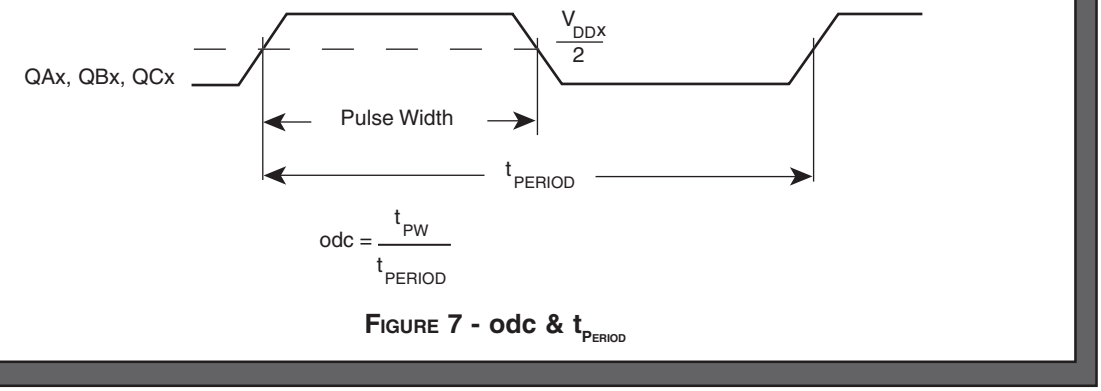


FIGURE 7 - odc & t_{PERIOD}

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

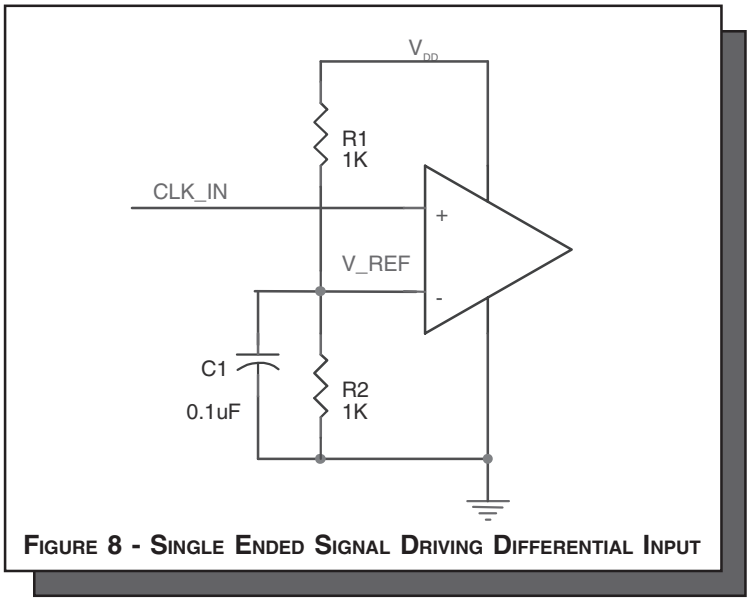


FIGURE 8 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87946-01 is: 1204

PACKAGE OUTLINE - Y SUFFIX

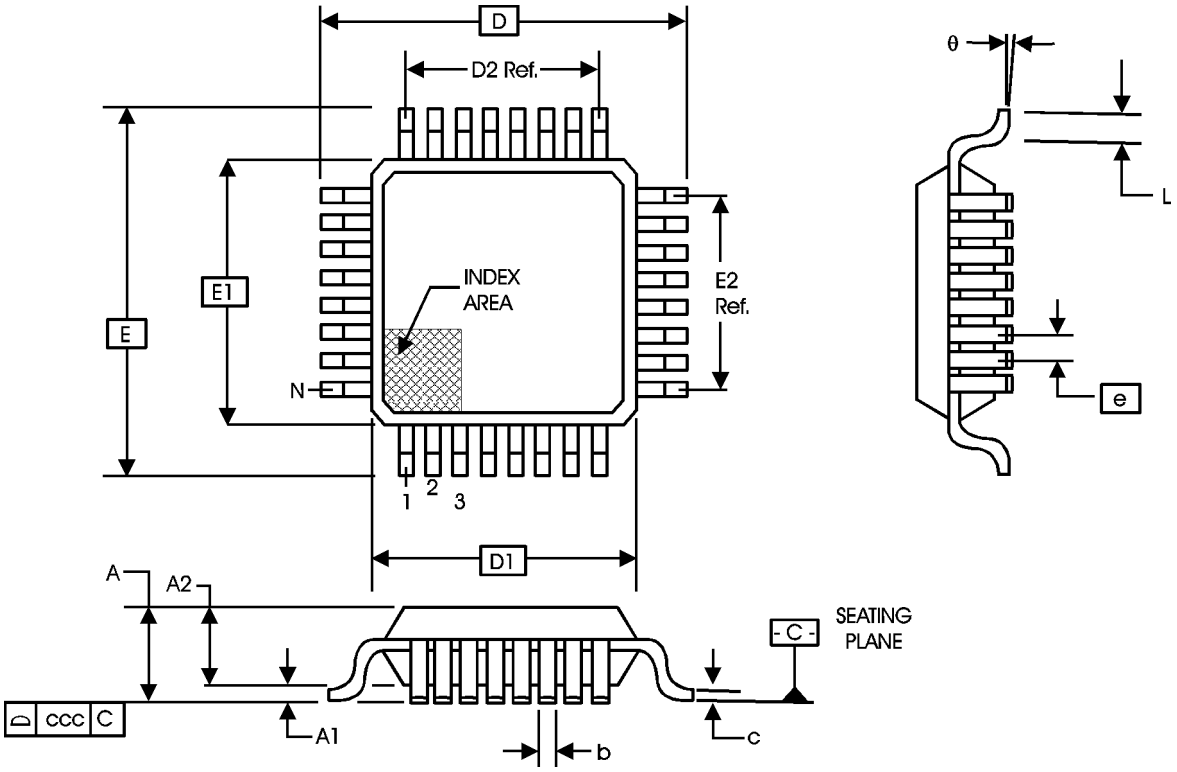


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87946AY-01	ICS87946AY-01	32 Lead LQFP	250 per tray	0°C to 70°C
ICS87946AY-01T	ICS87946AY-01	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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