

M50964-PGYS

PIGGYBACK for M50964-XXXSP, M50963-XXXSP

DESCRIPTION

The M50964-PGYS is an EPROM mounted-type micro-computer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputers the M50964-XXXSP/M50963-XXXSP. It is housed in a piggyback-type 64-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M50964-PGYS simplifies the development of programs for the M50964-XXXSP/M50963-XXXSP, and is excellent for making prototypes.

The differences between the M50964-XXXSP and the M50963-XXXSP are only ROM size.

Therefore the M50964-PGYS can be used for the development of programs for the M50964-XXXSP/M50963-XXXSP.

DISTINCTIVE FEATURES

- Differences with the M50964-XXXSP/M50963-XXXSP are:

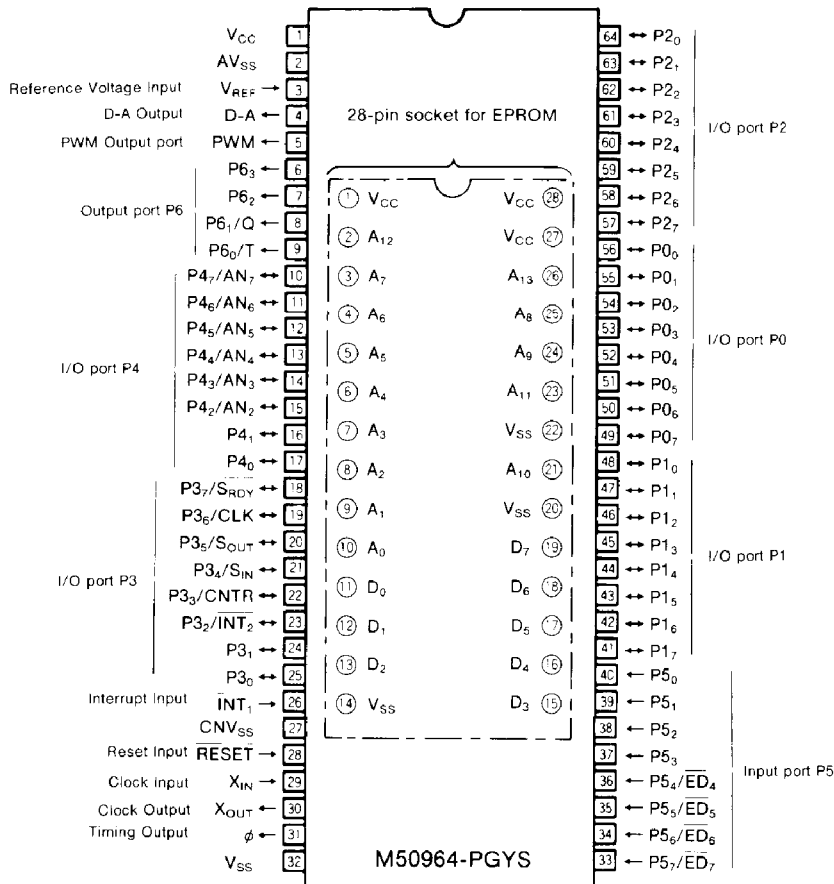
- (1) ROMless, EPROM is attached externally.
- (2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for the following systems;

- Office automation equipment
- VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol " " indicates sockets for EPROM.

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} V _{SS}	Supply voltage		Power supply inputs 5V±5% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is usually connected to V _{SS} .
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V _{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin.
INT ₁	Interrupt input	Input	This is the highest order interrupt input pin.
AV _{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters.
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A converter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
P3 ₀ ~P3 ₇	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, P3 ₇ , P3 ₆ , P3 ₅ , and P3 ₄ work as S _{RDY} , CLK, S _{OUT} , and S _{IN} pins, respectively. Also P3 ₃ and P3 ₂ work as CNTR pin and the lowest interrupt input pin (INT ₂), respectively.
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. P4 ₄ ~P4 ₇ work as analog input port AN ₄ ~AN ₇ .
P5 ₀ ~P5 ₇	Input port P5	Input	Port P5 is an 8-bit input port. P5 ₄ ~P5 ₇ can be used as the edge sense inputs.
P6 ₀ ~P6 ₃	Output port P6	Output	Port P6 is a 4-bit output port. At external trigger output mode, P6 ₀ and P6 ₁ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
A ₀ ~A ₁₃	Output port A	Output	These are for addresses to an EPROM mounted on the package.
D ₀ ~D ₇	Input port D	Input	These are for input data from an EPROM mounted on the package.

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BASIC FUNCTION BLOCK

The differences between the M50964-PGYS and the M50964-XXXSP/M50963-XXXSP are noted below. The following explanations apply to the M50964-PGYS. Specification variations for other chips are noted accordingly.

MEMORY

The memory map is shown in Figure 1. The M50964-PGYS is mounted an EPROM instead of an internal ROM. The address of an EPROM is C000₁₆ ~ FFFF₁₆, and this memory size is 16384 bytes. Other than these, the M50964-PGYS has the same functions as the M50964-XXXSP/M50963-XXXSP have.

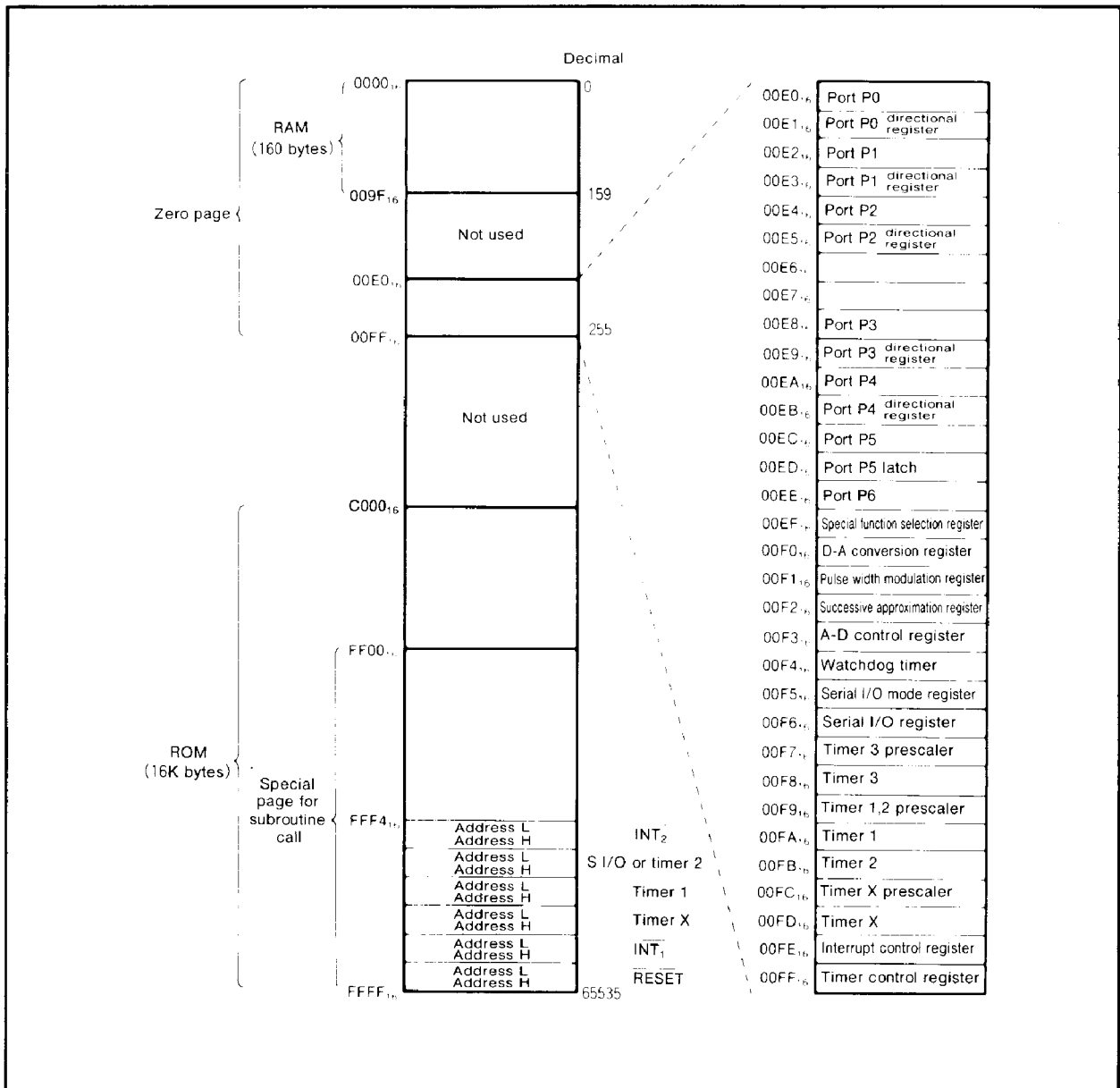


Fig.1 Memory map

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PROCESSOR MODE

External memory area differs from the M50964-XXXSP/ M50963-XXXSP in the memory expanding mode.
External memory map in the memory expanding mode is shown in Figure 2.

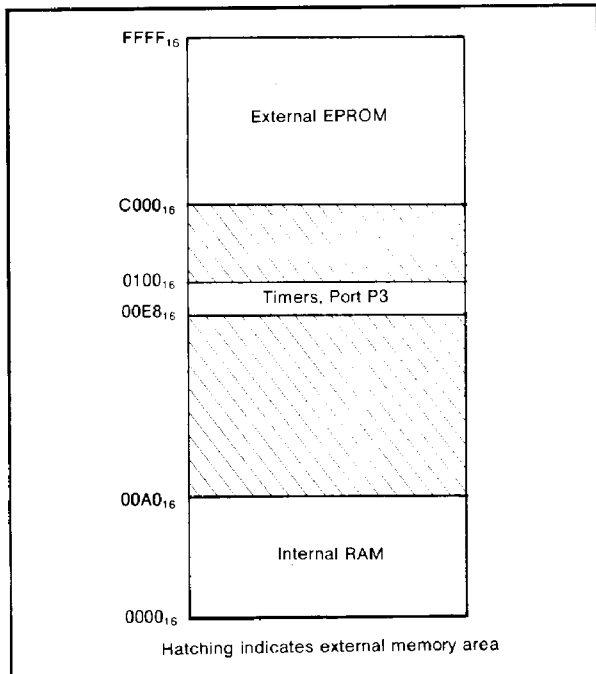


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

- (1) In case of the M5L2764K or the M5L27128K EPROM use the following areas (refer to Figure 1):
 - For the M50964-XXXSP, usable ROM area are
E800₁₆~FFFF₁₆.
M5L2764K..... addresses 0800₁₆~1FFF₁₆
M5L27128K..... addresses 2800₁₆~3FFF₁₆
 - For the M50963-XXXSP, usable ROM area are
D800₁₆~FFFF₁₆.
M5L27128K..... addresses 1800₁₆~3FFF₁₆
- (2) The M50964-PGYS has no options as the M50964-XXXSP/M50963-XXXSP. But, the M50964-PGYS can use the STP instruction.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~7	V
V_I	Input voltage X_{IN}		-0.3~7	V
V_I	Input voltage $P2_0\sim P2_7, P4_2\sim P4_7$		-0.3~ $V_{CC}+0.3$	V
V_I	Input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7$ $P4_0, P4_1, P5_0\sim P5_7, INT_1$	With respect to V_{SS} Output transistors cut-off	-0.3~13	V
V_I	Input voltage $CNV_{SS}, RESET$		-0.3~13	V
V_O	Output voltage $P2_0\sim P2_7, P4_2\sim P4_7, X_{OUT}, \phi, D-A$		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage $P0_0\sim P0_7, P1_0\sim P1_7, P3_0\sim P3_7$ $P4_0, P4_1, P6_0\sim P6_3, PWM$		-0.3~13	V
P_d	Power dissipation	$T_a=25^\circ C$	1000 (Note 1)	mW
T_{opr}	Operating temperature		-10~70	$^\circ C$
T_{stg}	Storage temperature		-40~125	$^\circ C$

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 5\%$, $T_a=-10\sim 70^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7$ $INT_1, RESET, X_{IN}, CNV_{SS}, P6_0$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0\sim P0_7$	0.45 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0\sim P0_7, P1_0\sim P1_7, P2_0\sim P2_7$ $P3_0\sim P3_7, P4_0\sim P4_7, P5_0\sim P5_7$ $INT_1, CNV_{SS}, P6_0$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage $RESET$	0		0.12 V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16 V_{CC}	V
V_{IL}	"L" output voltage $P0_0\sim P0_7$	0		0.15 V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0\sim P0_7, P1_0\sim P1_7$ $P2_0\sim P2_7, P3_0\sim P3_7$ $P4_0\sim P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0\sim P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0\sim P0_7, P1_0\sim P1_7$ $P2_0\sim P2_7, P3_0\sim P3_7$ $P4_0\sim P4_7$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0\sim P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0\sim P2_7$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P2_0\sim P2_7$ (Note 1)			-5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

- Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
 2 : Total of "L" output current I_{OL} of ports P0, P1, P2, P3, P4, P6, and PWM is 80mA max.
 Total of "H" output current I_{OH} of port P2 is 50mA max.
 3 : "H" input voltage of ports P0, P1, P3, P4₀~P4₃, P5, and INT₁ is available up to +12V.

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ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f_{XIN}=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V_{OH}	"H" output voltage P2 ₀ ~P2 ₇	$I_{OH}=-10mA$	3			V	
V_{OH}	"H" output voltage ϕ , A ₀ ~A ₁₃	$I_{OH}=-2.5mA$	3			V	
V_{OL}	"L" output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P6 ₀ ~P6 ₃	$I_{OL}=10mA$			2	V	
V_{OL}	"L" output voltage ϕ , PWM, A ₀ ~A ₁₃	$I_{OL}=5mA$			2	V	
$V_{T+}-V_{T-}$	Hysteresis INT ₁		0.3		1	V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₆	When used as CLK input	0.3	0.8		V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₂	When used as INT ₂ input	0.3		1	V	
$V_{T+}-V_{T-}$	Hysteresis P3 ₃	When used as CNTR input	0.5	1		V	
$V_{T+}-V_{T-}$	Hysteresis P6 ₀	When used as T input	0.5	1		V	
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V	
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.5	V	
I_{IL}	"L" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ P3 ₀ ~P3 ₇ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ P6 ₀ ~P6 ₃ , PWM	$V_i=0V$			-5	μA	
I_{IL}	"L" input current INT ₁ , RESET, X _{IN} , D ₀ ~D ₇	$V_i=0V$			-5	μA	
I_{IH}	"H" input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P3 ₀ ~P3 ₇ P4 ₀ ~P4 ₃ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₃ PWM	$V_i=12V$			12	μA	
I_{IH}	"H" input current INT ₁ , RESET, X _{IN} , P2 ₀ ~P2 ₇ P4 ₄ ~P4 ₇ , D ₀ ~D ₇	$V_i=5V$			5	μA	
V_{RAM}	RAM retention voltage	When clock stopped	2			V	
I_{CC}	Supply current	ϕ , X _{OUT} , and D-A pins opened, other pins at V_{SS} , and A-D converter in the finished condition.		$f_{XIN}=4MHz$ Square wave	3	6	mA
				When clock stopped		1	μA
				$T_a=25^\circ C$			
				When clock stopped		10	μA
				$T_a=75^\circ C$			

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f_{XIN}=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=AV_{SS}=0V$, $T_a=25^\circ C$, $f_{XIN}=4MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			± 1	%
t_{su}	Set up time	$V_{REF}=V_{CC}$			3	μs
R_o	Output resistance	$V_{REF}=V_{CC}$			3	k Ω
V_{REF}	Reference voltage		4		V_{CC}	V