NEC

MOS INTEGRATED CIRCUIT

μPD432232L

2M-BIT CMOS SYNCHRONOUS FAST SRAM
64K-WORD BY 32-BIT
PIPELINED OPERATION

Description

The μPD432232L is a 65,536-word by 32-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel four-transistor memory cell.

The μPD432232L integrates unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD432232L is suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State ("Sleep"). In the "Sleep" state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The μPD432232LGF is packaged in 100-pin plastic LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

Features

- 3.3 V (Chip) / 3.3V or 2.5V (I/O) Supply
- Synchronous Operation
- Internally self-timed Write control
- Burst Read / Write: Interleaved Burst and Linear Burst Sequence
- Fully Registered Inputs and Outputs for Pipelined operation
- All Registers triggered off Positive Clock Edge
- ★ Single-Cycle deselect timing
- 3.3 V or 2.5 V LVTTL Compatible: All Inputs and Outputs
- Fast Clock Access Time: 5 ns / 100 MHz, 7 ns / 83 MHz, 8 ns / 66 MHz
- Asynchronous Output Enable: /G
- Burst Sequence Selectable: MODE
- Sleep Mode: ZZ (ZZ =Open or Low: Normal Operation)
- Separate Byte Write Enable: /BW1 - /BW4, /BWE Global Write Enable: /GW
- Three Chip Enables for Easy Depth Expansion
- Common I/O Using Three State Outputs

Ordering Information

Part number	Access Time	Clock frequency	Package
μPD432232LGF-A5	5 ns	100 MHz	100-PIN PLASTIC LQFP (14 x 20)
μPD432232LGF-A7	7 ns	83 MHz	100-PIN PLASTIC LQFP (14 x 20)
μPD432232LGF-A8	8 ns	66 MHz	100-PIN PLASTIC LQFP (14 x 20)

Document No. M12180EJ6V0DSJ1 (6th edition)
Date Published November 2000 NS CP(K)
Printed in Japan

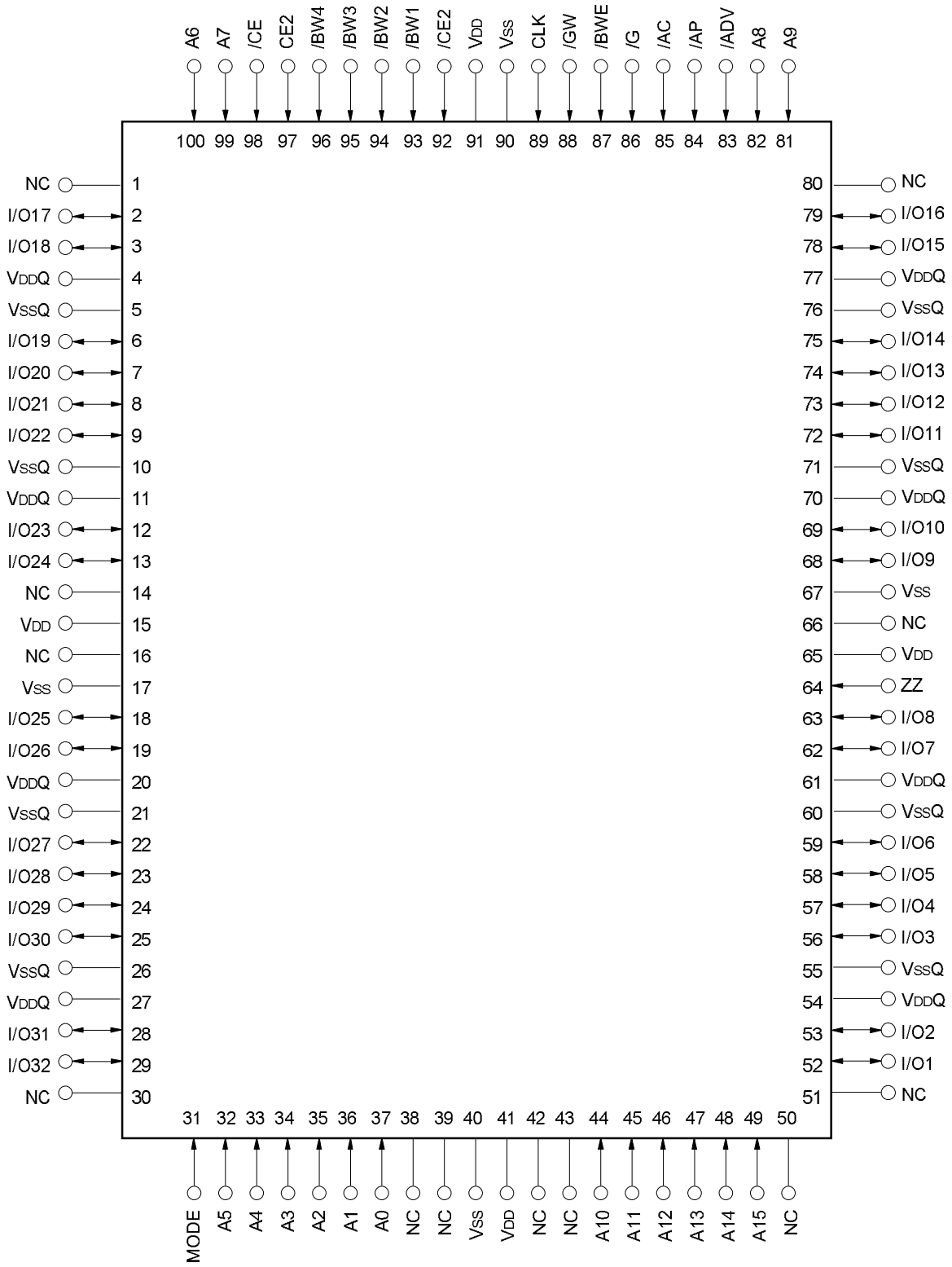
The mark ★ shows major revised points.

★ Pin Configuration (Marking Side)

/xxx indicates active low signal.

100-PIN PLASTIC LQFP (14 x 20)

[μPD432232LGF]

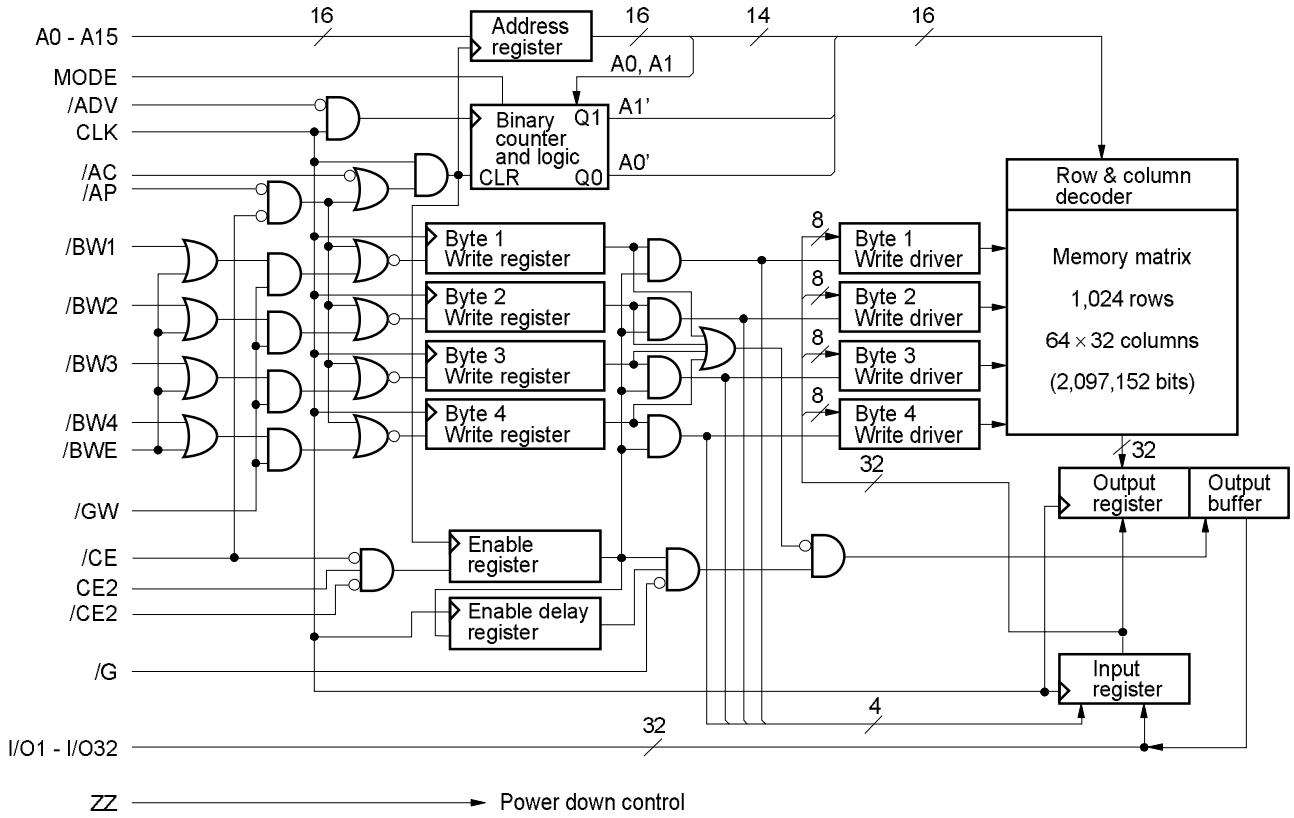


Remark Refer to **Package Drawing** for the 1-pin index mark.

Pin Identification

Symbol	Pin No.	Description
A0 - A15	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49	Synchronous Address Input
I/O1 - I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous / Asynchronous Data Out
/ADV	83	Synchronous Burst Address Advance Input
/AP	84	Synchronous Address Status Processor Input
AC	85	Synchronous Address Status Controller Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/BW1 - /BW4, /BWE	93, 94, 95, 96, 87	Synchronous Byte Write Enable Input
/GW	88	Synchronous Global Write Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
★ MODE	31	Asynchronous Burst Sequence Select Input Do not change state during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	15, 41, 65, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
V_{DDQ}	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
V_{SSQ}	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	1, 14, 16, 30, 38, 39, 42, 43, 50, 51, 66, 80	No Connection

Block Diagram



Burst Sequence

Interleaved Burst Sequence Table (MODE = Open or V_{DD})

External Address	A15 - A2, A1, A0
1st Burst Address	A15 - A2, A1, /A0
2nd Burst Address	A15 - A2, /A1, A0
3rd Burst Address	A15 - A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A15 - A2, 0, 0	A15 - A2, 0, 1	A15 - A2, 1, 0	A15 - A2, 1, 1
1st Burst Address	A15 - A2, 0, 1	A15 - A2, 1, 0	A15 - A2, 1, 1	A15 - A2, 0, 0
2nd Burst Address	A15 - A2, 1, 0	A15 - A2, 1, 1	A15 - A2, 0, 0	A15 - A2, 0, 1
3rd Burst Address	A15 - A2, 1, 1	A15 - A2, 0, 0	A15 - A2, 0, 1	A15 - A2, 1, 0

Asynchronous Truth Table

Operation	/G	I/O
Read Cycle	L	Dout
Read Cycle	H	Hi-Z
Write Cycle	X	Hi-Z, Din
Deselected	X	Hi-Z

Remark X means "don't care."

Synchronous Truth Table

Operation	/CE	CE2	/CE2	/AP	/AC	/ADV	/WRITE	CLK	Address
Deselected [Note]	H	X	X	X	L	X	X	L → H	N/A
Deselected [Note]	L	L	X	L	X	X	X	L → H	N/A
Deselected [Note]	L	X	H	L	X	X	X	L → H	N/A
Deselected [Note]	L	L	X	H	L	X	X	L → H	N/A
Deselected [Note]	L	X	H	H	L	X	X	L → H	N/A
Read Cycle / Begin Burst	L	H	L	L	X	X	X	L → H	External
Read Cycle / Begin Burst	L	H	L	H	L	X	H	L → H	External
Read Cycle / Continue Burst	X	X	X	H	H	L	H	L → H	Next
Read Cycle / Continue Burst	H	X	X	X	H	L	H	L → H	Next
Read Cycle / Suspend Burst	X	X	X	H	H	H	H	L → H	Current
Read Cycle / Suspend Burst	H	X	X	X	H	H	H	L → H	Current
Write Cycle / Begin Burst	L	H	L	H	L	X	L	L → H	External
Write Cycle / Continue Burst	X	X	X	H	H	L	L	L → H	Next
Write Cycle / Continue Burst	H	X	X	X	H	L	L	L → H	Next
Write Cycle / Suspend Burst	X	X	X	H	H	H	L	L → H	Current
Write Cycle / Suspend Burst	H	X	X	X	H	H	L	L → H	Current

Note Deselect status is held until new "Begin Burst" entry.

Remarks 1. X means "don't care."

2. /WRITE = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) and /BWE are LOW or /GW is LOW.

/WRITE = H means the following two cases.

(1) /BWE and /GW are HIGH.

(2) /BW1, /BW2, /BW3, /BW4 and /GW are HIGH, and /BWE is LOW.

Partial Truth Table for Write Enables

Operation	/GW	/BWE	/BW1	/BW2	/BW3	/BW4
Read Cycle	H	H	X	X	X	X
Read Cycle	H	L	H	H	H	H
Write Cycle / Byte 1 Only	H	L	L	H	H	H
Write Cycle / All Bytes	H	L	L	L	L	L
Write Cycle / All Bytes	L	X	X	X	X	X

Remark X means "don't care."

Pass-Through Truth Table

Previous Cycle				Present Cycle						Next Cycle
Operation	Add	/WRITE	I/O	Operation	Add	/CEs	/WRITE	/G	I/O	Operation
Write Cycle	Ak	L	Dn(Ak)	Read Cycle (Begin Burst)	Am	L	H	L	Q1(Ak)	Read Q1(Am)
				Deselected	-	H	X	X	Hi-Z	No Carry Over from Previous Cycle

Remarks **1.** X means "don't care."

2. /WRITE = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) and /BWE are LOW or /GW is LOW.

/WRITE = H means the following two cases.

(1) /BWE and /GW are HIGH.

(2) /BW1, /BW2, /BW3, /BW4 and /GW are HIGH, and /BWE is LOW.

/CEs = L means /CE is LOW, /CE2 is LOW and CE2 is HIGH.

/CEs = H means /CE is HIGH or /CE2 is HIGH or CE2 is LOW.

ZZ (Sleep) Truth Table

ZZ	Chip Status
≤ 0.2V	Active
Open	Active
≥ V_{DD} – 0.2V	Sleep

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+4.6	V	
Output supply voltage	V_{DDQ}		–0.5		V_{DD}	V	
Input voltage	V_{IN}		–0.5		V_{DD} + 0.5	V	1, 2
Input / Output voltage	$V_{I/O}$		–0.5		V_{DDQ} + 0.5	V	1, 2
Operating ambient temperature	T_A		0		70	°C	
Storage temperature	T_{stg}		–55		+125	°C	

Notes 1. –2.0 V (MIN.)(Pulse width : 2 ns)

2. V_{DDQ} + 2.3 V (MAX.)(Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

for 2.5 V LVTTL interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.1	3.3	3.6	V
Output supply voltage	V_{DDQ}		2.375	2.5	2.9	V
High level input voltage	V_{IH}		1.7		V_{DDQ} + 0.3	V
Low level input voltage	V_{IL}		–0.5 Note		+0.7	V

Note –0.8 V MIN. (Pulse Width : 2 ns)

for 3.3 V LVTTL interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.1	3.3	3.6	V
Output supply voltage	V_{DDQ}		3.1	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{DDQ} + 0.3	V
Low level input voltage	V_{IL}		–0.5 Note		+0.8	V

Note –0.8 V MIN. (Pulse Width : 2 ns)

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test conditions	MAX.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	pF
Input / Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	7	pF
Clock Input Capacitance	C_{clk}	V_{clk} = 0 V	4	pF

Remark These parameters are sampled and not 100% tested.

DC Characteristics (T_A = 0 to 70°C, V_{DD} = 3.1 to 3.6 V)

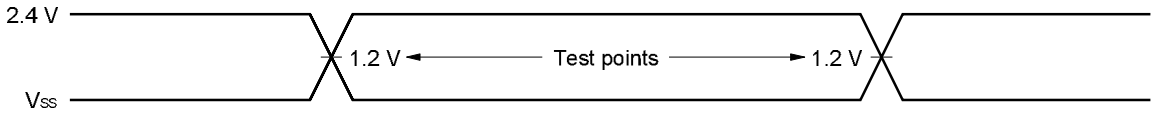
Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	I_{LI}	V_{IN}(except ZZ, MODE) = 0 V to V_{DD}	–2		+2	μA	
		ZZ, MODE = 0 V or V_{DD}	–5		+5		
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{DD}Q, Output disabled	–2		+2	μA	
Operating supply current	I_{DD}	Device selected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA			180	mA	
	I_{DD1}	Suspend cycle, Cycle = MAX. /AC, /AP, /ADV, /GW, /BWEs $\geq V_{IH}$ $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA			60		
Standby supply current	I_{SB}	Device deselected, Cycle = 0 MHz $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, All inputs static			20	mA	
	I_{SB1}	Device deselected, Cycle = 0 MHz $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{DD}$ – 0.2V, $V_{I/O} \leq$ 0.2 V, All inputs static		0.2	2.0		
	I_{SB2}	Device deselected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$			60		
Power down supply current	I_{SBZZ}	ZZ $\geq V_{DD}$ – 0.2V, $V_{I/O} \leq V_{DD}$Q + 0.2V		0.2	2.0	mA	
2.5 V LVTTL interface							
High level output voltage	V_{OH}	I_{OH} = –2.0 mA	2.1			V	
Low level output voltage	V_{OL}	I_{OL} = +2.0 mA			0.3	V	
3.3 V LVTTL interface							
High level output voltage	V_{OH}	I_{OH} = –4.0 mA	2.4			V	
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA			0.4	V	

AC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.1 to 3.6 V)

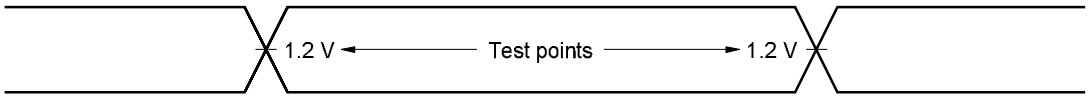
AC Test Conditions

2.5 V LVTTL interface

Input waveform (Rise / Fall time ≤ 2.4 ns)

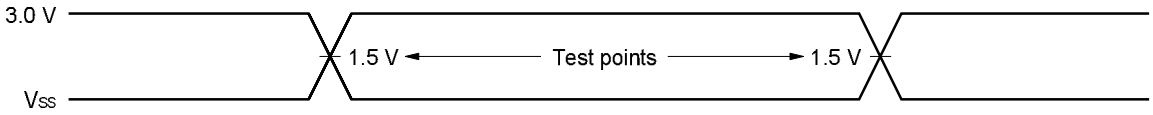


Output waveform

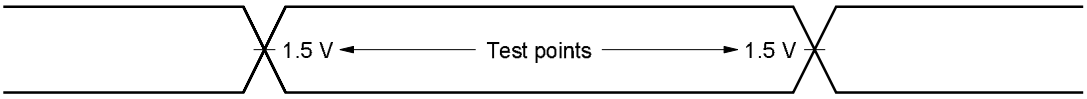


3.3 V LVTTL interface

Input waveform (Rise / Fall time ≤ 3.0 ns)



Output waveform

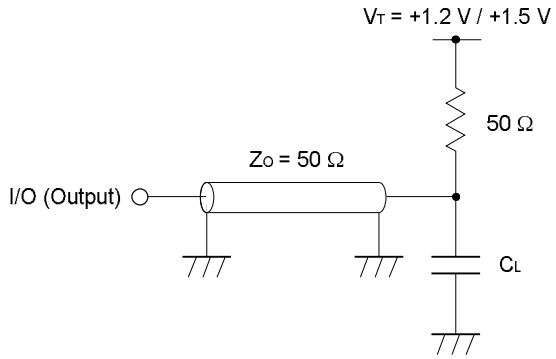


Output load condition

C_L : 30 pF

5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

External load at test



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle (2.5 V LVTTL interface)

Parameter		Symbol		-A5 (100 MHz)		-A7 (83 MHz)		-A8 (66 MHz)		Unit	Note
		Standard	Alias	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Cycle time		TKHKH	TCYC	10	–	12	–	15	–	ns	
Clock access time		TKHQV	TCD	–	5	–	7	–	8	ns	
Output enable access time		TGLQV	TOE	–	4.5	–	5	–	5	ns	
Clock high to output active		TKHQX1	TDC1	2	–	2	–	2	–	ns	
Clock high to output change		TKHQX2	TDC2	2.5	–	3	–	3	–	ns	
Output enable to output active		TGLQX	TOLZ	2	–	2	–	2	–	ns	
Output disable to output high-Z		TGHQZ	TOHZ	2	5	2	5	2	5	ns	
Clock high to output high-Z		TKHQZ	TCZ	2	5	2	5	2	5	ns	
Clock high pulse width		TKHKL	TCH	4	–	4.5	–	5	–	ns	
Clock low pulse width		TKLKH	TCL	4	–	4.5	–	5	–	ns	
Setup times	Address	TAVKH	TAS	2.5	–	2.5	–	2.5	–	ns	
	Address status	TADSVKH	TSS								
	Data in	TDVKH	TDS	2.2	–						
	Write enable	TWVKH	TWS	2.5	–						
	Address advance	TADVVKH	–								
	Chip enable	TEVKH	–								
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	0.5	–	ns	
	Address status	TKHADSX	TSH								
	Data in	TKHDX	TDH								
	Write enable	TKHWX	TWH								
	Address advance	TKHADVX	–								
	Chip enable	TKHEX	–								
Power down entry setup		TZZES	TZZES	8	–	8	–	8	–	ns	1
Power down entry hold		TZZEH	TZZEH	0	–	0	–	0	–	ns	1
Power down recovery setup		TZZRS	TZZRS	8	–	8	–	8	–	ns	1
Power down recovery hold		TZZRH	TZZRH	0	–	0	–	0	–	ns	1

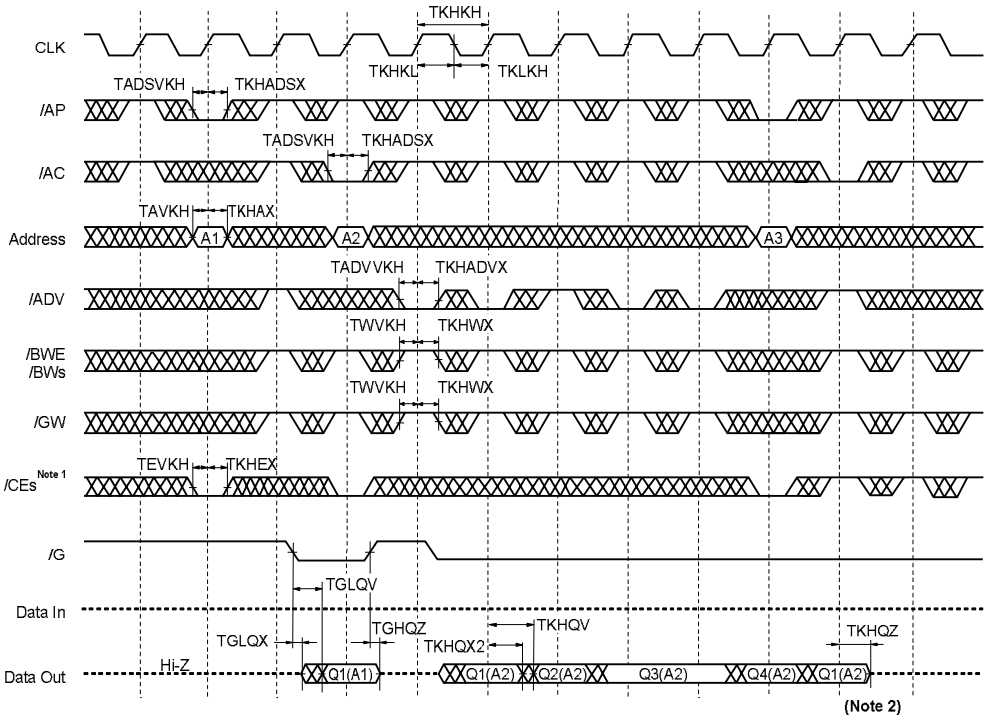
Note 1. Although ZZ signal input is asynchronous, the signal must meet specified setup and hold times in order to be recognized.

Read and Write Cycle (3.3 V LVTTL interface)

Parameter		Symbol		-A5 (100 MHz)		-A7 (83 MHz)		-A8 (66 MHz)		Unit	Note
		Standard	Alias	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Cycle time		TKHKH	TCYC	10	–	12	–	15	–	ns	
Clock access time		TKHQV	TCD	–	5	–	7	–	8	ns	
Output enable access time		TGLQV	TOE	–	4.5	–	5	–	5	ns	
Clock high to output active		TKHQX1	TDC1	2	–	2	–	2	–	ns	
Clock high to output change		TKHQX2	TDC2	2.5	–	3	–	3	–	ns	
Output enable to output active		TGLQX	TOLZ	2	–	2	–	2	–	ns	
Output disable to output high-Z		TGHQZ	TOHZ	2	5	2	5	2	5	ns	
Clock high to output high-Z		TKHQZ	TCZ	2	5	2	5	2	5	ns	
Clock high pulse width		TKHKL	TCH	4	–	4.5	–	5	–	ns	
Clock low pulse width		TKLKH	TCL	4	–	4.5	–	5	–	ns	
Setup times	Address	TAVKH	TAS	2.5	–	2.5	–	2.5	–	ns	
	Address status	TADSVKH	TSS								
	Data in	TDVKH	TDS	2.2	–						
	Write enable	TWVKH	TWS	2.5	–						
	Address advance	TADVVKH	–								
	Chip enable	TEVKH	–								
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	0.5	–	ns	
	Address status	TKHADSX	TSH								
	Data in	TKHDX	TDH								
	Write enable	TKHWX	TWH								
	Address advance	TKHADVX	–								
	Chip enable	TKHEX	–								
Power down entry setup		TZZES	TZZES	8	–	8	–	8	–	ns	1
Power down entry hold		TZZEH	TZZEH	0	–	0	–	0	–	ns	1
Power down recovery setup		TZZRS	TZZRS	8	–	8	–	8	–	ns	1
Power down recovery hold		TZZRH	TZZRH	0	–	0	–	0	–	ns	1

Note 1. Although ZZ signal input is asynchronous, the signal must meet specified setup and hold times in order to be recognized.

★ **READ CYCLE**

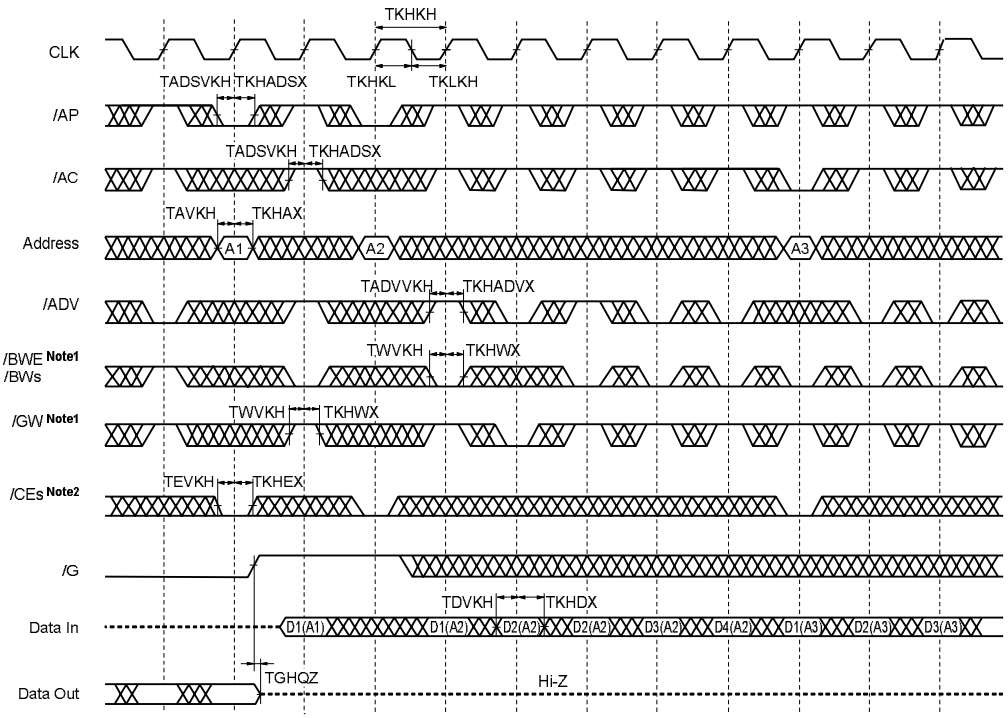


Notes 1. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

2. Outputs are disabled within one clock cycle after deselect.

Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

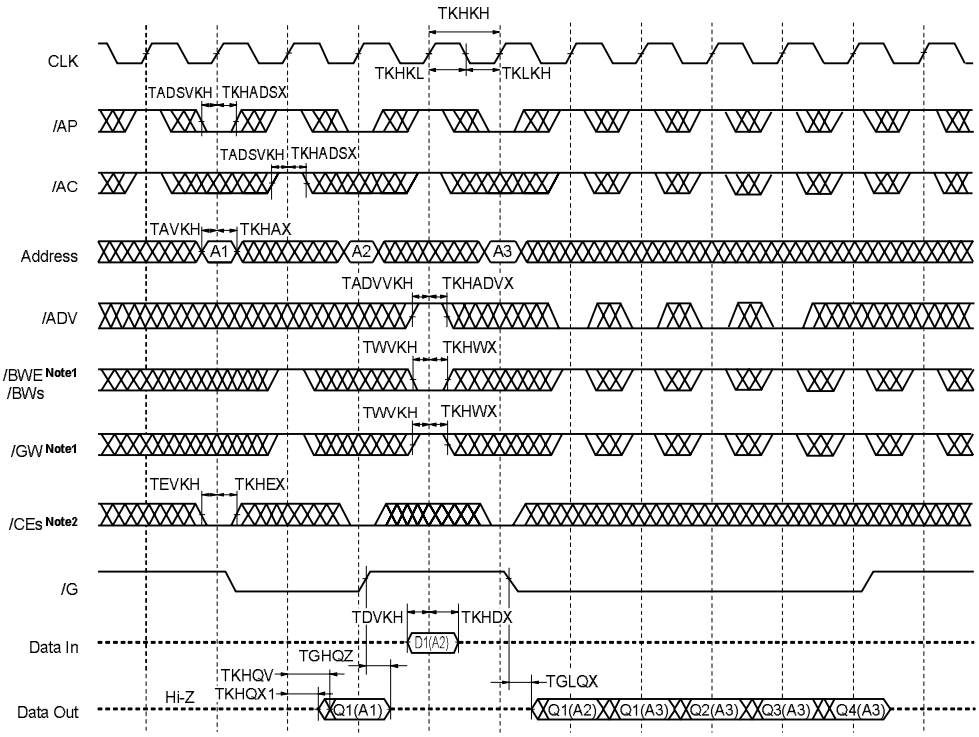
WRITE CYCLE



Notes 1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1-/BW4 LOW.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

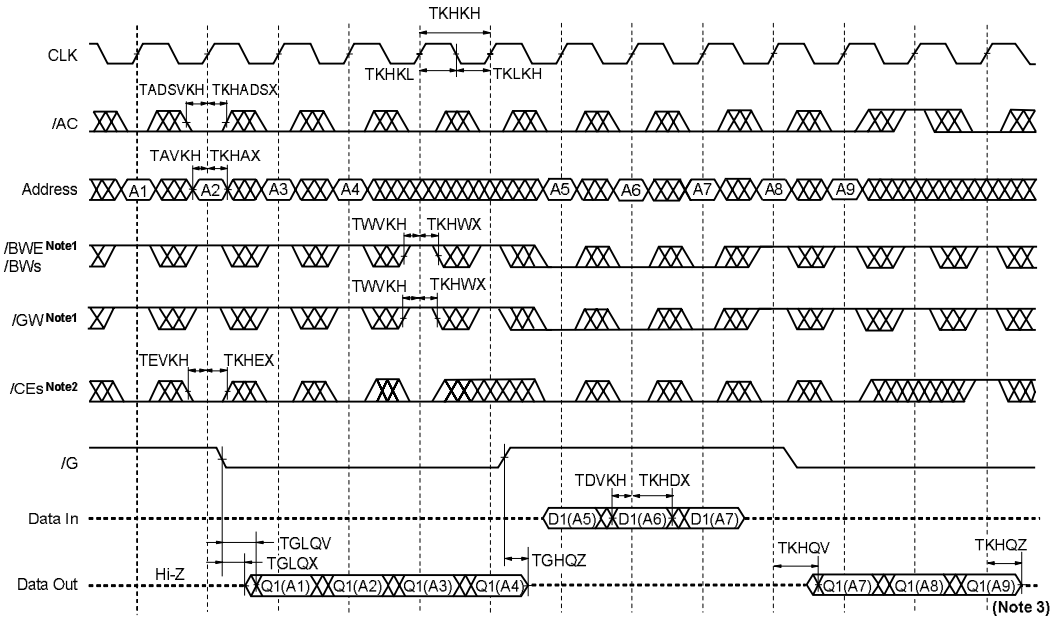
READ / WRITE CYCLE



Notes 1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1-/BW4 LOW.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

★ **SINGLE READ / WRITE CYCLE**



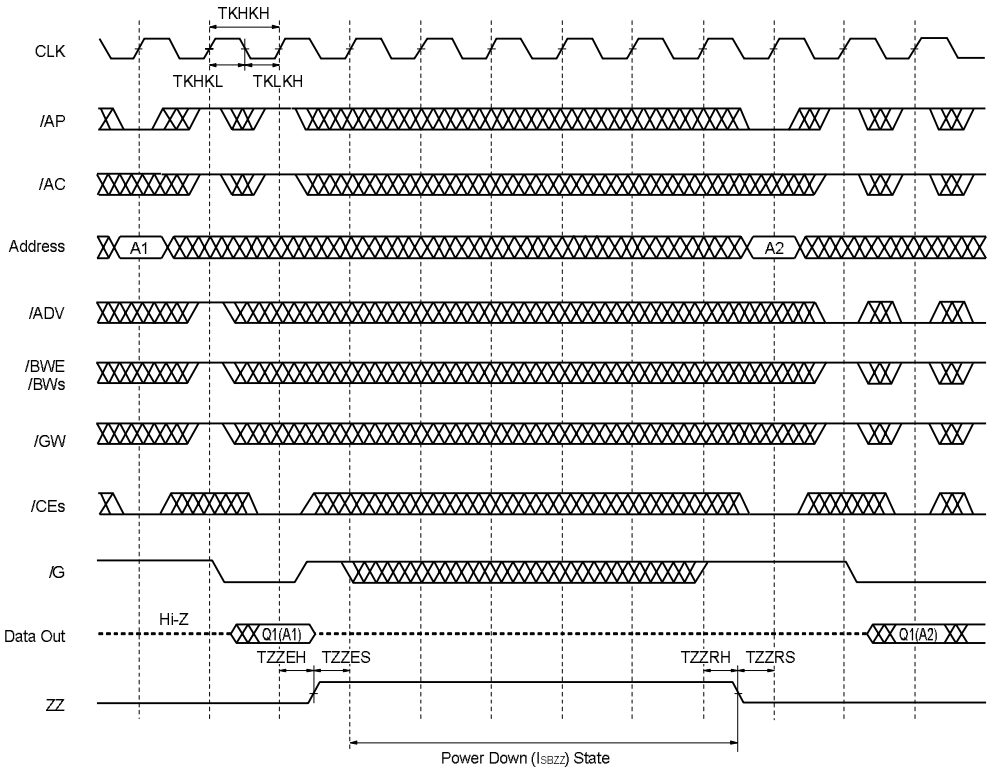
Notes 1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1-/BW4 LOW.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

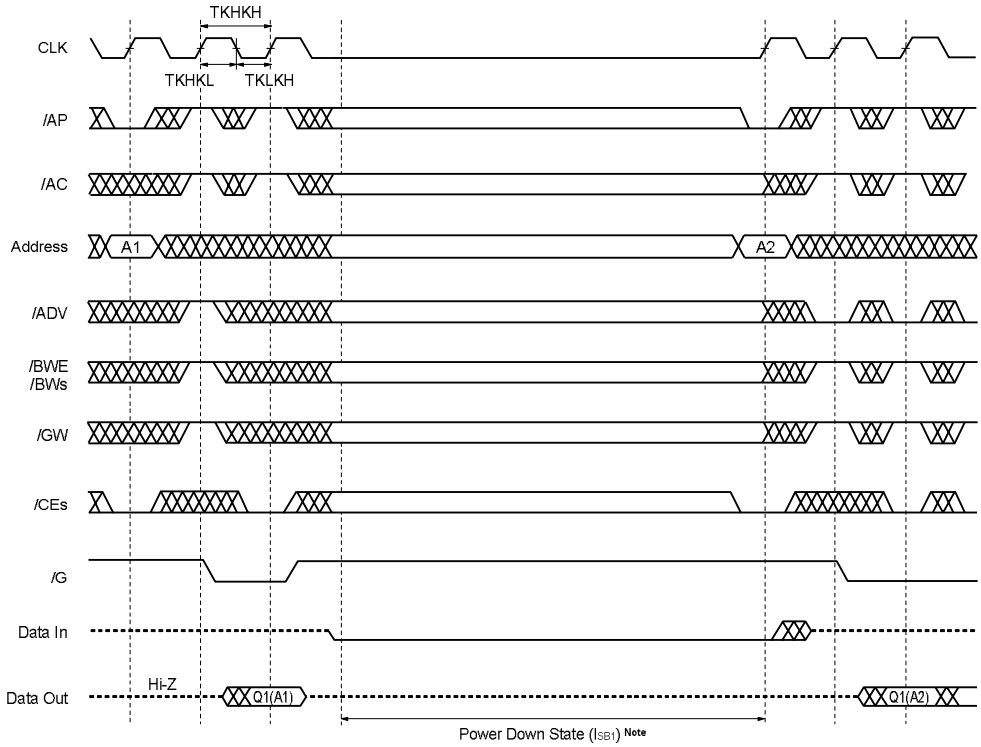
3. Outputs are disabled within one clock cycle after deselect.

Remark /AP is HIGH and /ADV is don't care.

POWER DOWN (ZZ) CYCLE



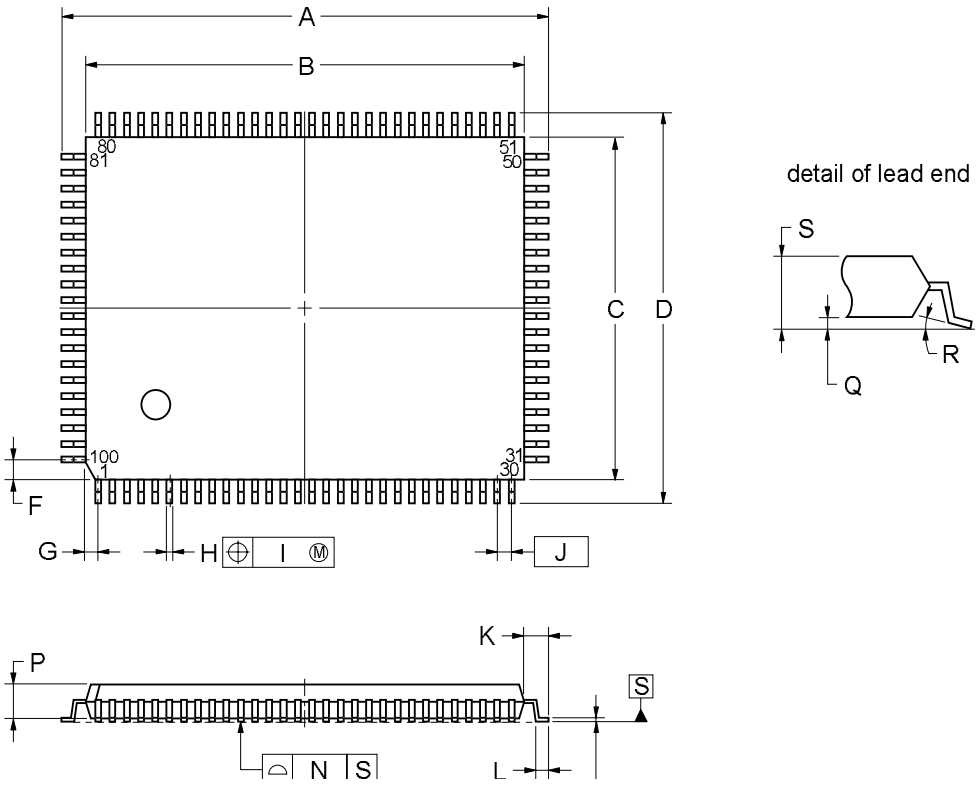
STOP CLOCK CYCLE



Note $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, $V_{I/O} \leq 0.2$ V

★ **Package Drawing**

100-PIN PLASTIC LQFP (14x20)



Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD432232L.

Type of Surface Mount Devices

μPD432232LGF : 100-PIN PLASTIC LQFP (14 x 20)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES