

Two-Channel ATM SATURN User Network Interface

FEATURES

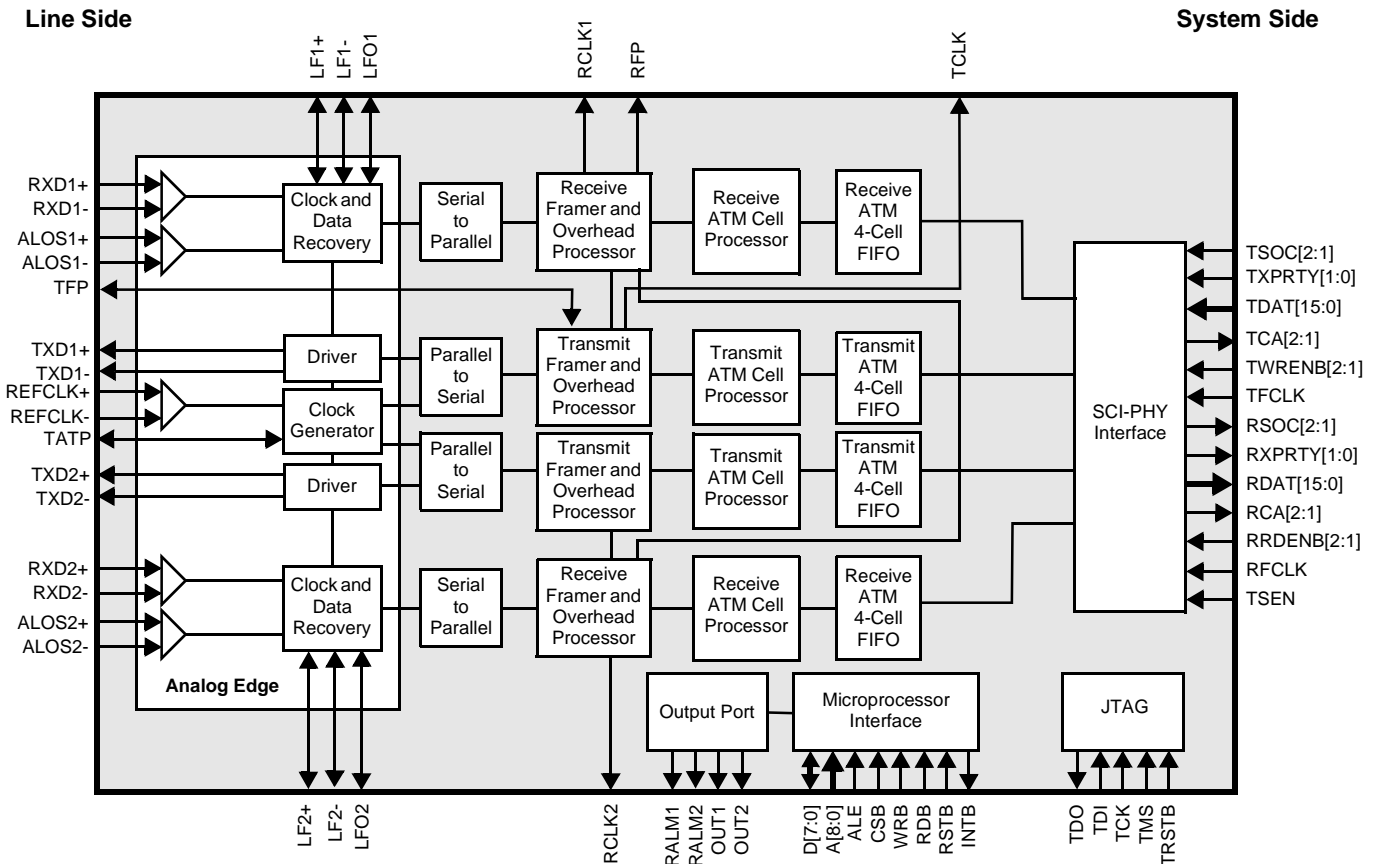
- Provides two independent SATURN[®]-compatible ATM PHY channels in one chip.
- Provides hardware and software backward compatibility with the industry-standard PM5346 S/UNI[®]-155-LITE chip.
- Implements the ATM Transmission Convergence (TC) sublayer according to ATM Forum specifications using the SONET/SDH 155.52 Mbit/s STS-3c/STM-1 and SONET 51.84 Mbit/s STS-1 formats.
- NRZ data format supports category-5 Unshielded Twisted Pair (UTP-5) or Shielded Twisted Pair (STP) wiring and optical datalink modules for fiber optic cable.
- Includes on-chip clock recovery and clock synthesis, compliant to Bellcore and ITU-T requirements.
- Operates in timing master or timing slave (loop timed LAN) modes.
- Frames to SONET framing bytes (A1, A2), processes the section and line Bit Interleaved Parity (B1, B2) and the Far-End Block Error (Z2) bytes.
- Interprets the H1, H2, and H3 payload pointer bytes.
- Processes the SONET path overhead BIP-8 (B3), signal label (C2) and path status (G1) bytes.
- Allows for protection switching by monitoring the APS (K1, K2) bytes, bit error rate thresholds and far-end synchronization status (S1) bits and providing interrupts when error conditions are detected.*
- Inserts and extracts ATM payloads using ATM cell delineation.
- Provides on-chip 4-cell FIFO buffers in both transmit and receive paths.
- Operates with a backward compatible dual 8-bit plus parity or a multi-PHY compatible 16-bit plus parity* SATURN-Compliant Interface for PHYSical layer devices (SCI-PHY[™]).
- Cell interface is also compatible with ATM Forum Level 2 UTOPIA direct-mode specifications.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and monitoring.
- Provides TTL/CMOS compatible inputs and outputs and differential PECL inputs.
- Low power, +5 V CMOS technology.
- Packaged in a 28 mm by 28 mm 160-pin Plastic Quad Flat Pack (PQFP).

*NOTE: Indicates new features not provided on S/UNI-155-LITE.

APPLICATIONS

- ATM Switches and Hubs
- ATM Routers
- Multichannel ATM Servers

BLOCK DIAGRAM



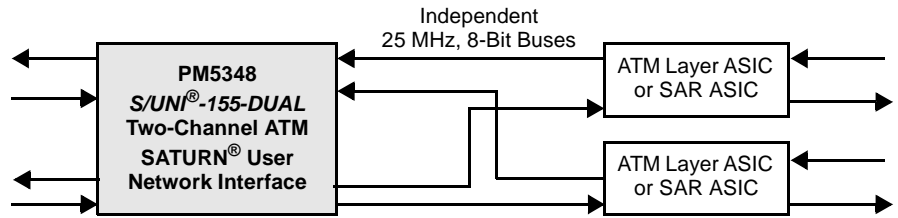
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TYPICAL APPLICATIONS

Split 8-bit bus mode for backward compatibility with multiple single-PHY applications.

Applications:

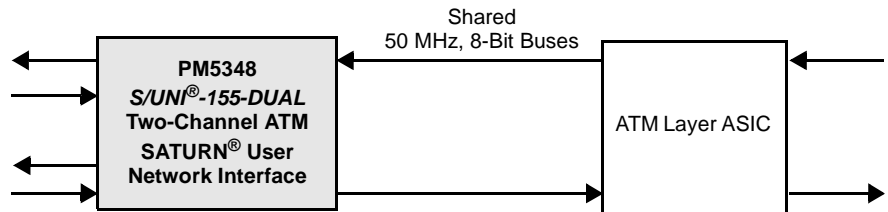
- Multi-SAR Servers
- Single-channel, 8-bit, 25 MHz ATM Layer Devices



Shared 8-bit bus mode for 8-bit direct mode multi-PHY applications.

Applications:

- Two-channel, 8-bit, 50 MHz ATM Layer Devices



Shared 16-bit bus mode for 16-bit direct mode multi-PHY applications.

Applications:

- Four-channel, 16-bit, 50 MHz ATM Layer Devices

