

PE3501

Product Description

The PE3501 is a high-performance dynamic CMOS prescaler with a fixed divide ratio of 2. Its operating frequency range is 400 MHz to 3.5 GHz. The PE3501 operates on a nominal 3 V supply and draws only 12 mA. It is packaged in a small 8-lead TSSOP and is ideal for frequency scaling and microwave PLL synthesis solutions.

The PE3501 is manufactured in Peregrine's patented Ultra-Thin Silicon (UTSi[®]) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

3.5 GHz Low Power CMOS Divide-by-2 Prescaler

Features

- High-frequency operation: 400 MHz to 3.5 GHz
- Fixed divide ratio of 2
- Low-power operation: 12 mA typical @ 3 V
- Small package: 8-lead TSSOP
- Low cost

Figure 1. Functional Schematic Diagram

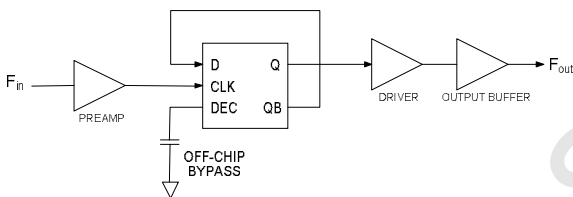


Figure 2. Package Drawing

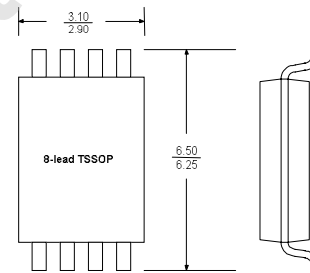
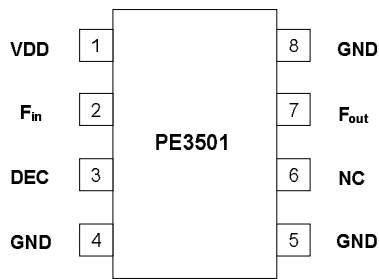


Table 1. Electrical Specifications ($Z_S = Z_L = 50 \Omega$)

$V_{DD} = 3.0 \text{ V}$, $-40^\circ \text{ C} \leq T_A \leq 85^\circ \text{ C}$, unless otherwise specified

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			12	15	mA
Input Frequency (F_{in})		400		3500	MHz
Input Power (P_{in})	$400\text{MHz} \leq F_{in} \leq 3000\text{MHz}$	-10		+10	dBm
	$3000\text{MHz} < F_{in} \leq 3500\text{MHz}$	0		+10	dBm
Output Power (P_{out})	$400\text{MHz} \leq F_{in} \leq 3000\text{MHz}$	-10			dBm
	$3000\text{MHz} < F_{in} \leq 3500\text{MHz}$	-15			dBm

Figure 3. Pin Configuration

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	VDD	Power supply pin. Bypassing is required.
2	F _{in}	Input signal pin. DC blocking capacitor required (15 pF typical)
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No Connection. This pin should be left open.
7	F _{out}	Divided frequency output pin. DC blocking capacitor required (47 pF typical)
8	GND	Ground pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
VDD	Supply voltage		4.0	V
P _{in}	Input Power		15	dBm
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	-40	85	°C
VESD	ESD voltage (Human Body Model)		250	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Functional Considerations

The PE3501 divides a 400 MHz to 3500 MHz input signal by two, producing a 200 MHz to 1750 MHz output signal. To work properly, pin 3 must be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4.

The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 11 for a layout example.

Figure 4. Test Circuit Block Diagram

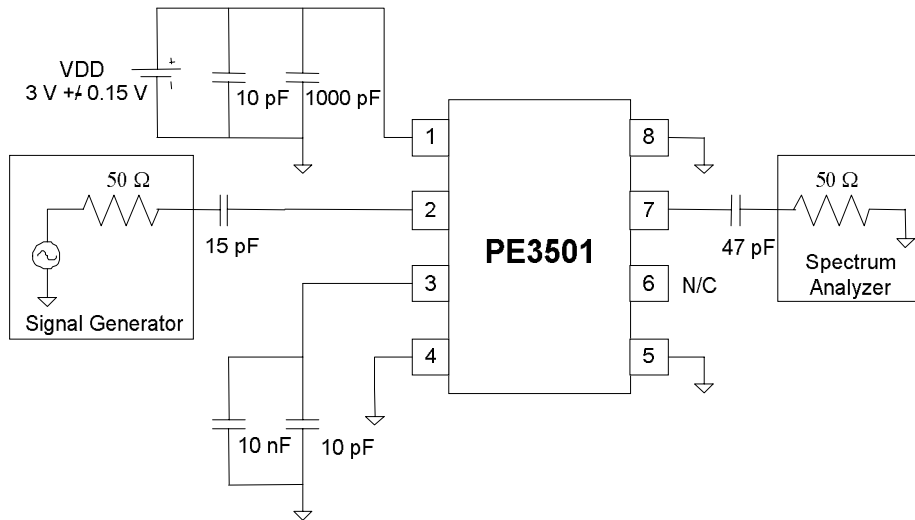


Figure 5. High Frequency System Application

The wideband frequency of operation of the PE3501 makes it an ideal part for use in a DBS down-converter system.

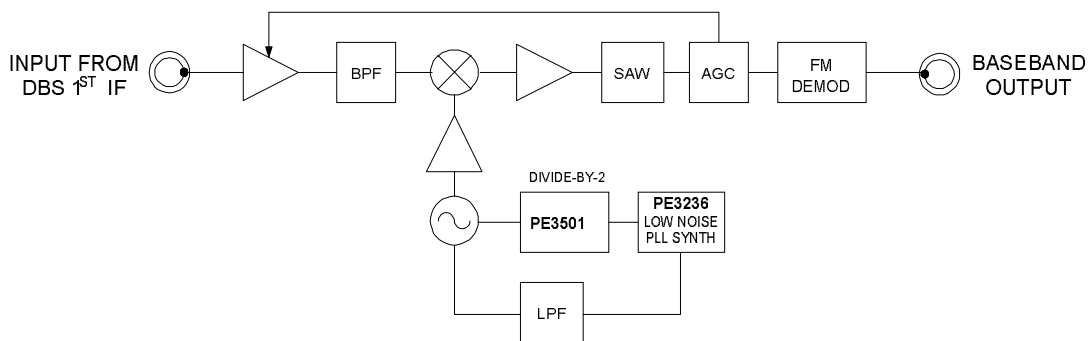


Figure 6. Typical Input Sensitivity

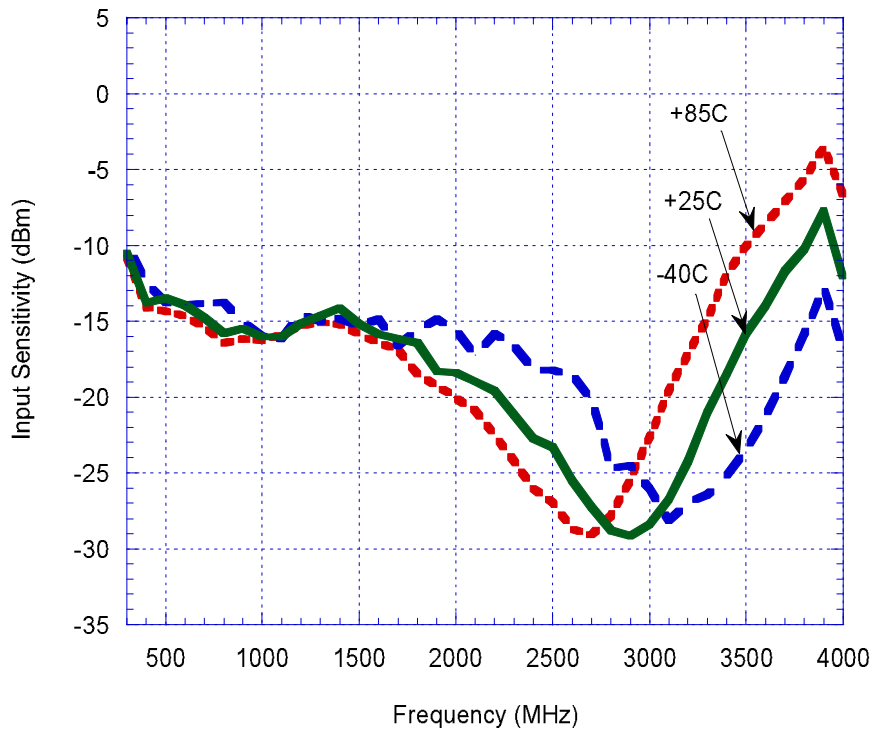
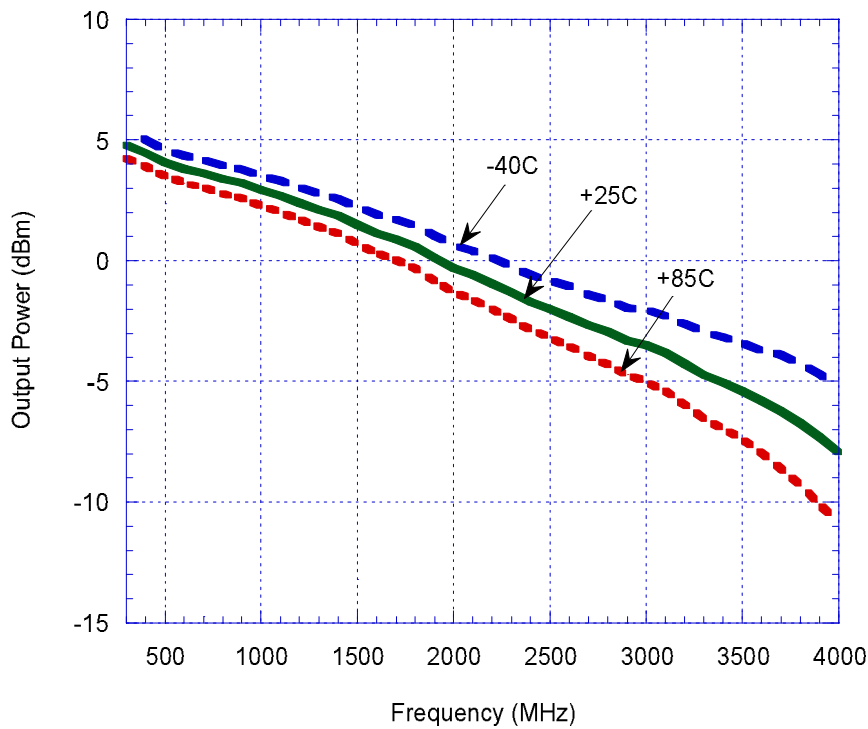


Figure 7. Typical Output Power



Typical Performance Data @ +25 °C

Table 4. S11

Input Freq (GHz)	S11 Magnitude (dB)	S11 Angle (deg)
0.4	-0.5523	-9.337
0.5	-0.6707	-11.253
0.6	-0.806	-13.193
0.7	-0.9642	-14.8
0.8	-1.109	-15.929
0.9	-1.1263	-17.103
1.0	-1.152	-18.594
1.1	-1.1703	-20.722
1.2	-1.2353	-22.915
1.3	-1.4078	-25.66
1.4	-1.6207	-28.199
1.5	-1.8965	-30.249
1.6	-2.1032	-31.079
1.7	-1.9731	-32.514
1.8	-1.8229	-36.258
1.9	-1.8517	-40.604
2.0	-2.0308	-44.918
2.1	-2.1353	-48.91
2.2	-2.2884	-53.156
2.3	-2.397	-56.979
2.4	-2.4811	-61.184
2.5	-2.5498	-64.955
2.6	-2.6367	-68.656
2.7	-2.655	-72.265
2.8	-2.7216	-75.379
2.9	-2.691	-78.326
3.0	-2.6813	-80.734
3.1	-2.6933	-82.87
3.2	-2.6638	-84.784
3.3	-2.6461	-86.468
3.4	-2.6266	-87.788
3.5	-2.5917	-89.118

Table 5. S22

Output Freq (GHz)	S22 Magnitude (dB)	S22 Angle (deg)
0.20	-8.7615	26.726
0.25	-8.2705	21.393
0.30	-7.7885	16.647
0.35	-7.6058	10.297
0.40	-7.7922	6.2004
0.45	-8.2309	2.4335
0.50	-8.5583	-0.3158
0.55	-8.8751	-0.2458
0.60	-8.8599	-3.0515
0.65	-9.1496	-2.6752
0.70	-8.8648	-6.0631
0.75	-9.0828	-5.7925
0.80	-9.2022	-6.8019
0.85	-9.2727	-9.3617
0.90	-9.6494	-12.806
0.95	-9.4383	-14.454
1.00	-9.5217	-16.286
1.05	-9.6043	-19.118
1.10	-9.7282	-23.597
1.15	-9.8069	-25.461
1.20	-9.8221	-29.038
1.25	-9.8694	-32.629
1.30	-9.8693	-34.669
1.35	-9.8667	-40.785
1.40	-9.8509	-43.139
1.45	-9.9141	-46.745
1.50	-9.7063	-51.695
1.55	-9.8686	-54.805
1.60	-9.4836	-56.589
1.65	-9.4498	-62.744
1.70	-9.3233	-66.237
1.75	-9.2206	-66.07

Figure 8. S11 vs. Input Frequency (VDD = 3 V)

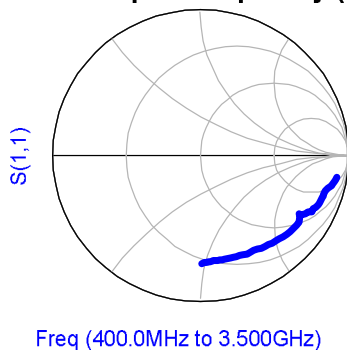


Figure 9. S22 vs. Output Frequency (VDD = 3 V)

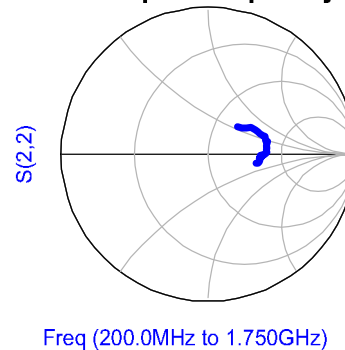


Figure 10. Evaluation Board Schematic Diagram

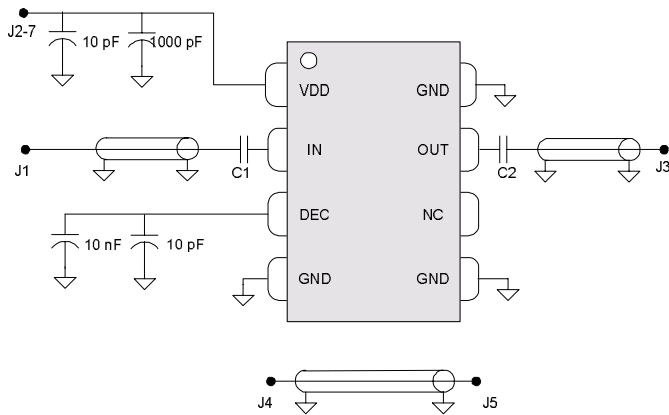
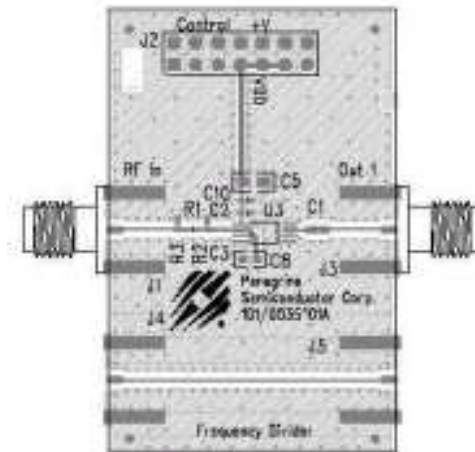


Figure 11. Evaluation Board Layout



Evaluation Kit Operation

The TSSOP Prescaler Evaluation Board was designed to help customers evaluate the PE3501 Divide-by-2 Prescaler. On this board, the device input (pin 2) is connected to connector J1 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 15 pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C2) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have a low impedance at the desired output frequency the device. The value of 47 pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace

gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and ϵ_r of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide.

J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device VDD pin (1). Two decoupling capacitors (10 pF, 1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

The DEC pin (3) must be connected to a low impedance AC ground for proper device operation. On the board, two decoupling capacitors (C6 = 10 nF, C4 = 10 pF), located on the back of the board, perform this function.

Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 455-0660 and ask for applications support. You may also contact us by fax or e-mail:

Fax: (858) 455-0770
E-Mail: help@peregrine-semi.com

Figure 12. Package Drawing

8-Lead TSSOP

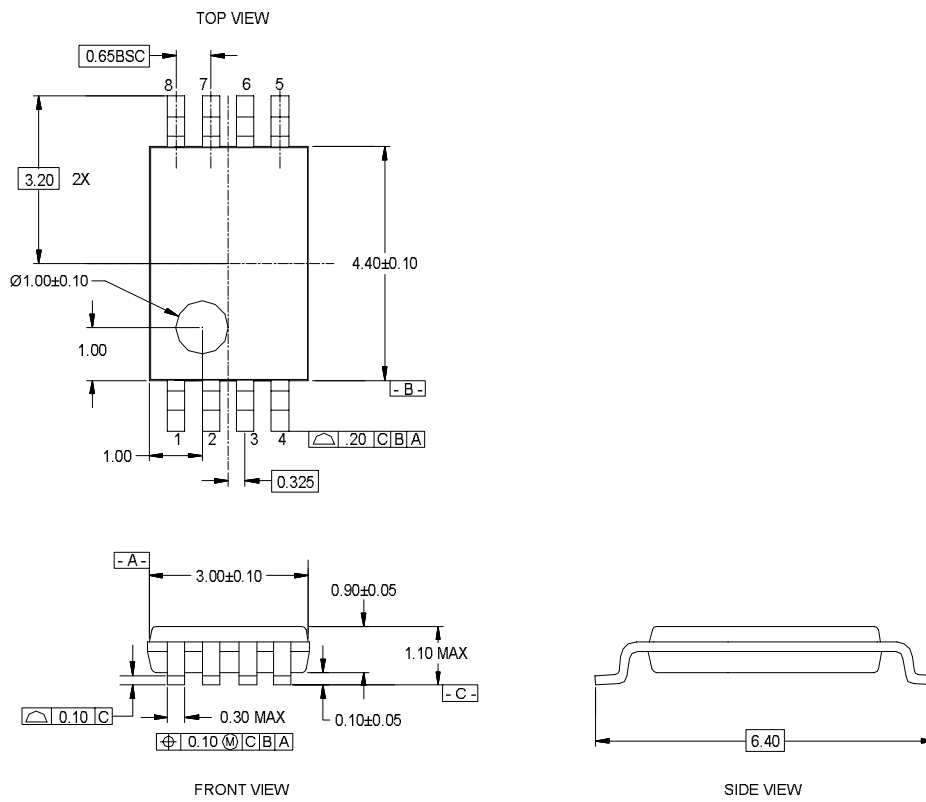


Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
3501-11	PE3501	PE3501-08TSSOP-100A	8-lead TSSOP	100 units / Tube
3501-12	PE3501	PE3501-08TSSOP-2000C	8-lead TSSOP	2000 units / T&R
3501-00	PE3501-EK	PE3501-08TSSOP-EK	Evaluation Board	1 / Box

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Data Sheet Identification

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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