

## 128K x8 bit Low Power CMOS Static RAM

### FEATURES

- Process Technology : 0.6µm CMOS
- Organization : 128Kx8
- Power Supply Voltage : Single 5.0V ±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard  
32-DIP, 32-SOP, 32-TSOP I R/F

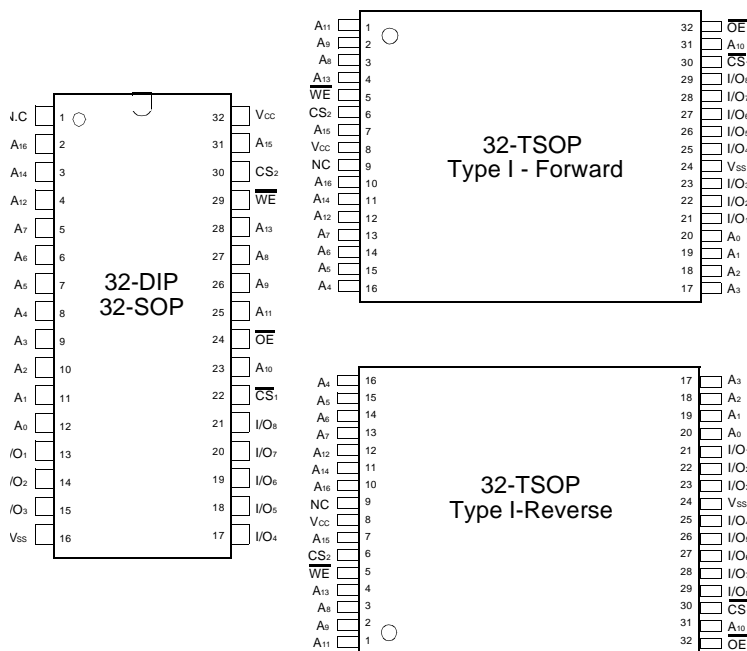
### GENERAL DESCRIPTION

The KM681000B family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

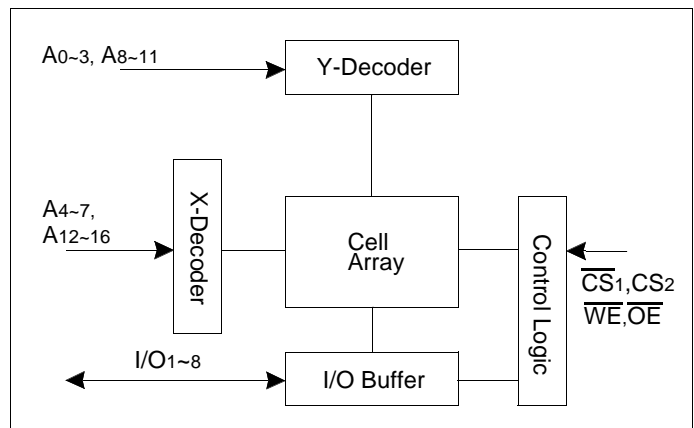
### PRODUCT FAMILY

Product Family	Operating Temperature	Speed	PKG Type	Power Dissipation	
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> )
KM681000BL KM681000BL-L	Commercial(0~75°C)	55/70ns	32-DIP,32-SOP 32-TSOP I R/F	100µW 20µW	70mA
KM681000BLE KM681000BLE-L	Extended(-25~85°C)	70/100ns	32-SOP 32-TSOP I R/F	100µW 50µW	
KM681000BLI KM681000BLI-L	Industrial(-40~85°C)	70/100ns	32-SOP 32-TSOP I R/F	100µW 50µW	

### PIN DESCRIPTION



### FUNCTIONAL BLOCK DIAGRAM



Name	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O1~I/O18	Data Inputs/Outputs
V <sub>CC</sub>	Power
V <sub>SS</sub>	Ground
N.C	No Connection



## ABSOLUTE MAXIMUM RATINGS\*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM681000BL/L-L
		-25 to 85	°C	KM681000BLE/LE-L
		-40 to 85	°C	KM681000BLI/LI-L
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS\*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5	V
Input low voltage	V <sub>IL</sub>	-0.5***	-	0.8	V

1) Commercial Product : T<sub>A</sub>=0 to 70°C, unless otherwise specified

2) Extended Product : T<sub>A</sub>=-25 to 85°C, unless otherwise specified

3) Industrial Product : T<sub>A</sub>=-40 to 85°C, unless otherwise specified

\*\* T<sub>A</sub>=25°C

\*\*\* V<sub>IL</sub>(min)=-3.0V for t<sub>p</sub> 50ns pulse width

## CAPACITANCE\* (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>in</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>io</sub> =0V	-	8	pF

\* Capacitance is sampled not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions*	Mi	Typ**	Max	Unit		
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA		
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA		
Operating power supply current	I <sub>CC</sub>	$\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>IO</sub> =0mA	-	7	15**	mA		
Average operating current	I <sub>CC1</sub>	Cycle time=100ns 100% duty $\overline{CS}_1 \hat{=} 0.2V$ , CS <sub>2</sub> $\hat{=} V_{CC}-0.2V$	-	-	10***	mA		
	I <sub>CC2</sub>	I <sub>IO</sub> =0mA $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> Min cycle, 100% duty	-	-	70	mA		
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V		
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V		
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub>	-	-	3	mA		
Standby Current (CMOS)	KM681000BL KM681000BL-L	I <sub>SB1</sub>	$\overline{CS}_1 \hat{=} V_{CC}-0.2V$ CS <sub>2</sub> $\hat{=} V_{CC}-0.2V$ or CS <sub>2</sub> $\hat{=} 0.2V$ Other input=0~V <sub>CC</sub>	L (Low Power)	-	-	100	μA
				LL (Low Low Power)	-	-	20	μA
	KM681000BLE KM681000BLE-L			L (Low Power)	-	-	100	μA
				LL (Low Low Power)	-	-	50	μA
	KM681000BLI KM681000BLI-L			L (Low Power)	-	-	100	μA
				LL (Low Low Power)	-	-	50	μA

\* 1) Commercial Product : T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified

2) Extended Product : T<sub>A</sub>=-25 to 85°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified

2) Industrial Product : T<sub>A</sub>=-40 to 85°C, V<sub>CC</sub>=5.0V ±10%, unless otherwise specified

\*\* 20mA for Extended and Industrial Products

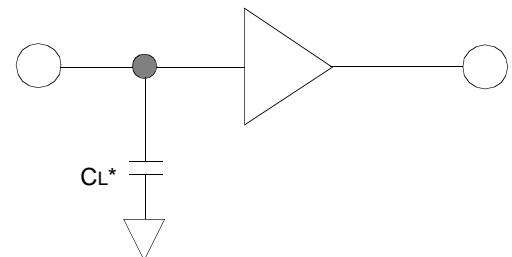
\*\*\* 15mA for Extended and Industrial Products

## A.C CHARACTERISTICS

### TEST CONDITIONS(1.Test Load and Test Input/Output Reference)\*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	C <sub>L</sub> =100pF+1TTL	-

\* See DC Operating conditions



\* Including scope and jig capacitance

## TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM681000BL/L-L	0~70jÉ	5.0Vj%10%	55/70ns	Commercial
KM681000BLE/LE-L	-25~85jÉ	5.0Vj%10%	70/100ns	Extended
KM681000BLI/LI-L	-40~85jÉ	5.0Vj%10%	70/100ns	Industrial

## PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO1,tCO2	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ1,tLZ2	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ1,tHZ2	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

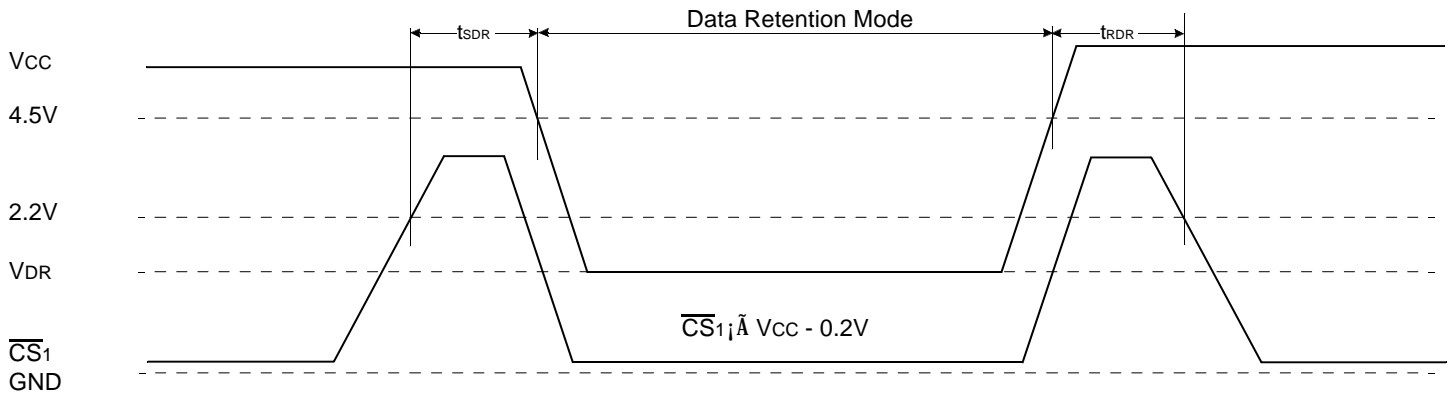
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*	Min	Typ**	Max	Unit	
Vcc for data retention	VDR	$\overline{CS}_1^{***}; \hat{A}V_{cc}-0.2V$	2.0	-	5.5	V	
Data retention current	IDR	$V_{cc}=3.0V$ $\overline{CS}_1; \hat{A}V_{cc}-0.2V$	L-Ver	-	1	50	μA
			L-Ver	-	-	50	
L-Ver	-	-	50	ms			
					LL-Ver	-	-
Data retention set-up time	tRDR	See data retention waveform	0				
Recovery time	tRDR		5		-	-	

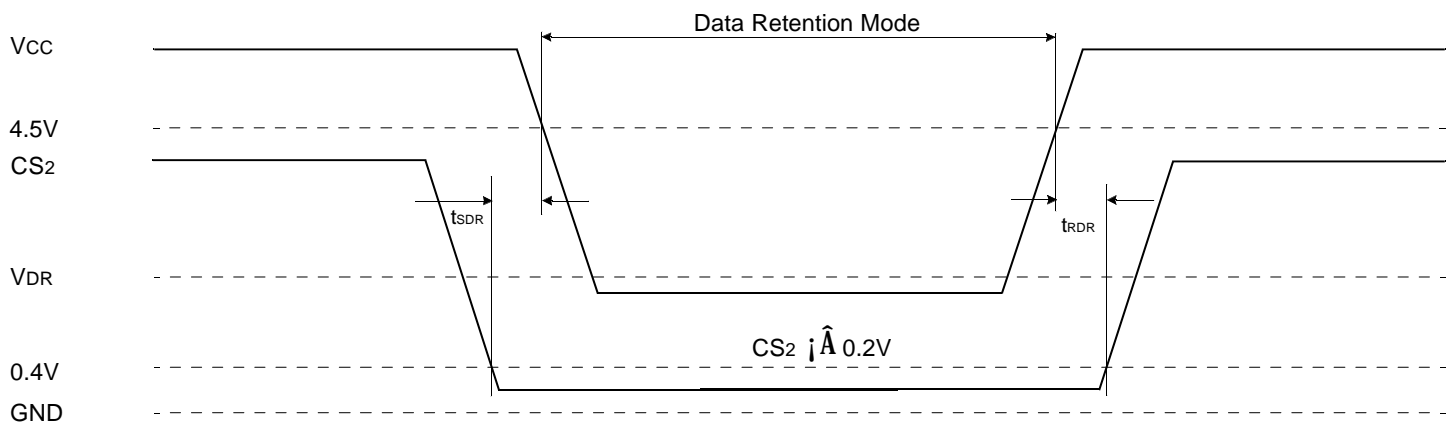
\* 1) Commercial Product : TA=0 to 70°C, unless otherwise specified  
 2) Extended Product : TA=-25 to 85°C, unless otherwise specified  
 2) Industrial Product : TA=-40 to 85°C, unless otherwise specified  
 \*\* TA=25°C  
 \*\*\*  $\overline{CS}_1; \hat{A}V_{cc}-0.2V, CS_2; \hat{A}V_{cc}-0.2V$  ( $\overline{CS}_1$  controlled) or  $CS_2; \hat{A}0.2V$  ( $CS_2$  controlled)

## DATA RETENTION TIMING DIAGRAM

### 1) $\overline{CS}_1$ Controlled



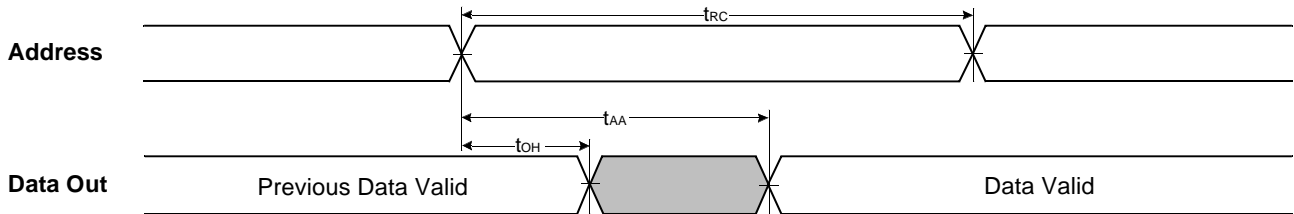
### 2) $\overline{CS}_2$ controlled



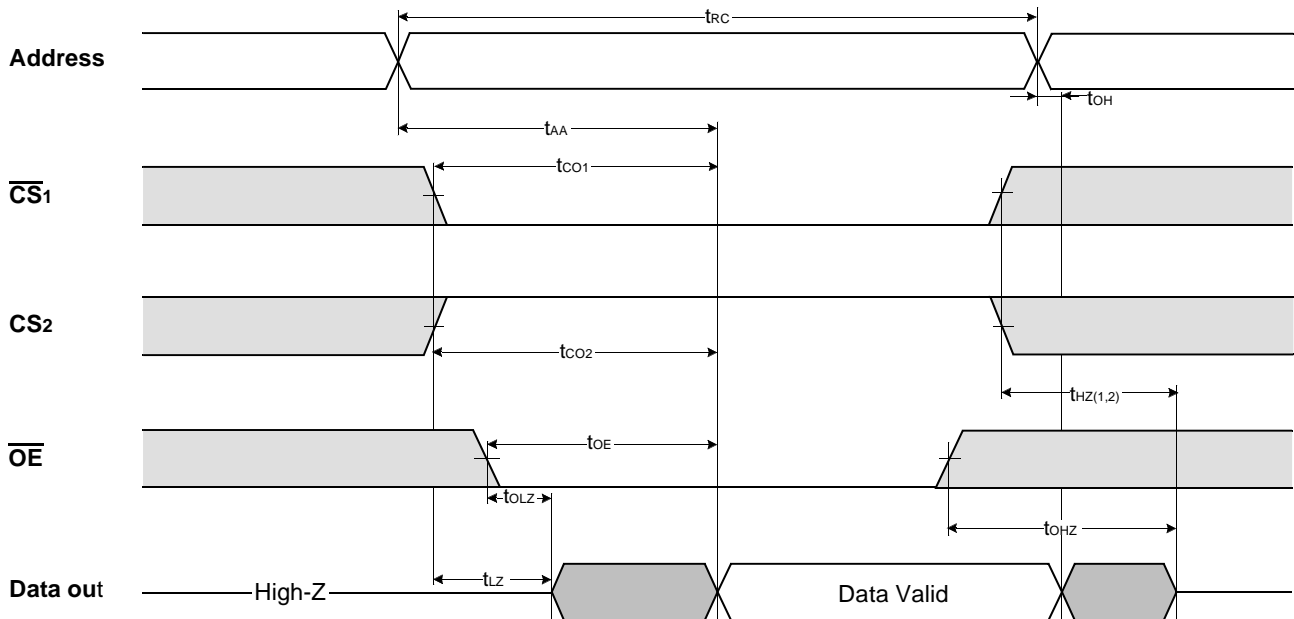
## TIMMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

( $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $CS_2 = \overline{WE} = V_{IH}$ )



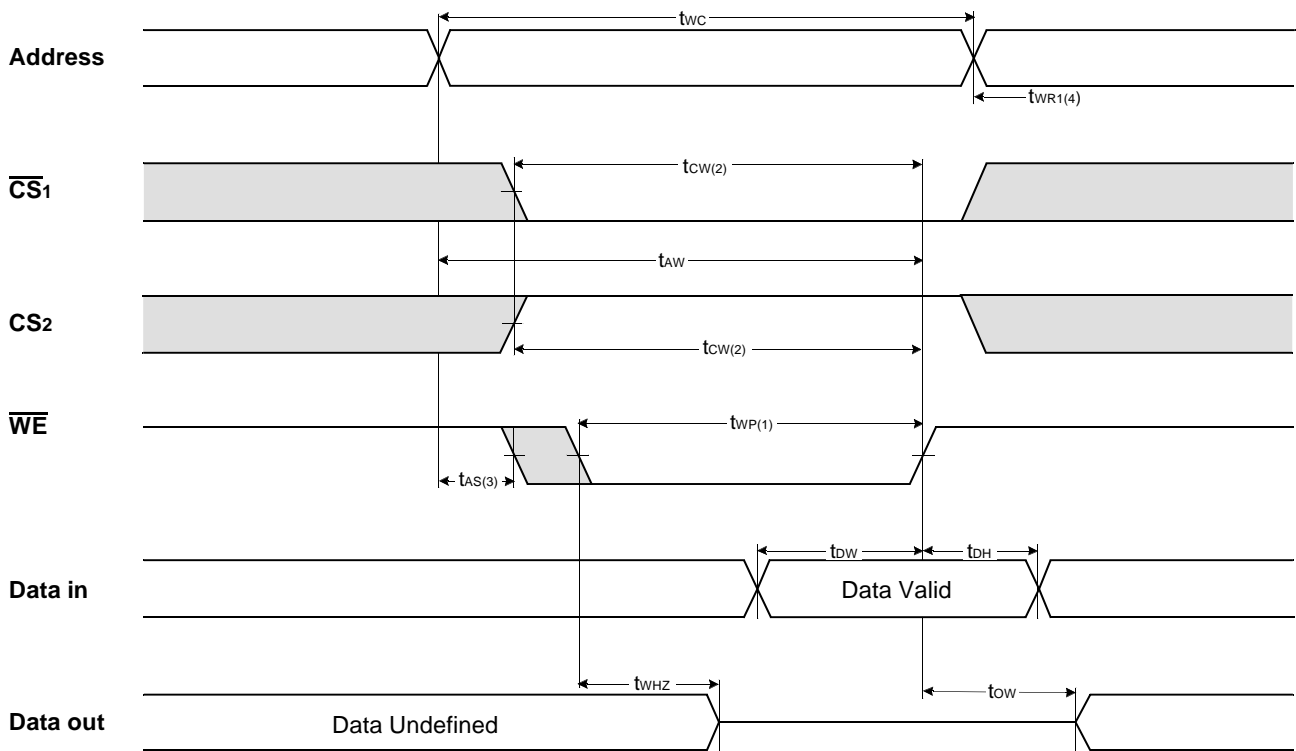
### TIMING WAVEFORM OF READ CYCLE ( $\overline{WE} = V_{IH}$ )



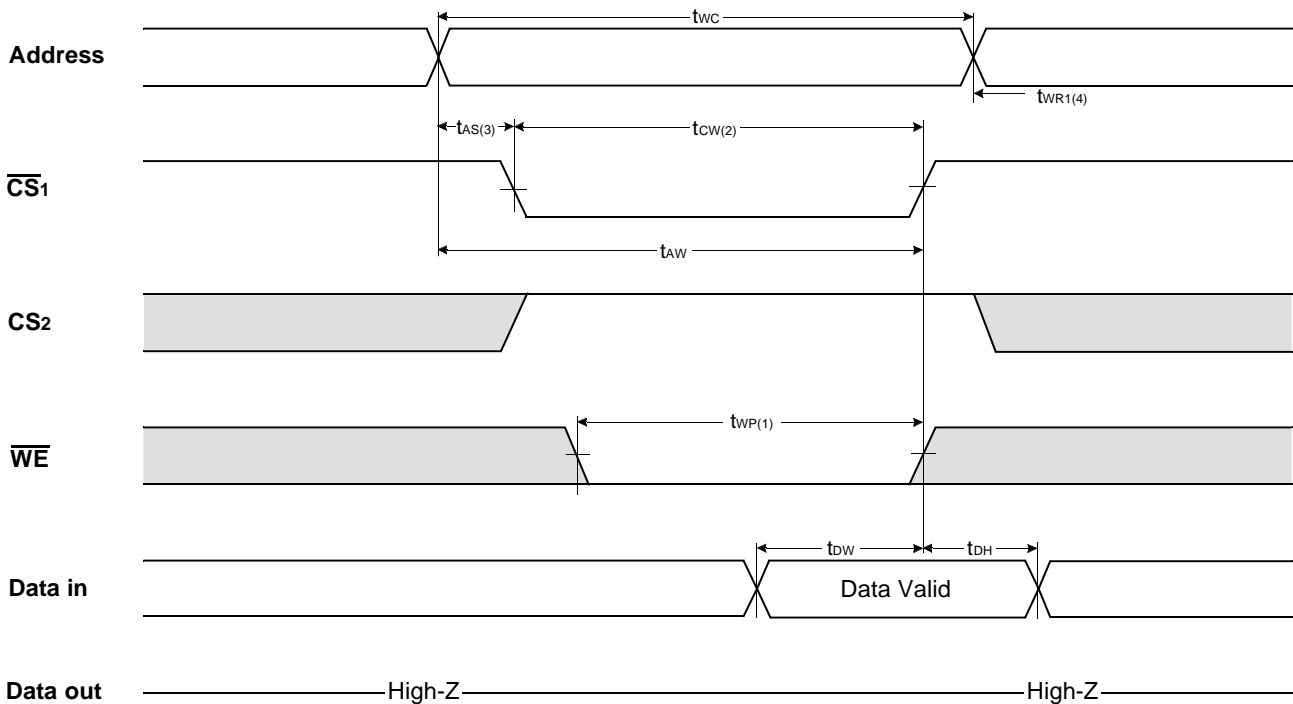
#### NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1)  $\overline{WE}$  Controlled

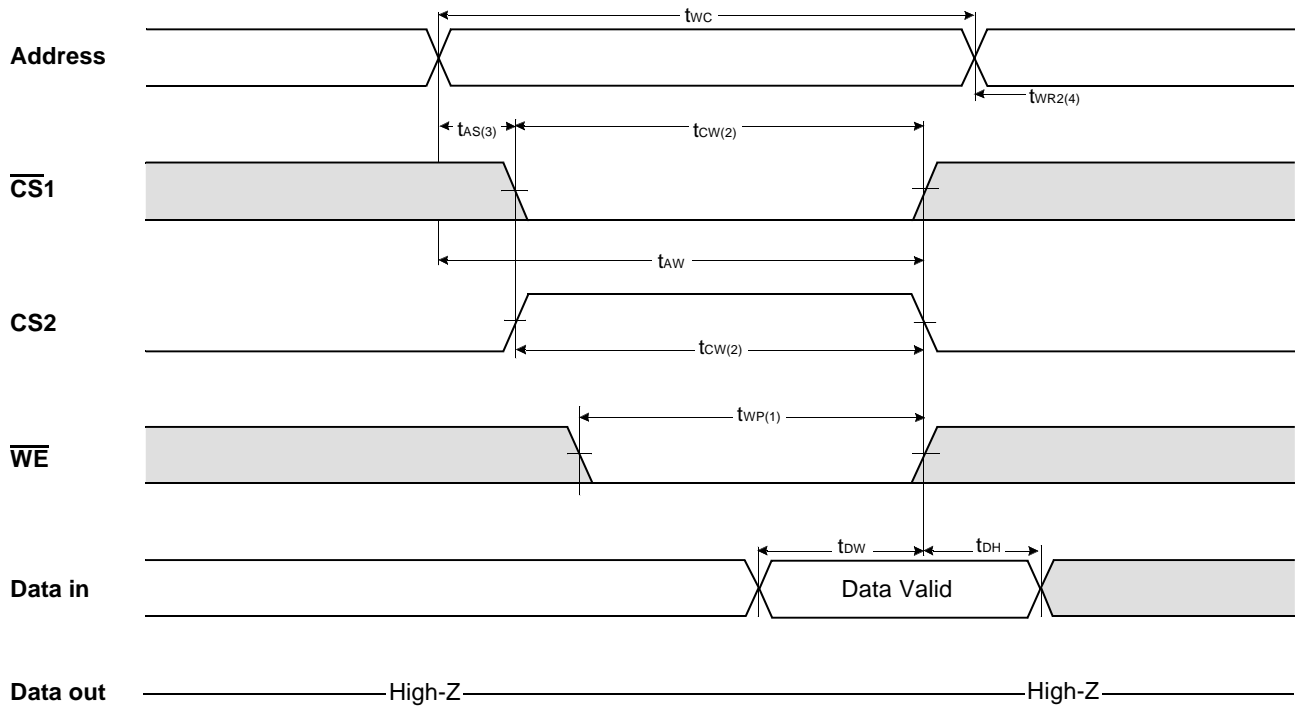


TIMING WAVEFORM OF WRITE CYCLE (2)  $\overline{CS1}$  Controlled





## TIMING WAVEFORM OF WRITE CYCLE (2 $\overline{CS}_2$ Controlled)



### NOTES (WRITE CYCLE)

1. A write occurs during the overlap of low  $\overline{CS}_1$ , high CS2 and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  going low, CS2 going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}_1$  going high, CS2 going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning or write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CS}_1$  going low or CS2 going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends at  $\overline{CS}_1$ , or  $\overline{WE}$  going high,  $t_{WR2}$  applied in case a write ends at CS2 going to low.

## FUNCTIONAL DESCRIPTION

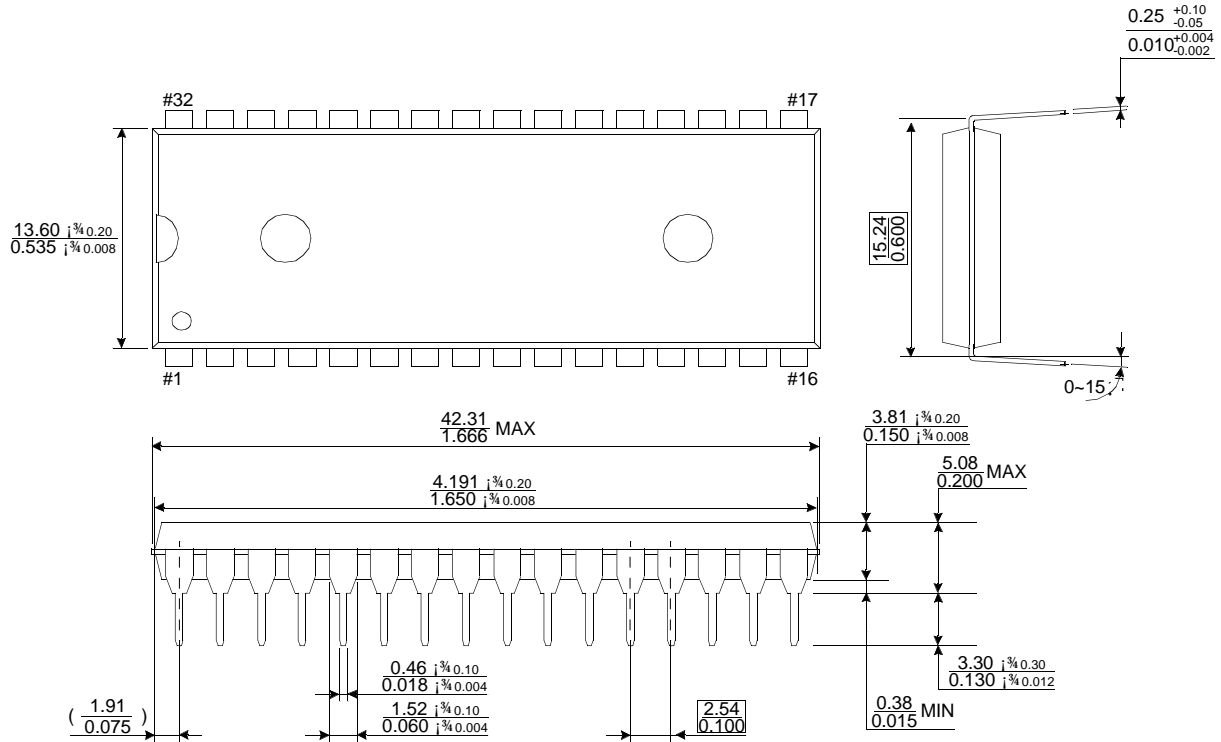
$\overline{CS}_1$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	X	Power Down	High-Z	ISB, ISB1
X	L	X	X	Power Down	High-Z	ISB, ISB1
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

\* X means don't care

PACKAGE DIMENSIONS

Units :MillimeterS(Inches)

32 DUAL INLINE PACKAGE (600mil)



32 PLASTIC SMALL OUTLINE PACKAGE (525mil)

