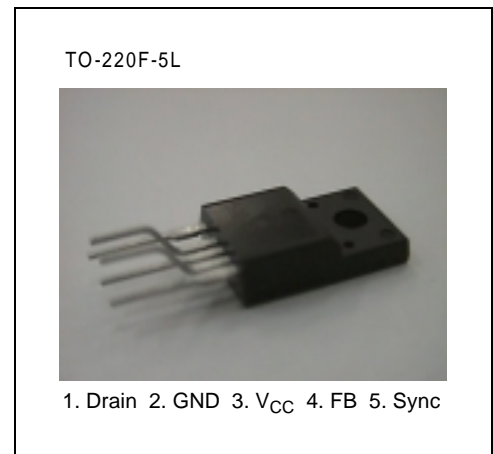


S P S

The SPS product family is specially designed for an off-line SMPS with minimal external components. The SPS consist of high voltage power SenseFET and current mode PWM IC. Included PWM controller features integrated fixed oscillator, under voltage lock out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shut down protection, over voltage protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or RCC switching converter solution, a SPS can reduce total component count, design size, and weight and at the same time increase efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in Quasi-Resonant Converter as C-TV power supply.



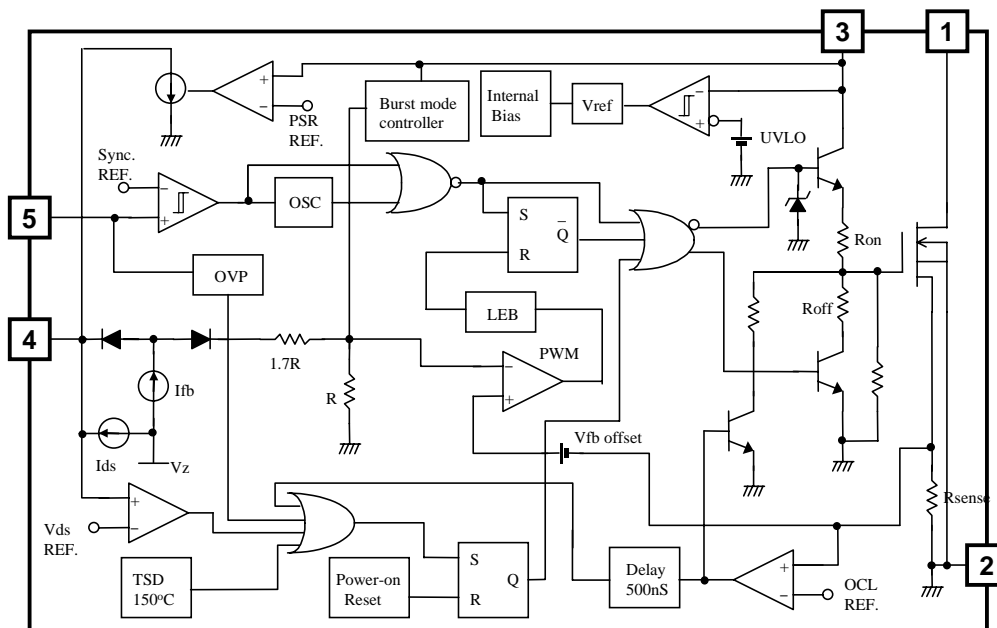
FEATURES

- Quasi Resonant Converter Controller
- Internal Burst mode Controller for Stand-by mode
- Pulse by pulse current limiting
- Over current Latch protection
- Over voltage protection (V_{sync}: Min. 11V)
- Internal thermal shutdown function
- Under voltage lockout
- Internal high voltage sense FET
- Auto-restart mode

ORDERING INFORMATION

Device	Package	Topr (°C)
KA5Q1265RT	TO-220F-5L	-25°C to +85°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Drain-source (GND) voltage ⁽¹⁾	V _{DSS}	650	V
Drain-Gate voltage (R _{GS} =1MΩ)	V _{DGR}	650	V
Gate-source (GND) voltage	V _{GS}	±30	V
Drain current pulsed ⁽²⁾	I _{DM}	48	A _{DC}
Single pulsed avalanche energy ⁽³⁾	E _{AS}	785	mJ
Avalanche current ⁽⁴⁾	I _{AS}	–	A
Continuous drain current (T _C =25°C)	I _D	12	A _{DC}
Continuous drain current (T _C =100°C)	I _D	8.4	A _{DC}
Supply voltage	V _{CC}	40	V
Analog input voltage range (F/B pin)	V _{FB}	–0.3 to V _{SD}	V
Analog input voltage range (Sync pin)	V _{SYNC}	–0.3 to 13	V
Total power dissipation	P _D (wt H/S)	135	W
	Derating	1.1	W/°C
Operating temperature	T _{OPR}	–25 to +85	°C
Storage temperature	T _{STG}	–55 to +150	°C

NOTES:

1. T_j=25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=24mH, starting T_j=25°C
4. L=13uH, starting T_j=25°C

ELECTRICAL CHARACTERISTICS (SFET part)

(Ta=25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=50\mu A$	650	–	–	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=\text{Max.}, \text{Rating}, V_{GS}=0V$	–	–	200	μA
		$V_{DS}=0.8*\text{Max.}, \text{Rating}, V_{GS}=0V, T_C=125^\circ C$	–	–	500	μA
Static drain-source on resistance ^(note)	$R_{DS(ON)}$	$V_{GS}=10V, I_D=6.0A$	–	0.72	–	Ω
Forward transconductance ^(note)	gfs	$V_{DS}=15V, I_D=6.0A$	5.7	–	–	S
Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V, f=1MHz$	–	2700	–	pF
Output capacitance	C_{oss}		–	300	–	
Reverse transfer capacitance	C_{rss}		–	61	–	
Turn on delay time	td(on)	$V_{DD}=0.5BV_{DSS}, I_D=12.0A$ (MOSFET switching time are essentially independent of operating temperature)	–	18	–	nS
Rise time	tr		–	37	–	
Turn off delay time	td(off)		–	88	–	
Fall time	tf		–	36	–	
Total gate charge (gate-source+gate-drain)	Qg	$V_{GS}=10V, I_D=12.0A, V_{DS}=0.5BV_{DSS}$ (MOSFET switching time are essentially independent of operating temperature)	–	–	140	nC
Gate-source charge	Qgs		–	20	–	
Gate-drain (Miller) charge	Qgd		–	69	–	

NOTE: Pulse test: Pulse width $\leq 300\mu S$, duty cycle $\leq 2\%$

ELECTRICAL CHARACTERISTICS (Control part)

(Ta=25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
OSCILLATOR SECTION						
Initial accuracy	F _{OSC}	Ta=25°C	18	20	22	KHz
Frequency change with temperature ⁽²⁾	–	-25°C≤Ta≤+85°C	–	±5	±10	%
PWM SECTION						
Maximum duty cycle	D _{MAX}	–	92	95	98	%
FEEDBACK SECTION						
Feedback Source Current	I _{FB}	Ta=25°C, 0V≤Vfb≤3V	0.7	0.9	1.1	mA
Shutdown Delay Current	I _{DELAY}	Ta=25°C, 5V≤Vfb≤V _{SD}	4	5	6	μA
OVER CURRENT PROTECTION SECTION						
Over Current Protection	I _{L(MAX)}	Max. inductor current	5.28	6.00	6.72	A
UVLO SECTION						
Start threshold voltage	I _{ST}	–	14	15	16	V
Minimum operation voltage	I _{OPR}	After turn on	8	9	10	V
TOTAL STANDBY CURRENT SECTION						
Start threshold voltage	V _{th(H)}	V _{CC} =14	–	0.1	0.2	mA
Operating supply current (Control part only)	V _{th(L)}	V _{CC} ≤28	–	10	18	mA
SHUTDOWN SECTION						
Shutdown Feedback voltage	V _{SD}	Vfb≥6.5V	6.9	7.5	8.1	V
Thermal shutdown temperature (Tj) ⁽¹⁾	T _{SD}	–	140	–	–	°C
Over Voltage Protection Voltage	V _{OVP}	Vsync≥11V	11	12	13	V
Over Current latch Protection ⁽¹⁾	V _{OCL}	–	0.9	1.0	1.1	V
BURST MODE SECTION						
Burst mode Threshold Voltage	V _{BURST}	Vfb=0V	10.6	11.0	11.4	V
Burst mode Hysteresis Voltage	V _{BURSTH}	Vfb=0V	0.7	1	1.2	V
Burst mode Enable Feedback voltage	V _{BURST_EN}	V _{CC} =11V	0.7	1.0	1.3	V
Burst mode Current Limit	I _{BURST}	V _{CC} =11.5V	0.7	0.85	1.0	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta=25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
SYNCHRONIZATION SECTION						
Burst Sync Threshold Voltage	V _{BSY}	V _{FB} =0V	3.1	3.5	3.9	V
Burst Sync Hysteresis Voltage	V _{BSYH}	V _{FB} =0V	2.0	2.25	2.5	V
Normal Sync Threshold Voltage	V _{NSY}	V _{FB} =5V	4.0	4.5	5.0	V
Normal Sync Hysteresis Voltage	V _{NSYH}	V _{FB} =5V	1.8	2.0	2.2	V
PRIMARY SIDE REGULATION SECTION						
Primary Reg. Threshold Voltage	V _{PR}	I _{FB} =0	32.0	32.3	32.6	V
Primary Reg. Transconductance	G _{PR}	–	–	2.6	–	mA/V

NOTE:

1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.