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HI-5700

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May 1997

8-Bit, 20 MSPS Flash A/D Converter

Features

- **20 MSPS with No Missing Codes**
- **18MHz Full Power Input Bandwidth**
- **No Missing Codes Over Temperature**
- **Sample and Hold Not Required**
- **Single +5V Supply Voltage**
- **CMOS/TTL**
- **Overflow Bit**
- **Improved Replacement for MP7684**
- **Evaluation Board Available**
- **/883 Version Available**

Applications

- **Video Digitizing**
- **Radar Systems**
- **Medical Imaging**
- **Communication Systems**
- **High Speed Data Acquisition Systems**

Description

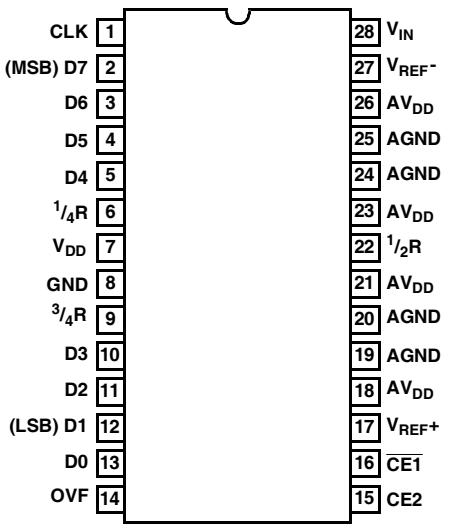
The HI-5700 is a monolithic, 8-bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700 delivers ±0.5 LSB differential nonlinearity while consuming only 725mW (typical) at 20 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9-bit resolution.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5700J-5	0°C to +70°C	28 Lead Plastic DIP
HI9P5700J-5	0°C to +70°C	28 Lead Plastic SOIC (W)
HI3-5700A-9	-40°C to +85°C	28 Lead Plastic DIP
HI9P5700A-9	-40°C to +85°C	28 Lead Plastic SOIC (W)

Pinout

HI-5700
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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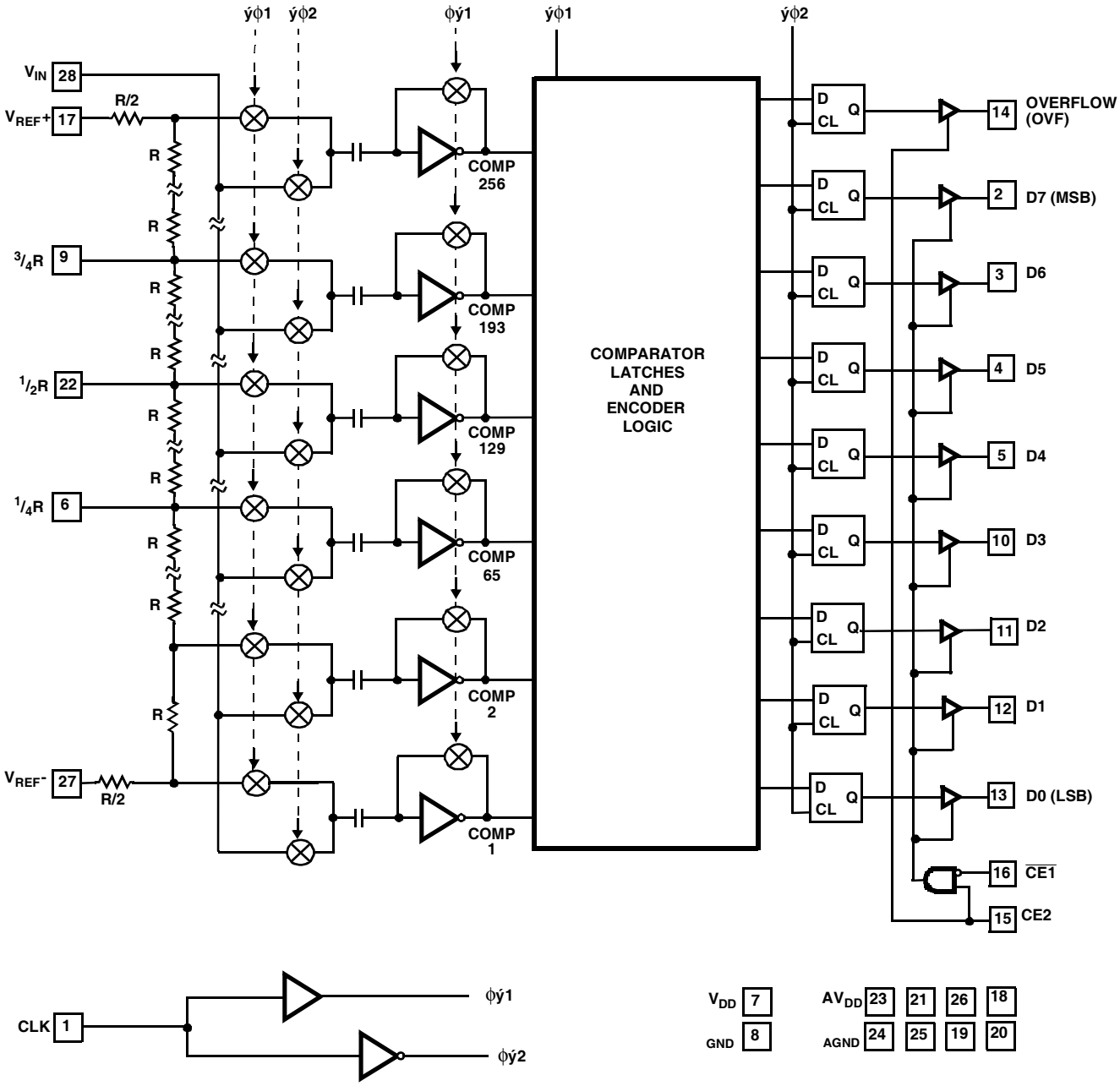
Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND . . . . . (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins. . . . (V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins . . . . . (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Thermal Information

Thermal Resistance	θ_{JA}
HI3-5700J-5, HI3-5700A-9	55°C/W
HI9P5700J-5, HI9P5700A-9	75°C/W

Maximum Power Dissipation +70°C 1.05W
Operating Temperature Range
HI3-5700J-5, HI9P5700J-5 . . . . . 0°C to +70°C
HI3-5700A-9, HI9P5700A-9 . . . . . -40°C to +85°C
Junction Temperature . . . . . +150°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

$AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C TO +70°C -40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		8	-	-	8	-	Bits
Integral Linearity Error (INL) (Best Fit Method)	F_S = 15MHz, f_{IN} = DC	-	±0.9	±2.0	-	±2.25	LSB
	F_S = 20MHz, f_{IN} = DC	-	±1.0	±2.25	-	±3.25	LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 15MHz, f_{IN} = DC	-	±0.4	±0.9	-	±1.0	LSB
	F_S = 20MHz, f_{IN} = DC	-	±0.5	±0.9	-	±1.0	LSB
Offset Error (VOS)	F_S = 15MHz, f_{IN} = DC	-	±5.0	±8.0	-	±9.5	LSB
	F_S = 20MHz, f_{IN} = DC	-	±5.0	±8.0	-	±9.5	LSB
Full Scale Error (FSE)	F_S = 15MHz, f_{IN} = DC	-	±0.5	±4.5	-	±8.0	LSB
	F_S = 20MHz, f_{IN} = DC	-	±0.6	±4.5	-	±8.0	LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	20	25	-	20	-	MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)	-	-	0.125	-	0.125	MSPS
Full Power Input Bandwidth	F_S = 20MHz	-	18	-	-	-	MHz
Signal to Noise Ratio (SNR) = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 15MHz, f_{IN} = 100kHz	-	46.5	-	-	-	dB
	F_S = 15MHz, f_{IN} = 3.58MHz	-	44.0	-	-	-	dB
	F_S = 15MHz, f_{IN} = 4.43MHz	-	43.4	-	-	-	dB
	F_S = 20MHz, f_{IN} = 100kHz	-	45.9	-	-	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	42.0	-	-	-	dB
	F_S = 20MHz, f_{IN} = 4.43MHz	-	41.6	-	-	-	dB
Signal to Noise and Distortion Ratio (SINAD) = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 15MHz, f_{IN} = 100kHz	-	43.4	-	-	-	dB
	F_S = 15MHz, f_{IN} = 3.58MHz	-	34.3	-	-	-	dB
	F_S = 15MHz, f_{IN} = 4.43MHz	-	32.3	-	-	-	dB
	F_S = 20MHz, f_{IN} = 100kHz	-	42.3	-	-	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	35.2	-	-	-	dB
	F_S = 20MHz, f_{IN} = 4.43MHz	-	32.8	-	-	-	dB
Total Harmonic Distortion (THD)	F_S = 15MHz, f_{IN} = 100kHz	-	-46.9	-	-	-	dBc
	F_S = 15MHz, f_{IN} = 3.58MHz	-	-34.8	-	-	-	dBc
	F_S = 15MHz, f_{IN} = 4.43MHz	-	-32.8	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 100kHz	-	-46.6	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 3.58MHz	-	-36.6	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 4.43MHz	-	-33.5	-	-	-	dBc
Differential Gain	F_S = 14MHz, f_{IN} = 3.58MHz	-	3.5	-	-	-	%
Differential Phase Error	F_S = 14MHz, f_{IN} = 3.58MHz	-	0.9	-	-	-	Degree

Electrical Specifications $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C TO +70°C -40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	$V_{IN} = 4V$	4	10	-	-	-	MΩ
Analog Input Capacitance, C_{IN}	$V_{IN} = 0V$	-	60	-	-	-	pF
Analog Input Bias Current, IB	$V_{IN} = 0V, 4V$	-	±0.01	±1.0	-	±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	330	-	235	-	Ω
Reference Resistance Tempco, T_C		-	+0.31	-	-	-	Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0	-	-	2.0	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Logic High Current, I_{IH}	$V_{IN} = 5V$	-	-	1.0	-	1.0	µA
Input Logic Low Current, I_{IL}	$V_{IN} = 0V$	-	-	1.0	-	1.0	µA
Input Capacitance, C_{IN}		-	7	-	-	-	pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$	3.2	-	-	3.2	-	mA
Output Logic Source Current, I_{OH}	$V_O = 4.5V$	-3.2	-	-	-3.2	-	mA
Output Leakage, I_{OZ}	CE2 = 0V, $V_O = 0V, 5V$	-	-	±1.0	-	±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V	-	5.0	-	-	-	pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}		-	6	-	-	-	ns
Aperture Jitter, t_{AJ}		-	30	-	-	-	ps
Data Output Enable Time, t_{EN}		-	18	25	-	30	ns
Data Output Disable Time, t_{DIS}		-	15	20	-	25	ns
Data Output Delay, t_{OD}		-	20	25	-	30	ns
Data Output Hold, t_H		10	20	-	5	-	ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	$V_{DD} = 5V$ ±10%	-	±0.1	±2.75	-	±5.0	LSB
Gain Error PSRR, ΔFSE	$V_{DD} = 5V$ ±10%	-	±0.1	±2.75	-	±5.0	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	$F_S = 20MHz$	-	145	180	-	190	mA

NOTES:

9. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

10. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

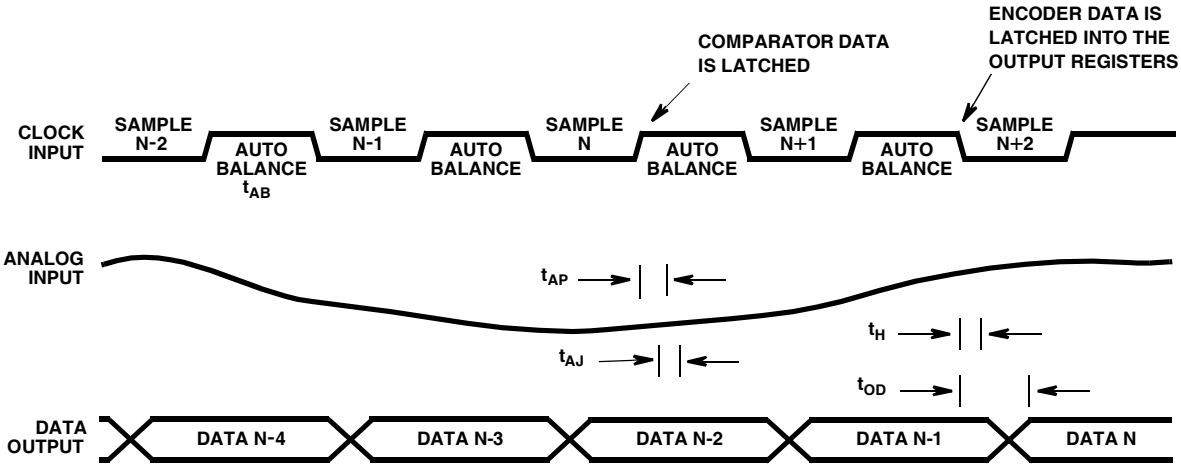


FIGURE 1. INPUT-TO-OUTPUT TIMING

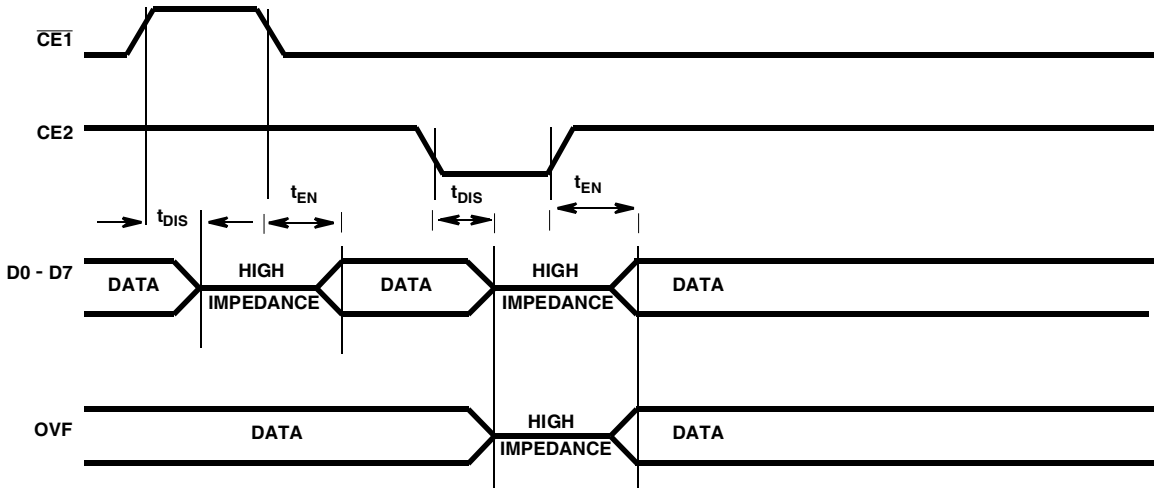


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

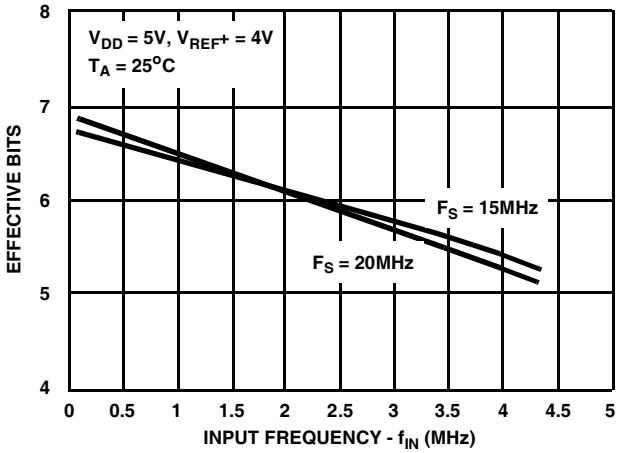


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

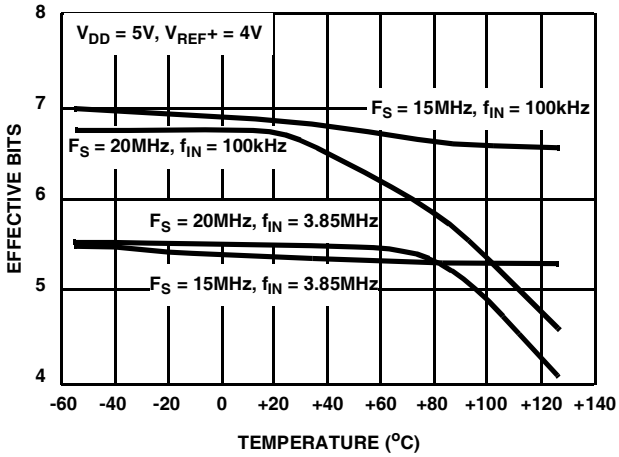


FIGURE 4. EFFECTIVE NUMBER OF BITS vs TEMPERATURE

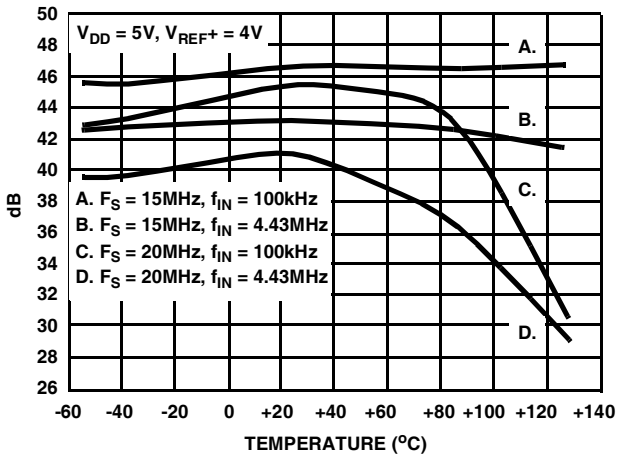


FIGURE 5. SNR vs TEMPERATURE

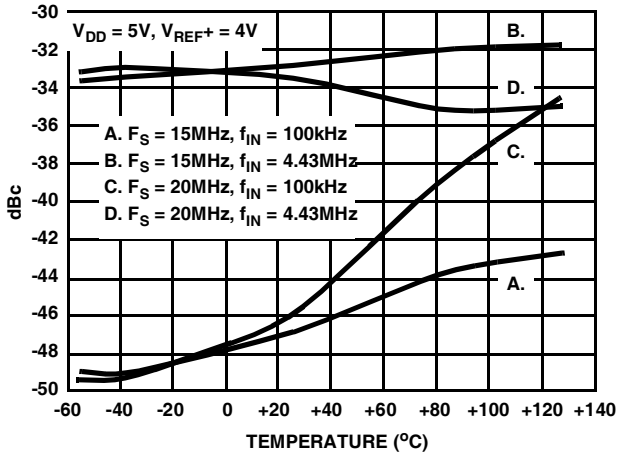


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

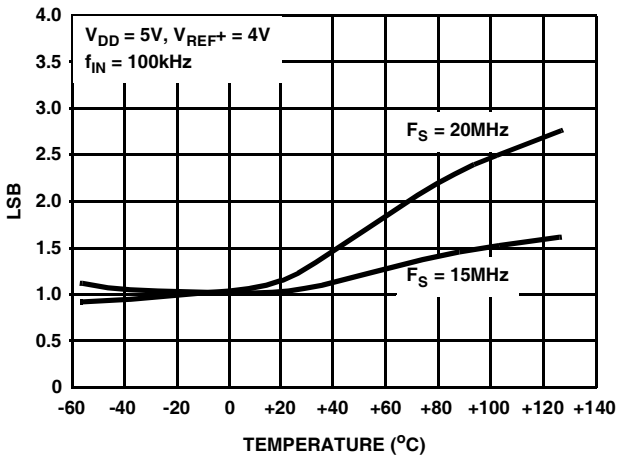


FIGURE 7. INL vs TEMPERATURE

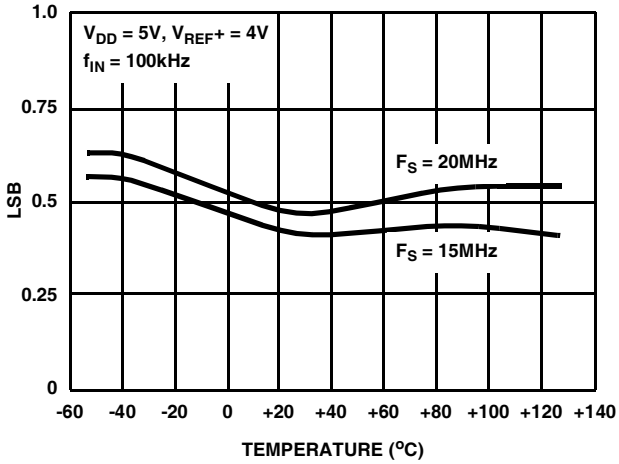


FIGURE 8. DNL vs TEMPERATURE

Typical Performance Curves (Continued)

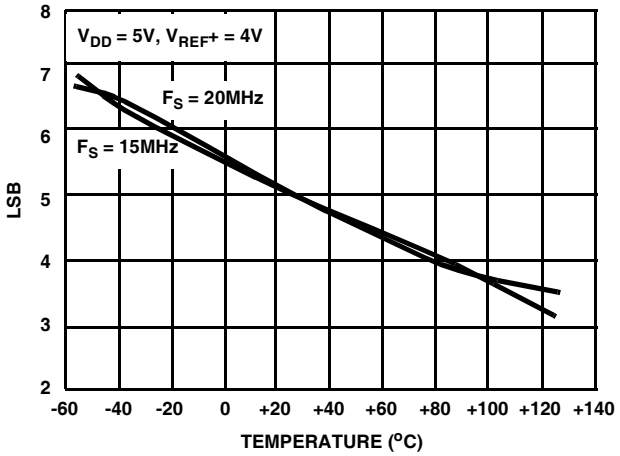


FIGURE 9. OFFSET VOLTAGE vs TEMPERATURE

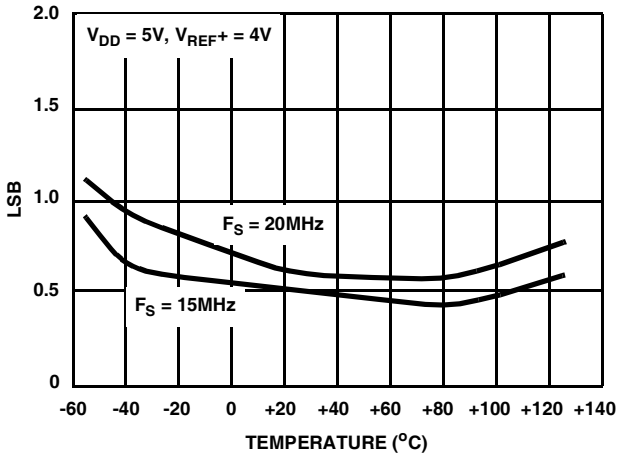


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

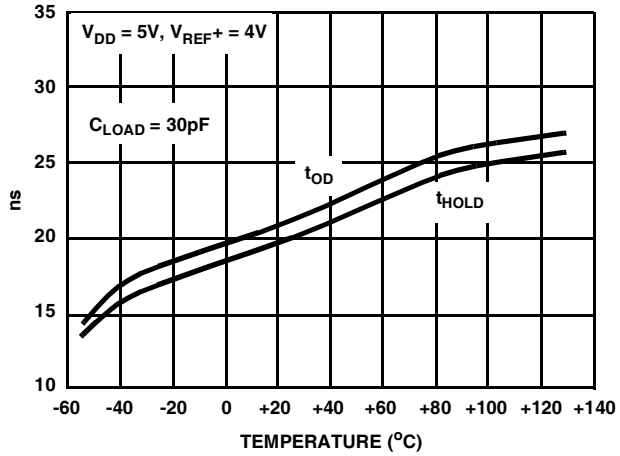


FIGURE 11. OUTPUT DELAY vs TEMPERATURE

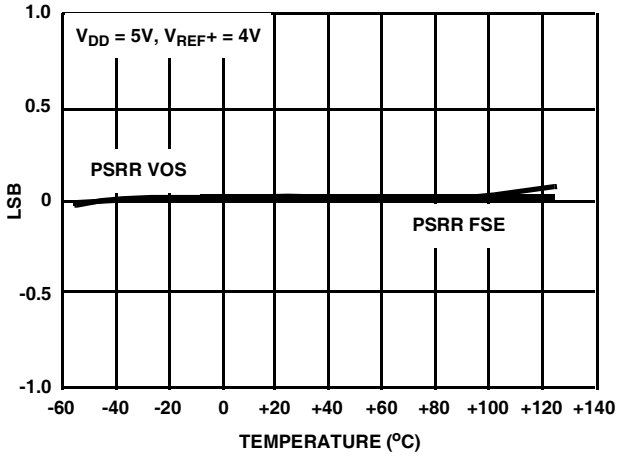


FIGURE 12. POWER SUPPLY REJECTION vs TEMPERATURE

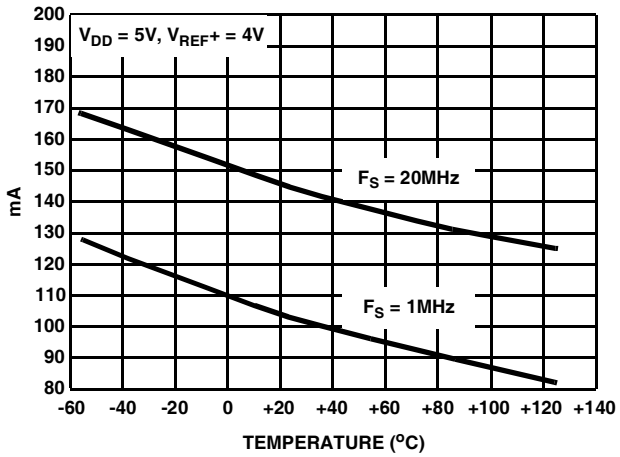


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

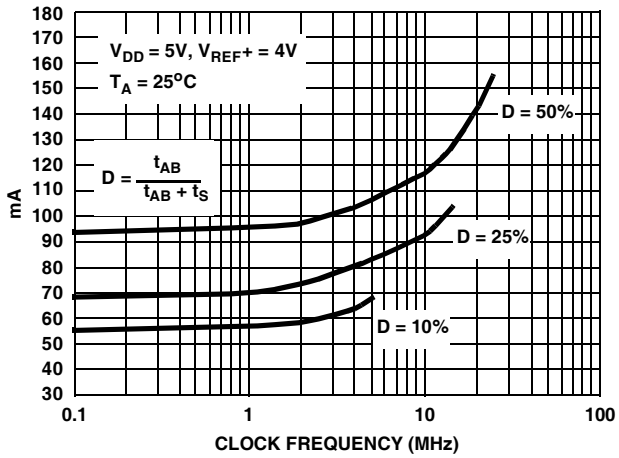


FIGURE 14. SUPPLY CURRENT vs CLOCK DUTY CYCLE

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	$^1/_4$R	$^1/_4$th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	$^3/_4$R	$^3/_4$th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Three-State Output Enable Input, Active High. (See Table 2)
16	$\overline{CE1}$	Three-State Output Enable Input, Active Low. (See Table 2)
17	V_{REF}+	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	$^1/_2$R	$^1/_2$ Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	V_{REF}-	Reference Voltage Negative Input
28	V_{IN}	Analog Input

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X's = Don't Care.

Theory of Operation

The HI-5700 is an 8-bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 256 comparators are used in the HI-5700: (2^8-1) comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5700 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5700 CMOS flash converter operates.

The input clock which controls the operation of the HI-5700 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between GND and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 256 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 256 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 Auto-Balancing state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 8 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds V_{REF}+ - 0.5 LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1

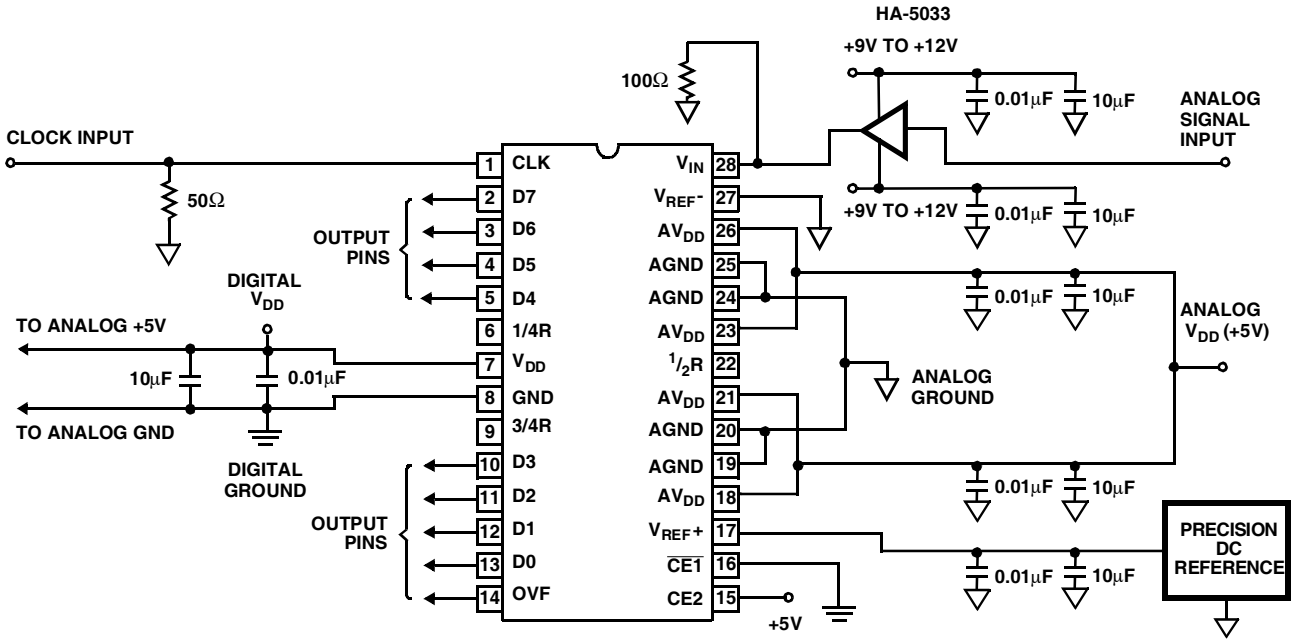


FIGURE 15. TEST CIRCUIT

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder between V_{REF}+ and V_{REF}-. In most applications, V_{REF}- is simply tied to analog ground such that the reference source drives V_{REF}+. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5700 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of (V_{REF}+ - V_{REF}-)/256, or 15.6mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2.5V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01μF and 10μF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap point pins for most applications.

It is possible to elevate V_{REF}- from ground if necessary. In this case, the V_{REF}- pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5700 provides a standard high speed interface to external CMOS and TTL logic families. Two chip enable inputs control the three-state outputs of output bits D0 through D7 and the Overflow (OVF) bit. As indicated in the Truth Table, all output bits are high impedance when CE2 is low, and output bits D0 through D7 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local group disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the “Theory of Operation” section. The Auto Balance ϕ1 half cycle of the clock may be reduced to approximately 20ns; the Sample ϕ2 half cycle may be varied from a minimum of 25ns to a maximum of 5μs.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feedthrough in the capacitor array. It varies with the amplitude of the analog input and the converter’s sampling

rate.

The signal source must absorb these transients prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HA-5004, HA-5002, and HA-5003.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +0.5 LSB are converted to all zeroes; input voltages of V_{REF}+ -0.5 LSB to V_{DD} +0.5V are converted to all ones with the Overflow bit set.

Full Scale Offset Error Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and reference tap point trims. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

Offset correction can be done in the preamp driving the converter by introducing a DC component to the input signal. An alternate method is to adjust V_{REF}- to produce the desired offset. It is adjusted such that the 0 to 1 code transition occurs at 0.5 LSB.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF}+ voltage. The reference voltage is the ideal location.

Quarter Point Adjustment

The reference tap points are brought out for linearity adjustment or creating a nonlinear transfer function if desired. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap points in most applications.

Power Supplies

The HI-5700 operates nominally from 5V supplies but will work from 3V to 6V. Power to the device is split such that analog and digital circuits within the HI-5700 are powered separately. The analog supply should be well regulated and “clean” from significant noise, especially high frequency noise. The digital supply should match the analog supply within about 0.5V and should be referenced externally to the analog supply at a single point. Analog and digital grounds should not be separated by more that 0.5V. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit.

Reducing Power Consumption

Power dissipation in the HI-5700 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by decreasing the Auto-Balance (ϕ1) portion of the clock duty cycle. This relationship is illustrated in the

TABLE 3. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE † V_{REF}+ = 4.0V V_{REF}- = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE								
			MSB								LSB
			OVF	D7	D6	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	511	1	1	1	1	1	1	1	1	1
Full Scale (FS)	3.9766	255	0	1	1	1	1	1	1	1	1
FS - 1 LSB	3.961	254	0	1	1	1	1	1	1	1	0
3/4 FS	2.992	192	0	1	1	0	0	0	0	0	0
1/2 FS	1.992	128	0	1	0	0	0	0	0	0	0
1/4 FS	0.992	64	0	0	1	0	0	0	0	0	0
1 LSB	0.0078	1	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0 LSB. The range of values possible is from -1.0 LSB (which implies a missing code) to greater than +1.0 LSB.

Full Power Input Bandwidth: Full power input bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 254 to 255 code transition and the ideal value of $V_{REF}+ - 1.5$ LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = $(V_{REF}+ - V_{REF}-)/256$. All HI-5700 specifications are given for a 15.6mV LSB size $V_{REF}+ = 4.0V$, $V_{REF}- = 0.0V$.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}- + 0.5$ LSB, V_{OS} Error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 254 to 255 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

Die Characteristics

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

TRANSISTOR COUNT: 8000

SUBSTRATE POTENTIAL (Powered Up): V+

Metallization Mask Layout

HI-5700