# SyncMOS

## F29C51002T/F29C51002B
## 2 MEGABIT (262,144 x 8 BIT)
## 5 VOLT CMOS FLASH MEMORY

### Features

- 256Kx8-bit Organization
- Address Access Time: 70, 90, 120, 150 ns
- Single 5V ± 10% Power Supply
- Sector Erase Mode Operation
- 16KB Boot Block (lockable)
- 512 bytes per Sector, 512 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Write Cycle Time: 35$\mu$s (Max)
- Minimum 10,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current: 20mA (Typ)
  - Active Program Current: 30mA (Typ)
  - Standby Current: 100$\mu$A (Max)
- Hardware Data Protection
- Low $V_{CC}$ Program Inhibit Below 3.5V
- Self-timed write/erase operations with end-of-cycle detection
  - $\overline{DATA}$ Polling
  - Toggle Bit
- CMOS and TTL Interface
- Available in one versions
  - F29C51002T (Top Boot Block)

- Packages:
  - 32-pin Plastic DIP
  - 32-pin TSOP-I
  - 32-pin PLCC

### Description

The F29C51002T/F29C51002B is a high speed 262,144 x 8 bit CMOS flash memory. Writing or erasing the device is done with a single 5 Volt power supply. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls to eliminate bus contention.

The F29C51002T/F29C51002B offers a combination of: Boot Block with Sector Erase/Write Mode. The end of write/erase cycle is detected by $\overline{DATA}$ Polling of I/O$_7$ or by the Toggle Bit I/O$_6$.
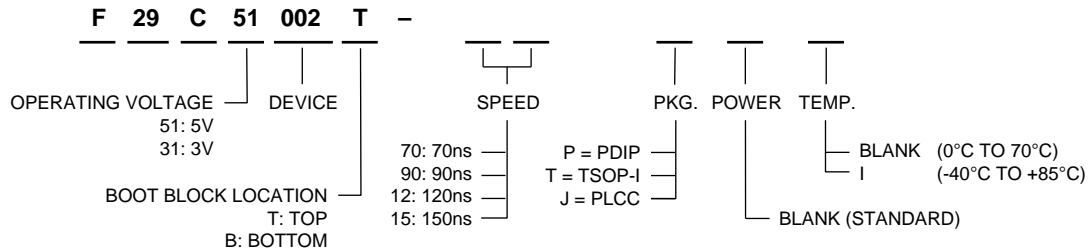
The F29C51002T/F29C51002B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

Boot block architecture enables the device to boot from a protected sector located either at the top (F29C51002T) or the bottom (F29C51002B). All inputs and outputs are CMOS and TTL compatible.

The F29C51002T/F29C51002B is ideal for applications that require updatable code and data storage.

### Device Usage Chart

| Operating Temperature Range | Package Outline | | | Access Time (ns) | | | | Power | Temperature Mark |
|---|---|---|---|---|---|---|---|---|---|
| | P | T | J | 70 | 90 | 120 | 150 | Std. | |
| 0°C to 70 °C | • | • | • | • | • | • | • | • | Blank |
| –40°C to +85°C | • | • | • | • | • | • | • | • | I |

# SyncMOS

```
F   29   C   51   002   T   –
```

OPERATING VOLTAGE
51: 5V
31: 3V

DEVICE

SPEED

PKG.  POWER  TEMP.

70: 70ns — 
90: 90ns — 
12: 120ns — 
15: 150ns — 

P = PDIP — 
T = TSOP-I — 
J = PLCC — 

BLANK  (0°C TO 70°C)
I       (-40°C TO +85°C)

BOOT BLOCK LOCATION
T: TOP
B: BOTTOM

BLANK (STANDARD)

51002-01

## Pin Configurations
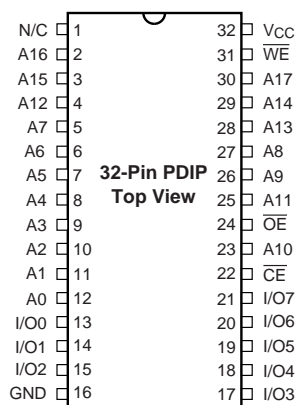


51002-02
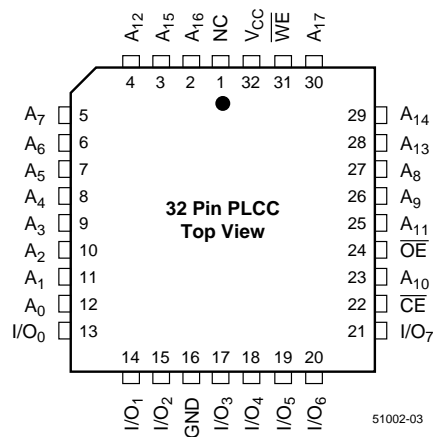


51002-03



51002-04

## Pin Names

| $A_0$–$A_{17}$ | Address Inputs |
|---|---|
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | 5V ± 10% Power Supply |
| GND | Ground |
| NC | No Connect |
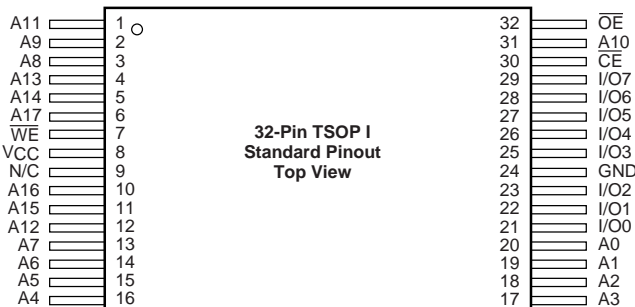
## Functional Block Diagram



51002-07
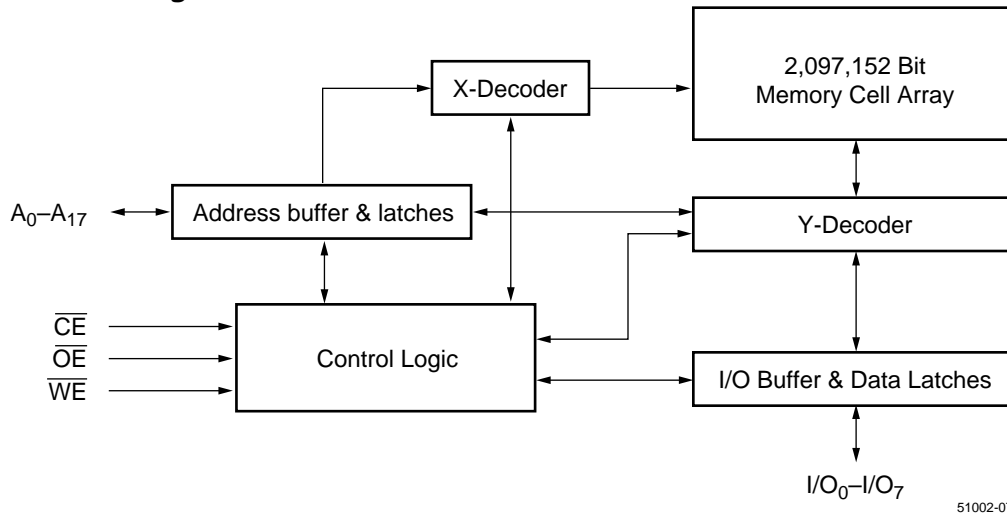
## Capacitance [1,2]

| Symbol | Parameter | Test Setup | Typ. | Max. | Units |
|--------|-----------|------------|------|------|-------|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0$ | 6 | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0$ | 8 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN} = 0$ | 8 | 10 | pF |

**NOTE:**
1. Capacitance is sampled and not 100% tested.
2. $T_A = 25°C$, $V_{CC} = 5V \pm 10\%$, f = 1 MHz.

## Latch Up Characteristics[1]

| Parameter | Min. | Max. | Unit |
|-----------|------|------|------|
| Input Voltage with Respect to GND on $A_9$, $\overline{OE}$ | -1 | +13 | V |
| Input Voltage with Respect to GND on I/O, address or control pins | -1 | $V_{CC} + 1$ | V |
| $V_{CC}$ Current | -100 | +100 | mA |

**NOTE:**
1. Includes all pins except $V_{CC}$. Test conditions: $V_{CC} = 5V$, one pin at a time.

## AC Test Load



51002-08
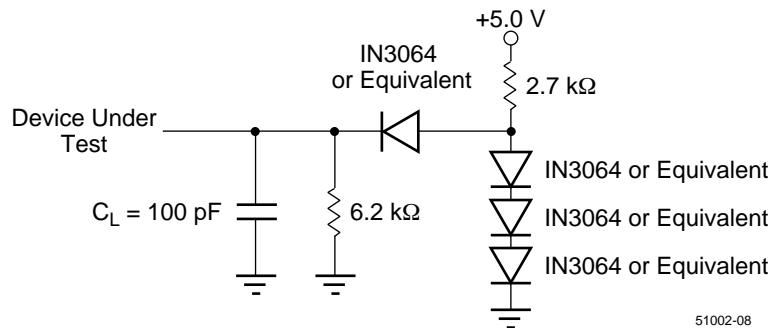
## Absolute Maximum Ratings[1]

| Symbol | Parameter | Commercial | Industrial | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage (input or I/O pins) | -2 to +7 | -2 to +7 | V |
| $V_{IN}$ | Input Voltage ($A_9$ pin, $\overline{OE}$) | -2 to +13 | -2 to +13 | V |
| $V_{CC}$ | Power Supply Voltage | -0.5 to +5.5 | -0.5 to +5.5 | V |
| $T_{STG}$ | Storage Temerpature (Plastic) | -65 to +125 | -65 to +150 | °C |
| $T_{OPR}$ | Operating Temperature | 0 to +70 | -40 to + 85 | °C |
| $I_{OUT}$ | Short Circuit Current[2] | 200 (Max.) | 200 (Max.) | mA |

**NOTE:**

1. Stress greater than those listed unders "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. No more than one output maybe shorted at a time and not exceeding one second long.

## DC Electrical Characteristics

(over the commercial operating range)

| Parameter Name | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | $V_{CC} = V_{CC}$ Min. | — | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC} = V_{CC}$ Max. | 2 | — | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$, $V_{CC} = V_{CC}$ Max. | — | ±1 | μA |
| $I_{OL}$ | Output Leakage Current | $V_{OUT}$ = GND to $V_{CC}$, $V_{CC} = V_{CC}$ Max. | — | ±10 | μA |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = V_{CC}$ Min., $I_{OL}$ = 2.1mA | — | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = V_{CC}$ Min, $I_{OH}$ = -400μA | 2.4 | — | V |
| $I_{CC1}$ | Read Current | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, all I/Os open, Address input = $V_{IL}/V_{IH}$, at f = 1/$t_{RC}$ Min., $V_{CC} = V_{CC}$ Max. | — | 40 | mA |
| $I_{CC2}$ | Write Current | $\overline{CE} = \overline{WE}$ = VIL, $\overline{OE} = V_{IH}$, $V_{CC} = V_{CC}$ Max. | — | 50 | mA |
| $I_{SB}$ | TTL Standby Current | $\overline{CE} = \overline{OE} = \overline{WE} = V_{IH}$, $V_{CC} = V_{CC}$ Max. | — | 2 | mA |
| $I_{SB1}$ | CMOS Standby Current | $\overline{CE} = \overline{OE} = \overline{WE} = V_{CC} - 0.3V$, $V_{CC} = V_{CC}$ Max. | — | 100 | μA |
| $V_H$ | Device ID Voltage for $A_9$ | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ | 11.5 | 12.5 | V |
| $I_H$ | Device ID Current for $A_9$ | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, A9 = $V_H$ Max. | — | 50 | μA |

## AC Electrical Characteristics

(over all temperature ranges)

### Read Cycle

| Parameter Name | Parameter | -70 | | -90 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 70 | — | 90 | — | 120 | — | 150 | — | ns |
| $t_{AA}$ | Address Access Time | — | 70 | — | 90 | — | 120 | — | 150 | ns |
| $t_{ACS}$ | Chip Enable Access Time | — | 70 | — | 90 | — | 120 | — | 150 | ns |
| $t_{OE}$ | Output Enable Access Time | — | 35 | — | 45 | — | 60 | — | 75 | ns |
| $t_{CLZ}$ | $\overline{CE}$ Low to Output Active | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{OLZ}$ | $\overline{OE}$ Low to Output Active | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{DF}$ | $\overline{OE}$ or $\overline{CE}$ High to Output in High Z | 0 | 30 | 0 | 40 | 0 | 50 | 0 | 60 | ns |
| $t_{OH}$ | Output Hold from Address Change | 0 | — | 0 | — | 0 | — | 0 | — | ns |

### Program (Erase/Program) Cycle

| Parameter Name | Parameter | -70 | | | -90 | | | -12 | | | -15 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{WC}$ | Write Cycle Time | 70 | — | — | 90 | — | — | 120 | — | — | 150 | — | — | ns |
| $t_{AS}$ | Address Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{AH}$ | Address Hold Time | 45 | — | — | 45 | — | — | 50 | — | — | 50 | — | — | ns |
| $t_{CS}$ | $\overline{CE}$ Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{CH}$ | $\overline{CE}$ Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{OES}$ | $\overline{OE}$ Setup Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{OEH}$ | $\overline{OE}$ High Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 35 | — | — | 45 | — | — | 50 | — | — | 50 | — | — | ns |
| $t_{WPH}$ | $\overline{WE}$ Pulse Width High | 20 | — | — | 30 | — | — | 35 | — | — | 35 | — | — | ns |
| $t_{DS}$ | Data Setup Time | 30 | — | — | 30 | — | — | 30 | — | — | 30 | — | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | — | ns |
| $t_{WHWH1}$ | Programming Cycle | — | — | 35 | — | — | 35 | — | — | 35 | — | — | 35 | μs |
| $t_{WHWH2}$ | Sector Erase Cycle | — | — | 10 | — | — | 10 | — | — | 10 | — | — | 10 | ms |
| $t_{WHWH3}$ | Chip Erase Cycle | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | — | 3.0 | sec |

## Waveforms of Read Cycle
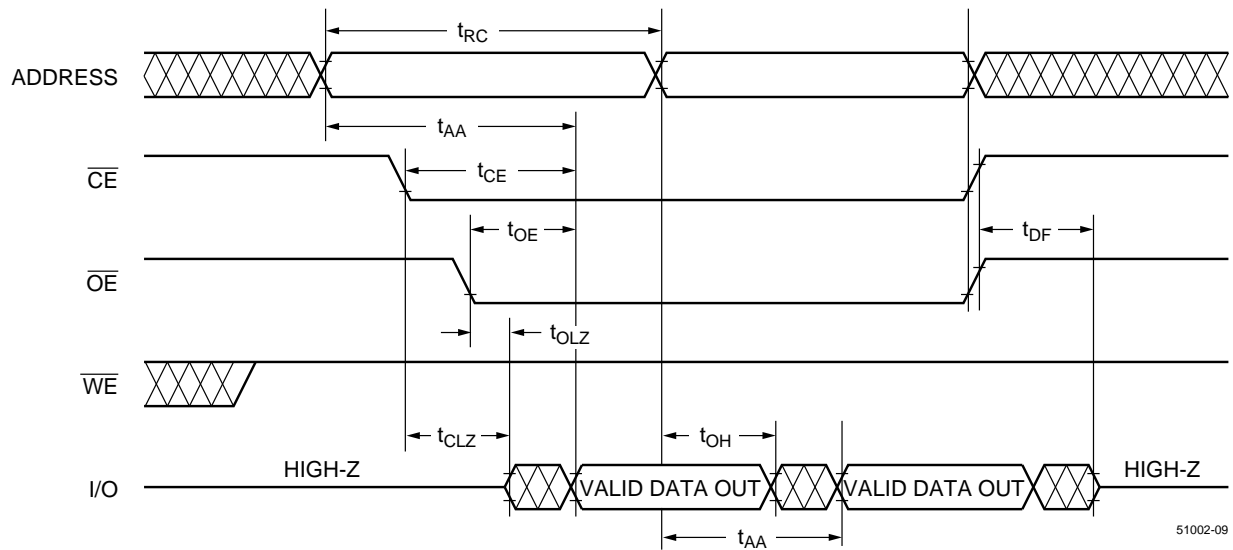


51002-09

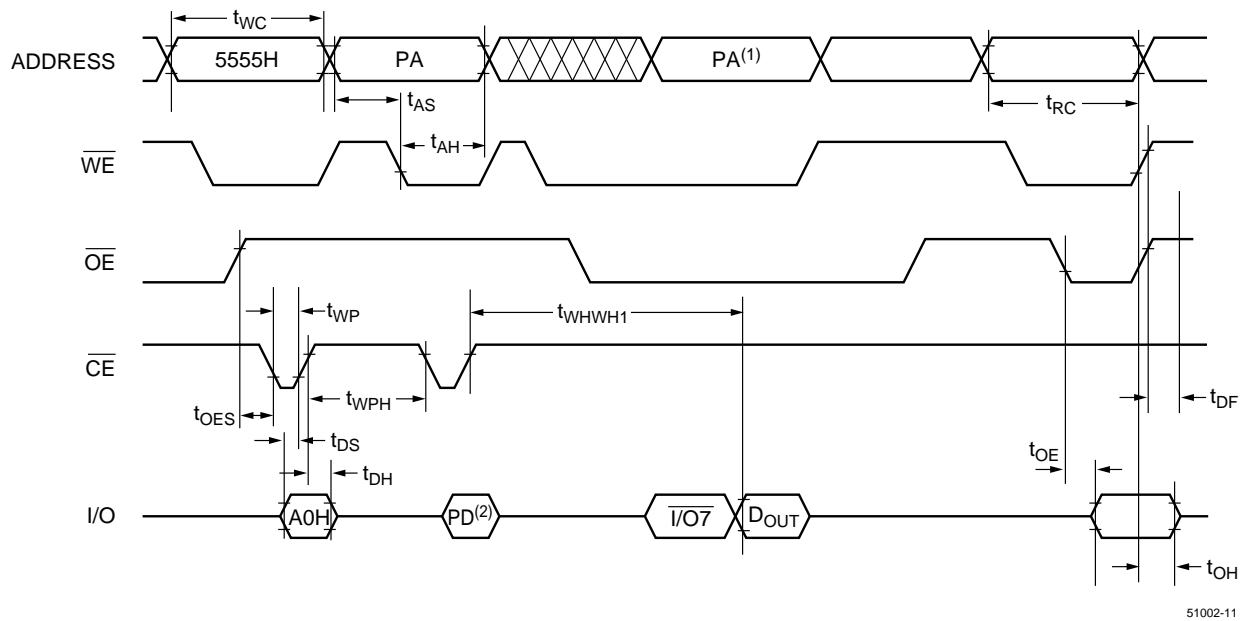## Waveforms of $\overline{WE}$ Controlled-Program Cycle
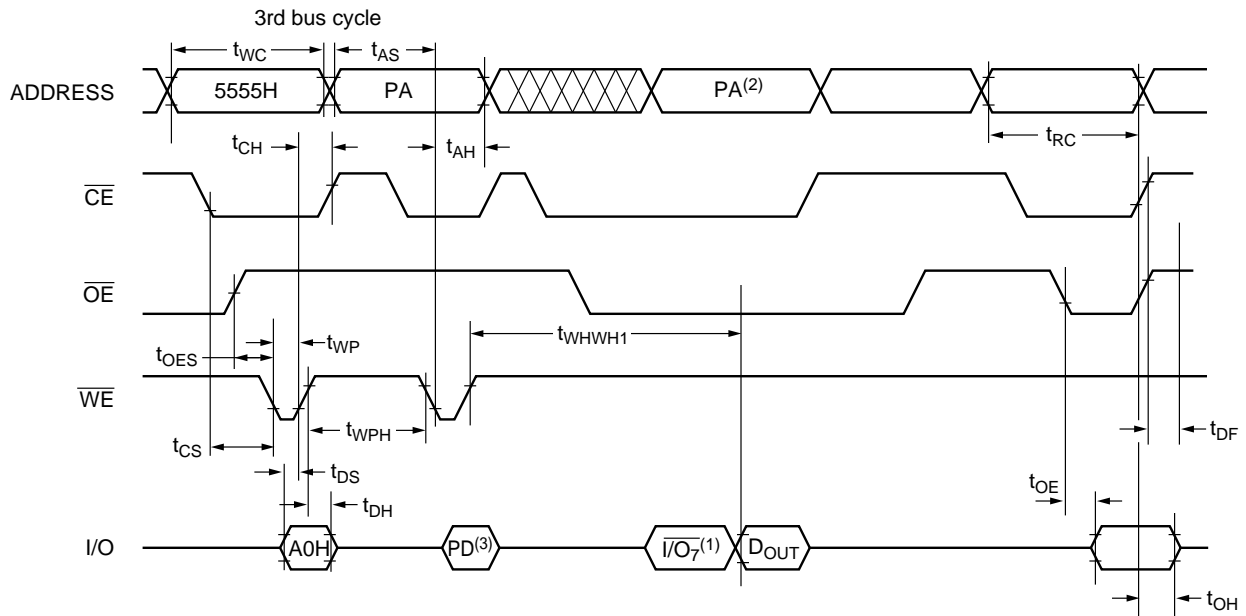


51002-10

**NOTES:**

1.  $I/O_7$: The output is the complement of the data written to the device.
2.  PA: The address of the memory location to be programmed.
3.  PD: The data at the byte address to be programmed.

## Waveforms of CE Controlled-Program Cycle



51002-11

## Waveforms of Erase Cycle[1]



51002-12
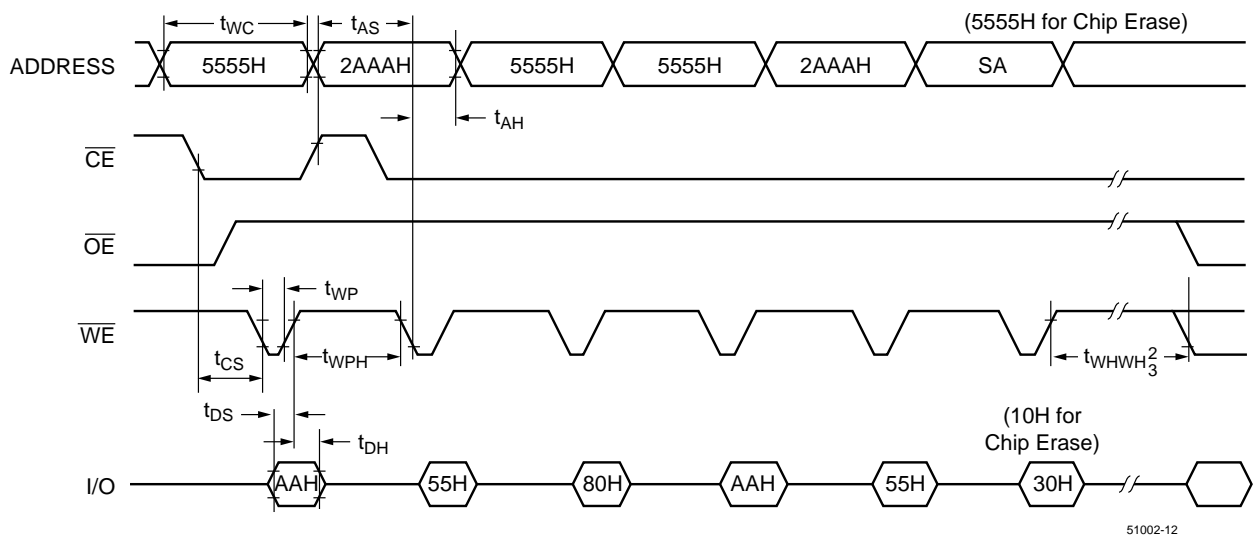
**NOTES:**
1.  PA: The address of the memory location to be programmed.
2.  PD: The data at the byte address to be programmed.
3.  SA: The sector address for Sector Erase.

### *Waveforms of $\overline{DATA}$ Polling Cycle*



51002-13

### *Waveforms of Toggle Bit Cycle*



51002-14

## Functional Description

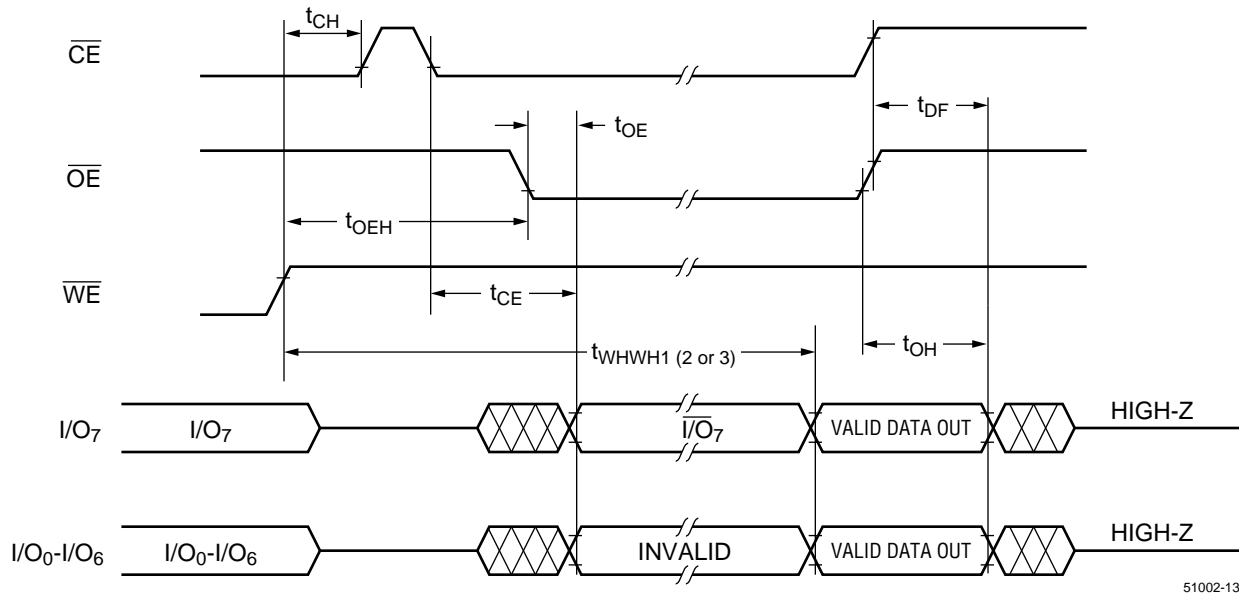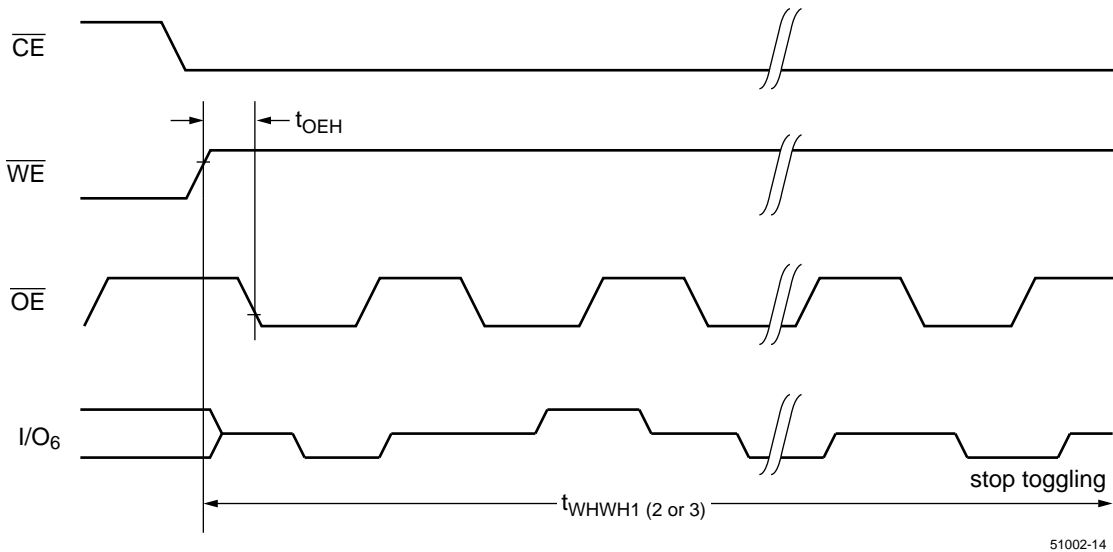The F29C51002T/F29C51002B consists of 512 equally-sized sectors of 512 bytes each. The 16 KB lockable Boot Block is intended for storage of the system BIOS boot code. The boot code is the first piece of code executed each time the system is powered on or rebooted.

The F29C51002 is available in two versions: the F29C51002T with the Boot Block address starting from 3C000H to 3FFFFH, and the F29C51002B with the Boot Block address starting from 00000H to 3FFFFH.

## Read Cycle

A read cycle is performed by holding both $\overline{CE}$ and $\overline{OE}$ signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle $\overline{WE}$ must be HIGH prior to $\overline{CE}$ and $\overline{OE}$ going LOW. $\overline{WE}$ must remain HIGH during the read operation for the read to complete (see Table 1).

## Output Disable

Returning $\overline{OE}$ or $\overline{CE}$ HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

## Standby

The device will enter standby mode when the $\overline{CE}$ signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the $\overline{OE}$ input state.

## Byte Write Cycle

The F29C51002T/F29C51002B is programmed on a byte-by-byte basis. The byte write operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).
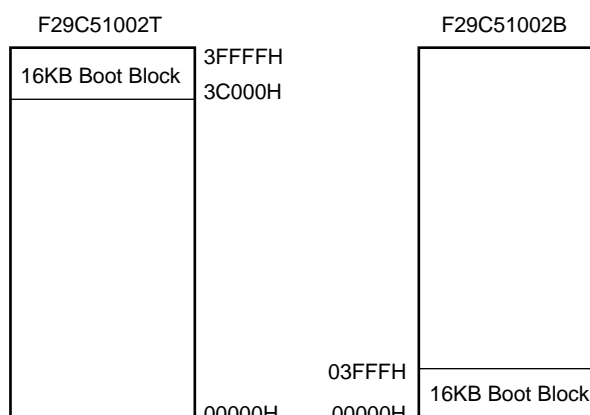


**16KB Boot Block = 32 Sectors**

During the byte write cycle, addresses are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever is last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The byte write cycle can be $\overline{CE}$ controlled or $\overline{WE}$ controlled.

## Sector Erase Cycle

The F29C51002T/F29C51002B features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (see Table 2). A sector must be first erased before it can be re-written. While in the internal erase mode, the device ignores any program attempt into the device. The internal erase completion can be determined via DATA polling or toggle bit status.

The F29C51002T/F29C51002B is shipped fully erased (all bits = 1).

## Table 1. Operation Modes Decoding

| Decoding Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $A_0$ | $A_1$ | $A_9$ | I/O |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $A_0$ | $A_1$ | $A_9$ | READ |
| Byte Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $A_0$ | $A_1$ | $A_9$ | PD |
| Standby | $V_{IH}$ | X | X | X | X | X | HIGH-Z |
| Autoselect Device ID | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $V_H$ | CODE |
| Autoselect Manufacture ID | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_H$ | CODE |
| Enabling Boot Block Protection Lock | $V_{IL}$ | $V_H$ | $V_{IL}$ | X | X | $V_H$ | X |
| Disabling Boot Block Protection Lock | $V_H$ | $V_H$ | $V_{IL}$ | X | X | $V_H$ | X |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | X | HIGH-Z |

**NOTES:**
1. X = Don't Care, $V_{IH}$ = HIGH, $V_{IL}$ = LOW, $V_H$ = 12.5V Max.
2. PD: The data at the byte address to be programmed.

### Table 2. Command Codes

| Command Sequence | First Bus Program Cycle | | Second Bus Program Cycle | | Third Bus Program Cycle | | Fourth Bus Program Cycle | | Fifth Bus Program Cycle | | Six Bus Program Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data |
| Read | XXXXH | F0H | | | | | | | | | | |
| Read | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | RA(1) | RD(2) | | | | |
| Autoselect Mode | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | See table 3 for detail. | | | | | |
| Byte Program | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | PA | PD(4) | | | | |
| Chip Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Sector Erase | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | SA(5) | 30H |

**NOTES:**
1. RA: Read Address
2. RD: Read Data
3. PA: The address of the memory location to be programmed.
4. PD: The data at the byte address to be programmed.
5. SA(5): Sector Address

### Chip Erase Cycle

The F29C51002T/F29C51002B features a chip-erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when the data on DQ7 is "1".

### Program Cycle Status Detection

There are two methods for determining the state of the F29C51002T/F29C51002B during a program (erase/write) cycle: $\overline{DATA}$ Polling ($I/O_7$) and Toggle Bit ($I/O_6$).

### $\overline{DATA}$ Polling ($I/O_7$)

The F29C51002T/F29C51002B features $\overline{DATA}$ polling to indicate the end of a program cycle. When the device is in the program cycle, any attempt to read the device will received the complement of the loaded data on $I/O_7$. Once the program cycle is completed, $I/O_7$ will show true data, and the device is then ready for the next cycle.

### Toggle Bit ($I/O_6$)

The F29C51002T/F29C51002B also features another method for determining the end of a program cycle. When the device is in the program cycle, any attempt to read the device will result in $I/O_6$ toggling between 1 and 0. Once the program is completed, the toggling will stop. The device is then ready for the next operation. Examining the toggle bit may begin at any time during a program cycle.

### Boot Block Protection Enabling/Disabling

The F29C51002T/F29C51002B features hardware Boot Block Protection. The boot block sector protection is enabled when high voltage (12.5V) is applied to $\overline{OE}$ and A9 pins with $\overline{CE}$ pin LOW and $\overline{WE}$ pin LOW. The sector protection is disabled when high voltage is applied to $\overline{OE}$, $\overline{CE}$ and A9 pins with $\overline{WE}$ pin LOW. Other pins can be HIGH or LOW. This is shown in table 1.

### Autoselect Mode

The F29C51002T/F29C51002B features an Autoselect mode to identify boot block locking status, device ID and manufacturer ID.

Entering Autoselect mode is accomplished by applying a high voltage (VH) to the A9 Pin, or through a sequence of commands (as shown in table 2). Device will exit this mode once high voltage on A9 is removed or another command is loaded into the device.

### Boot Block Protection Status

In Autoselect mode, performing a read at address location 3CXX2H (F29C51002T) or 0CXX2H (F29C51002B) will indicate boot block protection status. If the data is 01H, the boot block is protected. If the data is 00H, the boot block is unprotected. This is also shown is table 3.

### Device ID

In Autoselect mode, performing a read at address XXX1H will determine whether the device is a Top Boot Block device or a Bottom Boot Block device. If the data is 02H, the device is a Top Boot Block. If the data is A2H, the device is a Bottom Boot Block device (see Table 3).

### Manufacturer ID

In Autoselect mode, performing a read at address XXXX0H will determine the manufacturer ID. 40H is the manufacturer code for SyncMOS Flash.

### Hardware Data Protection

$V_{CC}$ *Detection:* the program operation is inhibited when VCC is less than 3.5V.

*Noise Protection:* a CE or WE pulse of less than 5ns will not initiate a program cycle.

*Program Inhibit:* holding any one of $\overline{OE}$ LOW, $\overline{CE}$ HIGH or $\overline{WE}$ HIGH inhibits a program cycle.

### Table 3. Autoselect Decoding

| Decoding Mode | Boot Block | Address | | | | Data I/O$_0$–I/O$_7$ |
|---|---|---|---|---|---|---|
| | | $A_0$ | $A_1$ | $A_2$–$A_{13}$ | $A_{14}$–$A_{17}$ | |
| Boot Block Protection | Top | $V_{IL}$ | $V_{IH}$ | X | $V_{IH}$ | 01H: protected |
| | Bottom | $V_{IL}$ | $V_{IH}$ | X | $V_{IL}$ | 00H: unprotected |
| Device ID | Top | $V_{IH}$ | $V_{IL}$ | X | X | 02H |
| | Bottom | | | | | A2H |
| Manufacture ID | | $V_{IL}$ | $V_{IL}$ | X | X | 40H |

**NOTE:**

1. X = Don't Care, $V_{IH}$ = HIGH, $V_{IL}$ = LOW.

## Byte Program Algorithm

```
┌─────────────────────────┐
│      Write Byte-Write    │
│     Command Sequence     │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐ ┐
│        Add/Data          │ │
│        5555H/AAH         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │  Four Bus
│        2AAAH/55H         │ │  Cycle
└─────────────────────────┘ │  Sequence
            │               │
            ▼               │
┌─────────────────────────┐ │
│        5555H/A0H         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │
│          PA/PD           │ │
└─────────────────────────┘ ┘
            │
            ▼
┌─────────────────────────┐
│ Data Polling or Toggle bit│
│  successfully completed   │
│  or t_WTWH (2 or 3) timeout│
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│        Writing           │
│       Completed          │
└─────────────────────────┘
```

Data Polling or Toggle bit successfully completed or $t_{WTWH\ (2\ or\ 3)}$ timeout
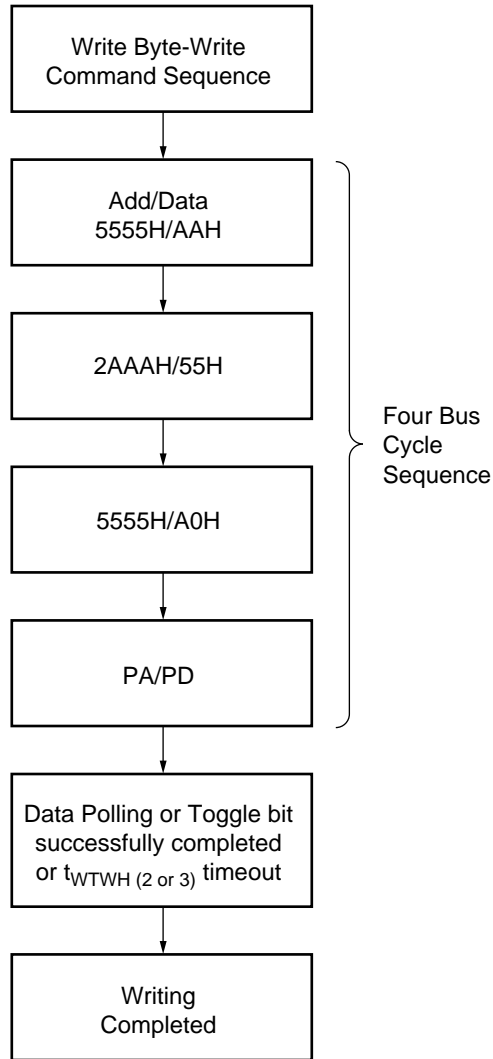
## Chip/Sector Erase Algorithm

```
┌─────────────────────────┐
│       Write Erase        │
│     Command Sequence     │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐ ┐
│        Add/Data          │ │
│        5555H/AAH         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │
│        2AAAH/55H         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │
│        5555H/80H         │ │
└─────────────────────────┘ │  Six Bus
            │               │  Cycle
            ▼               │  Sequence
┌─────────────────────────┐ │
│        5555H/AAH         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │
│        2AAAH/55H         │ │
└─────────────────────────┘ │
            │               │
            ▼               │
┌─────────────────────────┐ │
│  5555H/10H (Chip Erase)  │ │
│  SA/30H (Sector Erase)   │ │
└─────────────────────────┘ ┘
            │
            ▼
┌─────────────────────────┐
│ Data Polling or Toggle bit│
│  successfully completed   │
│  or t_WTWH (2 or 3) timeout│
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│     Erase Completed      │
└─────────────────────────┘
```

Data Polling or Toggle bit successfully completed or $t_{WTWH\ (2\ or\ 3)}$ timeout
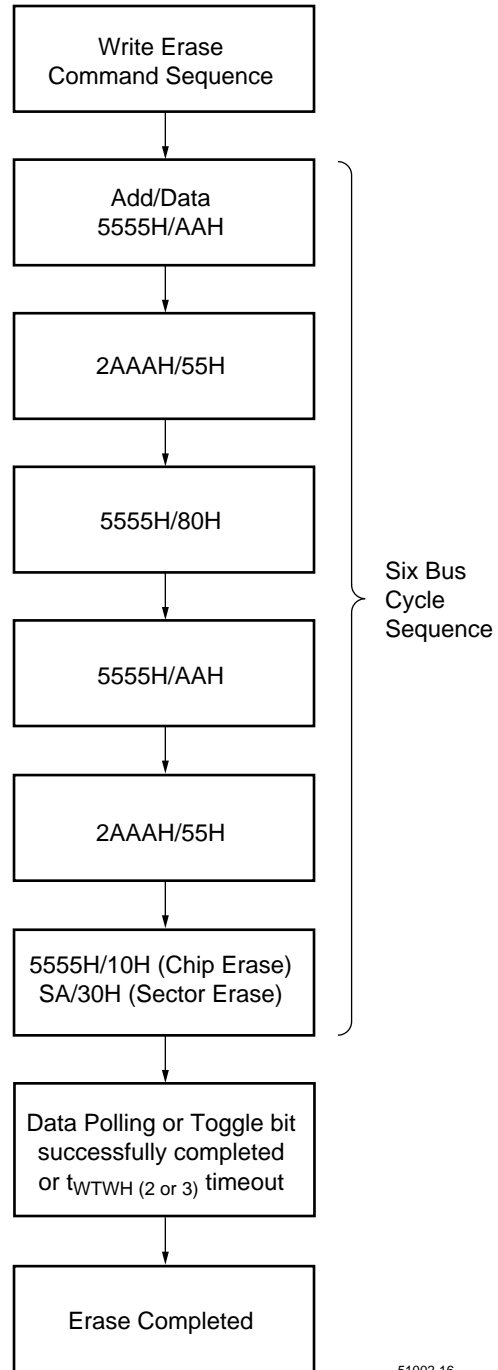
51002-16

## DATA Polling Algorithm

Read I/O$_7$
Address = PBA[1]

↓

I/O$_7$ = Data

No

Yes

Program
Done

## Toggle Bit Algorithm

Read I/O$_6$

↓

Read I/O$_6$

↓

I/O$_6$ Toggle

Yes

No
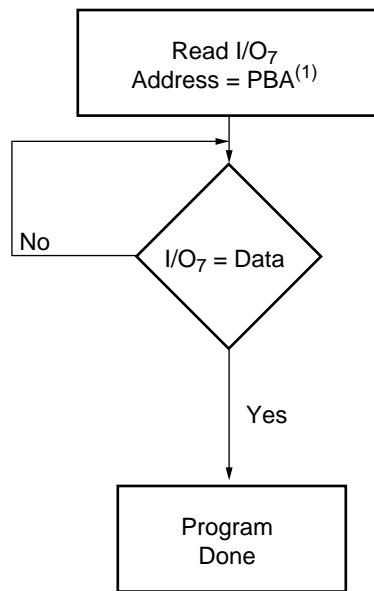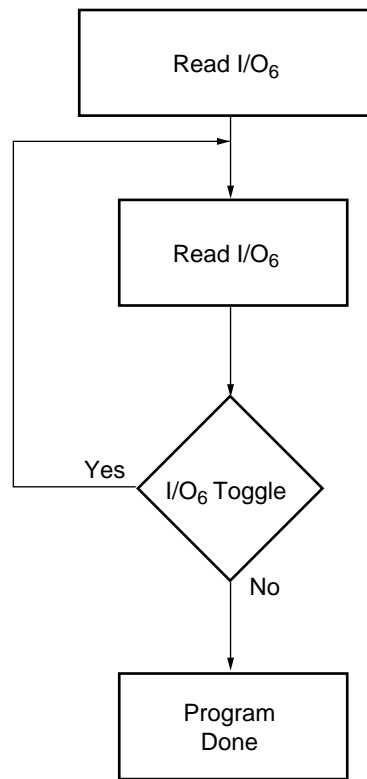
Program
Done

51002-17

**NOTE:**
1.    PBA: The byte address to be programmed.
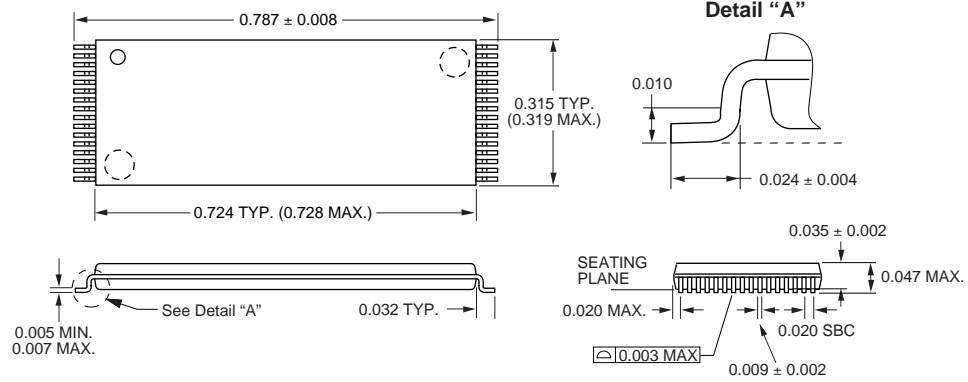
## Package Diagrams

### 32-pin Plastic DIP

INDEX-1
EJECTOR MARK
INDEX-2

1.660 MAX.

0.545/0.555

15° MAX

.600 TYP

$.010 \begin{smallmatrix} +.004 \\ -.0004 \end{smallmatrix}$

.050 MAX

0.210 MAX

0.120 MIN

0.010 MIN

$\frac{.100}{TYP}$

$.047 \begin{smallmatrix} +.012 \\ -0 \end{smallmatrix}$

$.018 \begin{smallmatrix} +.006 \\ -.002 \end{smallmatrix}$

$.032 \begin{smallmatrix} +.012 \\ -0 \end{smallmatrix}$

### 32-pin PLCC

.590 ± .005

.550 ± .003

.045X45°

.450 ± .003

.490 ± .005

.420 ± .003

.050 TYP

.136 ± .003

.046 ± .003

.025

.110

30°

.017

3° - 6°

3° - 6°

3° - 6°
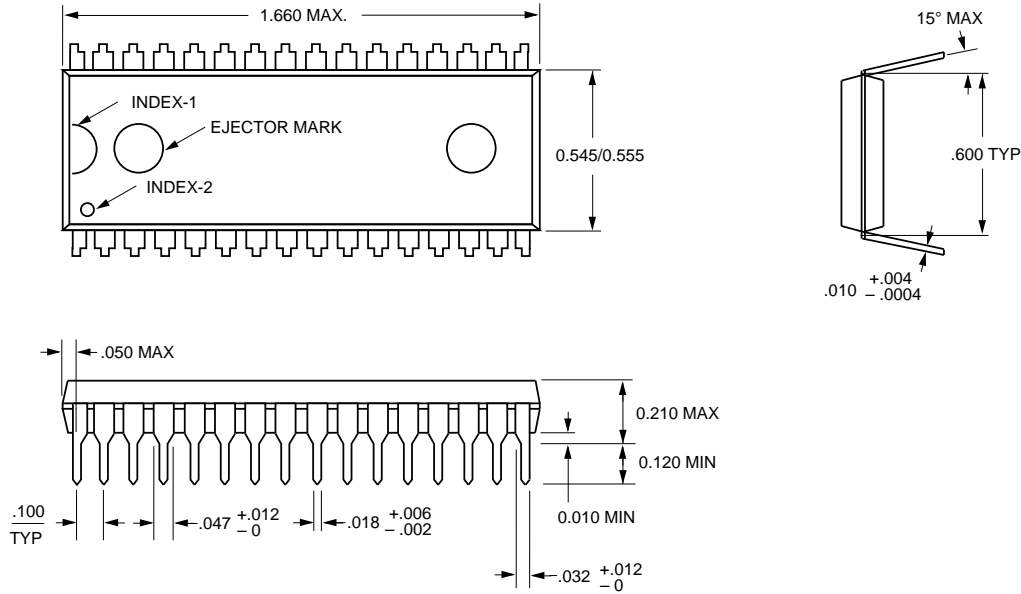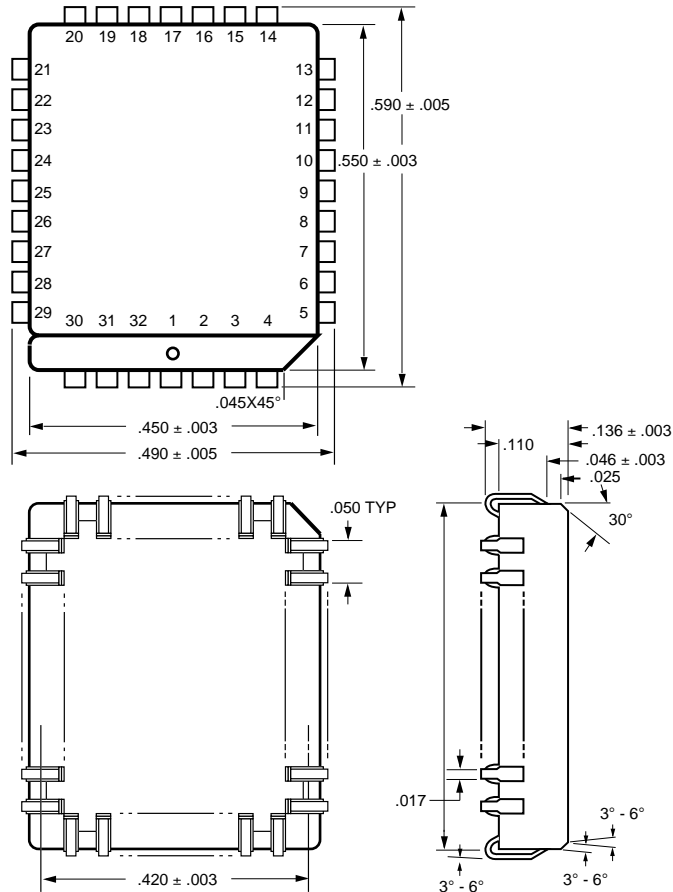
## 32-pin TSOP-I

**Units in inches**

0.787 ± 0.008

0.315 TYP.
(0.319 MAX.)

0.724 TYP. (0.728 MAX.)

**Detail "A"**

0.010

0.024 ± 0.004

See Detail "A"

0.032 TYP.

0.005 MIN.
0.007 MAX.

0.035 ± 0.002

SEATING
PLANE

0.047 MAX.

0.020 MAX.

0.020 SBC

0.003 MAX

0.009 ± 0.002

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**Note :**

1. Publication date : November 1998 Rev. A

2. All data and specification are subject changed with Program

   (Erase/Program) Cycle as below description :

   a. Chip erase time : 2.0 sec  →  3.0 sec maximum.

   b. Byte program time : 20 usec  →  35 usec maximum