T-49-19-08

Microchip

PIC1655

8-Bit Microcontroller

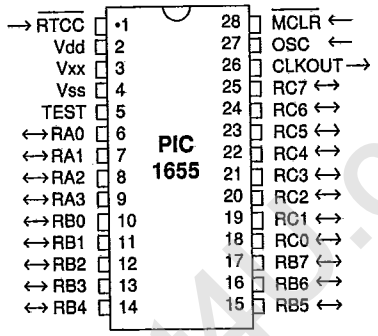
FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- External or RC input oscillator mask option
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in three temperature ranges: 0° to 70°C, -40° to 85°C and -40° to 110°C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting

PIN CONFIGURATION

28 LEAD DUAL INLINE

Top View



DESCRIPTION

The PIC®1655 microcontroller is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities for motor controls, telecommunication equipment, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1655 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICALC, a powerful macroassembler. PICALC is available in a MS-DOS version that can be run on an IBM PC or compatible computer system. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROMless PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROM's. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-along mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

4

ARCHITECTURAL DESCRIPTION

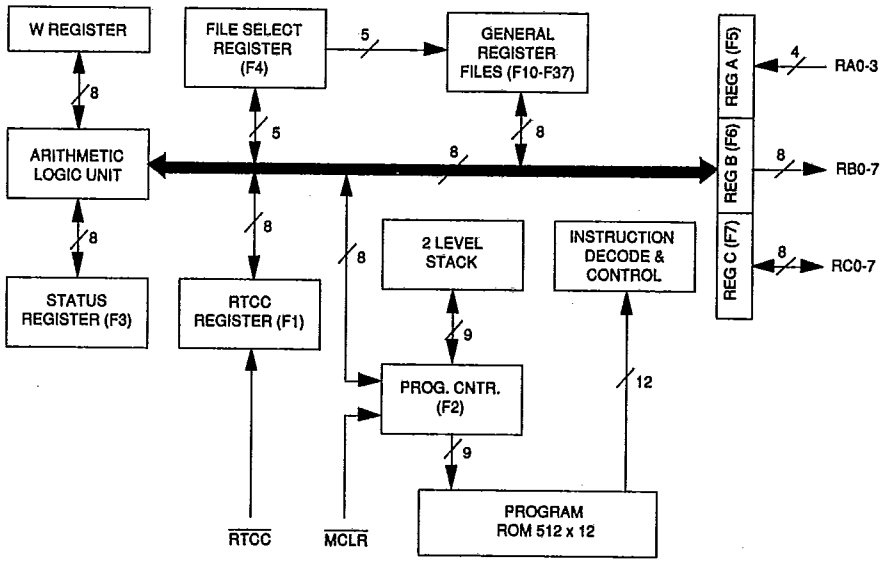
The firmware architecture of the PIC series microcontroller is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the ROM program to address 777$_8$.

PIC1655 BLOCK DIAGRAM



T-49-19-08

PIN FUNCTION TABLE

Name	Function
OSC1 (Input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
RTCC (Input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-3 (input)	4 input lines.
RB0-7 (output)	8 output lines.
RC0-7 (input/output)	8 user programmable input/output lines.
MCLR (input)	Master Clear. Used to initialize the internal ROM program to address 777$_8$ and latch all I/O register high. Should be held low at least 1 ms past the time when the power supply is valid. This is a Schmitt trigger input. RAM registers are not initialized by Master Clear
CLKOUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground.

4

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W + F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input RTCC. However, if data is being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction. (7) (6) (5) (4) (3) (2) (1) (0) 1 1 1 1 1 Z DC C C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source. DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant. Z (Zero): Set if the result of an Arithmetic operation is zero. Bits: 3-7 These bits are defined as logic ones.
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4 - A7 defined as zeros).
F6	Output Registers B (B0-B7).
F7	I/O Register C (C0-C7).
F10s-F37s	General Purpose Registers.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code that specifies the instruction type and one or more operands specifying the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit oriented instructions, "b" represents a bit field designator that selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight- or nine-bit constant or literal value.

For an oscillator frequency of 1 MHz the instruction execution time is 4 µsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these cases, the instruction execution time is 8 µsec.

T-49-19-08

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f(FILE #)

For d = 0, f → W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f → f (if d is omitted, assembler assigns d = 1).

INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
000	000	000	000	(0000)	No Operation	NOP	-	-	None
000	000	1ff	fff	(0040)	Move W to f (Note 1)	MOVWF	-	W→f	None
000	001	000	000	(0100)	Clear W	CLRW	-	0→W	Z
000	001	1ff	fff	(0140)	Clear f	CLRF	f	0→f	Z
000	010	dff	fff	(0200)	Subtract W from f	SUBWF	f,d	f-W→d [f + $\overline{W}$ + 1→d]	C,DC,Z
000	011	dff	fff	(0300)	Decrement f	DECF	f,d	f-1→d	Z
000	100	dff	fff	(0400)	Inclusive OR W and f	IORWF	f,d	Wvf→d	Z
000	101	dff	fff	(0500)	ANDbW and f	ANDWF	f,d	W•f→d	Z
000	110	dff	fff	(0600)	Exclusive OR W and f	XORWF	f,d	W ⊕ f→d	Z
000	111	dff	fff	(0700)	Add W and f	ADDWF	f,d	W + F→d	C,DC,Z
001	000	dff	fff	(1000)	Move f	MOVF	f,d	f→d	Z
001	001	dff	fff	(1100)	Complement f	COMF	f,d	f→d	Z
001	011	dff	fff	(1200)	Increment f	INCF	f,d	f + 1→d	Z
001	011	dff	fff	(1300)	Decrement f, Skip to Zero	DECFSZ	f,d	f - 1→d, skip if Zero	None
001	100	dff	fff	(1400)	Rotate Right f	RRF	f,d	f(n)→d(n-1), C→d(7), f(0)→C	C
001	101	dff	fff	(1500)	Rotate Left f	RLF	f,d	f(n)→d(n + 1), C→d(0), f(7)→C	C
001	110	dff	fff	(1600)	Swap halves f	SWAPF	f,d	f(0-3) ↔ f(4-7)→d	None
001	111	dff	fff	(1700)	Increment f, Skip if Zero	INCFSZ	f,d	f + 1→d, skip if Zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f(FILE #)

INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
010	0bb	bff	fff	(2000)	Bit Clear f	BCF	f,b	0→f(b)	None
010	1bb	bff	fff	(2400)	Bit Set f	BSF	f,b	1→f(b)	None
011	0bb	bff	fff	(3000)	Bit Test f, skip if Clear	BTFSC	f,b	Bit Test f(b): skip if clear	None
011	1bb	bff	fff	(3400)	Bit Test f, skip if Set	BTFSS	f,b	Bit Test f(b): skip if set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

INSTRUCTION-BINARY (Octal)					NAME	MNEMONIC, OPERANDS		OPERATION	STATUS AFFECTED
100	0kk	kkk	kkk	(4000)	Return and place Literal in W	RETLW	k	k→w, Stack→PC	None
100	1kk	kkk	kkk	(4400)	Call subroutine (Note 1)	CALL	k	PC + 1→Stack, k→PC	None
101	kkk	kkk	kkk	(5000)	Go to address (k is 9 bits)	GOTO	k	k→PC	None
110	0kk	kkk	kkk	(6000)	Move Literal to W	MOVLW	k	k→W	None
110	ikk	kkk	kkk	(6400)	Inclusive OR Literal and W	IORLW	k	k v W→W	Z
111	okk	kkk	kkk	(7000)	AND Literal and W	ANDLW	k	k • W→W	Z
111	1kk	kkk	kkk	(7400)	Exclusive OR Literal and W	XORLW	k	k ⊕ W→W	Z

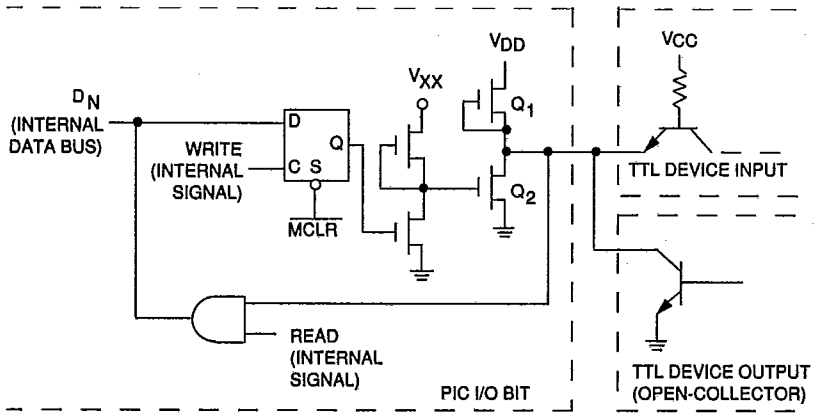
NOTES:
1. The 9th bit of the program counter in the PIC is zero or a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377s. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state. See example 2 on page 7.

4

I/O INTERFACING

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q2, allowing the TTL open collector device to drive the pad, pulled up by Q1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Note: Q1 can be disconnected via mask option to form an "open drain" pin.

Bidirectional I/O Ports

The bidirectional ports may be used for both inut and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output latch must be set in the high state. Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an inut (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655 consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeros. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5. Also, file register instructions which leave the results in W can be used.

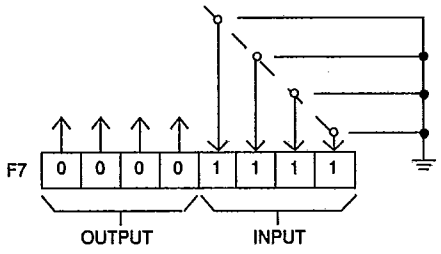
Output Only Port: (Port RB)

The output only port of the PIC1655 consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if tpd (See I.O Timing Diagram) is greater than 1/4tcy (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:

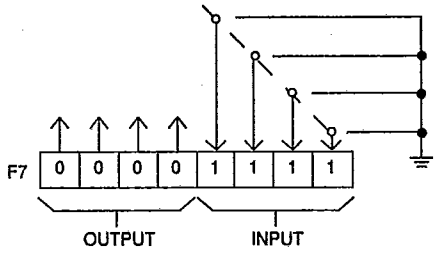


What is thought to be happening:
BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:
BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

4

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature under bias..... 125°C
Storage Temperature ..... - 55°C to +150°C
Voltage on any pin with respect to Vss ..... -0.3V to + 10.0V
Power Dissipation (Note 1) 1000mW

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS/PIC1655 Operating temperature T_A = 0°C to + 70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{CC}	4.5	-	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	65	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
		3.5	-	V_{DD}	V	I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current (MCLR, RTCC)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (open drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.4	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHi}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

DC CHARACTERISTICS/PIC1655I Operating temperature T_A = -40°C to + 85°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	70	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
						I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.8	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.8	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

4

DC CHARACTERISTICS/PIC1655H Operating temperature T_A = -40°C to + 110°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	-	5.5	V	
Output Buffer Supply Voltage	V_{XX}	4.5	-	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	-	30	70	mA	All I/O pins @ V_{DD} (Note 6)
Output Buffer Supply Current	I_{XX}	-	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	-0.2	-	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	-	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD} - 1	-	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	-	V_{DD}	V	I_{OH} = -100µA (Note 4)
						I_{OH} = 0
Output Low Voltage	V_{OL1}	-	-	0.45	V	I_{OL} = -1.6mA, V_{XX} = 4.5V
(I/O only)		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		-	-	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		-	-	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		-	-	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	-	-	0.45	V	I_{OL} = -1.6mA, (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	- 5	-	+ 5	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Leakage Current (open drain I/O pins)	I_{OLC}	-	-	10	µA	$V_{SS} \le V_{PIN} \le 10V$
Input Low Current (all I/O ports)	I_{IL}	- 0.2	-0.6	-1.8	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	- 0.1	-0.4	-1.8	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(I_{IOHI}) + \Sigma(V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. See Primary Supply current Chart for additional information.

AC CHARACTERISTICS/PIC1655, PIC1655I AND PIC1655H

Operating temperature T_A = 0°C to + 70°C
-40°C to +85°C and -40°C to + 110°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	-	20	µs	0.2 MHz - 1.0MHz external time base (Notes 1, 2 and 5)
RTCC Input						
Period	t_{RT}	t_{CY} = 0.2µs-	-	-		
High Pulse Width	t_{RTH}	1/2 t_{RT}	-	-	-	
Low Pulse Width	t_{RTL}	1/2 t_{RT}	-	-	-	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	ts	-	-	1/4t_{CY} - 125	ns	
Data Input Hold Time	tH	0	-	-	ns	
Data Output Propagation Delay	t_{PD}	-	600	1000	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	V_{OSC} = 5V Applies to external
External Input Impedance Low	R_{OSCL}	-	10^6	-	Ω	V_{OSC} = 0.4V OSC drive only

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:
1. Instruction cycle period (t_{CY}) equals four times the inut oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the RTCC input.
3. The maximum frequency which may be input to the RTCC pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example: if t_{CY} = 4µs, $f_{(max)} = \frac{1}{4.2\mu s}$ = 238KHz.

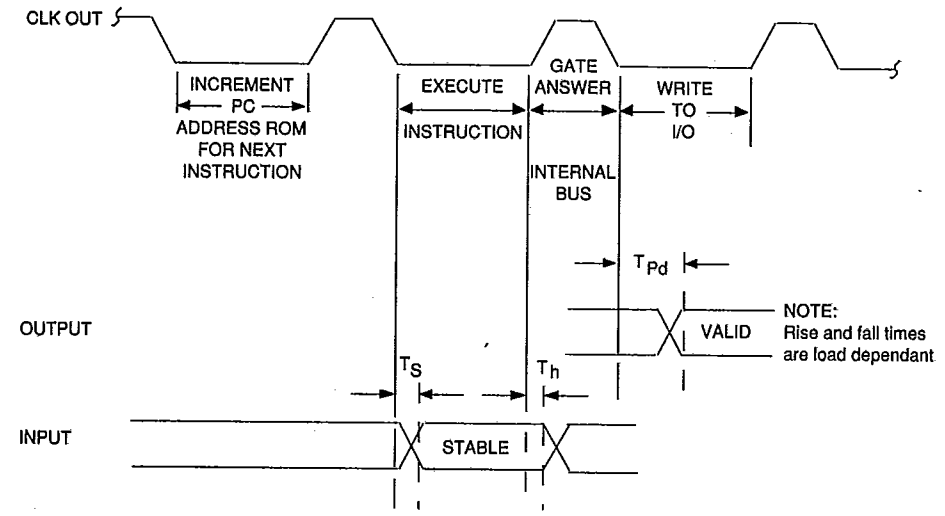
4. Caution must be exercised to allow for unit to unit variation of oscillator frequency when using RC option. (See RC Option Operation Graph).

PRIMARY SUPPLY CURRENT AT SELECTED TEMPERATURES: PIC1655, PIC1655I, PIC1655H

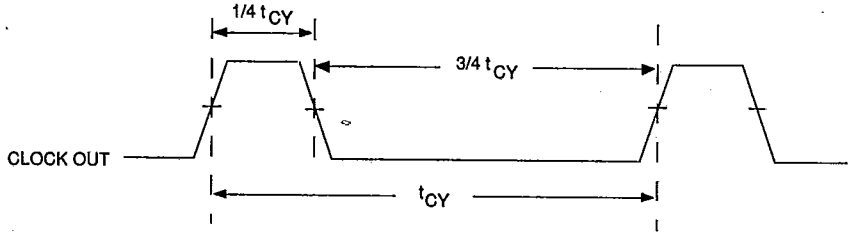
Characteristic	Sym	Max	Units	Conditions
Primary Supply Current	I_{DD}	70	mA	-40°C, All I/O pins at V_{DD}
		65	mA	0°C, All I/O pins at V_{DD}
		48	mA	70°C, All I/O pins at V_{DD}
		45	mA	85°C, All I/O pins at V_{DD}
		42	mA	110°C, All I/O pins at V_{DD}

4

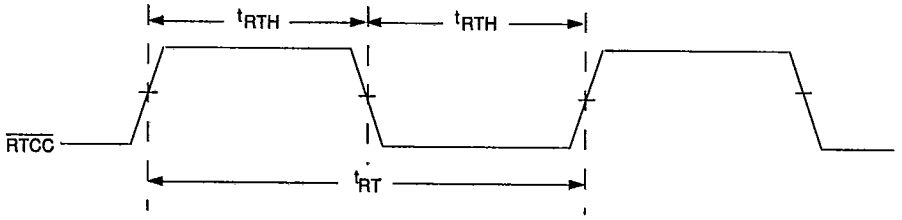
I/O TIMING



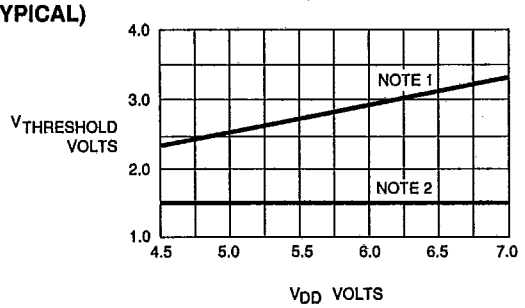
CLOCK OUT TIMING



RTCC TIMING

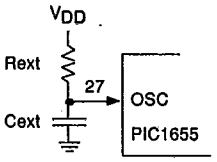


SCHMITT TRIGGER CHARACTERISTICS (RTCC, MCLR AND OSC PINS)
TA =25°C (TYPICAL)

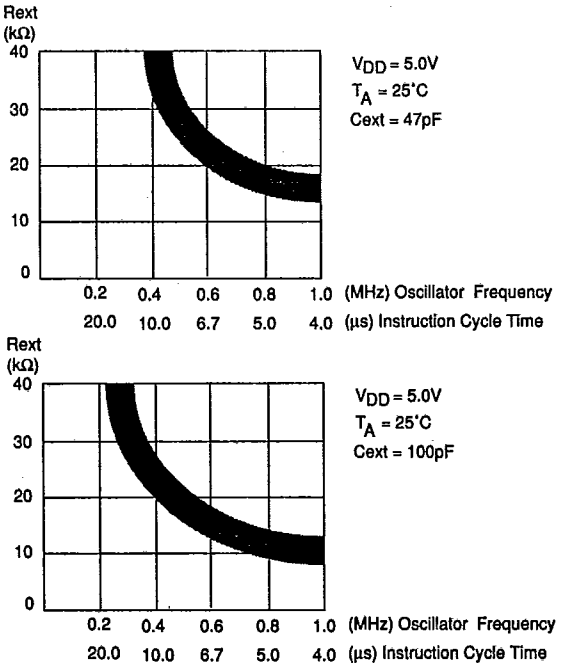


NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

RC OPTION OPERATION



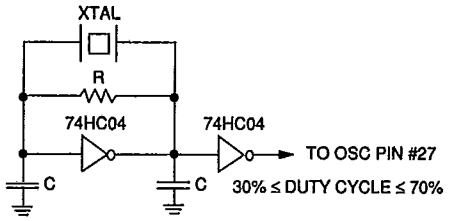
TYPICAL RC OSCILLATOR FREQUENCY RANGE



Unit to Unit Variation @ 5.0V, 25°C is ±25%
Variation from V_{DD} = 4.5V - 7.0V referenced to 5.0V is -3%, +9%
Variation from T_A = 0°C - 70°C referenced to 25°C is +3%, -5%

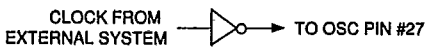
4

BUFFERED CRYSTAL INPUT OPERATION

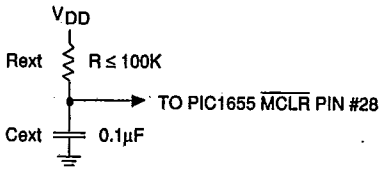


The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION

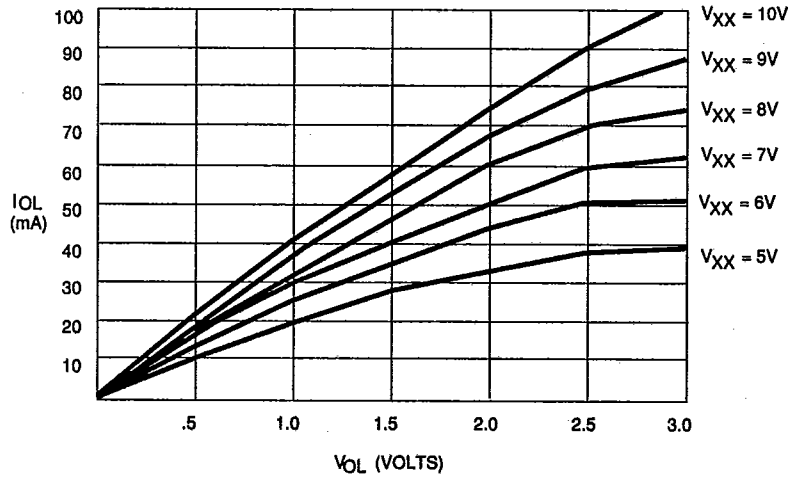


MASTER CLEAR (TYPICAL CIRCUIT)



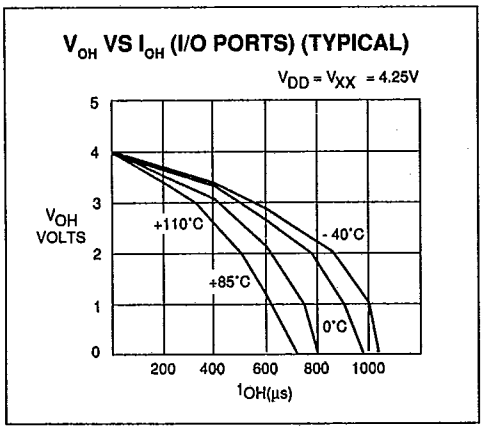
Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

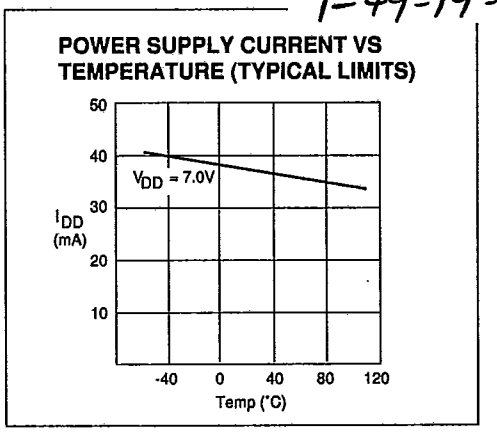
OUTPUT SINK CURRENT GRAPH



The Output Sink Current is dependent on the VXX supply and the output load. This chart shows the typical curves used to express the output drive capability.

T-49-19-08





PIC1655 EMULATION CAUTIONS

When emulating a PIC1655 using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1655 mode. (Refer to the PICES Manual). The PIC1655 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application the MCLR input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1655.

4

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the sales offices. For the *currently available code-combinations*, refer to previous page.

PART NUMBERS