# 3810 Group

## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The 3810 group is 8-bit microcomputer based on the 740 family core technology.

The 3810 group is designed mainly for VCR control, and include four 8-bit timers, a PWM function, and a 4-bit comparator circuit.

The various microcomputers in the 3810 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3810 group, refer to the section on group expansion.

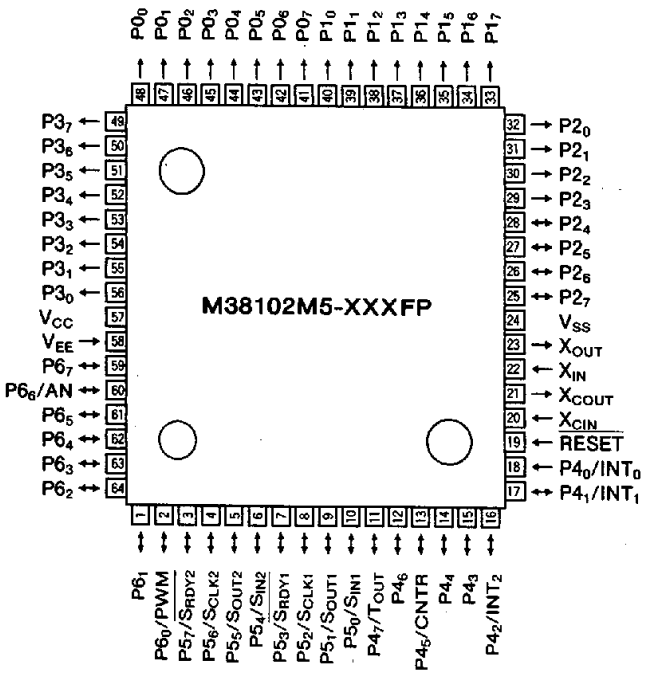
## FEATURES

- Basic machine-language instructions ..... 71
- The minimum instruction execution time ..... 0.95$\mu$s
  (at 4.19MHz oscillation frequency)
- Memory size
  ROM ..... 4K to 32K bytes
  RAM ..... 192 to 1024 bytes
- Programmable input/output ports ..... 27
- High-breakdown-voltage output ports ..... 28
- Interrupts ..... 11 sources, 11 vectors
- Timers ..... 8-bit×4
- Serial I/O ..... 8-bit×2 (Clock-synchronized)
- PWM output circuit ..... 14-bit×1
- Comparator circuit ..... 4-bit×1
- 2 Clock generating circuit
  Clock ($X_{IN}$-$X_{OUT}$) ..... Internal feedback resistor
  Sub-clock ($X_{CIN}$-$X_{COUT}$) ..... Without internal feedback resistor
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5V
  In low-speed mode ..... 2.8 to 5.5V
- Power dissipation
  In high-speed mode ..... 25mW
  (at 4.19MHz oscillation frequency)
  In low-speed mode ..... 300$\mu$W
  (at 32kHz oscillation frequency)
- Operating temperature range ..... −10 to +85°C

## APPLICATIONS

VCRs, tuners, musical instruments, office automation, etc.

## PIN CONFIGURATION (TOP VIEW)

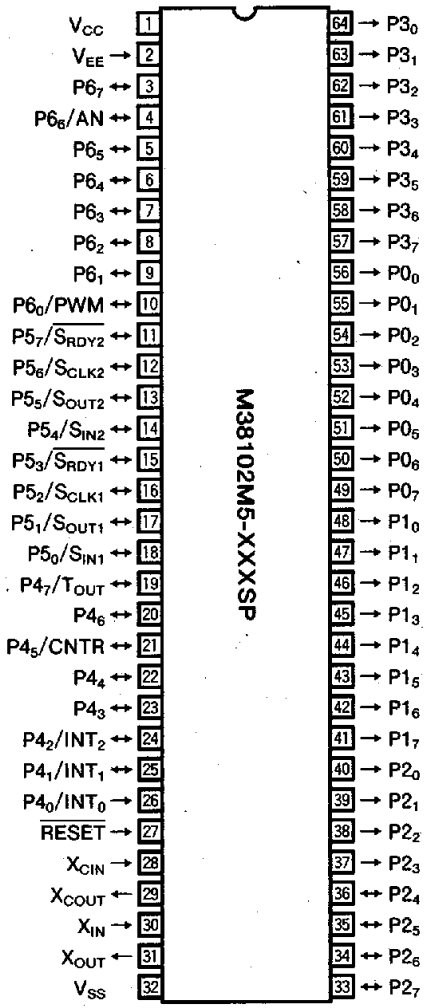



Package type : 64P6N-A

64-pin plastic-molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

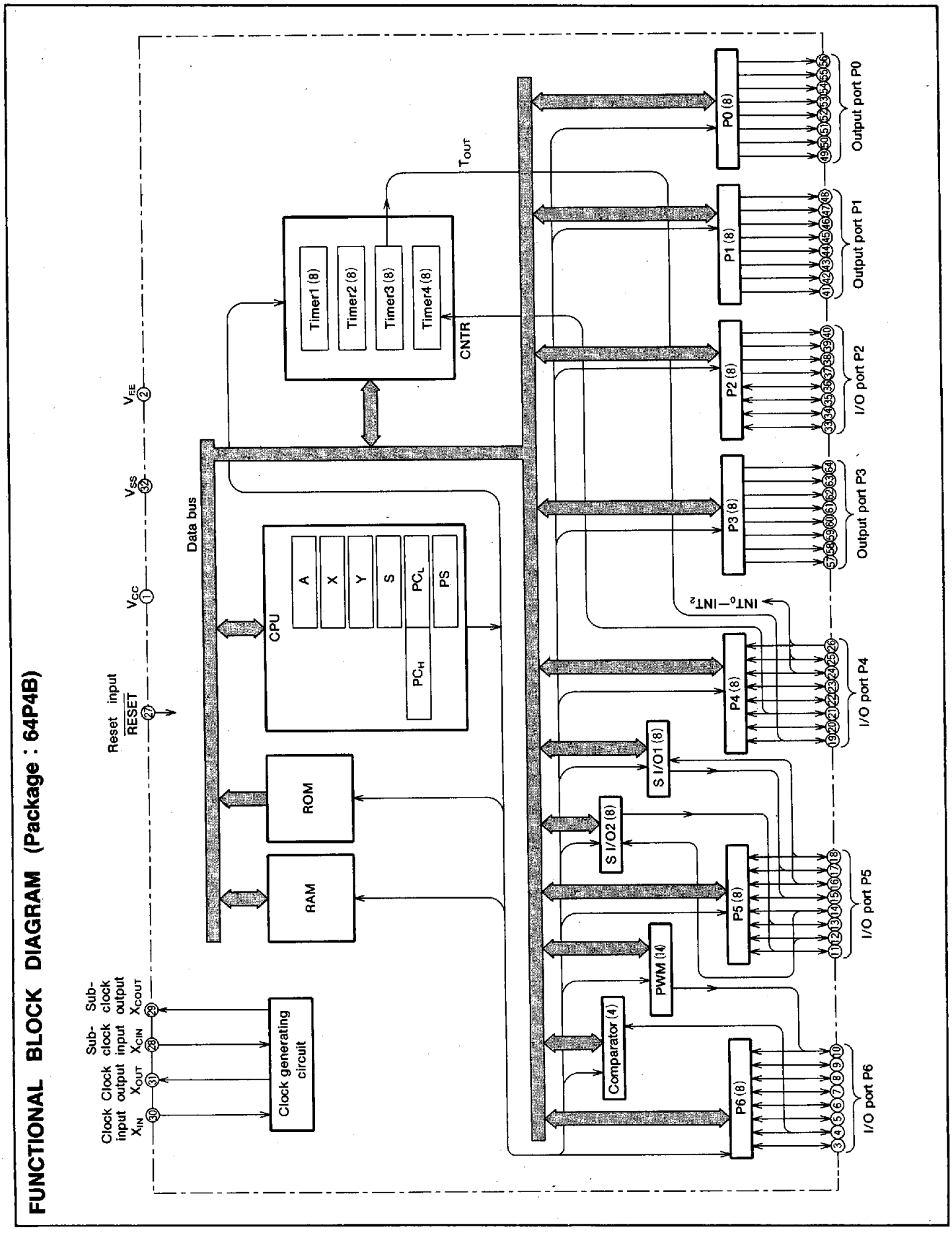
## PIN CONFIGURATION (TOP VIEW)




Package type : 64P4B

64-pin shrink plastic-molded DIP

## FUNCTIONAL BLOCK DIAGRAM (Package : 64P4B)



## PIN DESCRIPTION

| Pin | Name | Function | Function except a port function |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Power source | • Apply voltage of 4.0 to 5.5V to $V_{CC}$, and 0V to $V_{SS}$. | |
| $V_{EE}$ | Pull-down power input | • Applies voltage supplied to pull-down resistors of ports P0, P1, $P2_0$-$P2_3$, and P3. | |
| $\overline{RESET}$ | Reset input | • Reset input pin for active "L" | |
| $X_{IN}$ | Clock input | • Input and output signals for the clock generating circuit.<br>• It consist of internal feedback resistor.<br>• Connect a ceramic resonator or quartz-crystal oscillator between the $X_{IN}$ and $X_{OUT}$ pins to set the oscillation frequency.<br>• If an external clock is used, connect the clock source to the $X_{IN}$ pin and leave the $X_{OUT}$ pin open.<br>• This clock is used as the oscillating source of system clock | |
| $X_{OUT}$ | Clock output | | |
| $X_{CIN}$ | Sub clock input | • Input and output signals for the internal sub-clock generating circuit.<br>• It consist of without internal feedback resistor.<br>• Connect a ceramic resonator or quartz-crystal oscillator and external feedback resistor between the $X_{CIN}$ and $X_{COUT}$ pins.<br>• If an external clock is used, connect the clock source to the $X_{CIN}$ pin and leave the $X_{COUT}$ pin open.<br>• This clock can also be used as the oscillating source of system clock. | |
| $X_{COUT}$ | Sub clock output | | |
| $P0_0$-$P0_7$ | Output port P0 | • 8-bit output port.<br>• The output structure is high-breakdown-voltage P-channel open-drain with internal pull-down resistors connected between the output and the $V_{EE}$ pin.<br>• At reset this port is set to $V_{EE}$ pin level. | |
| $P1_0$-$P1_7$ | Output port P1 | | |
| $P2_0$-$P2_3$ | Output port P2 | • 4-bit output port with the same function as port P0. | |
| $P2_4$-$P2_7$ | I/O port P2 | • 4-bit I/O port.<br>• I/O direction register allows each pin to be individually programmed as either input or output.<br>• At reset this port is set to input mode.<br>• TTL input level<br>• CMOS 3-state output | |
| $P3_0$-$P3_7$ | Output port P3 | • 8-bit output port with the same function as port P0. | |
| $P4_0/INT_0$ | Input port $P4_0$ | • 1-bit CMOS input pin. | • External interrupt input pins |
| $P4_1/INT_1$, $P4_2/INT_2$ | I/O port P4 | • 7-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$<br>• CMOS compatible input level. | |
| $P4_3$, $P4_4$ | | | |
| $P4_5$/CNTR | | | • Timer 4 input pin |
| $P4_6$ | | | |
| $P4_7/T_{OUT}$ | | | • Timer 3 output pin |
| $P5_0/S_{IN1}$, $P5_1/S_{OUT1}$, $P5_2/S_{CLK1}$, $P5_3/\overline{S_{RDY1}}$ | I/O port P5 | • 8-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$.<br>• CMOS compatible input level<br>• N-channel open-drain output<br>• Keep the input voltage of this port between 0V and $V_{CC}$. | • Serial I/O1 I/O pins |
| $P5_4/S_{IN2}$, $P5_5/S_{OUT2}$, $P5_6/S_{CLK2}$, $P5_7/\overline{S_{RDY2}}$ | | | • Serial I/O2 I/O pins |

## PIN DESCRIPTION

| Pin | Name | Function | Function except a port function |
|---|---|---|---|
| $P6_0$/PWM | I/O port P6 | • 8-bit CMOS I/O port with the same function as port $P2_4$-$P2_7$.<br>• CMOS compatible input level. | • 14-bit PWM output pin |
| $P6_1$-$P6_5$ | | | |
| $P6_6$/AN | | | • Comparator input pin |
| $P6_7$ | | | |

## PART NUMBERING

Product M3810 2 M 5 - XXX SP

Package type
SP : 64P4B package
FP : 64P6N-A package
SS : 64S1B-E package
FS : 64D0 package

ROM number
Omitted in some types.

ROM/PROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes

The first 128 bytes and the last two bytes of ROM are reserved areas; they can not be used.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes

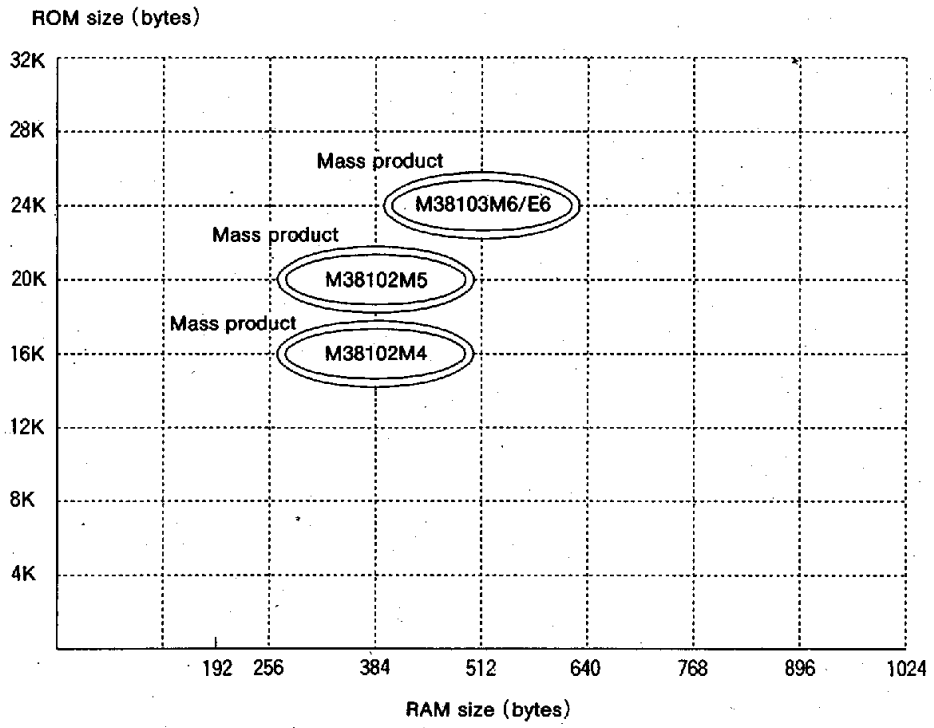
## GROUP EXPANSION

Mitsubishi plans to expand the M3810x group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions
ROM/PROM capacity ..... 12K to 24K bytes
RAM capacity ..... 384 to 512 bytes

(2) Packages
64P4B ..... Shrink plastic molded DIP
64P6N-A ..... Plastic molded QFP
64S1B-E ..... Shrink ceramic DIP
64D0 ..... Ceramic LCC

### Memory expansion plan




The development schedule and other details of products under development may be revised without notice.
Currently supported products are listed below.

As of May 1996

| Product name | (P) ROM size (bytes) | RAM size (bytes) | Package | Remarks |
|---|---|---|---|---|
| M38102M4-XXXSP | 16K | 384 | 64P4B | Mask ROM version |
| M38102M4-XXXFP | | | 64P6N-A | Mask ROM version |
| M38102M5-XXXSP | 20K | | 64P4B | Mask ROM version |
| M38102M5-XXXFP | | | 64P6N-A | Mask ROM version |
| M38103M6-XXXSP | 24K | 512 | 64P4B | Mask ROM version |
| M38103E6-XXXSP | | | | One Time PROM version |
| M38103E6SP | | | | One Time PROM version (blank) |
| M38103M6-XXXFP | | | 64P6N-A | Mask ROM version |
| M38103E6-XXXFP | | | | One Time PROM version |
| M38103E6FP | | | | One Time PROM version (blank) |
| M38103E6SS | | | 64S1B-E | EPROM version |
| M38103E6FS | | | 64D0 | EPROM version |

## FUNCTIONAL DESCRIPTION

### Central Processing Unit (CPU)

The 3810 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 〈Software〉 User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

### CPU Mode Register

The CPU mode register is allocated at address $003B_{16}$.

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

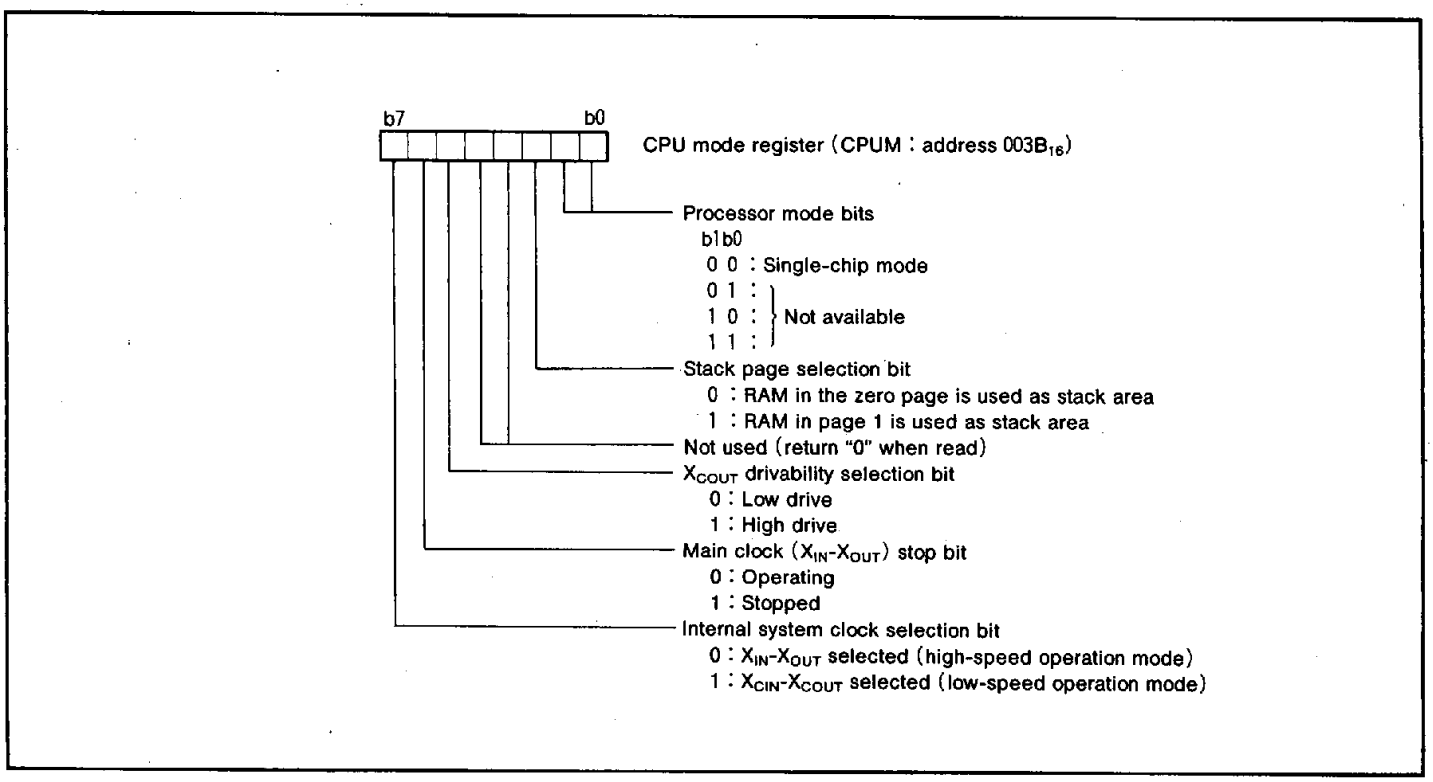



**Fig. 1 Structure of CPU mode register**

## MEMORY

### Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

### RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

### ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

### Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

### Zero Page

The 256 bytes from addresses $0000_{16}$ to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

### Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

| RAM capacity (bytes) | Address $XXXX_{16}$ |
|---|---|
| 192 | $00FF_{16}$ |
| 256 | $013F_{16}$ |
| 384 | $01BF_{16}$ |
| 512 | $023F_{16}$ |
| 640 | $02BF_{16}$ |
| 768 | $033F_{16}$ |
| 896 | $03BF_{16}$ |
| 1024 | $043F_{16}$ |

ROM area

| ROM capacity (bytes) | Address $YYYY_{16}$ | Address $ZZZZ_{16}$ |
|---|---|---|
| 4096 | $F000_{16}$ | $F080_{16}$ |
| 8192 | $E000_{16}$ | $E080_{16}$ |
| 12288 | $D000_{16}$ | $D080_{16}$ |
| 16384 | $C000_{16}$ | $C080_{16}$ |
| 20480 | $B000_{16}$ | $B080_{16}$ |
| 24576 | $A000_{16}$ | $A080_{16}$ |
| 28672 | $9000_{16}$ | $9080_{16}$ |
| 32768 | $8000_{16}$ | $8080_{16}$ |

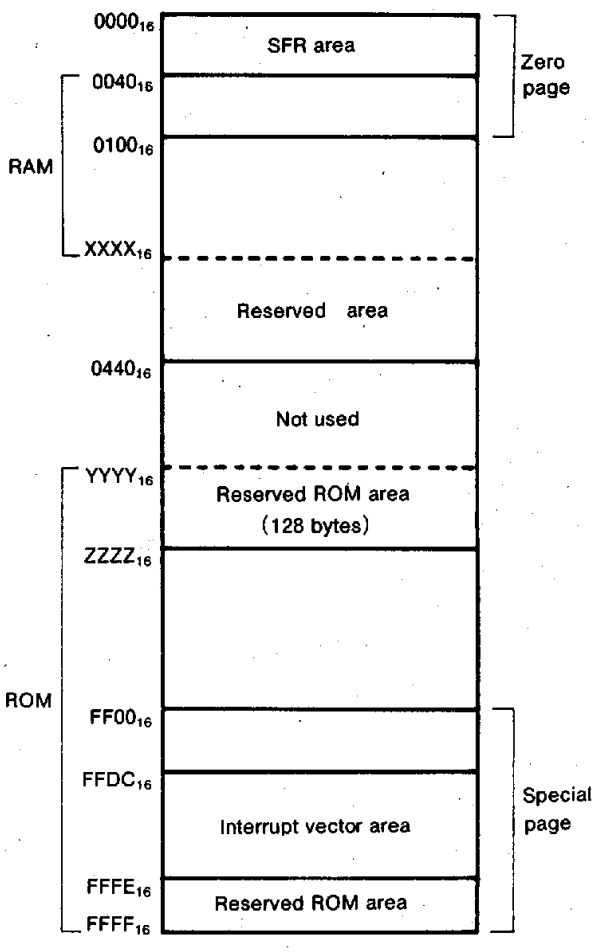



Fig. 2 Memory map diagram

| | |
|---|---|
| $0000_{16}$ | Port P0 (P0) |
| $0001_{16}$ | |
| $0002_{16}$ | Port P1 (P1) |
| $0003_{16}$ | |
| $0004_{16}$ | Port P2 (P2) |
| $0005_{16}$ | Port P2 direction register (P2D) |
| $0006_{16}$ | Port P3 (P3) |
| $0007_{16}$ | |
| $0008_{16}$ | Port P4 (P4) |
| $0009_{16}$ | Port P4 direction register (P4D) |
| $000A_{16}$ | Port P5 (P5) |
| $000B_{16}$ | Port P5 direction register (P5D) |
| $000C_{16}$ | Port P6 (P6) |
| $000D_{16}$ | Port P6 direction register (P6D) |
| $000E_{16}$ | |
| $000F_{16}$ | |
| $0010_{16}$ | |
| $0011_{16}$ | |
| $0012_{16}$ | |
| $0013_{16}$ | |
| $0014_{16}$ | |
| $0015_{16}$ | |
| $0016_{16}$ | |
| $0017_{16}$ | |
| $0018_{16}$ | |
| $0019_{16}$ | Serial I/O1 control register (SIO1CON) |
| $001A_{16}$ | |
| $001B_{16}$ | Serial I/O1 register (SIO1) |
| $001C_{16}$ | |
| $001D_{16}$ | Serial I/O2 control register (SIO2CON) |
| $001E_{16}$ | |
| $001F_{16}$ | Serial I/O2 register (SIO2) |

| | |
|---|---|
| $0020_{16}$ | |
| $0021_{16}$ | |
| $0022_{16}$ | |
| $0023_{16}$ | |
| $0024_{16}$ | Timer 1 (T1) |
| $0025_{16}$ | Timer 2 (T2) |
| $0026_{16}$ | Timer 3 (T3) |
| $0027_{16}$ | Timer 4 (T4) |
| $0028_{16}$ | Timer 12 mode register (T12M) |
| $0029_{16}$ | Timer 34 mode register (T34M) |
| $002A_{16}$ | |
| $002B_{16}$ | PWM control register (PWMCON) |
| $002C_{16}$ | PWM register (upper)(PWMH) |
| $002D_{16}$ | PWM register (lower)(PWML) |
| $002E_{16}$ | |
| $002F_{16}$ | |
| $0030_{16}$ | Comparator register (CMP) |
| $0031_{16}$ | |
| $0032_{16}$ | |
| $0033_{16}$ | |
| $0034_{16}$ | |
| $0035_{16}$ | |
| $0036_{16}$ | |
| $0037_{16}$ | |
| $0038_{16}$ | High-breakdown-voltage port control register (HVPC) |
| $0039_{16}$ | |
| $003A_{16}$ | Interrupt edge selection register (INTEDGE) |
| $003B_{16}$ | CPU mode register (CPUM) |
| $003C_{16}$ | Interrupt request register 1 (IREQ1) |
| $003D_{16}$ | Interrupt request register 2 (IREQ2) |
| $003E_{16}$ | Interrupt control register 1 (ICON1) |
| $003F_{16}$ | Interrupt control register 2 (ICON2) |

Fig. 3 Memory map of special function register (SFR)

## I/O PORTS

### Direction Registers

The 3810 group has 27 programmable I/O pins arranged in four I/O ports (ports $P2_4$—$P2_7$, $P4_1$—$P4_7$, P5, and P6). The I/O ports have direction registers which determine the input/ output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

### High-Breakdown-Voltage Output Ports

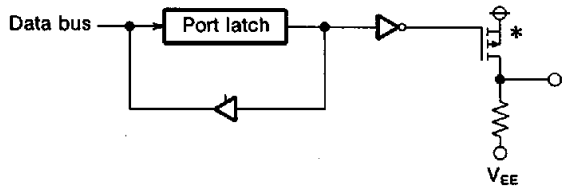
The 3810 group has four ports with high-breakdown-voltge pins (ports P0, P1, $P2_0$ — $P2_3$, and P3). The high-breakdown-voltage ports have P-channel open-drain output with a breakdown voltage of $V_{CC}$—40V. Each pin has an internal pull-down resistor connected to $V_{EE}$. At reset, the P-channel output transistor of each port latch is turned off, so becomes $V_{EE}$ level ("L") by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register (address $0038_{16}$) slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

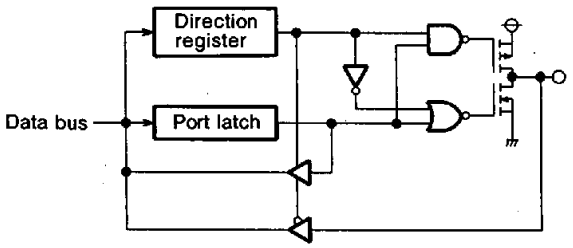
| Pin | Name | Input/Output | I/O Format | Non-Port Function | Related SFRs | Diagram No. |
|---|---|---|---|---|---|---|
| $P0_0$-$P0_7$ | Port P0 | Output | High-breakdown-voltage P-channel open-drain output with pull-down resistor | | High-breakdown-voltage port control register | (1) |
| $P1_0$-$P1_7$ | Port P1 | Output | High-breakdown-voltage P-channel open-drain output with pull-down resistor | | High-breakdown-voltage port control register | |
| $P2_0$-$P2_3$ | Port P2 | Output | High-breakdown-voltage P-channel open-drain output with pull-down resistor | | High-breakdown-voltage port control register | |
| $P2_4$-$P2_7$ | | Input/output, individual bits | TTL level input<br>CMOS 3-state output | | | (2) |
| $P3_0$-$P3_7$ | Port P3 | Output | High-breakdown-voltage P-channel open-drain output with pull-down resistor | | High-breakdown-voltage port control register | (1) |
| $P4_0/INT_0$ | Port P4 | Input | CMOS compatible input level | External interrupt input | Interrupt edge selection register | (3) |
| $P4_1/INT_1$,<br>$P4_2/INT_2$ | | Input/output, individual bits | CMOS compatible input level<br>CMOS 3-state output | | | (4) |
| $P4_3$, $P4_4$ | | | | | | (2) |
| $P4_5$/CNTR | | | | Timer 4 input | Timer 34 mode register | (4) |
| $P4_6$ | | | | | | (2) |
| $P4_7/T_{OUT}$ | | | | Timer 3 output | Timer 34 mode register | (5) |
| $P5_0/S_{IN1}$,<br>$P5_1/S_{OUT1}$,<br>$P5_2/S_{CLK1}$,<br>$P5_3/\overline{S_{RDY1}}$ | Port P5 | Input/output, individual bits | CMOS compatible input level<br>N-channel open-drain output | Serial I/O1 function I/O | Serial I/O1 control register | (6)<br>(7)<br>(8) |
| $P5_4/S_{IN2}$,<br>$P5_5/S_{OUT2}$,<br>$P5_6/S_{CLK2}$,<br>$P5_7/\overline{S_{RDY2}}$ | | | | Serial I/O2 function I/O | Serial I/O2 control register | (6)<br>(7)<br>(8) |
| $P6_0$/PWM | Port P6 | Input/output, individual bits | CMOS compatible input level<br>CMOS 3-state output | 14-bit PWM output | PWM control register<br>PWML register<br>PWMH register | (9) |
| $P6_1$-$P6_5$ | | | | | | (2) |
| $P6_6$/AN | | | | Comparator input | Comparator register | (10) |
| $P6_7$ | | | | | | (2) |

Note 1. For details of how to use double-function ports as function I/O ports, refer to the applicable sections.
2. Make sure that the input level at each pin is either 0V or $V_{CC}$ during execution of the STP instruction. If an input level is at an intermediate potential, a current will flow through the input-stage gate.

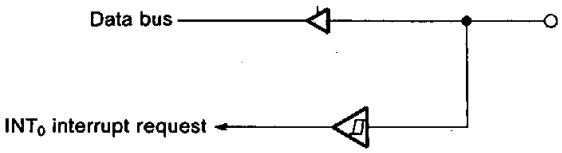
(1) Ports P0, P1, $P2_0$—$P2_3$, P3



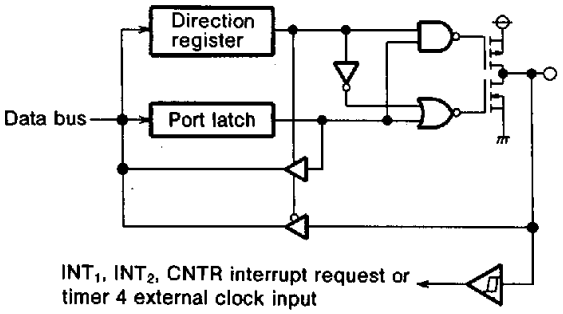

(2) Ports $P2_4$—$P2_7$, $P4_3$, $P4_4$, $P4_6$, $P6_1$—$P6_5$, $P6_7$



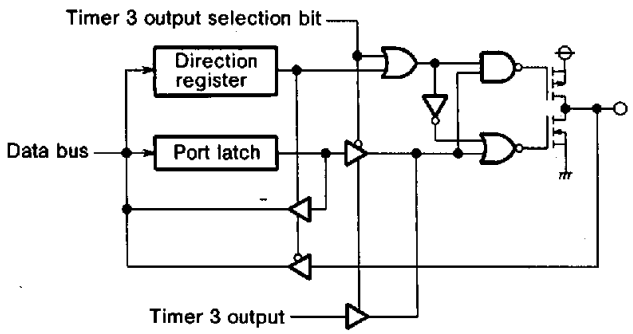

(3) Port $P4_0$



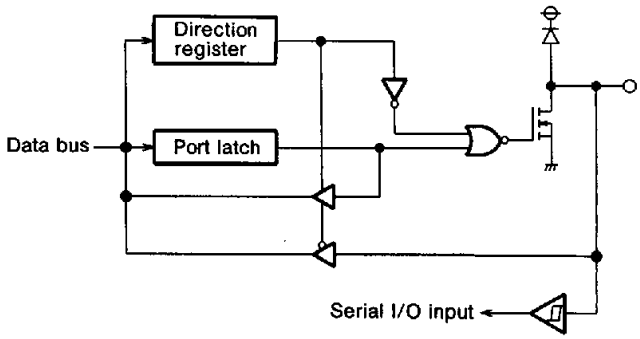

(4) Ports $P4_1$, $P4_2$, $P4_5$




(5) Port $P4_7$




(6) Ports $P5_0$, $P5_4$




*: High-breakdown-voltage P-channel transistor

**Fig. 4 Port block diagram (1)**

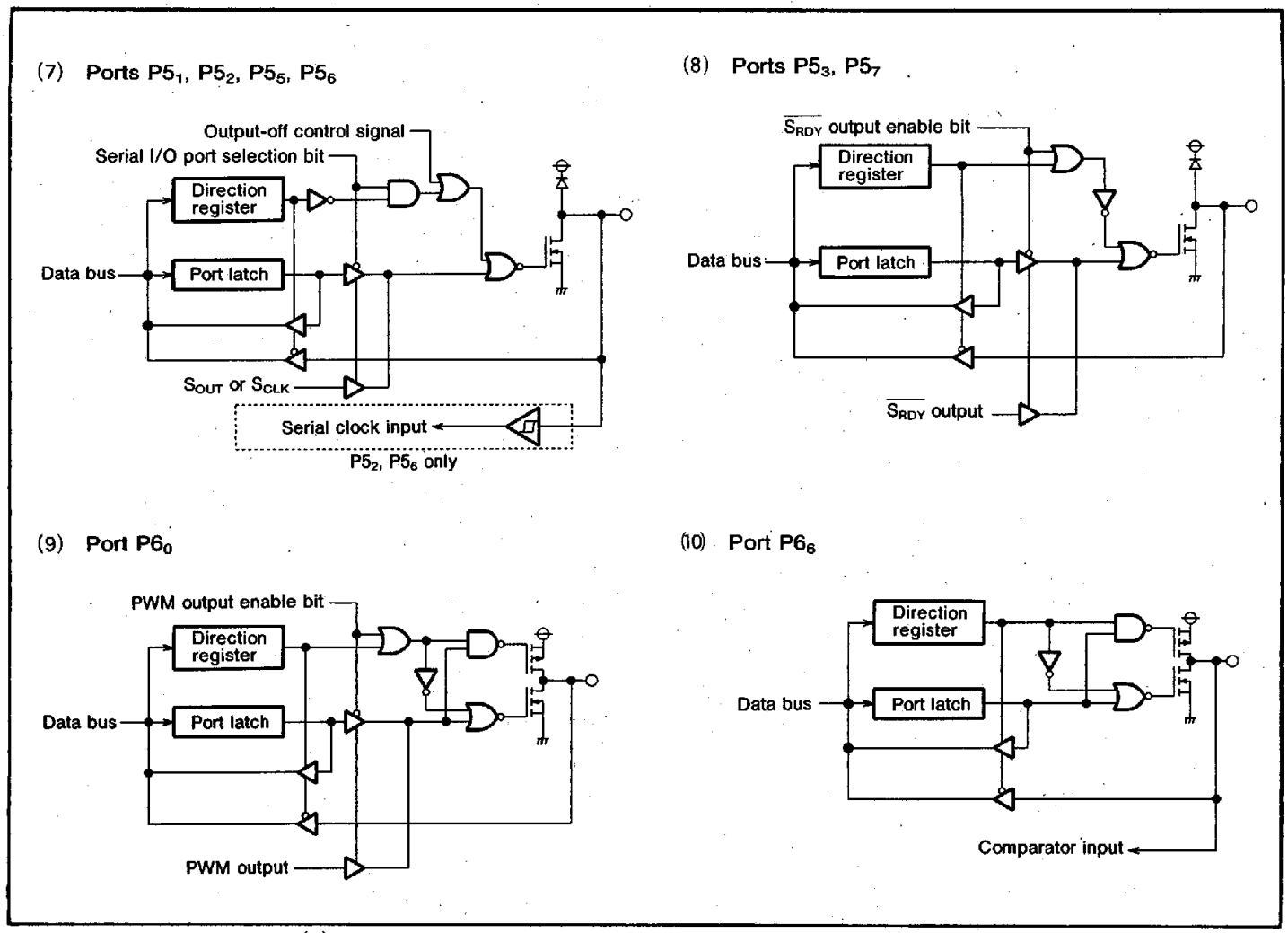



**Fig. 5 Port block diagram (2)**

## INTERRUPTS

Interrupts occur by eleven sources: four external, six internal, and one software.

### Interrupt Control

Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit.

The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

### Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

### Notes on Use

When the active edge of an external interrupt ($INT_0$-$INT_2$, CNTR) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

(1) Disable the external interrupt which is selected.
(2) Change the active edge selection.
(3) Clear the interrupt request bit which is selected to "0".
(4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

| Interrupt source | Priority | Vector addresses (Note 1) | | Interrupt request generating conditions | Remarks |
|---|---|---|---|---|---|
| | | High | Low | | |
| Reset (Note 2) | 1 | $FFFD_{16}$ | $FFFC_{16}$ | At reset | Non-maskable |
| $INT_0$ | 2 | $FFFB_{16}$ | $FFFA_{16}$ | At detection of either rising or falling edge of $INT_0$ input | External interrupt (active edge selectable) |
| $INT_1$ | 3 | $FFF9_{16}$ | $FFF8_{16}$ | At detection of either rising or falling edge of $INT_1$ input | External interrupt (active edge selectable) |
| $INT_2$ | 4 | $FFF7_{16}$ | $FFF6_{16}$ | At detection of either rising or falling edge of $INT_2$ input | External interrupt (active edge selectable) |
| Serial I/O1 | 5 | $FFF5_{16}$ | $FFF4_{16}$ | At completion of serial I/O1 data transfer | Valid when serial I/O1 is selected |
| Serial I/O2 | 6 | $FFF3_{16}$ | $FFF2_{16}$ | At completion of serial I/O2 data transfer | Valid when serial I/O2 is selected |
| Timer 1 | 7 | $FFF1_{16}$ | $FFF0_{16}$ | At timer 1 underflow | |
| Timer 2 | 8 | $FFEF_{16}$ | $FFEE_{16}$ | At timer 2 underflow | STP release timer underflow |
| Timer 3 | 9 | $FFED_{16}$ | $FFEC_{16}$ | At timer 3 underflow | |
| Timer 4 | 10 | $FFEB_{16}$ | $FFEA_{16}$ | At timer 4 underflow | |
| CNTR | 11 | $FFE9_{16}$ | $FFE8_{16}$ | At detection of either rising or falling edge of CNTR input | External interrupt (active edge selectable) |
| BRK instruction | 12 | $FFDD_{16}$ | $FFDC_{16}$ | At BRK instruction execution | Non-maskable software interrupt |

Note 1. Vector addresses contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

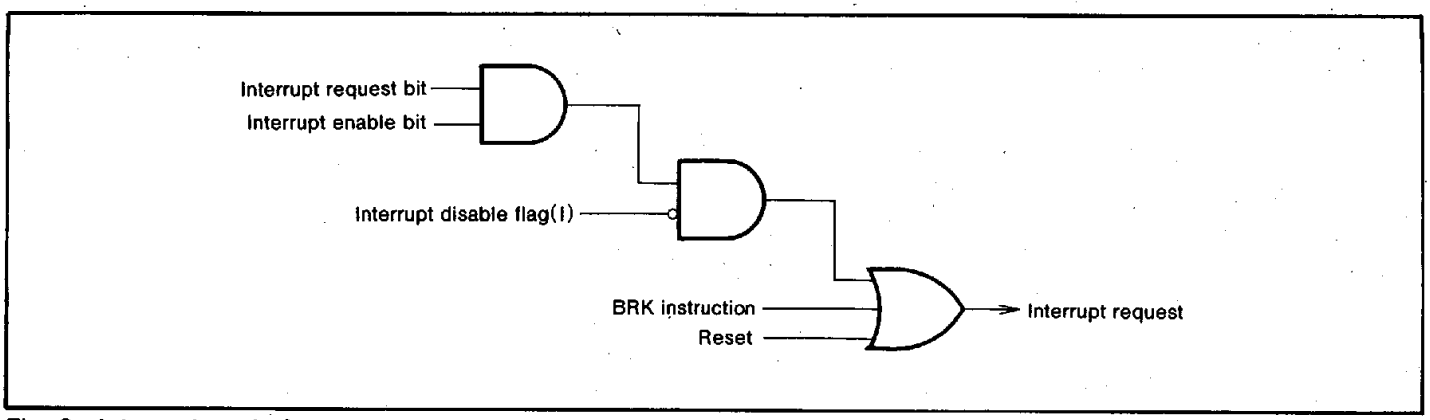



**Fig. 6 Interrupt control**

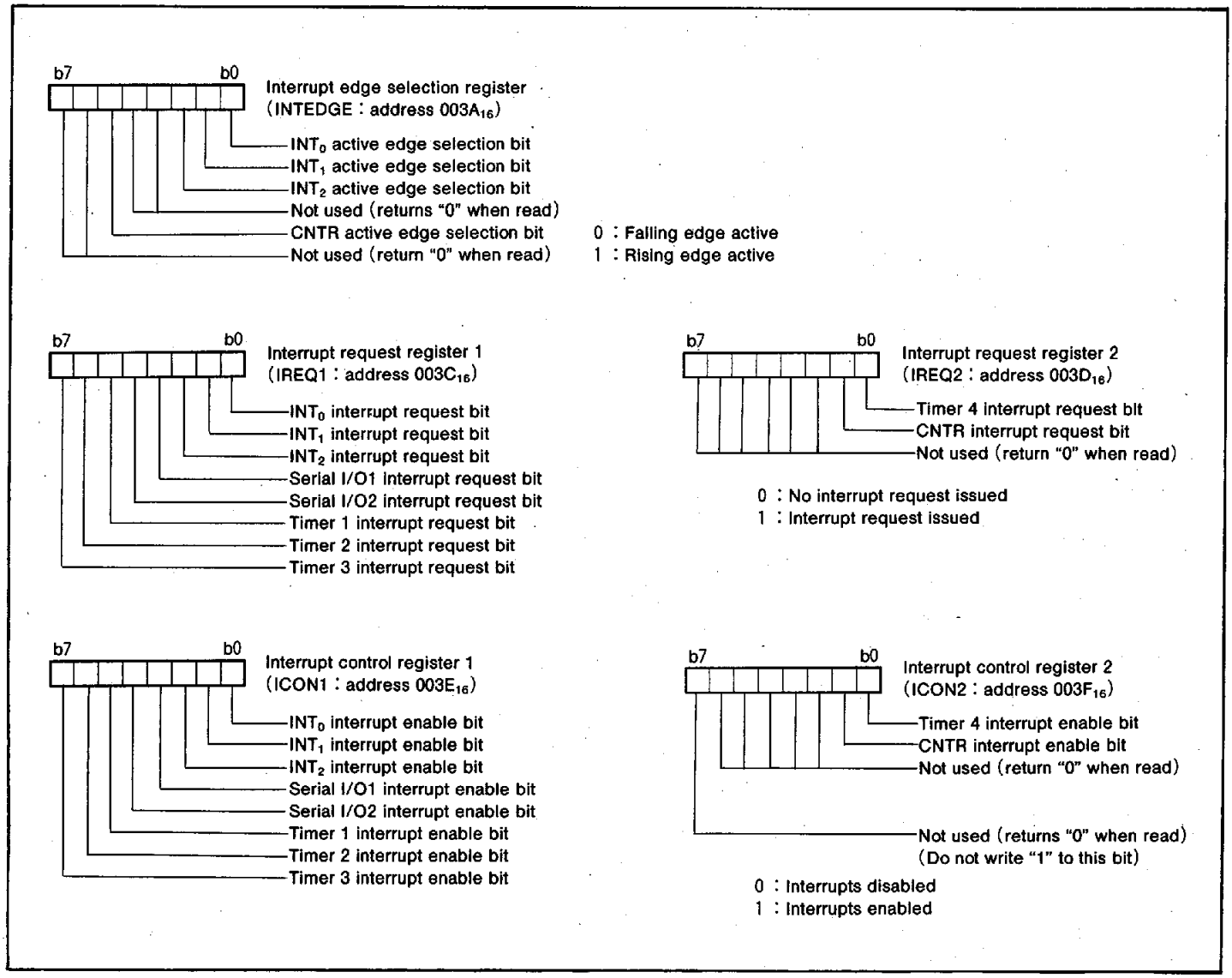



**Fig. 7 Structure of interrupt-related registers**

## TIMERS

The 3810 group has four built-in timers : time 1, timer 2, timer 3, and timer 4. All timers are count down. When the timer reaches "$00_{16}$", at the next count pulse the contents of the corresponding timer latch is loaded into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1" .

Note that the system clock $\phi$ can be set to either high-speed mode or low-speed mode by the CPU mode register.

### Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to "$FF_{16}$", and timer 2 is set to "$01_{16}$".

### Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

Timer 3 can also output a rectangular waveform from the $P4_7/T_{OUT}$ pin. The waveform changes polarity each time timer 3 underflows.

The external clock CNTR counts rising edge.

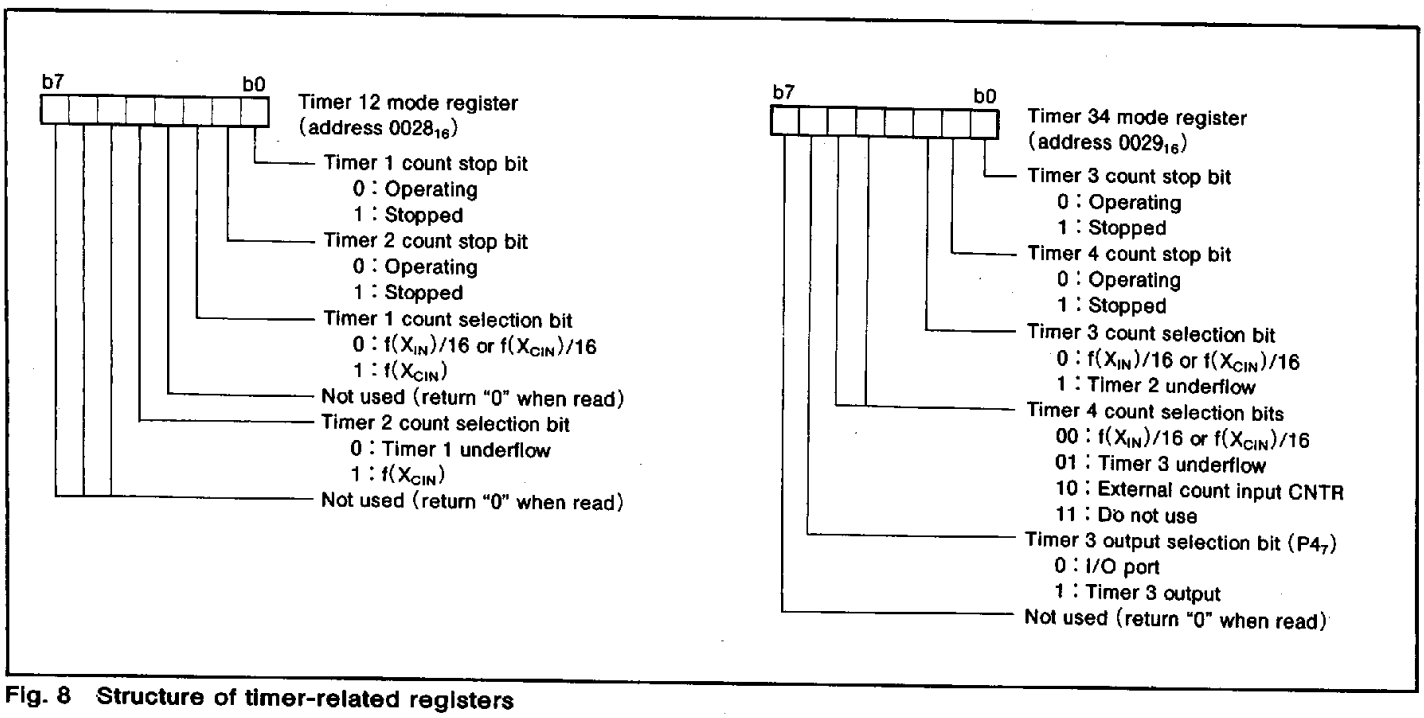



Fig. 8 Structure of timer-related registers

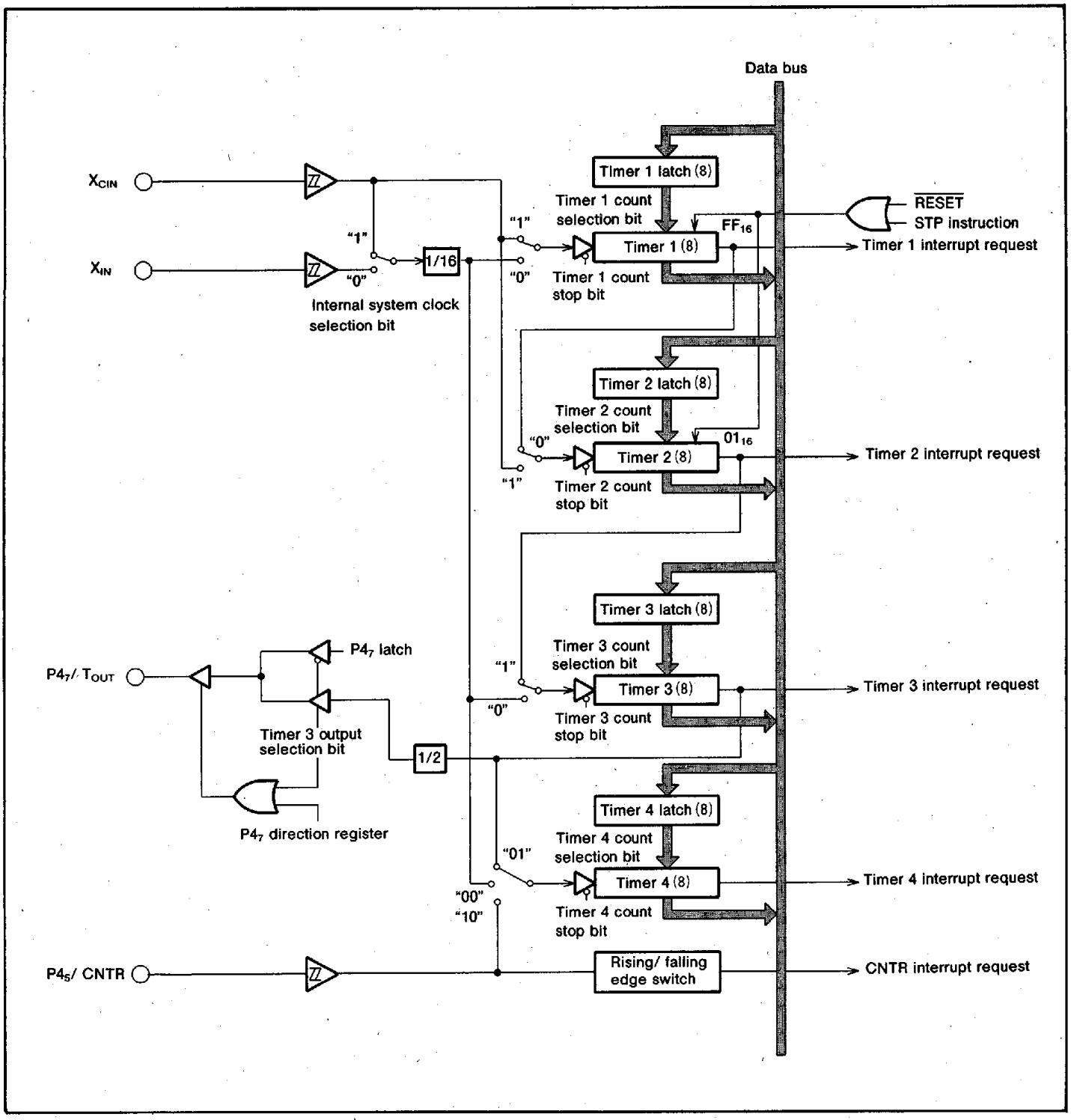



Fig. 9 Timer block diagram

## SERIAL I/O

The 3810 group has two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).
Serial I/O1 has the same function as serial I/O2.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (adresses $0019_{16}$ and $001D_{16}$).

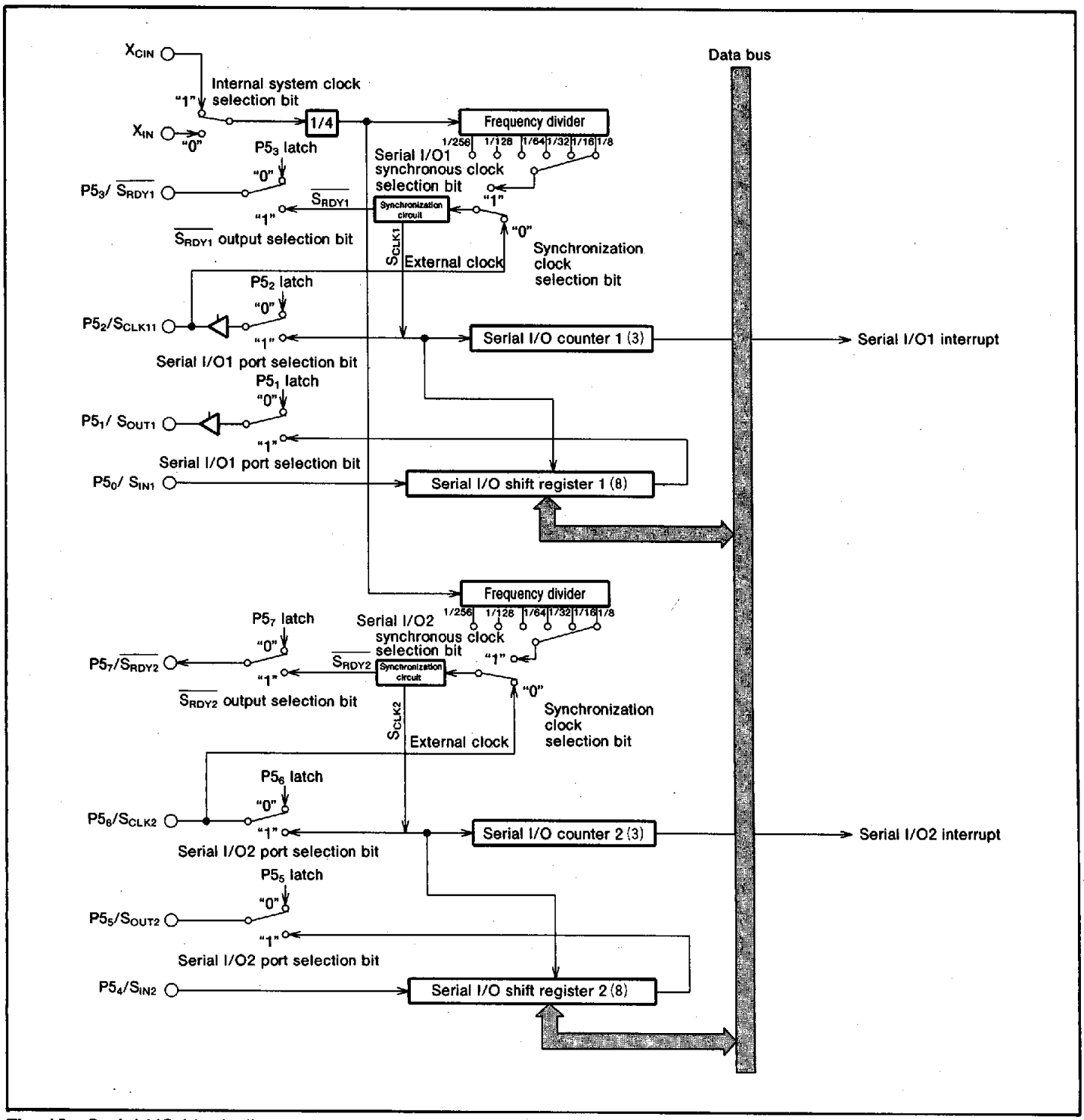
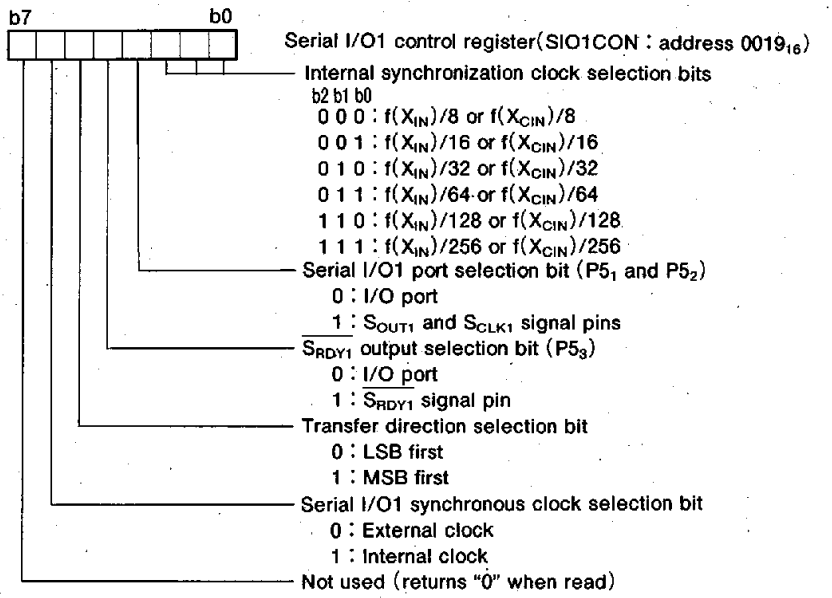



Fig. 10 Serial I/O block diagram

## [Serial I/O Control Registers] SIO1CON, SIO2CON

Each of the serial I/O control registers (addresses $0019_{16}$ and $001D_{16}$) contains seven bits that select various control parameters of the serial I/O function.



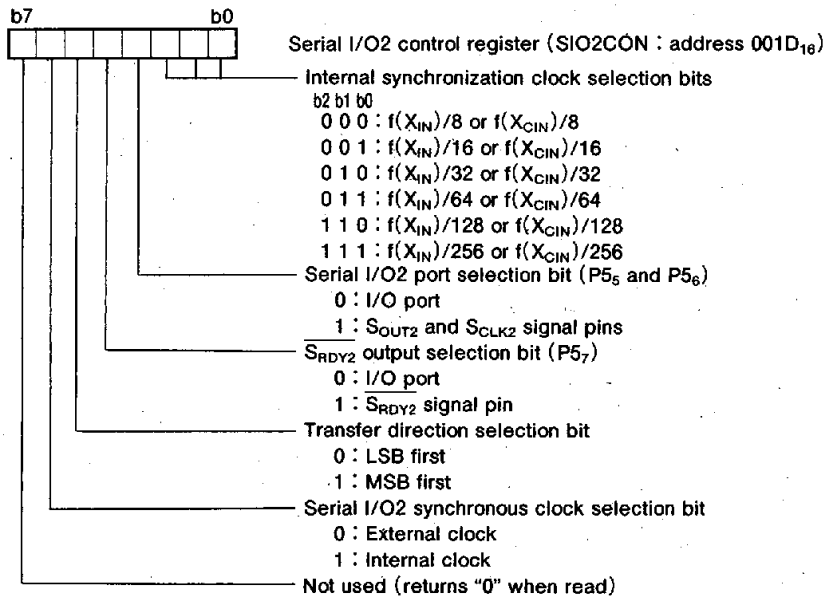



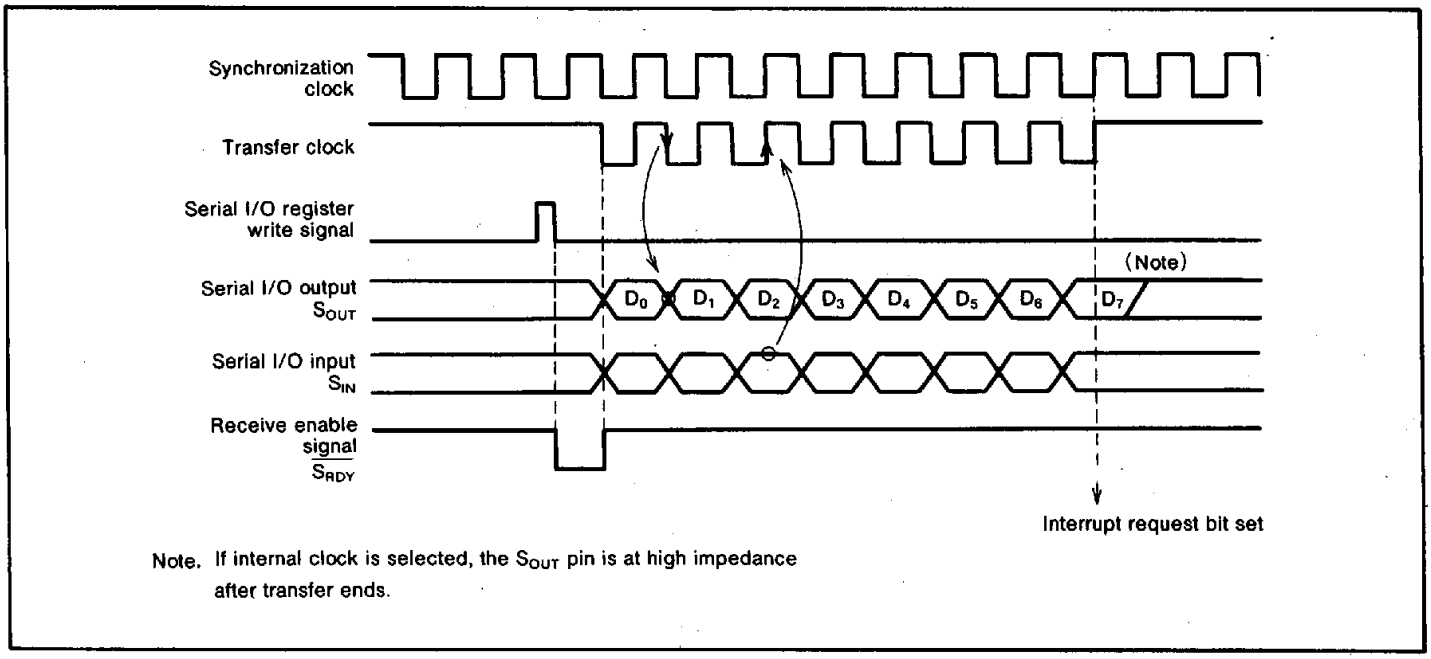

Fig. 11 Structure of serial I/O control registers

## Operation In Serial I/O Mode

Either an internal clock or an external clock can be selected as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address $001B_{16}$ or $001F_{16}$). After eight bits have been transferred, the $S_{OUT}$ pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the $S_{OUT}$ pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.




Note. If internal clock is selected, the $S_{OUT}$ pin is at high impedance after transfer ends.

**Fig. 12 Serial I/O timing (for LSB first)**

## PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT

The 3810 group has a PWM function with a 14-bit resolution. When the oscillation frequency $X_{IN}$ is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192$\mu$s. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the $X_{IN}$ clock.

The explanation in the rest of this data sheet assumes $f(X_{IN}) = 4MHz$.

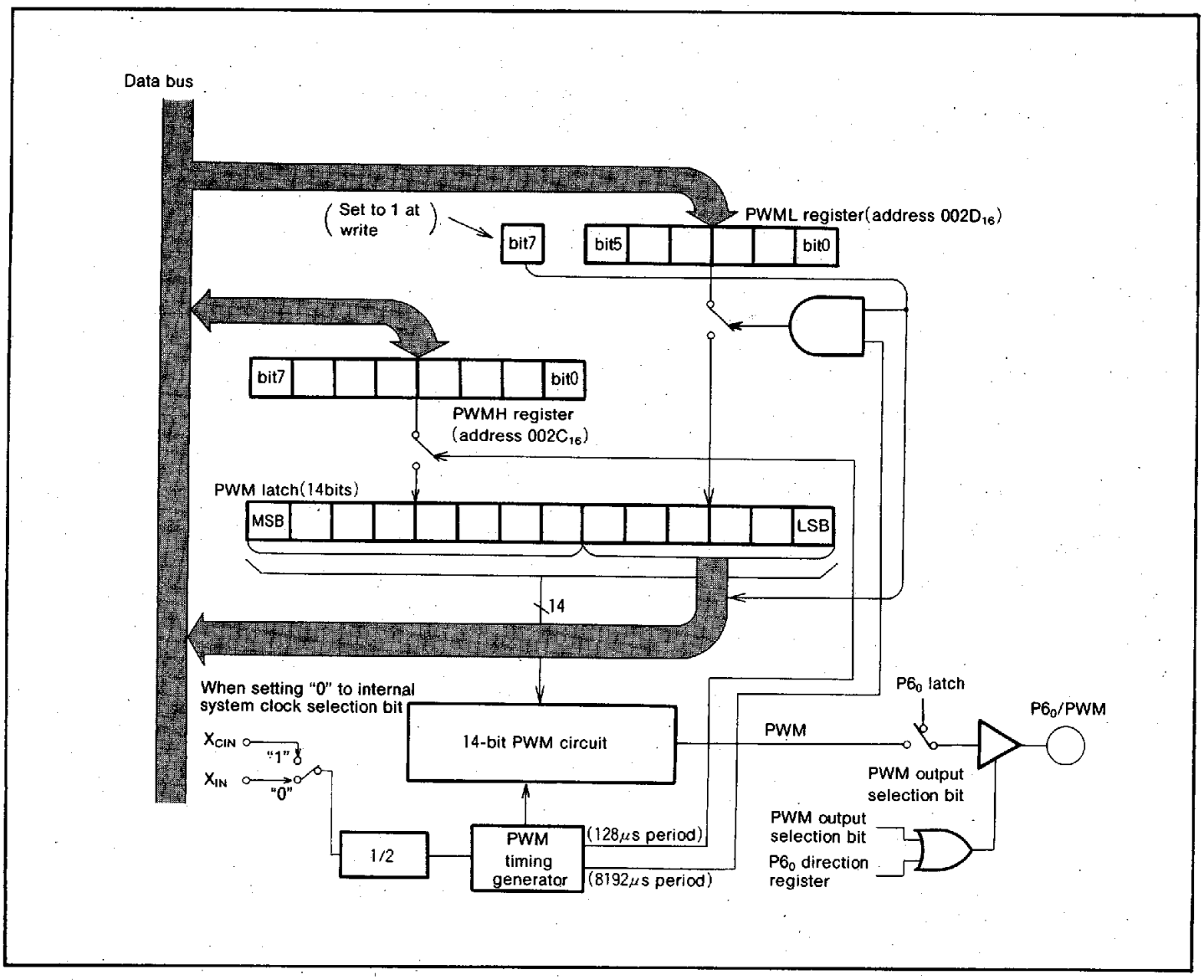



Fig. 13 PWM block diagram

(1) Data Set-up

The PWM output pin also functions as port $P6_0$. Set port $P6_0$ to be the PWM output pin by setting bit 0 of the PWM mode register (address $002B_{16}$). The high-order eight bits of output data are set in the high-order PWM register PWMH (address $002C_{16}$) and the low-order six bits are set in the low-order PWM register PWML (address $002D_{16}$).

(2) Transfer From Register to Latch

Date written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192$\mu$s), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128$\mu$s). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

**Table 2. Relationship between lower 6 bits of data and period set by the ADD bit**

| Lower 6 Bits of Data(PWML) (LSB) | Sub-periods tm Lengthened (m =0 to 63) |
|---|---|
| 0 0 0 0 0 0 | None |
| 0 0 0 0 0 1 | m=32 |
| 0 0 0 0 1 0 | m=16, 48 |
| 0 0 0 1 0 0 | m= 8 , 24, 40, 56 |
| 0 0 1 0 0 0 | m= 4 , 12, 20, 28, 36, 44, 52, 60 |
| 0 1 0 0 0 0 | m= 2 , 6 , 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62 |
| 1 0 0 0 0 0 | m= 1 , 3 , 5 , 7 , ····· , 57, 59, 61, 63 |

(3) PWM Operation

The timing of the 14-bit PWM function is shown in Fig. 16. The 14-bit PWM data is divided into the low-order six bits and the high-order eight bits in the PWM latch.

The high-order eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is 256$\times\tau$ (128$\mu$s) long. The signal is "H" for a length equal to N times $\tau$, where $\tau$ is the minimum resolution (500ns).

The contents of the low-order six bits of data enable the lengthening of the high signal by $\tau$ (500ns). As shown in Fig. 13, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 16, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the high-order eight bits of the 14-bit data are $03_{16}$ and the low-order six bits are $05_{16}$, the length of the "H"-level output in sub-periods $t_8$, $t_{24}$, $t_{32}$, $t_{40}$, and $t_{56}$ is 4$\tau$, and its length 3$\tau$ in all other sub-periods.

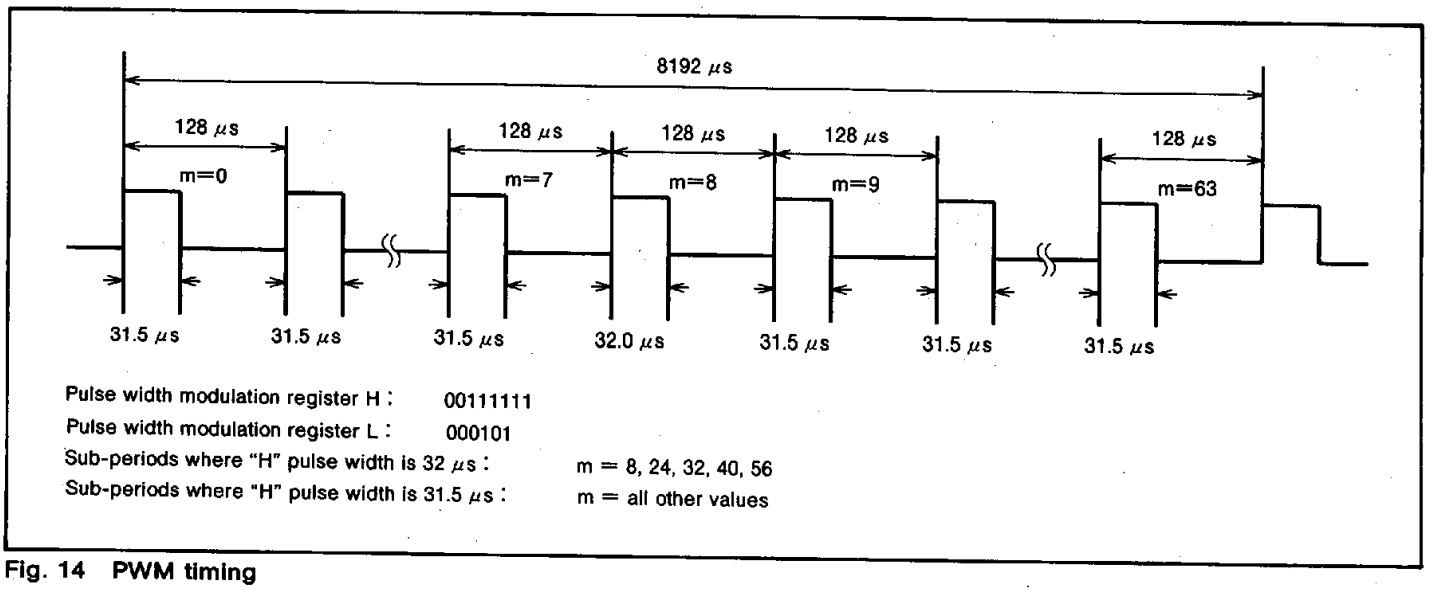



Fig. 14 PWM timing

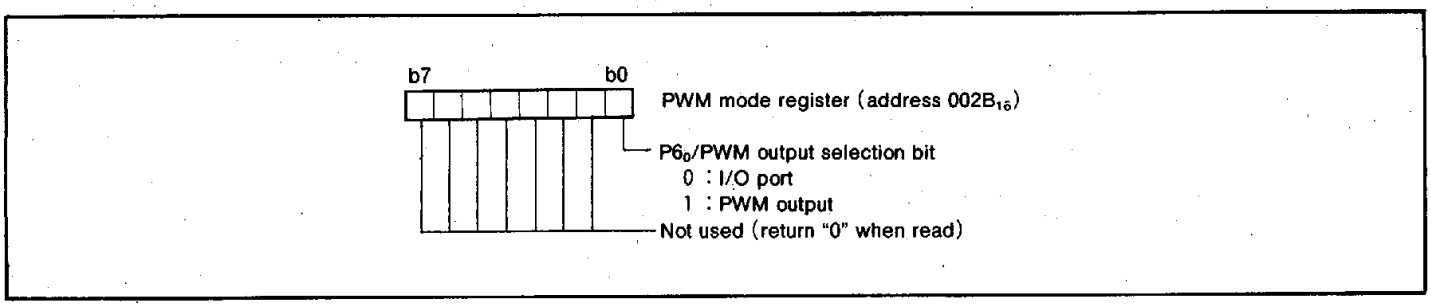



Fig. 15 Structure of PWM mode register

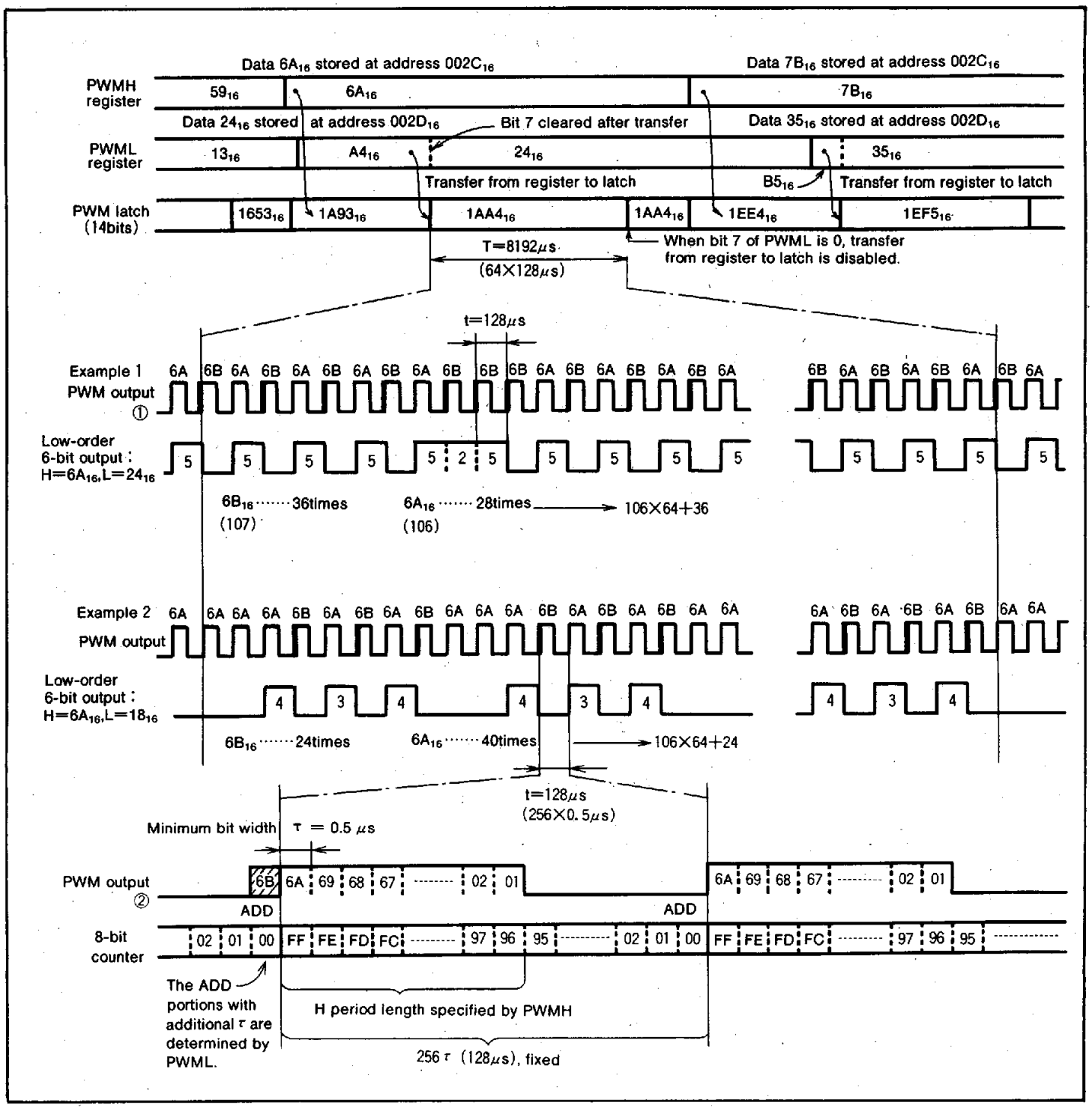



Fig. 16 14-bit PWM timing

## COMPARATOR CIRCUIT

### Comparator Configuration

The comparator circuit consists of a switch tree, ladder resistors, a comparator, a comparator control circuit, a comparator register (address $0030_{16}$), and an analog signal input pin ($P6_6$/AN). The analog signal input pin ($P6_6$/AN) also functions as an ordinary digital port.

### Comparator Register (CMP)

The comparator register is a 5-bit register of which bits 0 to 3 can be used to generate internal reference voltages in steps of 1/16 $V_{CC}$. The result of the comparison between the analog input voltage and an internal reference voltage is stored in bit 4 of the comparator register.

### Comparator Operation

To activate the comparator, first set port $P6_6$ to input mode by setting the corresponding direction register (address $000D_{16}$) to "0"—this ensures that port $P6_6$/AN is used as an analog voltage input pin. Then write a digital value corresponding to the internal comparison voltage into bits 0 to 3 of the comparator register (address $0030_{16}$). This write operation immediately activates the comparison. After 14 cycles of the system clock $\phi$ (the time required for the comparison), the comparison result is stored in bit 4 of the comparator.

If the analog input voltage is greater than the internal reference voltage, bit 4 is "1"; if it is less than the internal reference voltage, bit 4 is "0". To perform another comparison, the comparator must be written to again, even if the same internal reference voltage is to be used.

**Table 3. Correspondence between bits 0 to 3 of the comparator register and internal reference voltage**

| Comparator register | | | | Internal reference voltage |
|---|---|---|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0 | $1/32V_{CC}$ |
| 0 | 0 | 0 | 1 | $1/16V_{CC}+1/32V_{CC}$ |
| 0 | 0 | 1 | 0 | $2/16V_{CC}+1/32V_{CC}$ |
| 0 | 0 | 1 | 1 | $3/16V_{CC}+1/32V_{CC}$ |
| 0 | 1 | 0 | 0 | $4/16V_{CC}+1/32V_{CC}$ |
| 0 | 1 | 0 | 1 | $5/16V_{CC}+1/32V_{CC}$ |
| 0 | 1 | 1 | 0 | $6/16V_{CC}+1/32V_{CC}$ |
| 0 | 1 | 1 | 1 | $7/16V_{CC}+1/32V_{CC}$ |
| 1 | 0 | 0 | 0 | $8/16V_{CC}+1/32V_{CC}$ |
| 1 | 0 | 0 | 1 | $9/16V_{CC}+1/32V_{CC}$ |
| 1 | 0 | 1 | 0 | $10/16V_{CC}+1/32V_{CC}$ |
| 1 | 0 | 1 | 1 | $11/16V_{CC}+1/32V_{CC}$ |
| 1 | 1 | 0 | 0 | $12/16V_{CC}+1/32V_{CC}$ |
| 1 | 1 | 0 | 1 | $13/16V_{CC}+1/32V_{CC}$ |
| 1 | 1 | 1 | 0 | $14/16V_{CC}+1/32V_{CC}$ |
| 1 | 1 | 1 | 1 | $15/16V_{CC}+1/32V_{CC}$ |

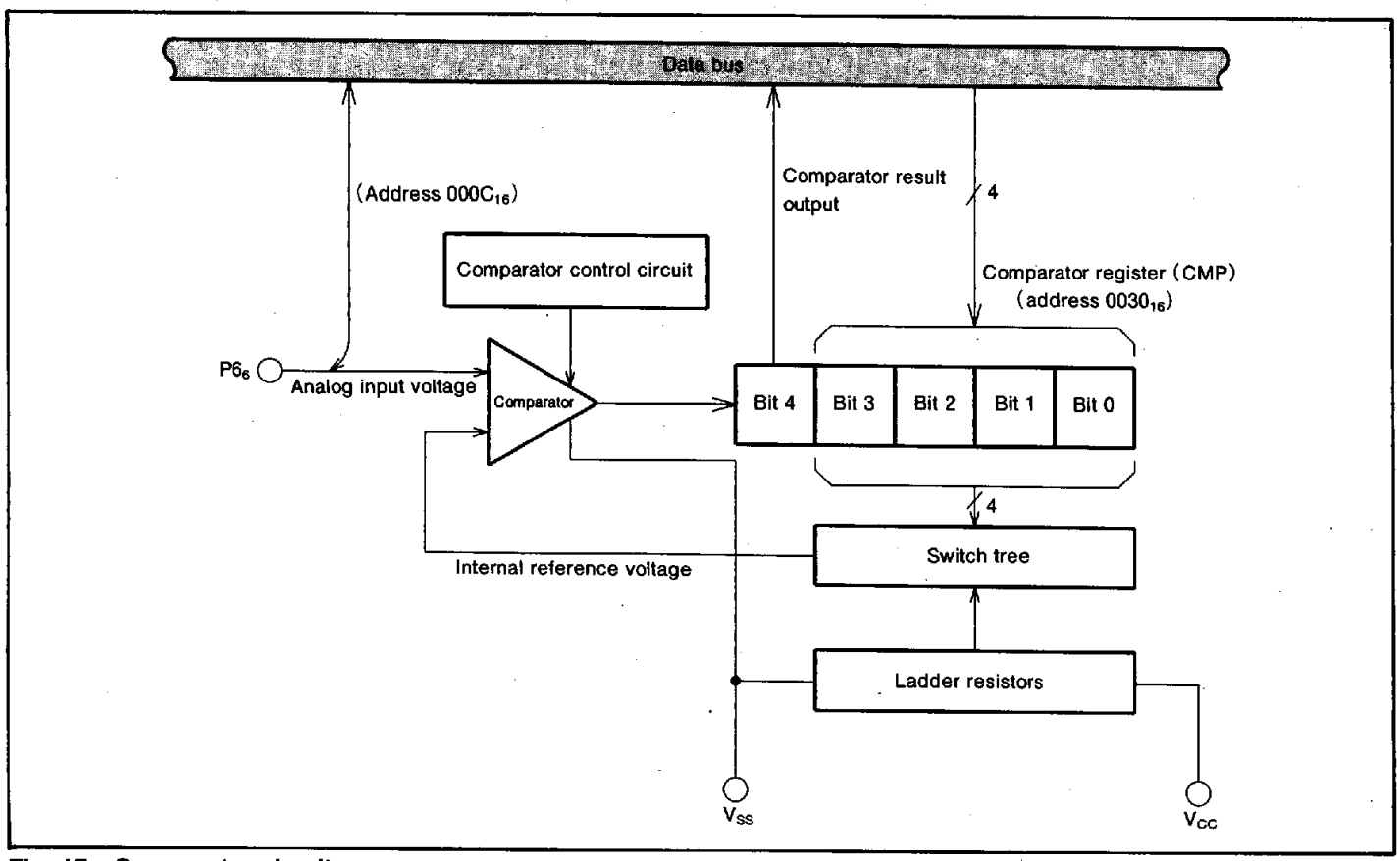



Fig. 17 Comparator circuit

## RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

### High-Speed Operation Start Mode

In high-speed operation start mode, to reset the microcomputer occurs, the $\overline{\text{RESET}}$ pin is held at an "L" level for 2$\mu$s or more. Then is returned to an "H" level (the power source voltage should be between 4.0V and 5.5V), reset is released. Both the $X_{IN}$ and the $X_{CIN}$ clocks begin oscillating. In order to give the $X_{IN}$ clock time to stabilize, internal operation begins until after 13 $X_{IN}$ clock cycles are completed. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte).

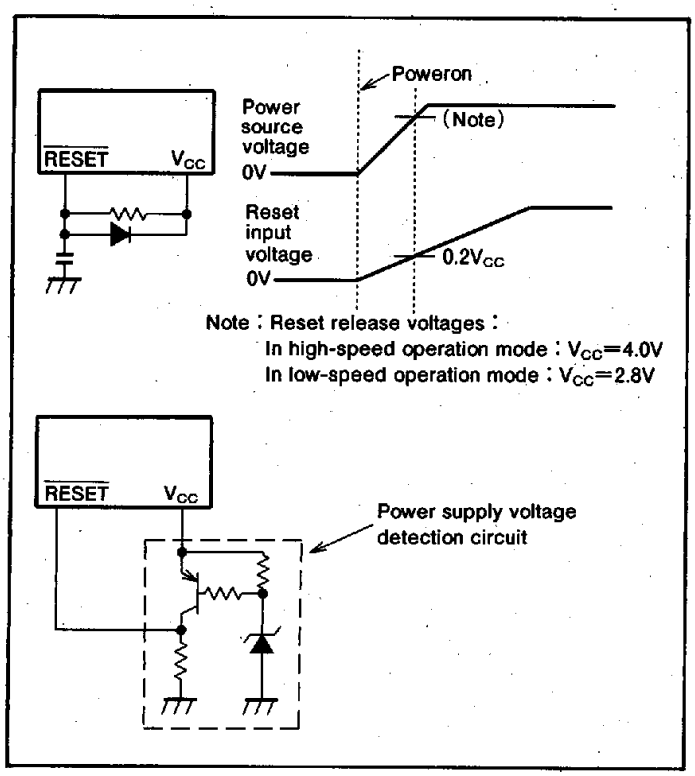



Fig. 18 Poweron reset circuit example

### Low-Speed Operation Start Mode

In low-speed operation start mode, to reset the microcomputer occurs, the $\overline{\text{RESET}}$ pin is held at a "L" level for 2$\mu$s or more. Then is returned to an "H" level (the power source voltage should be between 2.8V and 5.5V). The $X_{IN}$ clock does not begin oscillating. In order to give the $X_{CIN}$ time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the $X_{CIN}/16$ are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte).

If the $X_{CIN}$ clock is stable, reset will complete after approximately 250ms (assuming $f(X_{CIN})=32.768kHz$).

Immediately after a poweron, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.

### Note on Use

Make sure that the reset input voltage is less than 0.8V in high-speed operation start mode, or less than 0.5V in low-speed operation start mode.

| | | Address | Register contents |
|---|---|---|---|
| (1) | Port P0 register | $(0000_{16})$··· | $00_{16}$ |
| (2) | Port P1 register | $(0002_{16})$··· | $00_{16}$ |
| (3) | Port P2 register | $(0004_{16})$··· | $00_{16}$ |
| (4) | Port P2 direction register | $(0005_{16})$··· | $0F_{16}$ |
| (5) | Port P3 register | $(0006_{16})$··· | $00_{16}$ |
| (6) | Port P4 register | $(0008_{16})$··· | $00_{16}$ |
| (7) | Port P4 direction register | $(0009_{16})$··· | $00_{16}$ |
| (8) | Port P5 register | $(000A_{16})$··· | $00_{16}$ |
| (9) | Port P5 direction register | $(000B_{16})$··· | $00_{16}$ |
| (10) | Port P6 register | $(000C_{16})$··· | $00_{16}$ |
| (11) | Port P6 direction register | $(000D_{16})$··· | $00_{16}$ |
| (12) | Serial I/O1 control register | $(0019_{16})$··· | $00_{16}$ |
| (13) | Serial I/O2 control register | $(001D_{16})$··· | $00_{16}$ |
| (14) | Timer 1 register | $(0024_{16})$··· | $FF_{16}$ |
| (15) | Timer 2 register | $(0025_{16})$··· | $01_{16}$ |
| (16) | Timer 3 register | $(0026_{16})$··· | $FF_{16}$ |
| (17) | Timer 4 register | $(0027_{16})$··· | $FF_{16}$ |
| (18) | Timer 12 mode register | $(0028_{16})$··· | $00_{16}$ |
| (19) | Timer 34 mode register | $(0029_{16})$··· | $00_{16}$ |
| (20) | PWM control register | $(002B_{16})$··· | $00_{16}$ |
| (21) | Comparator | $(0030_{16})$··· | $00_{16}$ |
| (22) | High-breakdown-voltage port control register | $(0038_{16})$··· | $00_{16}$ |
| (23) | Interrupt edge selection register | $(003A_{16})$··· | $00_{16}$ |
| (24) | CPU mode register | $(003B_{16})$··· | * * 1 0 0 0 0 0 |
| (25) | Interrupt request register 1 | $(003C_{16})$··· | $00_{16}$ |
| (26) | Interrupt request register 2 | $(003D_{16})$··· | $00_{16}$ |
| (27) | Interrupt control register 1 | $(003E_{16})$··· | $00_{16}$ |
| (28) | Interrupt control register 2 | $(003F_{16})$··· | $00_{16}$ |
| (29) | Processor status register | (PS)··· | X X X X X 1 X X |
| (30) | Program counter | $(PC_H)$··· | Contents of address $FFFD_{16}$ |
| | | $(PC_L)$··· | Contents of address $FFFC_{16}$ |

Note : * : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option.
X : Undefined
The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values.

**Fig. 19 Internal status at reset**

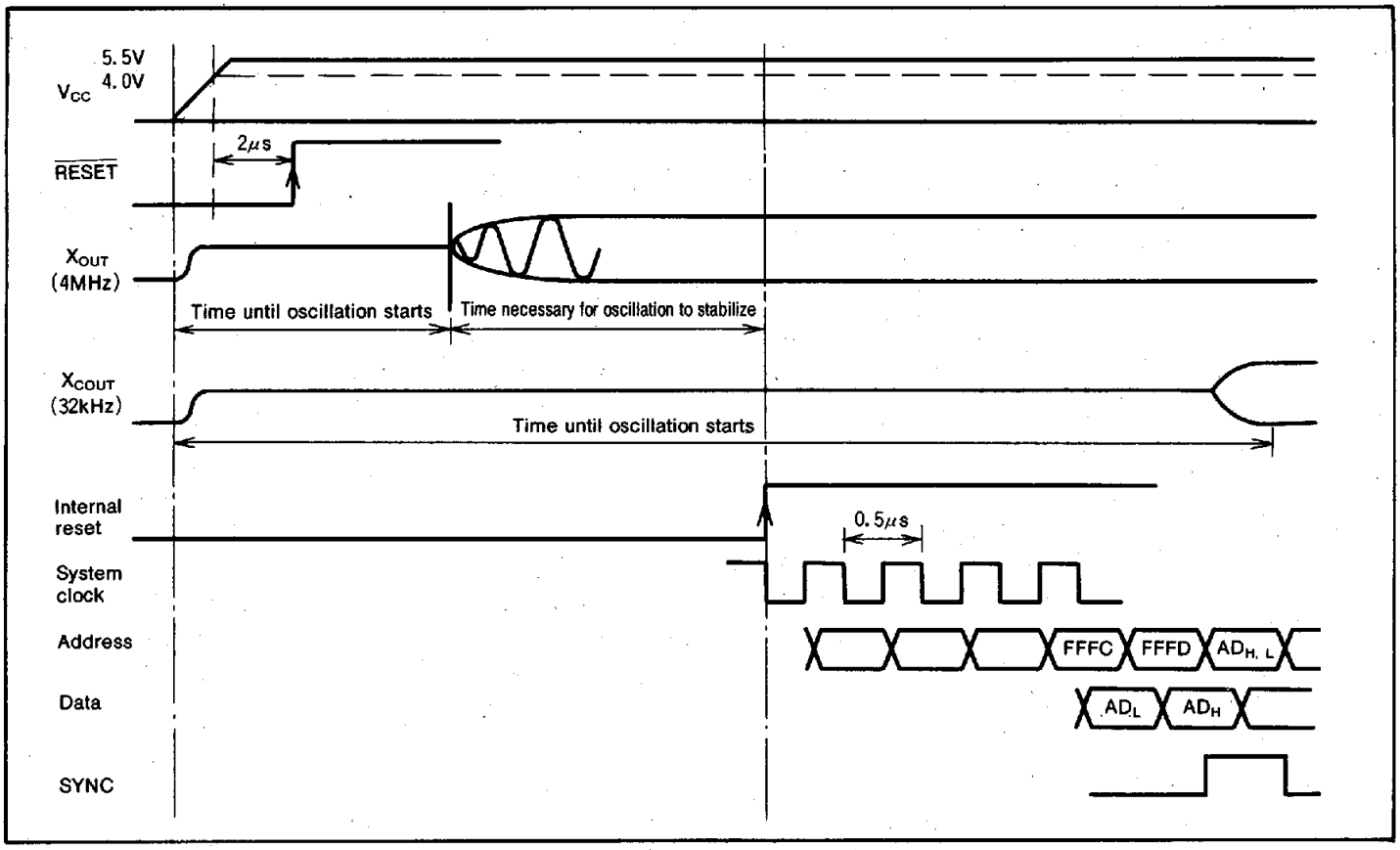



Fig. 20 Reset sequence in high-speed operation mode

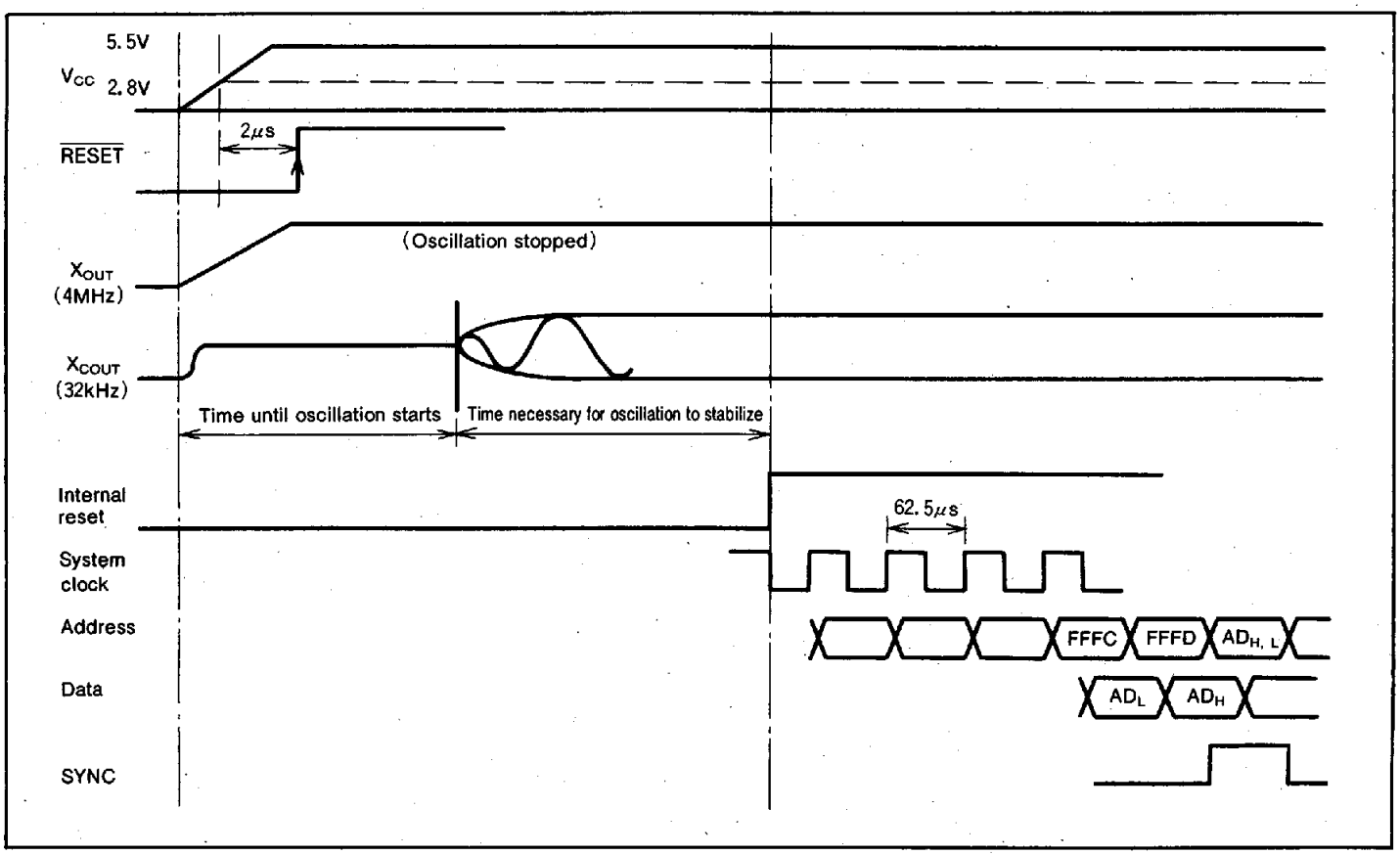



Fig. 21 Reset sequence in low-speed operation mode

## CLOCK GENERATING CIRCUIT

To supply a clock signal externally, input to the $X_{IN}$ ($X_{CIN}$) pin and make the $X_{OUT}$ ($X_{COUT}$) pin open. If the $X_{CIN}$ clock is not used, connect the $X_{CIN}$ pin to $V_{SS}$, and leave the $X_{COUT}$ pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

### High-Speed Operation Start Mode

After reset has completed, the internal clock $\phi$ is half the frequency of $X_{IN}$. Immediately after poweron, both the $X_{IN}$ and $X_{CIN}$ clock start oscillating. To set the internal clock $\phi$ to low-speed operation mode, set bit 7 of the CPU mode register (address $003B_{16}$) to "1".

### Low-Speed Operation Start Mode

After reset has completed, the internal clock $\phi$ is half the frequency of $X_{CIN}$. Immediately after poweron, only the $X_{CIN}$ clock starts oscillating. To set the internal clock $\phi$ to high-speed operation mode, first set bit 6 ($CM_6$) of the CPU mode register (address $003B_{16}$) to "0", the set bit 7 ($CM_7$) to "0". Note that the program must allow time for oscillation to stabilize.

### Oscillation Control

#### Stop Mode

If the STP instruction is executed, the internal clock $\phi$ stops at an "H" level. Timer 1 is set to "$FF_{16}$" and timer 2 is set to "$01_{16}$".

Either $X_{IN}$ or $X_{CIN}$ divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing a STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock $\phi$ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

#### Wait Mode

If the WIT instruction is executed, the internal clock $\phi$ stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

#### Low-Speed Mode

If the internal clock is generated from the sub-clock ($X_{CIN}$), a low power consumption operation can be entered by stopping only the main clock $X_{IN}$. To stop the main clock, set bit 6 ($CM_6$) of the CPU mode register ($003B_{16}$) to "1". When the main clock $X_{IN}$ is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the $X_{CIN}$-$X_{COUT}$ drivability can be reduced, allowing even lower power consumption (20$\mu$A with f($X_{CIN}$)= 32kHz). To reduce the $X_{CIN}$-$X_{COUT}$ drivability, clear bit 5 ($CM_5$) of the CPU mode register ($003B_{16}$) to "0". At reset or when a STP instruction is executed, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

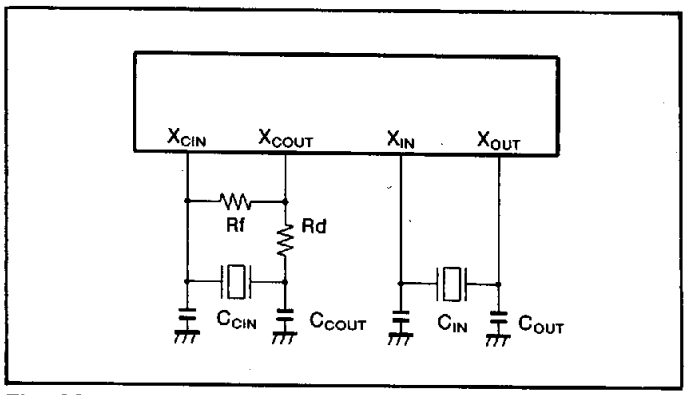



Fig. 22 Ceramic resonator circuit

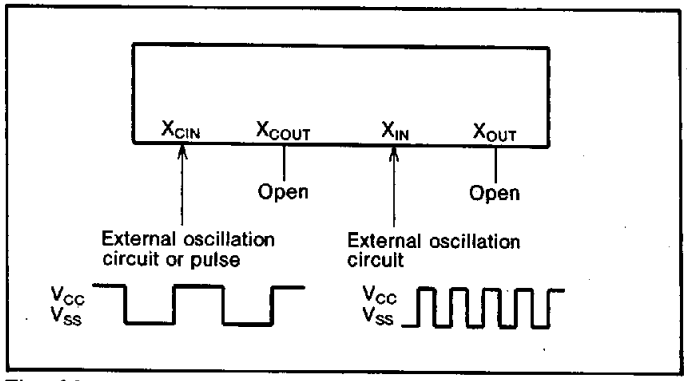
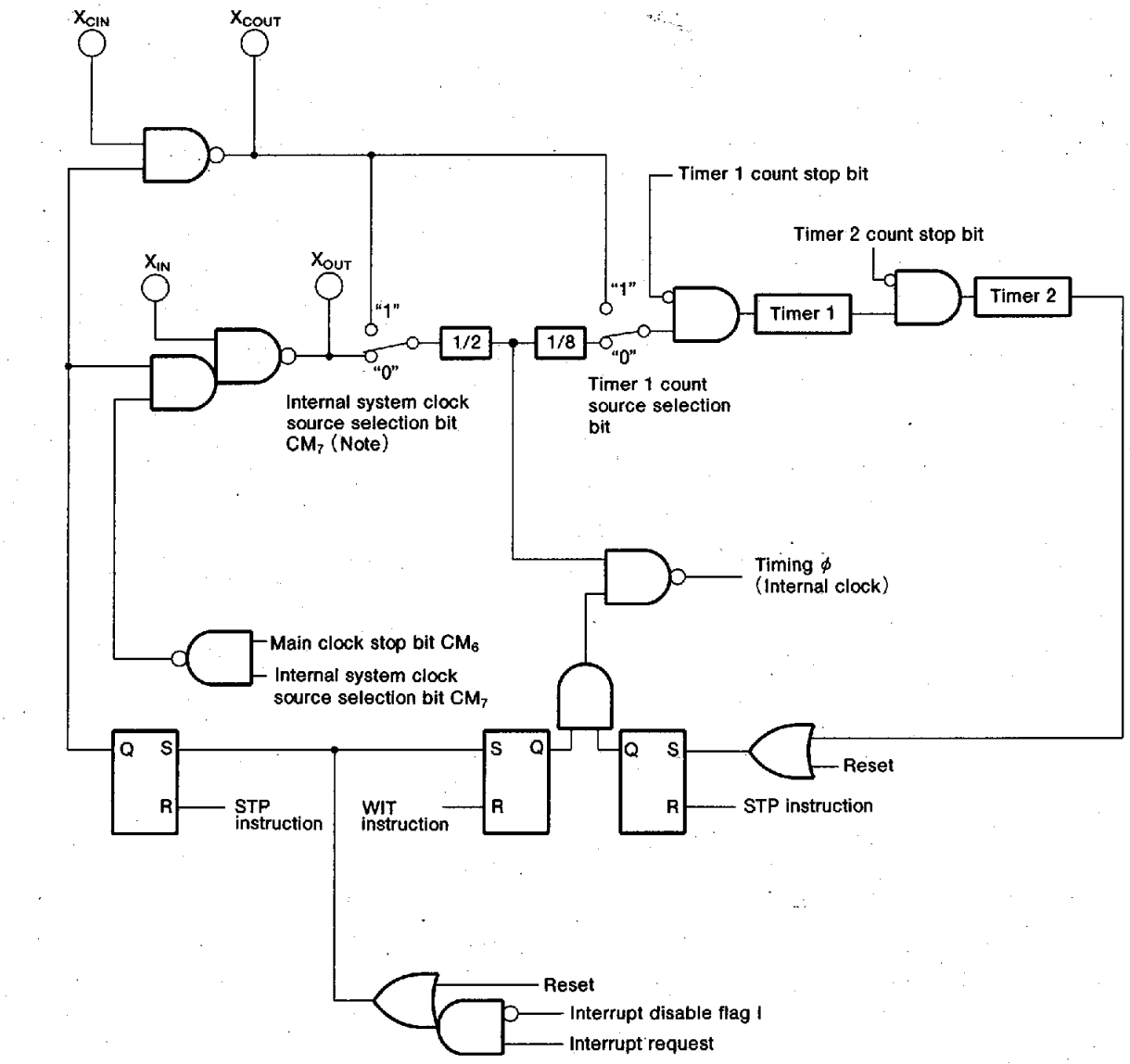
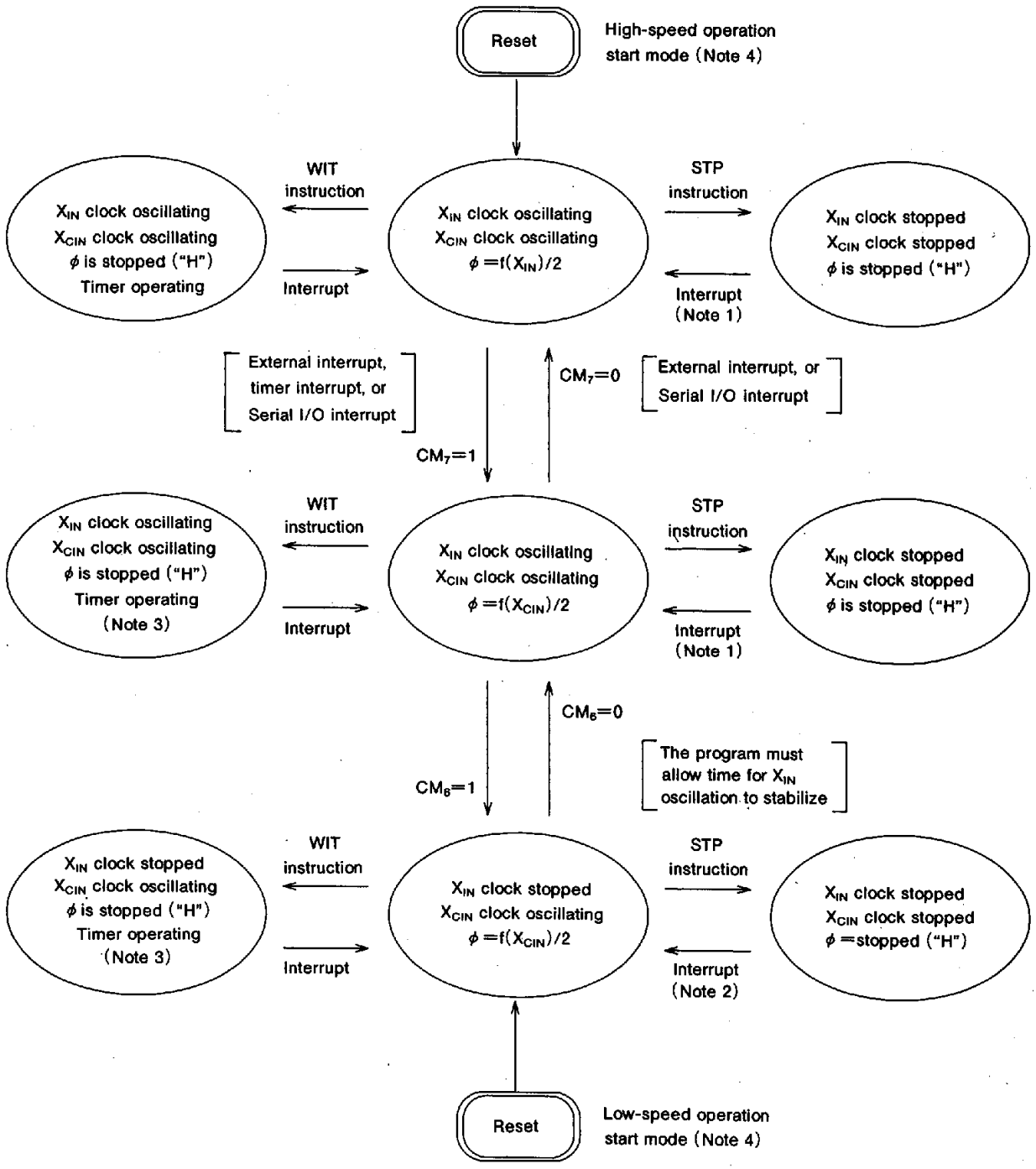



Fig. 23 External clock input circuit




Note : The values of $CM_7$ and $CM_6$ at reset are determined by a mask option.

**Fig. 24 System clock generating circuit block diagram**




The example assumes that 4 MHz is being applied to the $X_{IN}$ pin and 32 kHz to the $X_{CIN}$ pin.

Note 1. When the STP state is ended, a delay of approximately 2ms is automatically generated by timer 1 and timer 2.
2. The delay after the STP state ends is approximately 0.25s.
3. If the internal clock $\phi$ divided by 8 is used as the timer count source, the frequency of the count source is $f(X_{CIN})/16$.
4. Specify this option when ordering a mask ROM version.

Fig. 25 State transitions of system clock

# NOTES ON PROGRAMMING

## Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

## Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.

After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

## Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

## Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

## Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

## Ports

The contents of the port direction registers cannot be read. The following cannot be used :

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index.
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Do not write "1" to bit 0 of the port P4 direction register (address $0009_{16}$)

## Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

## Instruction Execution Timing

The instruction execution time is obtained by multiplying the frequency of the internal clock $\phi$ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock $\phi$ is half of the $X_{IN}$ or $X_{CIN}$ frequency.

## At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

The $X_{COUT}$ drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

## DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

If required, specify the following option on the Mask Confirmation Form:

- Operation start mode switching option

## PROM Programming Method

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.
Set the address of PROM programmer in the user ROM area.

| Package | Name of Programming Adapter |
|---|---|
| 64P4B, 64S1B | PCA4738S-64A |
| 64P6N-A | PCA4738F-64A |
| 64D0 | PCA4738L-64A |

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 26 is recommended to verify programming.

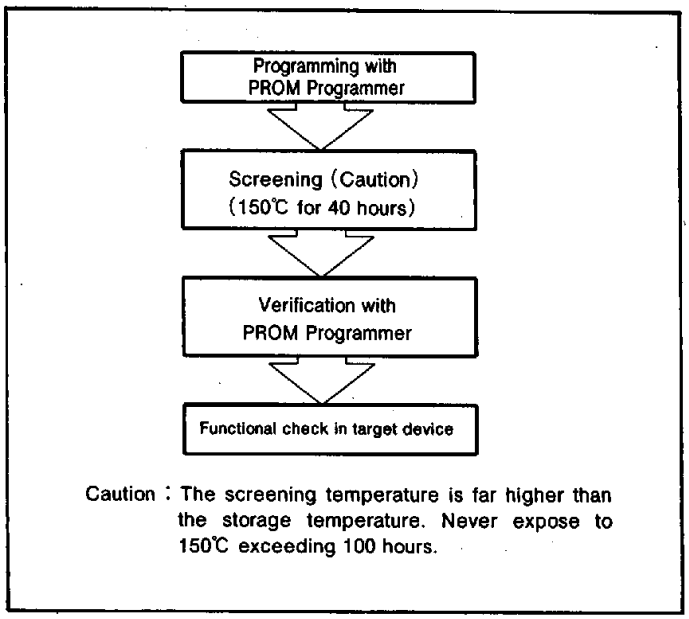



**Fig. 26 Programming and testing of One Time PROM version**

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Power source voltage | All voltages are based on the $V_{SS}$. Output transistors are cut off. | −0.3 to 7.0 | V |
| $V_{EE}$ | Pull-down power source voltage | | $V_{CC}$−40 to $V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ | | −0.3 to $V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $P4_0$ | | −0.3 to $V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $\overline{RESET}$, $X_{IN}$ | | −0.3 to $V_{CC}$+0.3 | V |
| $V_I$ | Input voltage $X_{CIN}$ | | −0.3 to $V_{CC}$+0.3 | V |
| $V_O$ | Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ | | $V_{CC}$−40 to $V_{CC}$+0.3 | V |
| $V_O$ | Output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_5$, $P7_0$-$P7_7$, $X_{OUT}$, $X_{COUT}$ | | −0.3 to $V_{CC}$+0.3 | V |
| $P_d$ | Power dissipation | $T_a$ = 25℃ | 1000(Note 1) | mW |
| Topr | Operating temperature | | −10 to 85 | ℃ |
| Tstg | Storage temperature | | −40 to 125 | ℃ |

Note 1. 600mW in case of the flat package.

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$ = 4.0 to 5.5V, $T_a$ = −10 to 85℃, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Power source voltage | High-speed operation mode | 4.0 | 5.0 | 5.5 | V |
| | | Low-speed operation mode | 2.8 | 5.0 | 5.5 | |
| $V_{SS}$ | Power source voltage | | | 0 | | V |
| $V_{EE}$ | Pull-down power supply voltage | | $V_{CC}$−38 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | 0 | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $P2_4$-$P2_7$ | | 0.4$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $P4_0$ | | 0.75$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ | | 0.75$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $\overline{RESET}$ | | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage $X_{IN}$, $X_{CIN}$ | | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $P2_4$-$P2_7$ | | 0 | | 0.16$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $P4_0$ | | 0 | | 0.25$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ | | 0 | | 0.25$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $\overline{RESET}$ | | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage $X_{IN}$, $X_{CIN}$ | | 0 | | 0.2$V_{CC}$ | V |

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$=4.0 to 5.5V, $T_a$=−10 to 85℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $\Sigma I_{OH(peak)}$ | "H" total peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$ (Note 1) | | | −240 | mA |
| $\Sigma I_{OH(peak)}$ | "H" total peak output current $P4_1$-$P4_7$, $P6_0$-$P6_7$ | | | −60 | mA |
| $\Sigma I_{OL(peak)}$ | "L" total peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$ | | | 100 | mA |
| $\Sigma I_{OL(peak)}$ | "L" total peak output current $P6_0$ | | | 3.0 | mA |
| $\Sigma I_{OH(avg)}$ | "H" total average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$ (Note 1) | | | −120 | mA |
| $\Sigma I_{OH(avg)}$ | "H" total average output current $P4_1$-$P4_7$, $P6_0$-$P6_7$ | | | −30 | mA |
| $\Sigma I_{OL(avg)}$ | "L" total average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$ | | | 50 | mA |
| $\Sigma I_{OL(avg)}$ | "L" total average output current $P6_0$ | | | 1.5 | mA |
| $I_{OH(peak)}$ | "H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ (Note 2) | | | −40 | mA |
| $I_{OH(peak)}$ | "H" peak output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$ | | | −10 | mA |
| $I_{OL(peak)}$ | "L" peak output current $P2_4$-$P2_7$, $P6_1$-$P6_7$ | | | 10 | mA |
| $I_{OL(peak)}$ | "L" peak output current $P4_1$-$P4_7$, $P5_0$-$P5_7$ | | | 10 | mA |
| $I_{OL(peak)}$ | "L" peak output current $P6_0$ | | | 3.0 | mA |
| $I_{OH(avg)}$ | "H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ (Note 3) | | | −18 | mA |
| $I_{OH(avg)}$ | "H" average output current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$ | | | −5.0 | mA |
| $I_{OL(avg)}$ | "L" average output current $P2_4$-$P2_7$, $P6_1$-$P6_7$ | | | 5.0 | mA |
| $I_{OL(avg)}$ | "L" average output current $P4_1$-$P4_7$, $P5_0$-$P5_7$ | | | 10 | mA |
| $I_{OL(avg)}$ | "L" average output current $P6_0$ | | | 1.5 | mA |
| f(CNTR) | Clock input frequency for timers 4 (duty cycle 50%) | | | 250 | kHz |
| $f(X_{IN})$ | Main clock input oscillation frequency (Note 4) | | | 4.2 | MHz |
| $f(X_{CIN})$ | Sub-clock input oscillation frequency (Note 4, 5) | | 32.768 | 50 | kHz |

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ns. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current in an average value measured over 100ms.
4. When the oscillation frequency has a duty cycle of 50%.
5. When using the microcomputer in low-speed mode, make sure that the sub-clock input frequency $f(X_{CIN})$ is less than $f(X_{IN})/3$.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 4.0 to 5.5V, $T_a$ = −10 to 85℃, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{OH}$ | "H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ | $I_{OH}$=−18mA, $V_{CC}$=4.5 to 5.5V | $V_{CC}$−2.0 | | | V |
| $V_{OH}$ | "H" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P6_0$-$P6_7$ | $I_{OH}$=−10mA, $V_{CC}$=4.5 to 5.5V | $V_{CC}$−2.0 | | | V |
| $V_{OL}$ | "L" output voltage $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_1$-$P6_7$ | $I_{OL}$=10mA, $V_{CC}$=4.5 to 5.5V | | | 2.0 | V |
| $V_{OL}$ | "L" output voltage $P6_0$ | $I_{OL}$=1.5mA, $V_{CC}$=4.5 to 5.5V | | | 0.5 | V |
| $V_{T+}-V_{T-}$ | Hysteresis $\overline{INT_0}$-$\overline{INT_2}$, $S_{IN1}$, $S_{IN2}$, CLK1, CLK2, CNTR | When using a non-port function | | 0.4 | | V |
| $V_{T+}-V_{T-}$ | Hysteresis $\overline{RESET}$, $X_{IN}$ | $\overline{RESET}$ : $V_{CC}$=2.8V to 5.5V | | 0.5 | | V |
| $V_{T+}-V_{T-}$ | Hysteresis $X_{CIN}$ | | | 0.5 | | V |
| $I_{IH}$ | "H" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ | $V_I$=$V_{CC}$ | | | 5.0 | μA |
| $I_{IH}$ | "H" input current $P4_0$ | $V_I$=$V_{CC}$ | | | 5.0 | μA |
| $I_{IH}$ | "H" input current $\overline{RESET}$, $X_{CIN}$ | $V_I$=$V_{CC}$ | | | 5.0 | μA |
| $I_{IH}$ | "H" input current $X_{IN}$ | $V_I$=$V_{CC}$ | | 4 | | μA |
| $I_{IL}$ | "L" input current $P2_4$-$P2_7$, $P4_1$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ | $V_I$=$V_{SS}$ | | | −5.0 | μA |
| $I_{IL}$ | "L" input current $P4_0$ | $V_I$=$V_{SS}$ | | | −5.0 | μA |
| $I_{IL}$ | "L" input current $\overline{RESET}$, $X_{CIN}$ | $V_I$=$V_{SS}$ | | | −5.0 | μA |
| $I_{IL}$ | "L" input current $X_{IN}$ | $V_I$=$V_{SS}$ | | −4 | | μA |
| $I_{LOAD}$ | Output load current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ | $V_{EE}$=$V_{CC}$−36V, $V_O$=$V_{CC}$, With output transistors off | 150 | 500 | 900 | μA |
| $I_{LEAK}$ | Output leakage current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_7$ | $V_{EE}$=$V_{CC}$−38V, $V_O$=$V_{CC}$−38V, With output transistors "off" (Except for reset) | | | −10 | μA |
| $V_{RAM}$ | RAM hold voltage | When clock is stopped | 2.0 | | 5.5 | V |
| $I_{CC}$ | Power source current | In high-speed operation mode<br>$f(X_{IN})$=4MHz<br>$f(X_{CIN})$=32kHz<br>Output transistors "off"<br>Comparator operating | | 5 | 10 | mA |
| | | In high-speed operation mode<br>$f(X_{IN})$=4MHz (in WIT state)<br>$f(X_{CIN})$=32kHz<br>Output transistors "off"<br>Comparator stopped | | 1 | | mA |
| | | In low-speed operation mode<br>$f(X_{IN})$= stopped $f(X_{CIN})$=32kHz<br>Low-power dissipation mode set<br>($CM_5$=0)<br>Output transistors "off" | | 60 | 200 | μA |
| | | In low-speed operation mode<br>$f(X_{IN})$= stopped<br>$f(X_{CIN})$=32kHz (in WIT state)<br>Low-power dissipation mode set<br>($CM_5$=0)<br>Output transistors "off" | | 20 | 40 | μA |
| | | All oscillation stopped (in STP state) Output transistors "off" $T_a$=25℃ | | 0.1 | 1.0 | μA |
| | | All oscillation stopped (in STP state) Output transistors "off" $T_a$=85℃ | | | 10 | μA |

## COMPARATOR CHARACTERISTICS

($V_{CC}$=4.0 to 5.5V, $V_{SS}$=0V, $T_a$=−10 to 85℃, high-speed operation mode, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Resolution | | | | 4 | Bits |
| — | Absolute accuracy | | | | 1/2 | LSB |
| $T_{CONV}$ | Conversion time | | | | 7 | μs |
| $I_{IA}$ | Analog port input current | | | | 5.0 | μA |
| $R_{LADDER}$ | Ladder resistor | | | 30 | | kΩ |

## TIMING REQUIREMENTS ($V_{CC}$ =4.0 to 5.5V, $V_{SS}$ = 0V, $T_a$ = −10 to 85℃, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{W(\overline{RESET})}$ | Reset input "L" pulse width | | 2 | | | μs |
| $t_{C(X_{IN})}$ | Main clock input cycle time ($X_{IN}$ input) | | 238 | | | ns |
| $t_{WH(X_{IN})}$ | Main clock input "H" pulse width | | 60 | | | ns |
| $t_{WL(X_{IN})}$ | Main clock input "L" pulse width | | 60 | | | ns |
| $t_{C(X_{CIN})}$ | Sub-clock input cycle time ($X_{CIN}$ input) | | 20 | | | μs |
| $t_{WH(X_{CIN})}$ | Sub-clock input "H" pulse width | | 5 | | | μs |
| $t_{WL(X_{CIN})}$ | Sub-clock input "L" pulse width | | 5 | | | μs |
| $t_{C(CNTR)}$ | CNTR input cycle time | | 4 | | | μs |
| $t_{WH(CNTR)}$ | CNTR input "H" pulse width | | 1.6 | | | μs |
| $t_{WL(CNTR)}$ | CNTR input "L" pulse width | | 1.6 | | | μs |
| $t_{WH(INT)}$ | $INT_0$—$INT_2$ input "H" pulse width | | 80 | | | ns |
| $t_{WL(INT)}$ | $INT_0$—$INT_2$ input "L" pulse width | | 80 | | | ns |
| $t_{C(SCLK)}$ | Serial I/O clock input cycle time | | 1 | | | μs |
| $t_{WH(SCLK)}$ | Serial I/O clock input clock "H" pulse width | | 400 | | | ns |
| $t_{WL(SCLK)}$ | Serial I/O clock input clock "L" pulse width | | 400 | | | ns |
| $t_{su(SCLK-SIN)}$ | Serial I/O input setup time | | 200 | | | ns |
| $t_{h(SCLK-SIN)}$ | Serial I/O input hold time | | 200 | | | ns |

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 4.0 to 5.5V, $V_{SS}$ = 0V, $T_a$ = −10 to 85℃, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{WH(SCLK)}$ | Serial I/O clock output "H" pulse width | $C_L$=100pF, $R_L$=1kΩ | $t_{C(SCLK)}$ /2−160 | | | ns |
| $t_{WL(SCLK)}$ | Serial I/O clock output "L" pulse width | $C_L$=100pF, $R_L$=1kΩ | $t_{C(SCLK)}$ /2−160 | | | ns |
| $t_{d(SCLK-SOUT)}$ | Serial I/O output delay time | | | | 0.2$t_C$ | ns |
| $t_{v(SCLK-SOUT)}$ | Serial I/O output hold time | | 0 | | | ns |
| $t_{f(SCLK)}$ | Serial I/O clock output falling time | $C_L$=100pF, $R_L$=1kΩ | | | 40 | ns |
| $t_{r(Pch\text{-}strg)}$ | P-channel high-breakdown voltage output rising time (Note 1) | $C_L$=100pF, $V_{EE}$=$V_{CC}$−36V | | 55 | | ns |
| $t_{r(Pch\text{-}weak)}$ | P-channel high-breakdown voltage output rising time (Note 2) | $C_L$=100pF, $V_{EE}$=$V_{CC}$−36V | | 1.8 | | μs |

Note 1. When bit 0 of the high-breakdown voltage port control register (address $0038_{16}$) is at "0".
2. When bit 0 of the high-breakdown voltage port control register (address $0038_{16}$) is at "1".

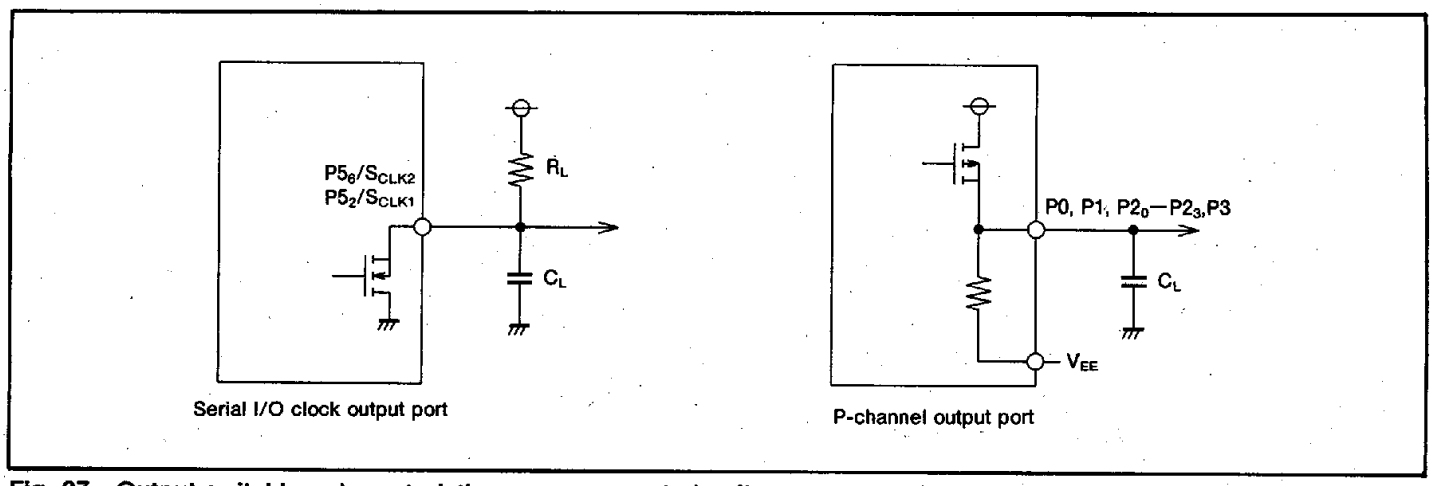



**Fig. 27 Output switching characteristics measurement circuit**

## TIMING CHART