ANALOG DEVICES

±0.5°C Accurate Digital Temperature Sensor and Quad Voltage Output 12-/10-/8-Bit DACs

ADT7316/ADT7317/ADT7318

FEATURES

ADT7316—four 12-Bit DACs
ADT7317—four 10-Bit DACs
ADT7318—four 8-Bit DACs
Buffered voltage output
Guaranteed monotonic by design over all codes
10-bit temperature-to-digital converter
Temperature range: –40°C to +120°C
Temperature sensor accuracy of ±0.5°C
Supply range: 2.7 V to 5.5 V
DAC output range: 0 V to 2 V_{REF}
Power-down current 1 μA
Internal 2.28 V_{REF} option
Double-buffered input logic
Buffered/unbuffered reference input option
Power-on reset to 0 V
Simultaneous update of outputs ($\overline{LDAC}$ function)
On-chip rail-to-rail output buffer amplifier
I²C®, SMBus, SPI®, QSPI™, MICROWIRE™, and DSP compatible 4-wire serial interface
SMBus packet error checking (PEC) compatible
16-lead QSOP package

APPLICATIONS

Portable battery-powered instruments
Personal computers
Telecommunications systems
Electronic test equipment
Domestic appliances
Process control

PIN CONFIGURATION

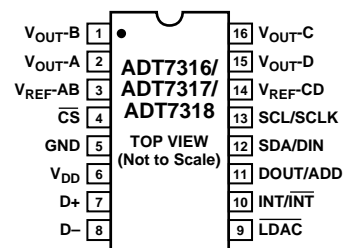|		
V_{OUT}-B	1	16	V_{OUT}-C
V_{OUT}-A	2	15	V_{OUT}-D
V_{REF}-AB	3	14	V_{REF}-CD
$\overline{CS}$	4	13	SCL/SCLK
GND	5	12	SDA/DIN
V_{DD}	6	11	DOUT/ADD
D+	7	10	INT/$\overline{INT}$
D–	8	9	$\overline{LDAC}$

ADT7316/ADT7317/ADT7318
TOP VIEW
(Not to Scale)

02661-A-006

Figure 1.

GENERAL DESCRIPTION

The ADT7316/ADT7317/ADT7318[1] combine a 10-bit temperature-to-digital converter and a quad 12-/10-/8-bit DAC, respectively, in a 16-lead QSOP package. This includes a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C. The ADT7316/ADT7317/ADT7318 operate from a single 2.7 V to 5.5 V supply. The output voltage of the DAC ranges from 0 V to 2 V_{REF}, with an output voltage settling time of typ 7 ms. The ADT7316/ADT7317/ADT7318 provide two serial interface options, a 4-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards, and a 2-wire SMBus/I²C interface. They feature a standby mode that is controlled via the serial interface.

The reference for the four DACs is derived either internally or from two reference pins (one per DAC pair). The outputs of all

DACs may be updated simultaneously using the software LDAC function or external $\overline{LDAC}$ pin. The ADT7316/ADT7317/ADT7318 incorporate a power-on-reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place.

The ADT7316/ADT7317/ADT7318's wide supply voltage range, low supply current, and SPI/I²C compatible interface make them ideal for a variety of applications, including personal computers, office equipment, and domestic appliances.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703 **© 2004 Analog Devices, Inc. All rights reserved.**

ADT7316/ADT7317/ADT7318

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REVISION HISTORY

6/04—Data Sheet Changed from Rev. 0 to Rev. A

8/03—Initial Version: Rev.0

SPECIFICATIONS

Table 1. Temperature ranges are as follows: A Version: −40°C to +120°C. V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.25 V, unless otherwise noted.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DAC DC PERFORMANCE[2,3]					
ADT7318					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic over all codes.
ADT7317					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic over all codes.
ADT7316					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.02	±0.9	LSB	Guaranteed monotonic over all codes.
Offset Error		±0.4	±2	% of FSR	
Gain Error		±0.4	±2	% of FSR	
Lower Dead Band		20	65	mV	Lower dead band exists only if offset error is negative. See Figure 2.
Upper Dead Band		60	100	mV	Upper dead band exists if V_{REF} = V_{DD} and offset plus gain error is positive. See Figure 3.
Offset Error Drift		−12		ppm of FSR/°C	
Gain Error Drift		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio		−60		dB	ΔV_{DD} = ±10%.
DC Crosstalk		200		µV	See Figure 6.
THERMAL CHARACTERISTICS INTERNAL TEMPERATURE SENSOR					Internal reference used. Averaging on.
Accuracy at V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C.
		±0.5	±3	°C	T_A = 0°C to +85°C.
		±2	±5	°C	T_A = −40°C to +120°C.
Accuracy at V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C.
		±3	±5	°C	T_A = −40°C to +120°C.
Resolution			10	Bits	Equivalent to 0.25°C.
Long Term Drift		0.25		°C	Drift over 10 years if part is operated at 55°C.
EXTERNAL TEMPERATURE SENSOR					External Transistor = 2N3906.
Accuracy at V_{DD} = 3.3 V ±10%			±1.5	°C	T_A = 85°C.
			±3	°C	T_A = 0°C to +85°C.
			±5	°C	T_A = −40°C to +120°C.
Accuracy at V_{DD} = 5 V ±5%		±2	±3	°C	T_A = 0°C to +85°C.
		±3	±5	°C	T_A = −40°C to +120°C.
Resolution			10	Bits	Equivalent to 0.25°C.
Output Source Current		180		µA	High level.
		11		µA	Low level.
Thermal Voltage Output					
8-Bit DAC Output					
Resolution	1			°C	
Scale Factor		8.79		mV/°C	0 V to V_{REF} Output. T_A = −40°C to +120°C.
		17.58		mV/°C	0 V to 2 V_{REF} Output. T_A = −40°C to +120°C.

[1] See Terminology.
[2] DC specifications tested with the outputs unloaded.
[3] Linearity is tested using a reduced code range: ADT7316 (code 115 to 4095); ADT7317 (code 28 to 1023); ADT7318 (code 8 to 255).

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
10-Bit DAC Output					
Resolution	0.25			°C	
Scale Factor		2.2		mV/°C	0 V to V_{REF} Output. T_A = −40°C to +120°C.
		4.39		mV/°C	0 V to 2 V_{REF} Output. T_A = −40°C to +120°C.
CONVERSION TIMES					Single Channel Mode.
Slow ADC					
V_{DD}		11.4		ms	Averaging (16 samples) on.
		712		µs	Averaging off.
Internal Temperature		11.4		ms	Averaging (16 samples) on.
		712		µs	Averaging off.
External Temperature		24.22		ms	Averaging (16 samples) on
		1.51		ms	Averaging off.
Fast ADC					
V_{DD}		712		µs	Averaging (16 samples) on.
		44.5		µs	Averaging off.
Internal Temperature		2.14		ms	Averaging (16 samples) on.
		134		µs	Averaging off.
External Temperature		14.25		ms	Averaging (16 samples) on.
		890		µs	Averaging off.
ROUND ROBIN UPDATE RATE[4]					Time to complete one measurement cycle through all channels.
Slow ADC at 25°C					
Averaging On		59.95		ms	
Averaging Off		6.52		ms	
Fast ADC at 25°C					
Averaging On		19.59		ms	
Averaging Off		2.89		ms	
DAC EXTERNAL REFERENCE INPUT[5]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference mode.
V_{REF} Input Range	0.25		V_{DD}	V	Unbuffered reference mode.
V_{REF} Input Impedance	37	45		kΩ	Unbuffered reference mode.
					0 V to 2 V_{REF} output range.
	74	90		kΩ	Unbuffered reference mode.
					0 V to V_{REF} output range.
		>10		MΩ	Buffered reference mode and power-down mode.
Reference Feedthrough		−90		dB	Frequency = 10 kHz.
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz.
ON-CHIP REFERENCE					
Reference Voltage[5]		2.28		V	
Temperature Coefficient[5]		80		ppm/C	
OUTPUT CHARACTERISTICS[5]					
Output Voltage[6]	0.001		V_{DD} to 0.001	V	This is a measure of the minimum and maximum drive capability of the output amplifier.
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V.
		16		mA	V_{DD} = 3 V.
Power-Up Time		2.5		µs	Coming out of power-down mode. V_{DD} = 5 V.
		5		µs	Coming out of power-down mode. V_{DD} = 3.3 V.

[4] Round robin is the continuous sequential measurement of the following three channels: V_{DD}, internal temperature, and external temperature.
[5] Guaranteed by design and characterization, but not production tested.
[6] In order for the amplifier output to reach its minimum voltage, the offset error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF} = V_{DD}, offset plus gain error must be positive.

Parameter[1]	Min	Typ	Max	Unit	Conditions/Comments
DIGITAL INPUTS[5]					
Input Current			±1	µA	V_{IN} = 0 V to V_{DD}.
Input Low Voltage, V_{IL}			0.8	V	
Input High Voltage, V_{IH}	1.89			V	
Pin Capacitance		3	10	pF	All digital inputs.
SCL, SDA Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns.
$\overline{LDAC}$ Pulse Width	20			ns	Edge triggered input.
DIGITAL OUTPUT					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = I_{SINK} = 200 µA.
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 3 mA.
Output High Current, I_{OH}			1	mA	V_{OH} = 5 V.
Output Capacitance, C_{OUT}			50	pF	
INT/$\overline{INT}$ Output Saturation Voltage			0.8	V	I_{OUT} = 4 mA.
I²C TIMING CHARACTERISTICS[7,8]					
Serial Clock Period, t_1	2.5			µs	Fast-mode I²C. See Figure 4.
Data In Setup Time to SCL High, t_2	50			ns	
Data Out Stable after SCL Low, t_3	0			ns	See Figure 4.
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	See Figure 4.
SDA High Hold Time after SCL High (Stop Condition), t_5	50			ns	See Figure 4.
SDA and SCL Fall Time, t_6			90	ns	See Figure 4.
SPI TIMING CHARACTERISTICS[9,10]					
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	See Figure 7.
SCLK High Pulse Width, t_2	50			ns	See Figure 7.
SCLK Low Pulse, t_3	50			ns	See Figure 7.
Data Access Time after SCLK Falling Edge, t_4[11]			35	ns	See Figure 7.
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	See Figure 7.
Data Hold Time after SCLK Rising Edge, t_6	0			ns	See Figure 7.
$\overline{CS}$ to SCLK Hold Time, t_7	0			ns	See Figure 7.
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	See Figure 7.
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of its final voltage level.
I_{DD} (Normal Mode)[12]			3	mA	V_{DD} = 3.3 V, V_{IH} = V_{DD} and V_{IL} = GND.
		2.2	3	mA	V_{DD} = 5 V, V_{IH} = V_{DD} and V_{IL} = GND.
I_{DD} (Power Down Mode)			10	µA	V_{DD} = 3.3 V, V_{IH} = V_{DD} and V_{IL} = GND.
			10	µA	V_{DD} = 5 V, V_{IH} = V_{DD} and V_{IL} = GND.
Power Dissipation			10	mW	V_{DD} = 3.3 V. Using Normal Mode.
			33	µW	V_{DD} = 3.3 V. Using Shutdown Mode.

[7]The SDA and SCL timing is measured with the input filters turned on so as to meet the fast-mode I²C specification. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[8]Guaranteed by design. Not tested in production.
[9]Guaranteed by design and characterization, but not production tested.
[10]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[11]Measured with the load circuit of Figure 5.
[12]I_{DD} specification is valid for all DAC codes. Interface inactive. All DACs active. Load currents excluded.
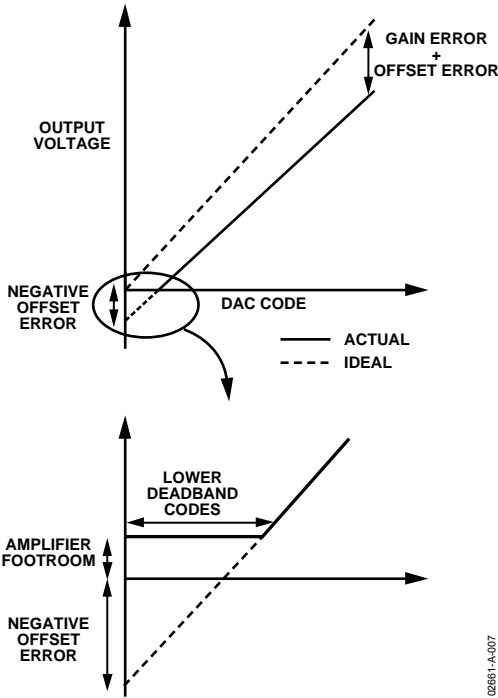
Figure 2. DAC Transfer Function with Negative Offset

Figure 3. DAC Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)
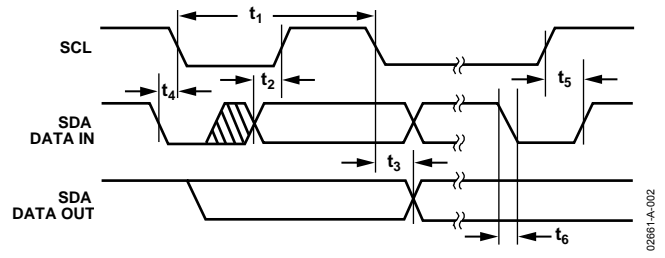
Figure 4. I²C Bus Timing Diagram
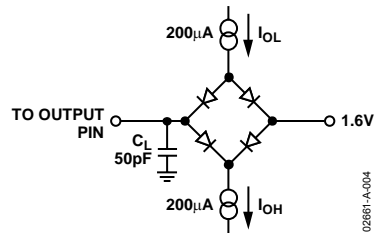
Figure 5. Load Circuit for Access Time and Bus Relinquish Time
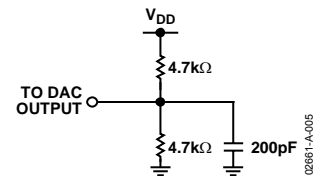
Figure 6. Load Circuit for DAC Outputs
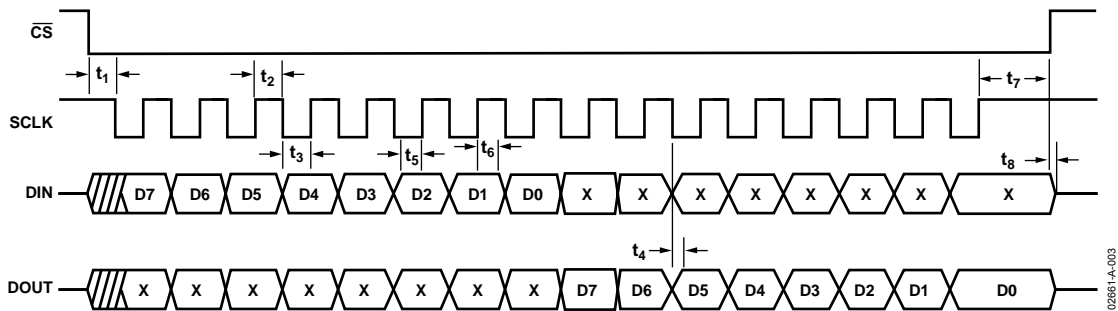
Figure 7. SPI Bus Timing Diagram

FUNCTIONAL BLOCK DIAGRAM
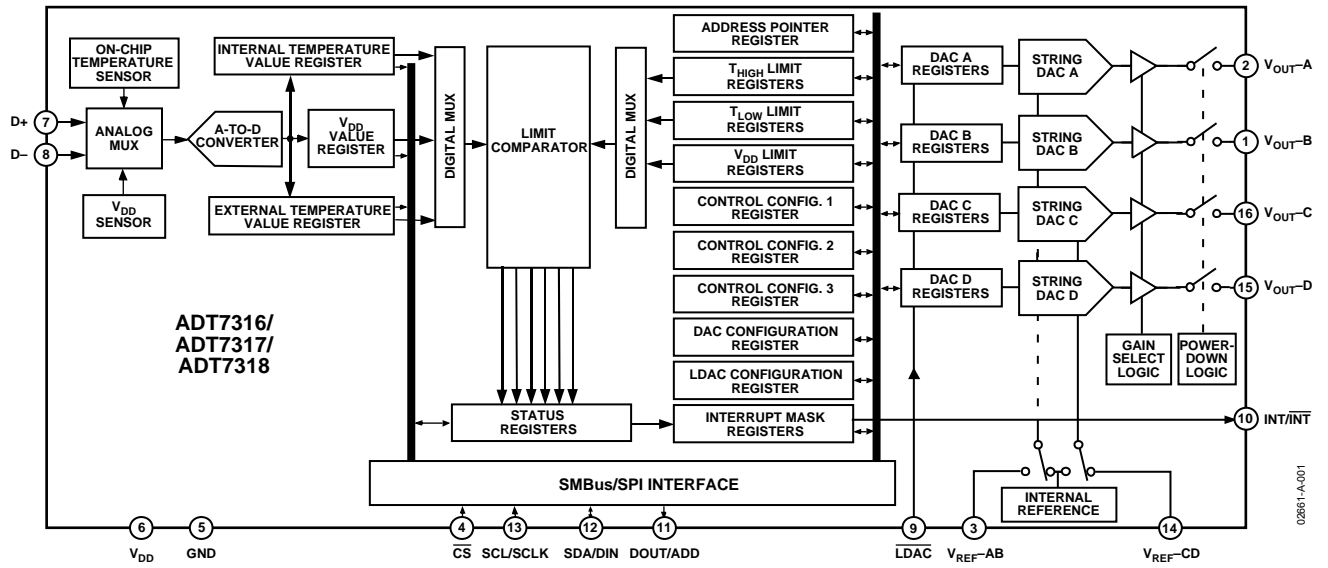
Figure 8.

DAC AC CHARACTERISTICS

Table 2. Guaranteed by design and characterization, but not production tested. V_{DD} = 2.7 V to 5.5 V; R_L = 4.7 kΩ to GND; C_L = 200 pF to GND; 4.7 kΩ to V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter[1]	Min	Typ (@ 25°C)	Max	Unit	Conditions and Comments
Output Voltage Settling Time					V_{REF} = V_{DD} = +5 V
ADT7318		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0).
ADT7317		7	9	µs	1/4 scale to 3/4 scale change (0x100 to 0x300).
ADT7316		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00).
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry.
Digital Feedthrough		0.5			
Digital Crosstalk		1		nV-s	
Analog Crosstalk		0.5		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p.
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz.

[1] See Terminology section.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +120°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead QSOP Package	
Power Dissipation[1]	$(T_J \, max − T_A)/\theta_{JA}$
Thermal Impedance[2]	
θ_{JA} Junction-to-Ambient	105.44°C/W
θ_{JC} Junction-to-Case	38.8°C/W
IR Reflow Soldering	
Peak Temperature	220°C (0/5°C)
Time at Peak Temperature	10 sec to 20 sec
Ramp-Up Rate	2°C/sec to 3°C/sec
Ramp-Down Rate	−6°C/sec

[1] Values relate to package being used on a 4-layer board.
[2] Junction-to-case resistance is applicable to components featuring a preferential flow direction, e.g., components mounted on a heat sink. Junction-to-ambient resistance is more useful for air-cooled PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. I²C Address Selection

ADD Pin	I²C Address
Low	1001 000
Float	1001 010
High	1001 011

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
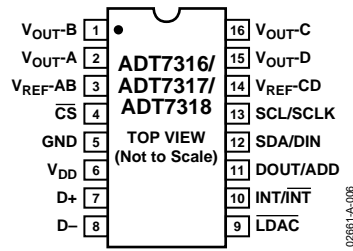
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 9. Pin Configuration QSOP

Table 5. ADT7316/ADT7317/ADT7318 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}-B	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
2	V_{OUT}-A	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V_{REF}-AB	Reference Input Pin for DACs A and B. It may be configured as a buffered or unbuffered input to both DACs A and B. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode. DACs A and B default on power-up to this pin.
4	$\overline{CS}$	SPI Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pin be tied high to V_{DD} when operating the serial interface in I²C mode.
5	GND	Ground Reference Point for All Circuitry on the Part. Analog and digital ground.
6	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
7	D+	Positive connection to external temperature sensor.
8	D−	Negative connection to external temperature sensor.
9	$\overline{LDAC}$	Active low control input that transfers the contents of the input registers to their respective DAC registers. A falling edge on this pin forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20 ns must be applied to the $\overline{LDAC}$ pin to ensure proper loading of a DAC register. This allows simultaneous update of all DAC outputs. Bit C3 of Control Configuration 3 register enables $\overline{LDAC}$ pin. Default is with $\overline{LDAC}$ pin controlling the loading of DAC registers.
10	INT/$\overline{INT}$	Over Limit Interrupt. The output polarity of this pin can be set to give an active low or active high interrupt when temperature or V_{DD} limits are exceeded. Default is active low. Open-drain output—needs a pull-up resistor.
11	DOUT/ADD	SPI, Serial Data Output. Logic output. Data is clocked out of any register at this pin. Data is clocked out on the falling edge of SCLK. Open-drain output—needs a pull-up resistor.
		ADD, I²C Serial Bus Address Selection Pin. Logic input. A low on this pin gives the address 1001 000, leaving it floating gives the address 1001 010 and setting it high gives the address 1001 011. The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent changes on this pin will have no affect on the I²C serial bus address.
12	SDA/DIN	SDA, I²C Serial Data Input. I²C serial data that is loaded into the device's registers is provided on this input. Open-drain configuration—needs a pull-up resistor.
		DIN, SPI Serial Data Input. Serial data to be loaded into the device's registers is provided on this input. Data is clocked into a register on the rising edge of SCLK. Open-drain configuration—needs a pull-up resistor.
13	SCL/SCLK	Serial Clock Input. This is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7316/ADT7317/ADT7318 and also to clock data into any register that can be written to. Open-drain configuration—needs a pull-up resistor.
14	V_{REF} -CD	Reference Input Pin for DACs C and D. It may be configured as a buffered or unbuffered input to both DACs C and D. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode. DACs C and D default on power-up, to this pin.
15	V_{OUT} -D	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
16	V_{OUT} -C	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.

TERMINOLOGY

Relative Accuracy

Relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL versus code plots can be seen in Figure 10, Figure 11, and Figure 12.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±0.9 LSB maximum ensures monotonicity. Typical DAC DNL versus code plots can be seen in Figure 13, Figure 14, and Figure 15.

Offset Error

This is a measure of the offset error of the DAC and the output amplifier. (See Figure 2 and Figure 3.) It can be negative or positive. It is expressed as a percentage of the full-scale range.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift

This is a measure of the change in offset error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in ppm of full-scale range/°C.

Long Term Temperature Drift

This is a measure of the change in temperature error with the passage of time. It is expressed in degrees Celsius. The concept of long term stability has been used for many years to describe by what amount an IC's parameter would shift during its lifetime. This is a concept that has been typically applied to both voltage references and monolithic temperature sensors. Unfortunately, integrated circuits cannot be evaluated at room temperature (25°C) for 10 years or so to determine this shift. As a result, manufacturers very typically perform accelerated lifetime testing of integrated circuits by operating ICs at elevated temperatures (between 125°C and 150°C) over a shorter period of time (typically between 500 and 1000 hours). As a result of this operation, the lifetime of an integrated circuit is significantly accelerated due to the increase in rates of reaction within the semiconductor material.

DC Power Supply Rejection Ratio (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC. It is expressed in μV.

Reference Feedthrough

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{LDAC}$ is high). It is expressed in decibels.

Channel-to-Channel Isolation

This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in decibels.

Major-Code Transition Glitch Energy

Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011…11 to 100…00 or 100...00 to 011…11).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device but is measured when the DAC is not being written to. It is specified in nV-s and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s or vice versa.

Digital Crosstalk

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{LDAC}$ high. Pulse $\overline{LDAC}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

Round Robin

This term is used to describe the ADT7316/ADT7317/ADT7318 cycling through the available measurement channels in sequence, taking a measurement on each channel.

DAC Output Settling Time

This is the time required, following a prescribed data change, for the output of a DAC to reach and remain within ±0.5 LSB of the final value. A typical prescribed change is from 1/4 scale to 3/4 scale.

TYPICAL PERFORMANCE CHARACTERISTICS
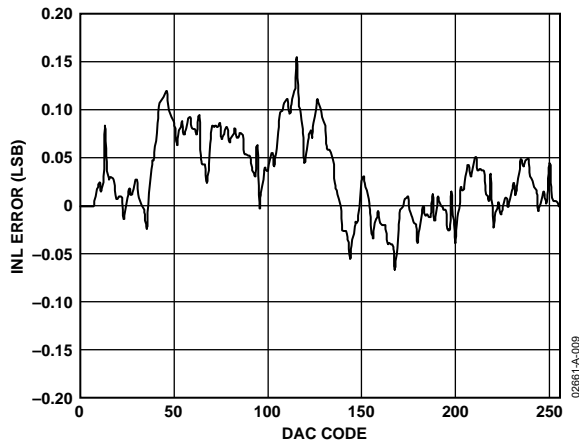
Figure 10. ADT7318 Typical INL Plot
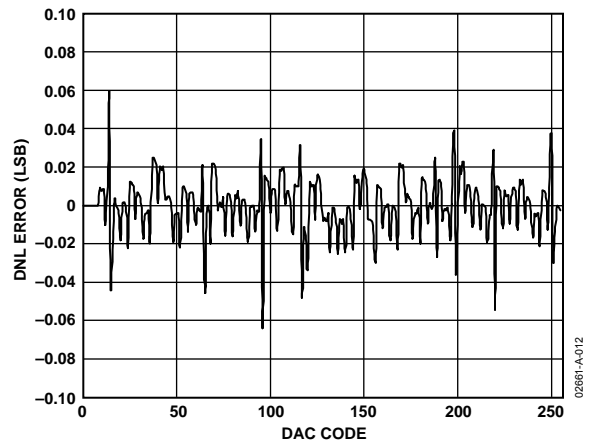
Figure 13. ADT7318 Typical DNL Plot
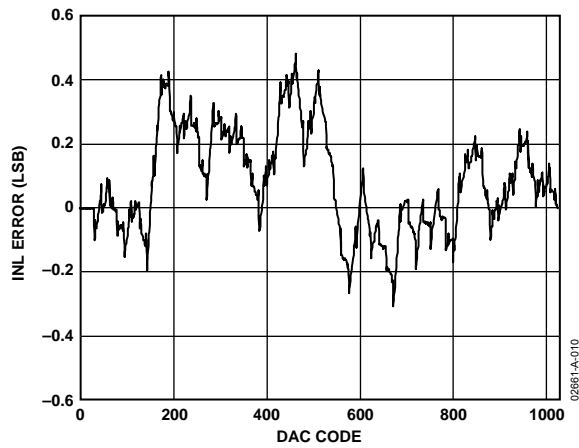
Figure 11. ADT7317 Typical INL Plot
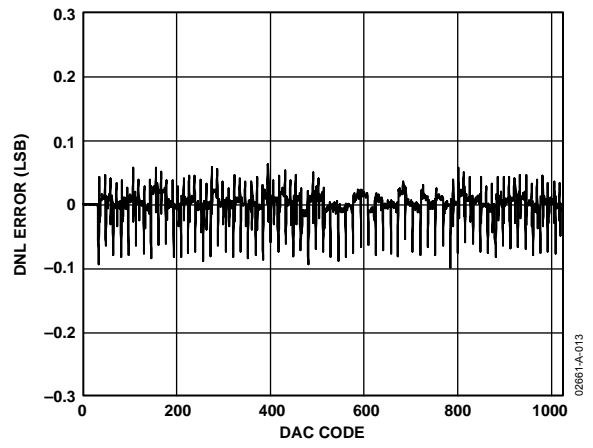
Figure 14. ADT7317 Typical DNL Plot
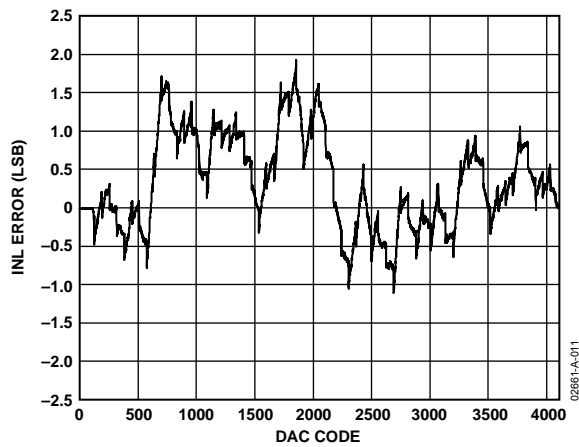
Figure 12. ADT7316 Typical INL Plot
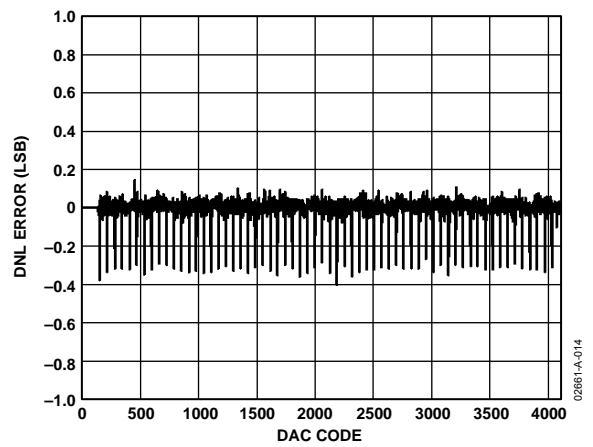
Figure 15. ADT7316 Typical DNL Plot
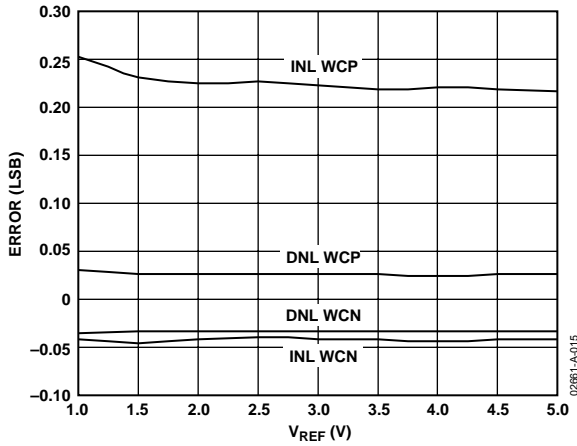
Figure 16. ADT7318 INL Error and DNL Error vs. V_REF

Figure 17. ADT7318 INL Error and DNL Error vs. Temperature

Figure 18. Offset Error and Gain Error vs. Temperature

Figure 19. Offset Error and Gain Error vs. V_DD

Figure 20. V_OUT Source and Sink Current Capability
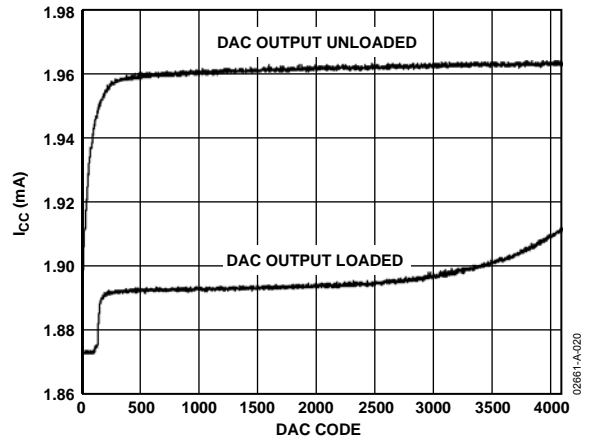
Figure 21. Supply Current vs. DAC Code
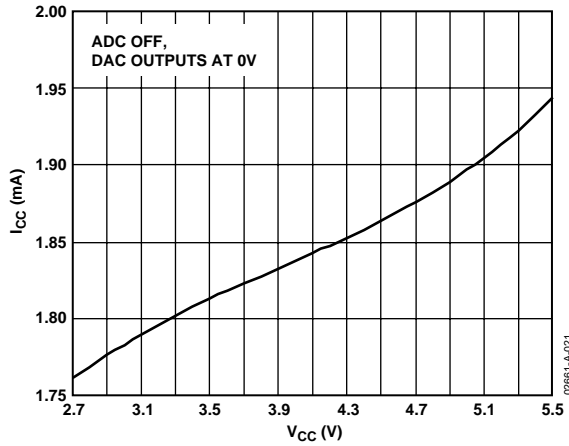
Figure 22. Supply Current vs. Supply Voltage @25℃

Figure 23. Power-Down Current vs. Supply Voltage @ 25℃

Figure 24. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

Figure 25. Exiting Power-Down to Midscale

Figure 26. ADT7316 Major-Code Transition Glitch Energy—0….11 to 100…00
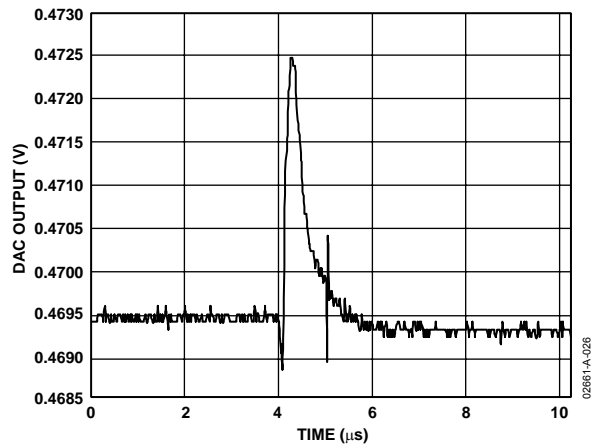
Figure 27. ADT7316 Major-Code Transition Glitch Energy—100…00 to 011…11
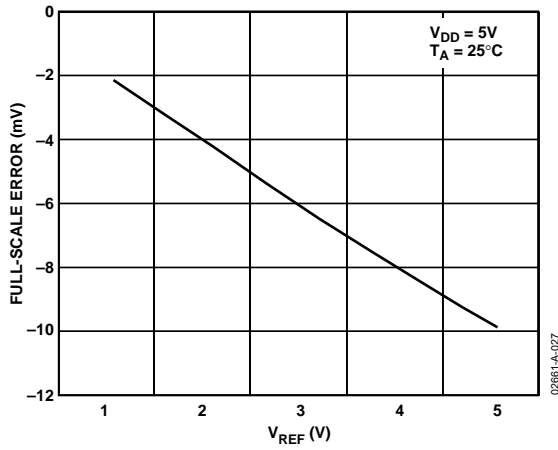
Figure 28. Full-Scale Error vs. V_{REF}
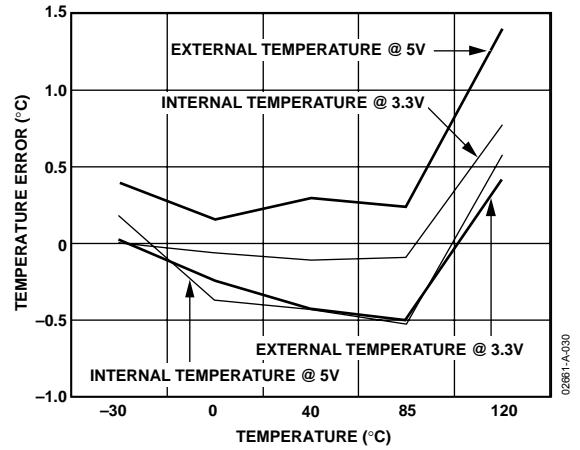
Figure 31. Temperature Error @ 3.3 V and 5 V
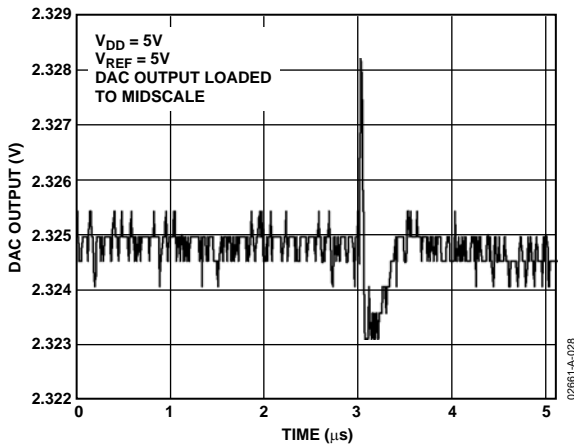
Figure 29. DAC-to-DAC Crosstalk
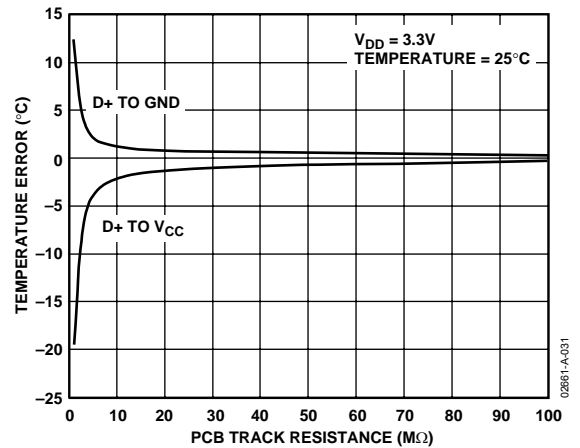
Figure 32. External Temperature Error vs. PCB Track Resistance
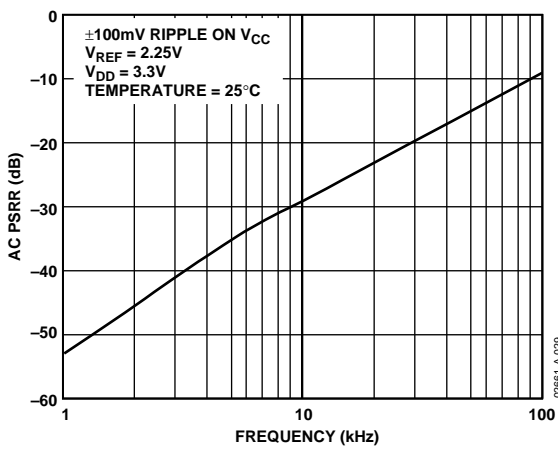
Figure 30. PSRR vs. Supply Ripple Frequency
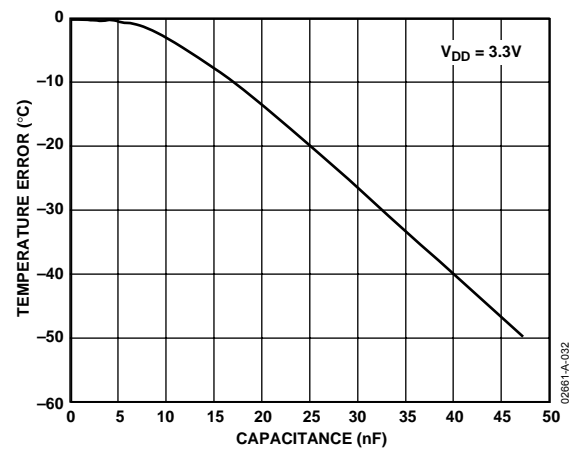
Figure 33. External Temperature Error vs. Capacitance Between D+ and D−
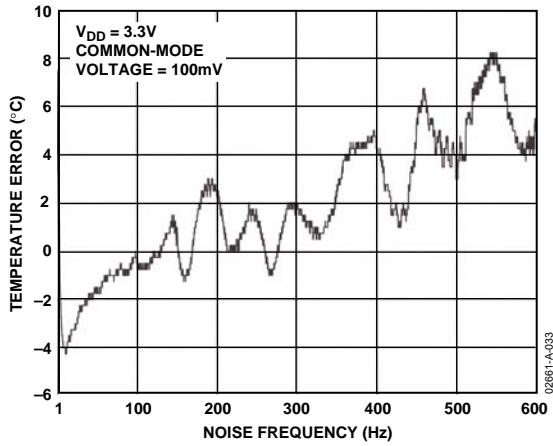
Figure 34. External Temperature Error vs. Common-Mode Noise Frequency

Figure 35. External Temperature Error vs. Differential-Mode Noise Frequency

Figure 36. Internal Temperature Error vs. Power Supply Noise Frequency

Figure 37. Temperature Sensor Response to Thermal Shock

Figure 38. Multiplying Bandwidth (Small-Signal Frequency Response)

THEORY OF OPERATION

Directly after the power-up calibration routine, the ADT7316/ ADT7317/ADT7318 go into idle mode. In this mode, the device is not performing any measurements and is fully powered up. All four DAC outputs are at 0 V.

To begin monitoring, write to Control Configuration 1 register (Address = 18h), and set Bit C0 = 1. The ADT7316/ADT7317/ ADT7318 go into their power-up default measurement mode, which is round robin. The device proceeds to take measurements on the V_{DD} channel, the internal temperature sensor channel, and the external temperature sensor channel. Once it finishes taking measurements on the external temperature sensor channel, the device immediately loops back to start taking measurements on the V_{DD} channel and repeats the same cycle as before. This loop continues until the monitoring is stopped by resetting Bit C0 of Control Configuration 1 register to 0.

It is also possible to continue monitoring as well as switching to single-channel mode by writing to Control Configuration 2 register (Address = 19h) and setting Bit C4 = 1. Further explanation of the single-channel and round robin measurement modes are given in later sections. All measurement channels have averaging enabled on power-up. Averaging forces the device to take an average of 16 readings before giving a final measured result. To disable averaging and consequently decrease the conversion time by a factor of 16, set C5 = 1 in Control Configuration 2 register.

Controlling the DAC outputs can be done by writing to the DAC's MSB and LSB registers (Addresses 10h to 17h). The power-up default setting is to have a low going pulse on the LDAC pin controlling the updating of the DAC outputs from the DAC registers. Alternatively, users can configure the updating of the DAC outputs to be controlled by means other than the LDAC pin by setting C3 = 1 of the Control Configuration 3 register (Address = 1Ah). The DAC Configuration register (Address = 1Bh), and the LDAC Configuration register (Address = 1Ch) can now be used to control the DAC updating. These two registers also control the output range of the DACs, enabling or disabling the external reference buffer, and selecting between the internal or external reference. DAC A and DAC B outputs can be configured to give a voltage output proportional to the temperature of the internal and external temperature sensors, respectively.

The dual-serial interface defaults to the I²C protocol on power-up. To select and lock in the SPI protocol, follow the selection process as described in the Serial Interface Selection section. The I²C protocol cannot be locked in, while the SPI protocol,

when selected, is automatically locked in. The interface can only be switched back to be I²C when the device is powered off and on. When using I²C, the $\overline{CS}$ pin should be tied to either V_{DD} or GND.

There are a number of different operating modes on the ADT7316/ADT7317/ADT7318 devices, and all of them can be controlled by the configuration registers. These features consist of enabling and disabling interrupts, polarity of the INT/$\overline{INT}$ pin, enabling and disabling the averaging on the measurement channels, SMBus timeout, and software reset.

POWER-UP CALIBRATION

It is recommended that no communication to the part is initiated until approximately 5 ms after V_{DD} has settled to within 10% of its final value. It is generally accepted that most systems take a maximum of 50 ms to power-up. Power-up time is directly related to the amount of decoupling on the voltage supply line.
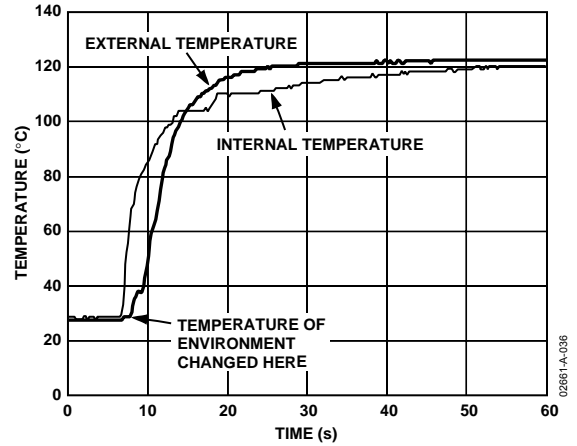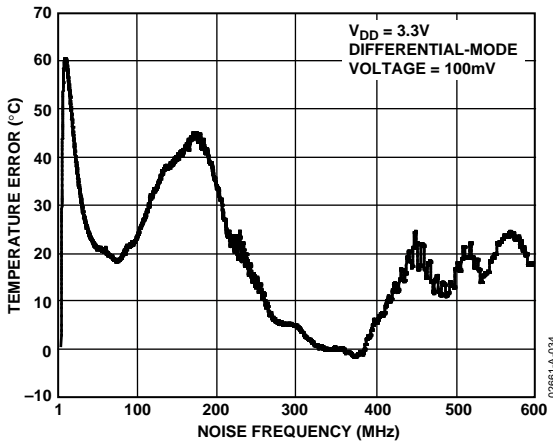
During this 5 ms after V_{DD} has settled, the part is performing a calibration routine, and any communication to the device will interrupt this routine and could cause erroneous temperature measurements. If it is not possible to have V_{DD} at its nominal value by the time 50 ms has elapsed, or that communication to the device has started prior to V_{DD} settling, then it is recommended that a measurement be taken on the V_{DD} channel before a temperature measurement is taken. The V_{DD} measurement is used to calibrate out any temperature measurement error due to different supply voltage values.

CONVERSION SPEED

The internal oscillator circuit used by the ADC has the capability to output two different clock frequencies. This means that the ADC is capable of running at two different speeds when performing a conversion on a measurement channel. Thus the time taken to perform a conversion on a channel can be reduced by setting C0 of Control Configuration 3 register (Address 1Ah). This increases the ADC clock speed from 1.4 kHz to 22 kHz. At the higher clock speed, the analog filters on the D+ and D− input pins (external temperature sensor) are switched off. This is why the power-up default setting is to have the ADC working at the slow speed. The typical times for fast and slow ADC speeds are given in the specification pages.

The ADT7316/ADT7317/ADT7318 power up with averaging on. This means every channel is measured 16 times and internally averaged to reduce noise. The conversion time can also be sped up by turning the averaging off by setting Bit C5 of Control Configuration 2 register (Address = 19h) to a 1.

FUNCTIONAL DESCRIPTION—VOLTAGE OUTPUT

DIGITAL-TO-ANALOG CONVERTERS

The ADT7316/ADT7317/ADT7318 have four resistor-string DACs fabricated on a CMOS process, with resolutions of 12, 10, and 8 bits, respectively. They contain four output buffer amplifiers, and are written to via an I²C serial interface or an SPI serial interface. See the Serial Interface Selection section for more information.

The ADT7316/ADT7317/ADT7318 operate from a single supply of 2.7 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/μs. DACs A and B share a common external reference input, namely V_{REF}-AB. DACs C and D share a common external reference input, namely V_{REF}-CD. Each reference input may be buffered to draw virtually no current from the reference source or unbuffered to give a reference input range from GND to V_{DD}. The devices have a power-down mode in which all DACs may be turned off completely with a high impedance output.

Each DAC output will not be updated until it receives the LDAC command. Therefore, while the DAC registers would have been written to with a new value, this value will not be represented by a voltage output until the DACs have received the LDAC command. Reading back from any DAC register prior to issuing an LDAC command will result in the digital value that corresponds to the DAC output voltage. Therefore, the digital value written to the DAC register cannot be read back until after the LDAC command has been initiated. This LDAC command can be given by either pulling the $\overline{LDAC}$ pin low (falling edge loads DACs), setting up Bits D4 and D5 of DAC Configuration register (Address = 1Bh), or using the LDAC register (Address = 1Ch).

When using the $\overline{LDAC}$ pin to control DAC register loading, the low going pulse width should be 20 ns minimum. The $\overline{LDAC}$ pin has to go high and low again before the DAC registers can be reloaded.
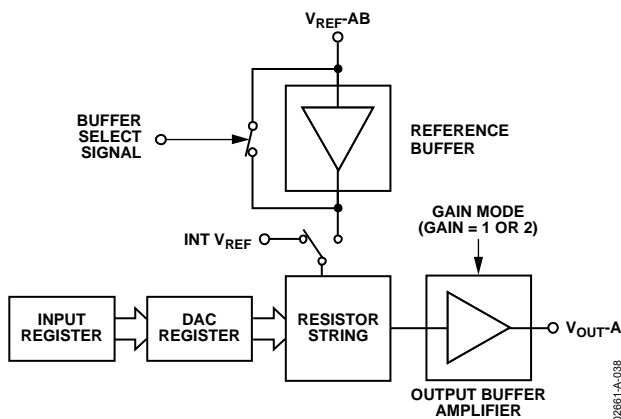
Figure 39. Single DAC Channel Architecture

DIGITAL-TO-ANALOG SECTION

The architecture of a DAC channel consists of a resistor string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin or the on-chip reference of 2.28 V provides the reference voltage for the corresponding DAC. Figure 39 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:

D = the decimal equivalent of the binary code that is loaded to the DAC register:

0–255 for ADT7318 (8 bits)
0–1023 for ADT7317 (10 bits)
0–4095 for ADT7316 (12 bits)
N = the DAC resolution

RESISTOR STRING

The resistor string section is shown in Figure 40. It is simply a string of resistors, each of value 603 Ω approximately. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.
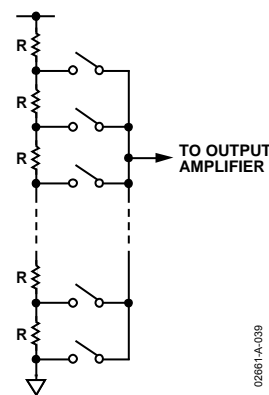
Figure 40. Resistor String

DAC EXTERNAL REFERENCE INPUTS

There is a reference pin for each pair of DACs. The reference inputs are buffered, but can also be individually configured as unbuffered.

The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However, if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V_{DD}, since there is no restriction due to headroom and footroom of the reference amplifier.

If there is a buffered reference in the circuit, there is no need to use the on-chip buffers. In unbuffered mode, the input impedance is still large at typically 90 kΩ per reference input for 0 V to V_{REF} output mode and 45 kΩ for 0 V to 2 V_{REF} output mode.

The buffered/unbuffered option is controlled by the DAC Configuration register (Address 1Bh, see Registers section). The LDAC Configuration register controls the option to select between internal and external voltage references. The default setting is for external reference selected.
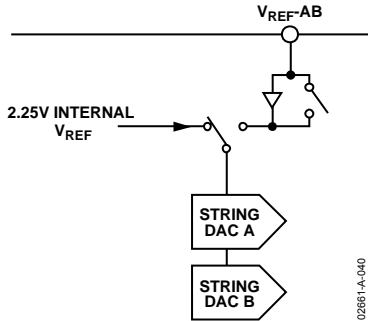
Figure 41. DAC Reference Buffer Circuit

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, gain and offset error.

If a gain of 1 is selected (Bits 0–3 of DAC Configuration register = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (Bits 0–3 of DAC Configuration register = 1), the output range is 0.001 V to $2V_{REF}$. Because of clamping, however, the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 4.7 kΩ to V_{DD} or 4.7 kΩ to GND in parallel with 200 pF to GND (see Figure 6). The source and sink capabilities of the output amplifier can be seen in the plot in Figure 20.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 µs.

THERMAL VOLTAGE OUTPUT

The ADT7316/ADT7317/ADT7318 are capable of outputting voltages that are proportional to temperature. DAC A output can be configured to represent the temperature of the internal sensor while DAC B output can be configured to represent the external temperature sensor. Bits C5 and C6 of Control Configuration 3 register select the temperature proportional to output voltage. Each time a temperature measurement is taken the DAC output is updated. The output resolution for the ADT7318 is 8 bits with the 1°C change corresponding to the one LSB change. The output resolution for the ADT7316 and ADT7317 is capable of 10 bits with a 0.25°C change corresponding to the 1 LSB change
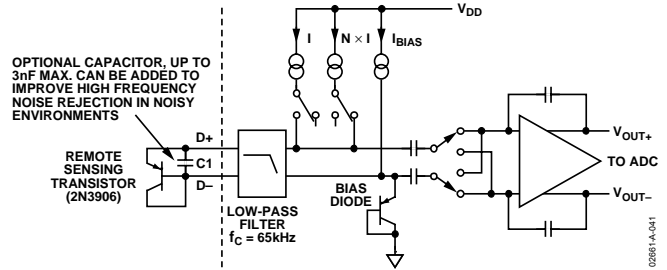
Figure 42. Signal Conditioning for External Diode Temperature Sensors

The default output resolution for the ADT7316 and ADT7317 is 8 bits. To increase this to 10 bits, set C1 = 1 of Control Configuration 3 register. The default output range is 0 V to V_{REF}-AB, and this can be increased to 0 V to 2 V_{REF}-AB. The user can select the internal V_{REF} (V_{REF} = 2.28 V) by setting D4 = 1 in the LDAC Configuration register (Address 1Ch). Increasing the output voltage span to 2 V_{REF} can be done by setting D0 = 1 for DAC A (internal temperature sensor), and D1 = 1 for DAC B (external temperature sensor) in DAC Configuration register (Address 1Bh).

The output voltage is capable of tracking a maximum temperature range of −128°C to +127°C, but the default setting is −40°C to +127°C. If the output voltage range is 0 V to V_{REF}-AB (V_{REF}-AB = 2.25 V), then this corresponds to 0 V representing −40°C, and 1.48 V representing +127°C. This of course will give an upper dead band between 1.48 V and V_{REF}-AB.

The internal and external analog temperature offset registers can be used to vary this upper dead band and consequently the temperature that 0 V corresponds to. Table 6 and Table 7 give examples of how this is done using a DAC output voltage span of V_{REF} and 2 V_{REF}, respectively. Simply write in the temperature value, in twos complement format, at which 0 V is to start. For example, if using the DAC A output with 0 V to start at −40°C, program D8h into the internal analog temperature offset register (Address 21h). This is an 8-bit register and thus only has a temperature offset resolution of 1°C for all device models. Use the following formulas to determine the value to program into the offset registers.

Negative temperatures:

$$Offset\ Register\ Code\ (d) = (0\ V\ Temp) + 128$$

where:

D7 of Offset Register Code is set to 1 for negative temperatures.

Example:

$$Offset\ Register\ Code\ (d) = (-40) + 128 = 88d = 58h$$

Since a negative temperature has been input into the equation, DB7 (MSB) of the Offset Register Code is set to a '1'. Therefore, 58h becomes D8h.

$$58h + DB7\ (1) = D8h$$

Positive temperatures:

$$Offset\ Register\ Code\ (d) = 0\ V\ Temp$$

Example:

$$Offset\ Register\ Code\ (d) = 10d = 0Ah$$

The following equation is used to work out the various temperatures for the corresponding 8-bit DAC output:

$$8 - Bit\ Temp = (DAC\ O/P \div 1 LSB) + (0\ V\ Temp)$$

For example, if the output is 1.5 V, V_{REF}-AB = 2.25 V, 8-bit DAC has an LSB size = 2.25 V/256 = 8.79×10^{-3}, and 0 V temp is at −128°C, then the resultant temperature is

$$(1.5 \div 8.79 \times 10^{-3}) + (-128) = +43°C$$

The following equation is used to work out the various temperatures for the corresponding 10-bit DAC output

$$10 - Bit\ Temp = ((DAC\ O/P \div 1\ LSB) \times 0.25) + (0\ V\ Temp)$$

For example, if the output is 0.4991 V, V_{REF}-AB = 2.25 V, 10-bit DAC has an LSB size = 2.25 V/1024 = 2.197×10-3, and 0 V temp is at −40°C, then the resultant temperature works out to be

$$((0.4991 \div 2.197 \div 10^{-3}) \times 0.25) + (-40) + 16.75°C$$

Table 6. Thermal Voltage Output (0 V to V_{REF}-AB)

O/P Voltage (V)	Default (°C)	Max (°C)	Sample (°C)
0	−40	−128	0
0.5	+17	−71	+56
1	+73	−15	+113
1.12	+87	−1	+127
1.47	+127	+39	UDB[1]
1.5	UDB[1]	+42	UDB[1]
2	UDB[1]	+99	UDB[1]
2.25	UDB[1]	+127	UDB[1]

Table 7. Thermal Voltage Output (0 V to 2 V_{REF}-AB)

O/P Voltage (V)	Default (°C)	Max (°C)	Sample (°C)
0	−40	−128	0
0.25	−26	−114	+14
0.5	+12	−100	+28
0.75	+3	−85	+43
1	+17	−71	+57
1.12	+23	−65	+63
1.47	+43	−45	+83
1.5	+45	−43	+85
2	+73	−15	+113
2.25	+88	0	+127
2.5	+102	+14	UDB[1]
2.75	+116	+28	UDB[1]
3	UDB[1]	+42	UDB[1]
3.25	UDB[1]	+56	UDB[1]
3.5	UDB[1]	+70	UDB[1]
3.75	UDB[1]	+85	UDB[1]
4	UDB[1]	+99	UDB[1]
4.25	UDB[1]	+113	UDB[1]
4.5	UDB[1]	+127	UDB[1]

Figure 43 shows DAC output versus temperature for a V_{REF}-AB= 2.25 V.
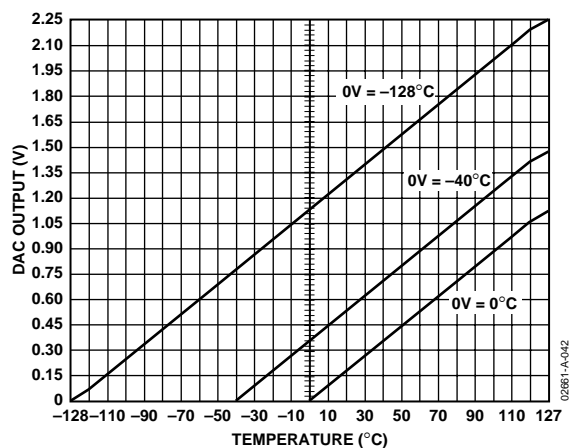
Figure 43. 10-DAC Output vs. Temperature, V_{REF}-AB = 2.25 V

[1] Upper dead band has been reached. DAC output is not capable of increasing (see Figure 3).

FUNCTIONAL DESCRIPTION—MEASUREMENT

TEMPERATURE SENSOR

The ADT7316/ADT7317/ADT7318 contain an ADC with special input signal conditioning to enable operation with external and on-chip diode temperature sensors. When the ADT7316/ADT7317/ADT7318 are operating in single-channel mode, the ADC continually processes the measurement taken on one channel only. This channel is preselected by Bits C0 and C1 in Control Configuration 2 register (Address 19h). When in round robin mode, the analog input multiplexer sequentially selects the V_{DD} input channel, the on-chip temperature sensor to measure its internal temperature, and the external temperature sensor. These signals are digitized by the ADC and the results stored in the various value registers.

The measured results are compared with the internal and external, T_{HIGH} and T_{LOW}, limits. These temperature limits are stored in on-chip registers. If the temperature limits are not masked out, any out-of-limit comparisons generate flags that are stored in the Interrupt Status 1 register. One or more out-of-limit results will cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting.

Theoretically, the temperature measuring circuit can measure temperatures from −128°C to +127°C with a resolution of 0.25°C. Temperatures outside T_A, however, are outside the guaranteed operating temperature range of the device. Temperature measurement from −128°C to +127°C is possible using an external sensor.

Temperature measurement is initiated by three methods. The first method is applicable when the part is in single-channel measurement mode. The temperature is measured 16 times and internally averaged to reduce noise. In single-channel mode, the part is continuously monitoring the selected channel, i.e., as soon as one measurement is taken then another one is started on the same channel. The total time to measure a temperature channel with the ADC operating at slow speed is typically 11.4 ms (712 μs × 16) for the internal temperature sensor, and 24.22 ms (1.51 ms × 16) for the external temperature sensor. The new temperature value is stored in two 8-bit registers and ready for reading by the I²C or SPI interface. The user has the option of disabling the averaging by setting a bit (Bit 5) in the Control Configuration 2 register (Address 19h). The ADT7316/ADT7317/ADT7318 default on power-up, with the averaging enabled.

The second method is applicable when the part is in round robin measurement mode. The part measures both the internal and external temperature sensors as it cycles through all possible measurement channels. The two temperature channels are measured each time the part runs a round robin sequence. In round robin mode, the part is continuously measuring all channels.

Temperature measurement is also initiated after every read or write to the part when the part is in either single-channel measurement mode or round robin measurement mode. Once serial communication has started, any conversion in progress is stopped and the ADC reset. Conversion will start again immediately after the serial communication has finished. The temperature measurement proceeds normally as described above.

V_{DD} MONITORING

The ADT7316/ADT7317/ADT7318 also have the capability of monitoring their own power supplies. The parts measure the voltage on their V_{DD} pin to a resolution of 10 bits. The resultant value is stored in two 8-bit registers, the 2 LSBs stored in Register Address 03h and the 8 MSBs are stored in Register Address 06h. This allows the user to have the option of just doing a one byte read if 10-bit resolution is not important. The measured result is compared with V_{HIGH} and V_{LOW} limits. If the V_{DD} interrupt is not masked out, any out-of-limit comparison generates a flag in Interrupt Status 2 register and one or more out-of-limit results will cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting.

Measuring the voltage on the V_{DD} pin is regarded as monitoring a channel. Therefore, along with the internal and external temperature sensors, the V_{DD} voltage makes up the third and final monitoring channel. The user can select the V_{DD} channel for single-channel measurement by setting Bit C4 = 1 and setting Bits C0 to C2 to all 0s in Control Configuration 2 register.

When measuring the V_{DD} value, the reference for the ADC is sourced from the internal reference. Table 8 shows the data format. As the maximum V_{DD} voltage measurable is 7 V, internal scaling is performed on the V_{DD} voltage to match the 2.28 V internal reference value. Below is an example of how the transfer function works.

$V_{DD} = 5\ V$

$ADC\ Reference = 2.28\ V$

$1\ LSB = ADC\ Reference/2^{10} = 2.28/1024 = 2.226\ mV$

$Scale\ Factor = Full\text{-}Scale\ V_{CC}/ADC\ Reference = 7/2.28 = 3.07$

$Conversion\ Result = V_{DD}/(Scale\ Factor \times LSB\ Size)$

$= 5/(3.07 \times 2.226\ mV)$

$= 2DBh$

Table 8. V$_{DD}$ Data Format, V$_{REF}$ = 2.28 V

V$_{DD}$ Value (V)	Digital Output	
	Binary	Hex
2.5	01 0110 1110	16E
3.0	01 1011 0111	1B7
3.5	10 0000 0000	200
4.0	10 0100 1001	249
4.5	10 1001 0010	292
5.0	10 1101 1100	2DC
5.5	11 0010 0101	325
6.0	11 0110 1110	36E
6.5	11 1011 0111	3B7
7.0	11 1111 1111	3FF

ON-CHIP REFERENCE

The ADT7316/ADT7317/ADT7318 has an on-chip 1.2 V band gap reference that is gained up by a switched capacitor amplifier to give an output of 2.28 V. The amplifier is powered up for the duration of the device monitoring phase and is powered down once monitoring is disabled. This saves on current consumption. The internal reference is used as the reference for the ADC. The ADC is used for measuring V$_{DD}$ and the internal and external temperature sensors. The internal reference is always used when measuring V$_{DD}$, and the internal and external temperature sensors. The external reference is the default power-up reference for the DACs.

ROUND ROBIN MEASUREMENT

On power-up, the ADT7316/ADT7317/ADT7318 go into round robin mode, but monitoring is disabled. Setting Bit C0 of Configuration Register 1 to a 1 enables conversions. It sequences through the three channels of V$_{DD}$, internal temperature sensor, and external temperature sensor and takes a measurement from each. Once the conversion is completed on the external temperature sensor, the device loops around for another measurement cycle on all three channels. This method of taking a measurement on all three channels in one cycle is called round robin. Setting Bit 4 of Control Configuration 2 (Address 19h) disables the round robin mode and in turn sets up the single-channel mode. The single-channel mode is where only one channel, e.g., internal temperature sensor, is measured in each conversion cycle.

The time taken to monitor all channels will normally not be of interest, since the most recently measured value can be read at any time.

For applications where the round robin time is important, typical times at 25°C are given in the specification pages.
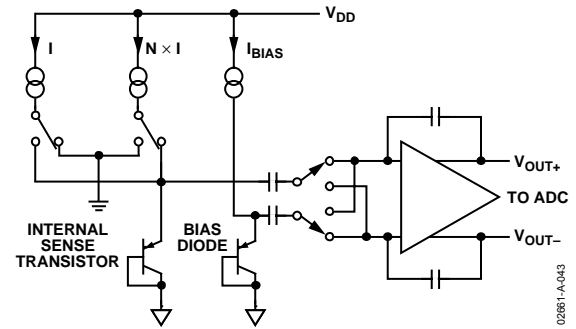
Figure 44. Top Level Structure of Internal Temperature Sensors

SINGLE-CHANNEL MEASUREMENT

Setting C4 of Control Configuration 2 register enables the single-channel mode and allows the ADT7316/ADT7317/ADT7318 to focus on one channel only. A channel is selected by writing to Bits C0:C1 in Control Configuration 2 register. For example, to select the V$_{DD}$ channel for monitoring, write to the Control Configuration 2 register and set C4 to 1 (if not done so already), then write all 0s to Bits C0 to C1. All subsequent conversions will be done on the V$_{DD}$ channel only. To change the channel selection to the internal temperature channel, write to the Control Configuration 2 register and set C0 = 1. When measuring in single-channel mode, conversions on the channel selected occur directly after each other. Any communication to the ADT7316/ADT7317/ADT7318 stops the conversions, but they are restarted once the read or write operation is completed.

TEMPERATURE MEASUREMENT METHOD
Internal Temperature Measurement

The ADT7316/ADT7317/ADT7318 contain an on-chip band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the internal temperature value register. As both positive and negative temperatures can be measured, the temperature data is stored in twos comple-ment format, as shown in Table 9. The thermal characteristics of the measurement sensor could change, and therefore an offset is added to the measured value to enable the transfer function to match the thermal characteristics. This offset is added before the temperature data is stored. The offset value used is stored in the internal temperature offset register.

External Temperature Measurement

The ADT7316/ADT7317/ADT7318 can measure the temperature of one external diode sensor or diode-connected transistor.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V$_{BE}$ varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production.

The technique used in the ADT7316/ADT7317/ADT7318 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by

$$\Delta V_{BE} = KT/q \times In(N)$$

where:

K is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

Figure 42 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a discrete substrate transistor. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base to the D+ input.

We recommend that a 2N3906 be used as the external transistor.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a low-pass filter to remove noise, then to a chopper stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

TEMPERATURE VALUE FORMAT

One LSB of the ADC corresponds to 0.25°C. The ADC can theoretically measure a temperature span of 255°C. The internal temperature sensor is guaranteed to a low value limit of −40°C. It is possible to measure the full temperature span using the external temperature sensor. The temperature data format is shown in Table 9. The result of the internal or external temperature measurements is stored in the temperature value registers and is compared with limits programmed into the internal or external high and low registers.

Table 9. Temperature Data Format (Internal and External Temperature)

Temperature	Digital Output DB9..........DB0
−40°C	11 0110 0000
−25°C	11 1001 1100
−10°C	11 1101 1000
−0.25°C	11 1111 1111
0°C	00 0000 0000
0.25°C	00 0000 0001
10°C	00 0010 1000
25°C	00 0110 0100
50°C	00 1100 1000
75°C	01 0010 1100
100°C	01 1001 0000
105°C	01 1010 0100
125°C	01 1111 0100

Temperature Conversion Formula:

Positive Temperature = ADC Code/4

Negative Temperature = (ADC Code* – 512)/4

*DB9 is removed from the ADC code.
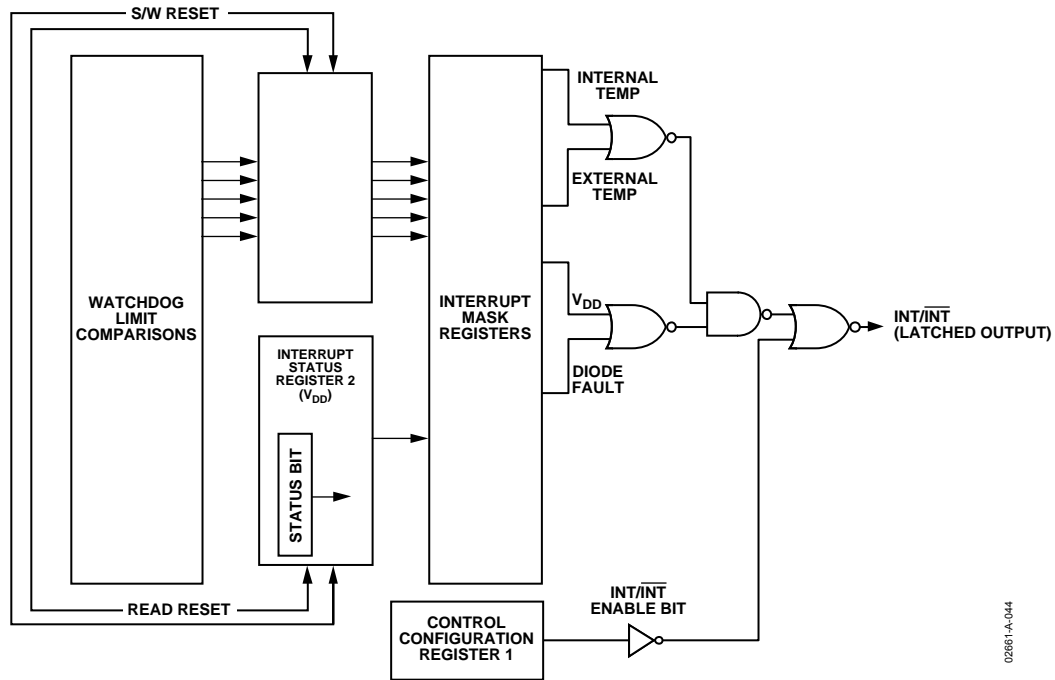
Figure 45. ADT7316/ADT7317/ADT7318 Interrupt Structure

INTERRUPTS

The measured results from the internal temperature sensor, external temperature sensor, and the V_{DD} pin are compared with the T_{HIGH}/V_{HIGH} (greater than comparison) and T_{LOW}/V_{LOW} (less than or equal to comparison) limits. An interrupt occurs if the measurement exceeds or equals the limit registers. These limits are stored in on-chip registers. Note that the limit registers are 8 bits long, while the conversion results are 10 bits long. If the limits are not masked out, then any out-of-limit comparisons generate flags that are stored in Interrupt Status 1 register (Address = 00h) and Interrupt Status 2 register (Address = 01h).

One or more out-of-limit results will cause the INT/$\overline{INT}$ output to pull either high or low depending on the output polarity setting. It is good design practice to mask out interrupts for channels that are of no concern to the application.

Figure 45 shows the interrupt structure for the ADT7316/ ADT7317/ ADT7318. It gives a block diagram representation of how the various measurement channels affect the INT/$\overline{INT}$ pin.

REGISTERS

The ADT7316/ADT7317/ADT7318 contain registers that are used to store the results of external and internal temperature measurements, V_{DD} value measurements, high and low temperature and supply voltage limits. They also set output DAC voltage levels, configure multipurpose pins, and generally control the device. A description of these registers follows.

The register map is divided into registers of 8 bits. Each register has its own individual address, but some consist of data that is linked with other registers. These registers hold the 10-bit conversion results of measurements taken on the temperature and V_{DD} channels. For example, the 8 MSBs of the V_{DD} measurement are stored in Register Address 06h, while the 2 LSBs are stored in Register Address 03h. The link involved between these types of registers is that when the LSB register is read first then the MSB registers associated with that LSB register are locked out to prevent any updates. To unlock these MSB registers, the user has only to read any one of them, which will have the effect of unlocking all previously locked out MSB registers. So for the example given above, if Register 03h was read first, then MSB Registers 06h and 07h would be locked out to prevent any updates to them. If Register 06h was read, then this register and Register 07h would be subsequently unlocked.
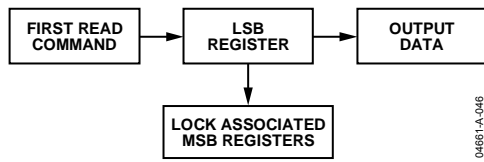
Figure 46. Phase 1 of 10-Bit Read
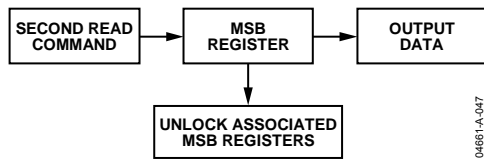
Figure 47. Phase 2 of 10-Bit Read

If an MSB register is read first, its corresponding LSB register is not locked out, leaving the user with the option of just reading back 8 bits (MSB) of a 10-bit conversion result. Reading an MSB register first does not lock out other MSB registers, and likewise, reading an LSB register first does not lock out other LSB registers.

Table 10. List of ADT7316/ADT7317/ADT7318 Registers

RD/WR Address	Name	Power-On Default
00h	Interrupt Status 1	00h
01h	Interrupt Status 2	00h
02h	Reserved	00h
03h	Internal Temp and V_{DD} LSBs	00h
04h	External Temp LSBs	00h
05h	Reserved	00h
06h	V_{DD} MSBs	xxh
07h	Internal Temp MSBs	00h
08h	External Temp MSBs	00h
09h–0Fh	Reserved	00h
10h	DAC A LSBs (ADT7316/ADT7317 only)	00h
11h	DAC A MSBs	00h
12h	DAC B LSBs (ADT7316/ADT7317 only)	00h
13h	DAC B MSBs	00h
14h	DAC C LSBs (ADT7316/ADT7317 only)	00h
15h	DAC C MSBs	00h
16h	DAC D LSBs (ADT7316/ADT7317 only)	00h
17h	DAC D MSBs	00h
18h	Control Configuration 1	00h
19h	Control Configuration 2	00h
1Ah	Control Configuration 3	00h
1Bh	DAC Configuration	00h
1Ch	LDAC Configuration	00h
1Dh	Interrupt Mask 1	00h
1Eh	Interrupt Mask 2	00h
1Fh	Internal Temp Offset	00h
20h	External Temp Offset	00h
21h	Internal Analog Temp Offset	D8h
22h	External Analog Temp Offset	D8h
23h	V_{DD} V_{HIGH} Limit	C7h
24h	V_{DD} V_{LOW} Limit	62h
25h	Internal T_{HIGH} Limit	64h
26h	Internal T_{LOW} Limit	C9h
27h	External T_{HIGH} Limit	FFh
28h	External T_{LOW} Limit	00h
29h–4Ch	Reserved	
4Dh	Device ID	01h/09h/05h
4Eh	Manufacturer's ID	41h
4Fh	Silicon Revision	04h
50h–7Eh	Reserved	00h
7F	SPI Lock Status	00h
80–FF	Reserved	00h

Interrupt Status 1 Register (Read-Only) [Add. = 00h]

This 8-bit read-only register reflects the status of some of the interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active. This register is reset by a read operation, provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 11. Interrupt Status 1 Register

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 12.

Bit	Function
D0	1 when internal temperature value exceeds T_{HIGH} limit. Any internal temperature reading greater than the limit set will cause an out-of-limit event.
D1	1 when internal temperature value exceeds T_{LOW} limit. Any internal temperature reading less than or equal to the limit set will cause an out-of-limit event.
D2	1 when external temperature value exceeds T_{HIGH} limit. The default value for this limit register is −1°C, so any external temperature reading greater than the limit set will cause an out-of-limit event.
D3	1 when external temperature value exceeds T_{LOW} limit. The default value for this limit register is 0°C, so any external temperature reading less than or equal to the limit set will cause an out-of-limit event.
D4	1 indicates a fault (open or short) for the external temperature sensor.

Interrupt Status 2 Register (Read-Only) [Add. = 01h]

This 8-bit read-only register reflects the status of the V_{DD} interrupt that can cause the INT/$\overline{\text{INT}}$ pin to go active. This register is reset by a read operation provided that any out-of-limit event has been corrected. It is also reset by a software reset.

Table 13. Interrupt Status 2 Register

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 14.

Bit	Function
D4	1 when V_{DD} value is greater than corresponding V_{HIGH} limit. 1 when V_{DD} is less than or equal to corresponding V_{LOW} limit.

Internal Temperature Value/V_{DD} Value Register LSBs (Read-Only) [Add. = 03h]

This 8-bit read-only register stores the 2 LSBs of the 10-bit temperature reading from the internal temperature sensor and the 2 LSBs of the 10-bit supply voltage reading.

Table 15. Internal Temperature/V_{DD} LSBs

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	V1	LSB	T1	LSB
N/A	N/A	N/A	N/A	0*	0*	0*	0*

*Default settings at power-up.

Table 16.

Bit	Function
D0	LSB of Internal Temperature Value.
D1	B1 of Internal Temperature Value.
D2	LSB of V_{DD} Value.
D3	B1 of V_{DD} Value.

External Temperature Value Register LSBs (Read-Only) [Add. = 04h]

This 8-bit read-only register stores the 2 LSBs of the 10-bit temperature reading from the external temperature sensor.

Table 17. External Temperature LSBs

D7	D6	D5	D4	D3	D2	D1	D0
N/A	N/A	N/A	N/A	N/A	N/A	T1	LSB
N/A	N/A	N/A	N/A	N/A	N/A	0*	0*

*Default settings at power-up.

Table 18.

Bit	Function
D0	LSB of External Temperature Value.
D1	B1 of External Temperature Value.

V_{DD} Value Register MSBs (Read-Only) [Add. = 06h]

This 8-bit read-only register stores the supply voltage value. The 8 MSBs of the 10-bit value are stored in this register.

Table 19. V_{DD} Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
V9	V8	V7	V6	V5	V4	V3	V2
X*	X*	x*	x*	x*	x*	x*	x*

*Loaded with V_{DD} value after power-up.

Internal Temperature Value Register MSBs (Read-Only) [Add. = 07h]

This 8-bit read-only register stores the internal temperature value from the internal temperature sensor in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 20. Internal Temperature Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

External Temperature Value Register MSBs (Read-Only) [Add. = 08h]

This 8-bit read-only register stores the external temperature value from the external temperature sensor in twos complement format. The 8 MSBs of the 10-bit value are stored in this register.

Table 21. External Temperature Value MSBs

D7	D6	D5	D4	D3	D2	D1	D0
T9	T8	T7	T6	T5	T4	T3	T2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

DAC A Register LSBs (Read/Write) [Add. = 10h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7316/ADT7317 DAC A word, respectively. The value in this register is combined with the value in the DAC A Register MSBs and converted to an analog voltage on the V_{OUT}-A pin. On power-up, the voltage output on the V_{OUT}-A pin is 0 V.

Table 22. DAC A (ADT7316) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 23. DAC A (ADT7317) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at power-up.

DAC A Register MSBs (Read/Write) [Add. = 11h]

This 8-bit read/write register contains the 8 MSBs of the DAC A word. The value in this register is combined with the value in the DAC A Register LSBs and converted to an analog voltage on the V_{OUT}-A pin. On power-up, the voltage output on the V_{OUT}-A pin is 0 V.

Table 24. DAC A MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

DAC B Register LSBs (Read/Write) [Add. = 12h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7316/ADT7317 DAC B word, respectively. The value in this register is combined with the value in the DAC B register MSBs and converted to an analog voltage on the V_{OUT}-B pin. On power-up, the voltage output on the V_{OUT}-B pin is 0 V.

Table 25. DAC B (ADT7316) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 26. DAC B (ADT7317) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at power-up.

DAC B Register MSBs (Read/Write) [Add. = 13h]

This 8-bit read/write register contains the 8 MSBs of the DAC B word. The value in this register is combined with the value in the DAC B register LSBs and converted to an analog voltage on the V_{OUT}-B pin. On power-up, the voltage output on the V_{OUT}-B pin is 0 V.

Table 27. DAC B MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

DAC C Register LSBs (Read/Write) [Add. = 14h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7316/ADT7317 DAC C word, respectively. The value in this register is combined with the value in the DAC C register MSBs and converted to an analog voltage on the V_{OUT}-C pin. On power-up, the voltage output on the V_{OUT}-C pin is 0 V.

Table 28. DAC C (ADT7316) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 29. DAC C (ADT7317) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at power-up.

DAC C Register MSBs (Read/Write) [Add. = 15h]

This 8-bit read/write register contains the 8 MSBs of the DAC C word. The value in this register is combined with the value in the DAC C register LSBs and converted to an analog voltage on the V_{OUT}-C pin. On power-up, the voltage output on the V_{OUT}-C pin is 0 V.

Table 30. DAC C MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

DAC D Register LSBs (Read/Write) [Add. = 16h]

This 8-bit read/write register contains the 4/2 LSBs of the ADT7316/ADT7317 DAC D word, respectively. The value in this register is combined with the value in the DAC D register MSBs and converted to an analog voltage on the V_{OUT}-D pin. On power-up, the voltage output on the V_{OUT}-D pin is 0 V.

Table 31. DAC D (ADT7316) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B3	B2	B1	LSB	N/A	N/A	N/A	N/A
0*	0*	0*	0*	N/A	N/A	N/A	N/A

*Default settings at power-up.

Table 32. DAC D (ADT7317) LSBs

D7	D6	D5	D4	D3	D2	D1	D0
B1	LSB	N/A	N/A	N/A	N/A	N/A	N/A
0*	0*	N/A	N/A	N/A	N/A	N/A	N/A

*Default settings at power-up.

DAC D Register MSBs (Read/Write) [Add. = 17h]

This 8-bit read/write register contains the 8 MSBs of the DAC D word. The value in this register is combined with the value in the DAC D register LSBs and converted to an analog voltage on the V_{OUT}-D pin. On power-up, the voltage output on the V_{OUT}-D pin is 0 V.

Table 33. DAC D MSBs

D7	D6	D5	D4	D3	D2	D1	D0
MSB	B8	B7	B6	B5	B4	B3	B2
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Control Configuration 1 Register (Read/Write) [Add. = 18h]

This configuration register is an 8-bit read/write register that is used to setup some of the operating modes of the ADT7316/ADT7317/ADT7318.

Table 34. Control Configuration 1

D7	D6	D5	D4	D3	D2	D1	D0
PD	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 35.

Bit	Function
C0	This bit enables/disables conversions in round robin and single-channel mode. ADT7316/ADT7317/ADT7318 power up in round robin mode but monitoring is not initiated until this bit is set. Default = 0. 0 = Stop Monitoring. 1 = Start Monitoring.
C1:4	Reserved. Only write 0s.
C5	0 = Enable INT/$\overline{INT}$ Output. 1 = Disable INT/$\overline{INT}$ Output.
C6	Configures INT/$\overline{INT}$ output polarity. 0 = Active Low. 1 =Active High.
PD	Power-down Bit. Setting this bit to 1 puts the ADT7316/ADT7317/ADT7318 into standby mode. In this mode, both ADC and DACs are fully powered down, but serial interface is still operational. To power up the part again, write a 0 to this bit.

Control Configuration 2 Register (Read/Write) [Add. = 19h]

This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7316/ADT7317/ADT7318.

Table 36. Control Configuration 2

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 37.

Bit	Function
C1:0	In single-channel mode, these bits select between V_{DD}, the internal temperature sensor, and the external temperature sensor for conversion. Default is V_{DD}. 00 = V_{DD}. 01 = Internal Temperature Sensor. 10 = External Temperature Sensor. 11 = Reserved.
C2:C3	Reserved.
C4	Selects between single-channel and round robin conversion cycle. Default is round robin. 0 = Round Robin. 1 = Single Channel.
C5	Default condition is to average every measurement on all channels 16 times. This bit disables this averaging. Channels affected are temperature and V_{DD}. 0 = Enable Averaging. 1 = Disable Averaging.
C6	SMBus timeout on the serial clock puts a 25 ms limit on the pulse width of the clock. Ensures that a fault on the master SCL does not lock up the SDA line. SMBus timeout. 0 = Disable. 1 = Enable SMBus Timeout.
C7	Software Reset. Setting this bit to a 1 causes a software reset. All registers and DAC outputs will reset to their default settings.

ADT7316/ADT7317/ADT7318

Control Configuration 3 Register (Read/Write) [Add. = 1Ah]
This configuration register is an 8-bit read/write register that is used to set up some of the operating modes of the ADT7316/ADT7317/ADT7318.

Table 38. Control Configuration 3

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 39.

Bit	Function
C0	Selects between fast and normal ADC conversion speeds for all three monitoring channels. 0 = ADC clock at 1.4 kHz. 1 = ADC clock at 22.5 kHz. D+ and D− analog filters are disabled.
C1	On the ADT7316 and ADT7317, this bit selects between 8-bits and 10-bits DAC output resolution on the thermal voltage output feature. Default = 8 bits. This bit has no effect on the ADT7318 output since this part has only an 8-bit DAC. In the ADT7318 case, write 0 to this bit. 0 = 8 Bits Resolution. 1 = 10 Bits Resolution.
C2	Reserved. Only write 0.
C3	0 = $\overline{\text{LDAC}}$ pin controls updating of DAC outputs. 1 = DAC configuration register and LDAC configuration register control the updating of the DAC outputs.
C4	Reserved. Only write 0.
C5	Setting this bit selects DAC A voltage output to be proportional to the internal temperature measurement.
C6	Setting this bit selects DAC B voltage output to be proportional to the external temperature measurement.
C7	Reserved. Only write 0.

DAC Configuration Register (Read/Write) [Add. = 1Bh]
This configuration register is an 8-bit read/write register that is used to control the output ranges of all four DACs and to control the loading of the DAC registers if the $\overline{\text{LDAC}}$ pin is disabled (Bit C3 = 1, Control Configuration 3 Register).

Table 40. DAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 41.

Bit	Function
D0	Selects the output range of DAC A. 0 = 0 V to V_{REF}. 1 = 0 V to 2 V_{REF}.
D1	Selects the output range of DAC B. 0 = 0 V to V_{REF}. 1 = 0 V to 2 V_{REF}.
D2	Selects the output range of DAC C. 0 = 0 V to V_{REF}. 1 = 0 V to 2 V_{REF}.
D3	Selects the output range of DAC D. 0 = 0 V to V_{REF}. 1 = 0 V to 2 V_{REF}.
D5:D4	00 MSB write to any DAC register will generate LDAC command, which updates that DAC only. 01 MSB write to DAC B or DAC D register will generate LDAC command, which updates DACs A, B or DACs C, D, respectively. 10 MSB write to DAC D register will generate LDAC command, which updates all 4 DACs. 11 LDAC command generated from LDAC register.
D6	Setting this bit allows the external V_{REF} to bypass the reference buffer when supplying DACs A and B.
D7	Setting this bit allows the external V_{REF} to bypass the reference buffer when supplying DACs C and D.

LDAC Configuration Register (Write-Only) [Add. = 1Ch]
This configuration register is an 8-bit write register that is used to control the updating of the quad DAC outputs if the $\overline{\text{LDAC}}$ pin is disabled and Bits D4 and D5 of DAC Configuration register are both set to 1. It also selects either the internal or external V_{REF} for all four DACs. Bits D0–D3 in this register are self clearing, i.e., reading back from this register will always give 0s for these bits.

Table 42. LDAC Configuration

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 43.

Bit	Function
D0	Writing a 1 to this bit will generate the LDAC command to update the DAC A output only.
D1	Writing a 1 to this bit will generate the LDAC command to update the DAC B output only.
D2	Writing a 1 to this bit will generate the LDAC command to update the DAC C output only.
D3	Writing a 1 to this bit will generate the LDAC command to update the DAC D output only.
D4	Selects either internal V_{REF} or external V_{REF}-AB for DACs A and B. 0 = External V_{REF}. 1 = Internal V_{REF}.
D5	Selects either internal V_{REF} or external V_{REF}-CD for DACs C and D. 0 = External V_{REF}. 1 = Internal V_{REF}.
D6:D7	Reserved. Only write 0s.

Interrupt Mask 1 Register (Read/Write) [Add. = 1Dh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active.

Table 44. Interrupt Mask 1

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 45.

Bit	Function
D0	0 = Enable internal T$_{HIGH}$ interrupt. 1 = Disable internal T$_{HIGH}$ interrupt.
D1	0 = Enable internal T$_{LOW}$ interrupt. 1 = Disable internal T$_{LOW}$ interrupt.
D2	0 = Enable external T$_{HIGH}$ interrupt. 1 = Disable external T$_{HIGH}$ interrupt.
D3	0 = Enable external T$_{LOW}$ interrupt. 1 = Disable external T$_{LOW}$ interrupt.
D4	0 = Enable external temperature fault interrupt. 1 = Disable external temperature fault interrupt.
D5:D7	Reserved. Only write 0s.

Interrupt Mask 2 Register (Read/Write) [Add. = 1Eh]

This mask register is an 8-bit read/write register that can be used to mask out any interrupts that can cause the INT/$\overline{\text{INT}}$ pin to go active.

Table 46. Interrupt Mask 2

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Table 47.

Bit	Function
D0:D3	Reserved. Only write 0s.
D4	0 = Enable VDD interrupts. 1 = Disable VDD interrupts.
D5:D7	Reserved. Only write 0s.

Internal Temperature Offset Register (Read/Write) [Add. = 1Fh]

This register contains the offset value for the internal temperature channel. A twos complement number can be written to this register which is then added to the measured result before it is stored or compared to limits. In this way, a one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register, the temperature resolution is 1°C.

Table 48. Internal Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0	0*

*Default settings at power-up.

External Temperature Offset Register (Read/Write) [Add. = 20h]

This register contains the offset value for the external temperature channel. A twos complement number can be written to this register which is then added to the measured result before it is stored or compared to limits. In this way, one-point calibration can be done whereby the whole transfer function of the channel can be moved up or down. From a software point of view, this may be a very simple method to vary the characteristics of the measurement channel if the thermal characteristics change. As it is an 8-bit register, the temperature resolution is 1°C.

Table 49. External Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Internal Analog Temperature Offset Register (Read/Write) [Add. = 21h]

This register contains the offset value for the internal thermal voltage output. A twos complement number can be written to this register which is then added to the measured result before it is converted by DAC A. Varying the value in this register has the affect of varying the temperature span. For example, the output voltage can represent a temperature span of −128°C to +127°C or even 0°C to 127°C. In essence, this register changes the position of 0 V on the temperature scale. Anything other than −128°C to +127°C will produce an upper dead band on the DAC A output. As it is an 8-bit register, the temperature resolution is 1°C. The default value is −40°C.

Table 50. Internal Analog Temperature Offset

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

*Default settings at power-up.

External Analog Temperature Offset Register (Read/Write) [Add. = 22h]

This register contains the offset value for the external thermal voltage output. A twos complement number can be written to this register which is then added to the measured result before it is converted by DAC B. Varying the value in this register has the affect of varying the temperature span. For example, the output

voltage can represent a temperature span of −128°C to +127°C or even 0°C to 127°C. In essence, this register changes the position of 0 V on the temperature scale. Anything other than −128°C to +127°C will produce an upper dead band on the DAC B output. As it is an 8-bit register, the temperature resolution is 1°C. The default value is −40°C.

Table 51. External Analog Temperature

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	1*	1*	0*	0*	0*

*Default settings at power-up.

V$_{DD}$ V$_{HIGH}$ Limit Register (Read/Write) [Add. = 23h]
This limit register is an 8-bit read/write register which stores the V$_{DD}$ upper limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured V$_{DD}$ value has to be greater than the value in this register. The default value is 5.46 V.

Table 52. V$_{DD}$ V$_{HIGH}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	0*	1*	1*	1*

*Default settings at power-up.

V$_{DD}$ V$_{LOW}$ Limit Register (Read/Write) [Add. = 24h]
This limit register is an 8-bit read/write register which stores the V$_{DD}$ lower limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured V$_{DD}$ value has to be less than or equal to the value in this register. The default value is 2.7 V

Table 53. V$_{DD}$ V$_{LOW}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	0*	1*	0*

*Default settings at power-up.

Internal T$_{HIGH}$ Limit Register (Read/Write) [Add. = 25h]
This limit register is an 8-bit read/write register which stores the twos complement of the internal temperature upper limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be greater than the value in this register. As it is an 8-bit register the temperature resolution is 1°C. Default value is +100°C.

Table 54. Internal T$_{HIGH}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	1*	1*	0*	0*	1*	0*	0*

*Default settings at power-up.

Internal T$_{LOW}$ Limit Register (Read/Write) [Add. 26h]
This limit register is an 8-bit read/write register which stores the twos complement of the internal temperature lower limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured internal temperature value has to be more negative than or equal to the value in this register. As it is an 8-bit register, the temperature resolution is 1°C. The default value is −55°C.

Table 55. Internal T$_{LOW}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	0*	0*	1*	0*	0*	1*

*Default settings at power-up.

External T$_{HIGH}$ Limit Register (Read/Write) [Add. = 27h]
This limit register is an 8-bit read/write register which stores the twos complement of the external temperature upper limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be greater than the value in this register. As it is an 8-bit register, the temperature resolution is 1°C. The default value is −1°C.

Table 56. External T$_{HIGH}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
1*	1*	1*	1*	1*	1*	1*	1*

*Default settings at power-up.

External T$_{LOW}$ Limit Register (Read/Write) [Add. = 28h]

This limit register is an 8-bit read/write register which stores the twos complement of the external temperature lower limit that will cause an interrupt and activate the INT/$\overline{INT}$ output (if enabled). For this to happen, the measured external temperature value has to be more negative than or equal to the value in this register. As it is an 8-bit register, the temperature resolution is 1°C. The default value is 0°C.

Table 57. External T$_{LOW}$ Limit

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	0*	0*	0*	0*

*Default settings at power-up.

Device ID Register (Read-Only) [Add. = 4Dh]
This 8-bit read-only register indicates which part the device is in the model range. ADT7316 = 01h, ADT7317 = 09h, and ADT7318 = 05h.

Manufacturer's ID Register (Read-Only) [Add. = 4Eh]
This register contains the manufacturers identification number. ADI's ID is 41h.

Silicon Revision Register (Read-Only) [Add. = 4Fh]
This register is divided into the 4 LSBs representing the
stepping and the 4 MSBs representing the version. The stepping
contains the manufacturer's code for minor revisions or
steppings to the silicon. The version is the ADT7316/ADT7317/
ADT7318 version number.

SPI Lock Status Register (Read-Only) [Add. = 7Fh]
Bit D0 (LSB) of this read-only register indicates whether the SPI
interface is locked or not. Writing to this register will cause the
device to malfunction. The default value is 00h.

  0 = I²C Interface.

  1 = SPI Interface Selected and Locked.
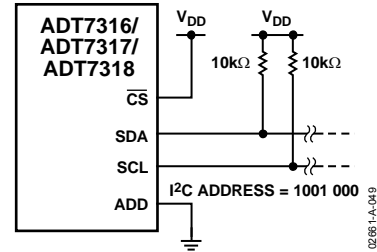
Figure 48. Typical I²C Interface Connection
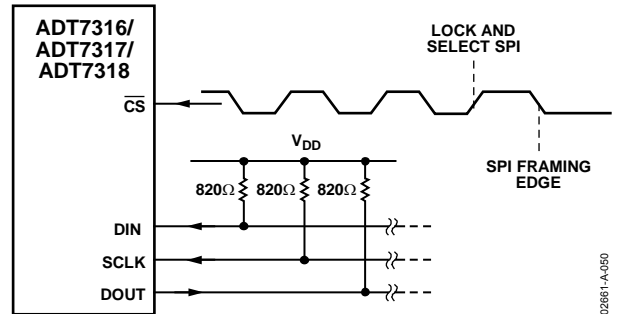
Figure 49. Typical SPI Interface Connection
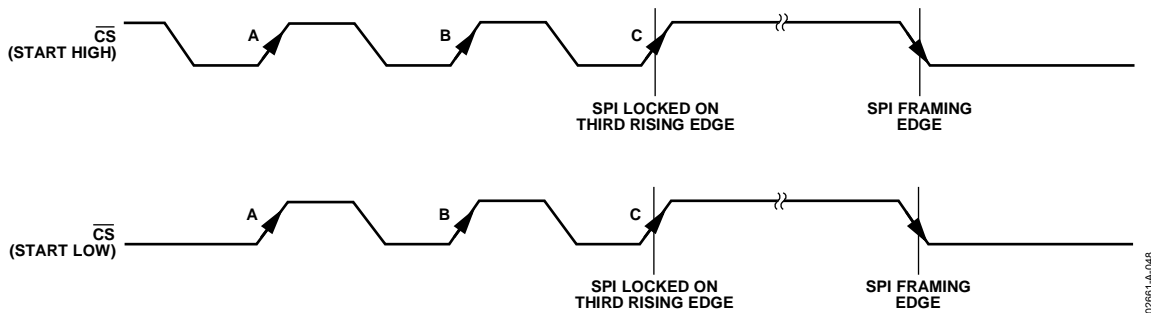
Figure 50. Serial Interface—Selecting and Locking SPI Protocol
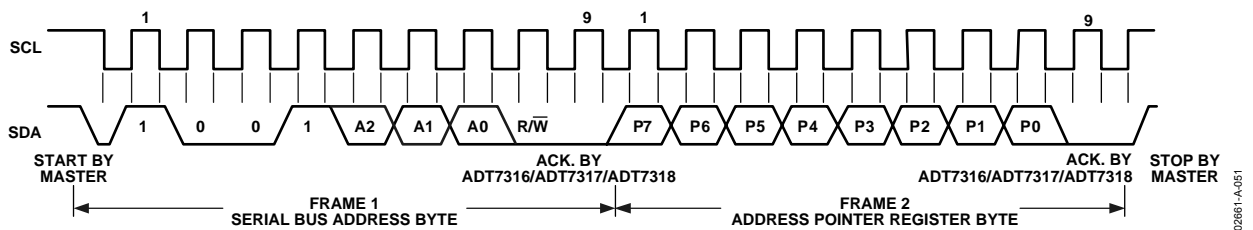
Figure 51. I²C—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

SERIAL INTERFACE

There are two serial interfaces that can be used on this part, I²C and SPI. The device will power up with the serial interface in I²C mode, but it is not locked into this mode. To stay in I²C mode, it is recommended that the user ties the $\overline{CS}$ line to either V_CC or GND. It is not possible to lock the I²C mode, but it is possible to select and lock the SPI mode.

To select and lock the interface into the SPI mode, a number of pulses must be sent down the $\overline{CS}$ (Pin 4) line. The following section describes how this is done.

Once the SPI communication protocol has been locked in, it cannot be unlocked while the device is still powered up. Bit D0 of SPI Lock Status register (Address = 7Fh) is set to 1 when a successful SPI interface lock has been accomplished. To reset the serial interface, the user must power down the part and power up again. A software reset does not reset the serial interface.

SERIAL INTERFACE SELECTION

The $\overline{CS}$ line controls the selection between I²C and SPI. Figure 49 shows the selection process necessary to lock the SPI interface mode.

If the user wants to communicate to the ADT7316/ADT7317/ADT7318 using the SPI protocol, send three pulses down the $\overline{CS}$ line as shown in Figure 49. On the third rising edge (marked as C in Figure 49), the part selects and locks the SPI interface. The user is now limited to communicating to the device using the SPI protocol.

As per most SPI standards, the $\overline{CS}$ line must be low during every SPI communication to the ADT7316/ADT7317/ADT7318 and high all other times. Typical examples of how to connect up the dual interface as I²C or SPI is shown in Figure 48 and Figure 49.

The following sections describe in detail how to use the I²C and SPI protocols associated with the ADT7316/ADT7317/ADT7318.

I²C SERIAL INTERFACE

Like all I²C compatible devices, the ADT7316/ADT7317/ADT7318 have a 7-bit serial address. The 4 MSBs of this address for the ADT7316/ADT7317/ADT7318 are set to 1001. The 3 LSBs are set by Pin 11, ADD. The ADD pin can be configured three ways to give three different address options: low, floating, and high. Setting the ADD pin low gives a serial bus address of 1001 000, leaving it floating gives the address 1001 010, and setting it high gives the address 1001 011. The recommended pullup resistor value is 10 kΩ.

There is a programmable SMBus timeout. When this is enabled the SMBus will timeout after 25 ms of no activity. To enable it, set Bit 6 of Control Configuration 2 register. The power-up default is with the SMBus timeout disabled.

The ADT7316/ADT7317/ADT7318 support SMBus packet error checking (PEC) and its use is optional. It is triggered by supplying the extra clocks for the PEC byte. The PEC is calculated using CRC-8. The frame clock sequence (FCS) conforms to CRC-8 by the polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult SMBus specification (www.smbus.org) for more information.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the start condition and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus now remain idle, while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master will write to the slave device. If the R/$\overline{W}$ bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master will pull the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device will pull the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data may be transferred over the serial bus in one operation but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

The I²C address set up by the ADD pin is not latched by the device until after this address has been sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. This is the SCL cycle directly after the device has seen its own I²C serial bus address. Any subsequent changes on this pin will have no effect on the I²C serial bus address.

Writing to the ADT7316/ADT7317/ADT7318

Depending on the register being written to, there are two different writes for the ADT7316/ADT7317/ADT7318. It is not possible to do a block write to this part, i.e., no I²C auto-increment.

Writing to the Address Pointer Register for a Subsequent Read

In order to read data from a particular register, the address pointer register must contain the address of that register. If it does not, the correct address must be written to the address pointer register by performing a single-byte write operation, as shown in Figure 51. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation is then performed to read the register.

Writing Data to a Register

All registers are 8-bit registers so only one byte of data can be written to each register. Writing a single byte of data to one of these read/write registers consists of the serial bus address, the data register address written to the address pointer register, followed by the data byte written to the selected data register. This is illustrated in Figure 52. To write to a different register, another start or repeated start is required. If more than one byte of data is sent in one communication operation, the addressed register will be repeatedly loaded until the last data byte has been sent.

Reading Data from the ADT7316/ADT7317/ADT7318

Reading data from the ADT7316/7317/7318 is done in a one byte operation. Reading back the contents of a register is shown in Figure 56. The register address previously had been set up by a single byte write operation to the address pointer register. To read from another register, write to the address pointer register again to set up the relevant register address. Therefore, block reads are not possible, i.e., no I²C auto-increment.

SPI SERIAL INTERFACE

The SPI serial interface of the ADT7316/ADT7317/ADT7318 consists of four wires, CS, SCLK, DIN, and DOUT. The CS is used to select the device when more than one device is connected to the serial clock and data lines. The CS is also used to distinguish between any two separate serial communications (see Figure 58). The SCLK is used to clock data in and out of the part. The DIN line is used to write to the registers and the DOUT line is used to read data back from the registers. The recommended pull-up resistor value is between 500 Ω to 820 Ω

The part operates in a slave mode and requires an externally applied serial clock to the SCLK input. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations, a read and a write. Command words are used to distinguish between a read and a write operation. These command words are given in Table 58. Address auto-increment is possible in SPI mode.

Table 58. SPI Command Words
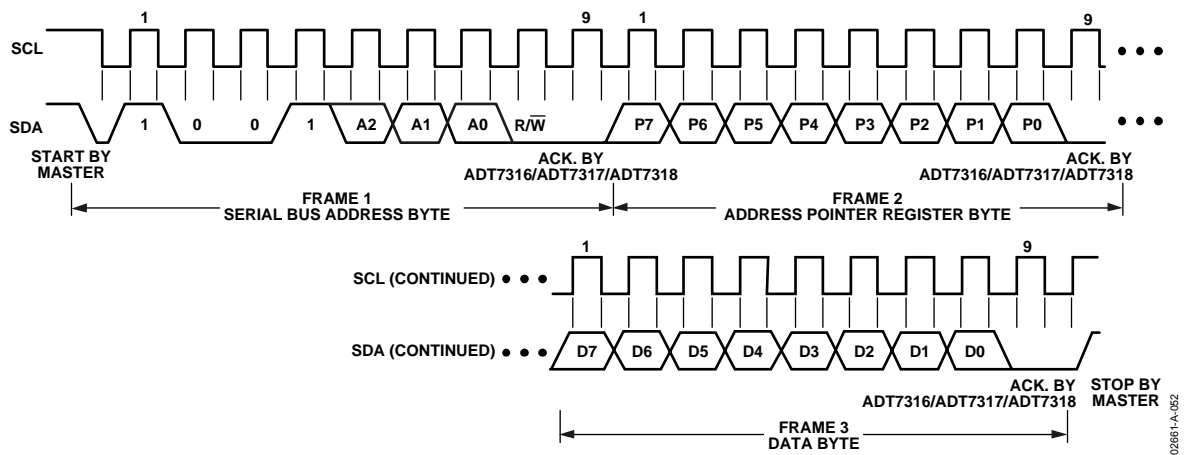
Write	Read
90h (1001 0000)	91h (1001 0001)

Figure 52. I²C—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register

Write Operation

Figure 53 and Figure 54 show the timing diagrams for a write operation to the ADT7316/ADT7317/ADT7318. Data is clocked into the registers on the rising edge of SCLK. When the $\overline{CS}$ line is high, the DIN and DOUT lines are in three-state mode. Only when the $\overline{CS}$ goes from a high to a low does the part accept any data on the DIN line. In SPI mode, the address pointer register is capable of auto-increment to the next register in the register map without having to load the address pointer register each time. In Figure 54, the register address portion of the diagram gives the first register that will be written to. Subsequent data bytes will be written into sequential writable registers. Therefore, after each data byte has been written into a

register, the address pointer register auto-increments its value to the next available register. The address pointer register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

Read Operation

Figure 55 and Figure 57 show the timing diagrams necessary to accomplish correct read operations. To read back from a register, first write to the address pointer register with the address of the register to read from. This operation is shown in Figure 53. Figure 55 shows the procedure for reading back a single byte of data. The read command is first sent to the part during the first eight clock cycles, during the following eight clock cycles the data contained in the register
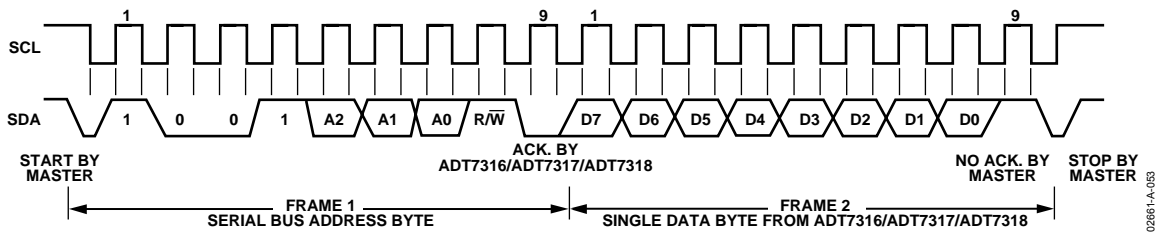

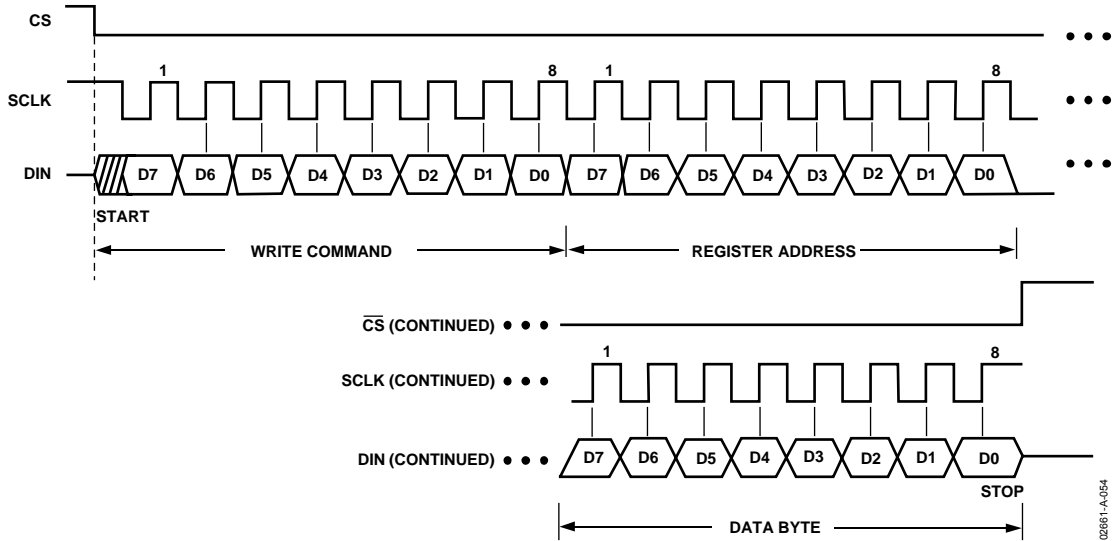Figure 53. I²C — Reading a Single Byte of Data From a Selected Register

Figure 54. SPI—Writing to the Address Pointer Register Followed by a Single Byte of Data to the Selected Register
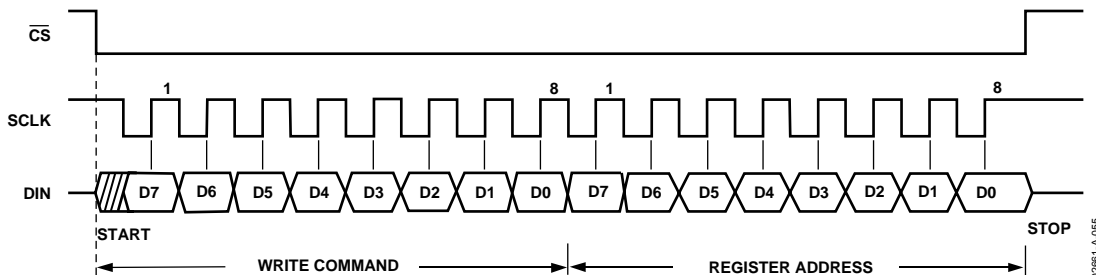

Figure 55. SPI—Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation
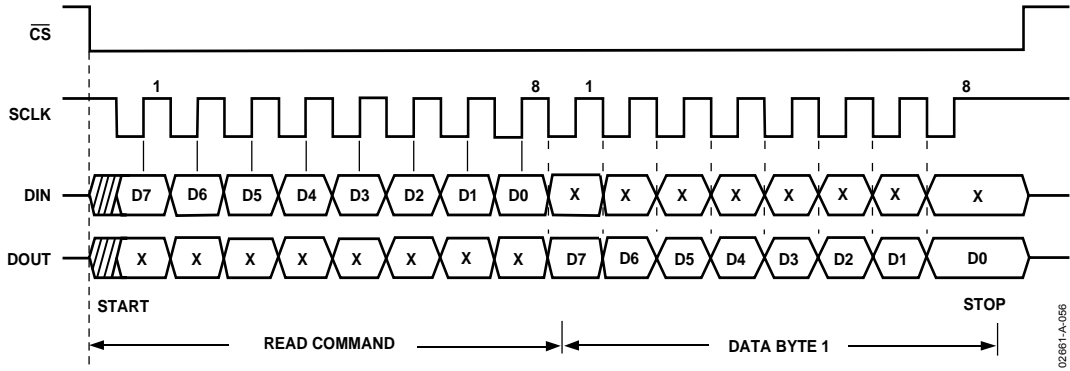
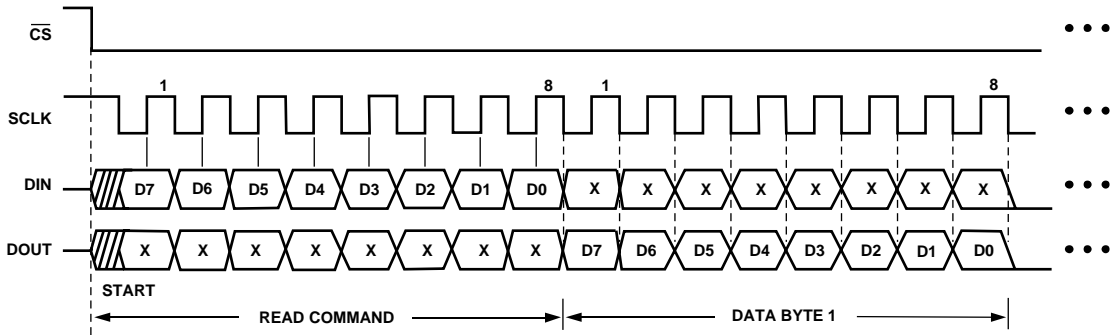*Figure 56. SPI —Reading a Single Byte of Data From a Selected Register*

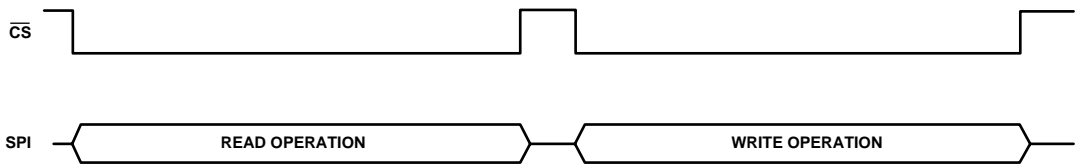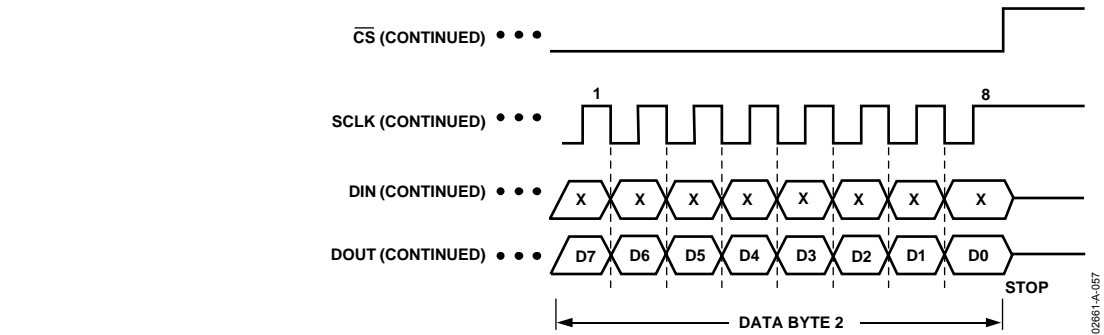*Figure 57. SPI—Reading Two Bytes of Data from Two Sequential Registers*

Figure 58. SPI—Correct Use of $\overline{CS}$ During SPI Communication

selected by the address pointer register is outputted onto the DOUT line. Data is outputted onto the DOUT line on the falling edge of SCLK. Figure 57 shows the procedure when reading data from two sequential registers. Multiple data reads are possible in SPI interface mode as the address pointer register is auto-incremental. The address pointer register will auto-increment from 00h to 3Fh and will loop back to start all over again at 00h when it reaches 3Fh.

SMBUS/SPI INT/$\overline{INT}$

The ADT7316/ADT7317/ADT7318 INT/$\overline{INT}$ output is an interrupt line that signals an over-limit/under-limit event on any of the measurement channels if the interrupt on that event has not been disabled. The ADT7316/ADT7317/ADT7318 are a slave-only device and use the SMBus/SPI INT/$\overline{INT}$ as their only means to signal other devices that an event has occurred.

The INT/$\overline{\text{INT}}$ pin has an open-drain configuration that allows the outputs of several devices to be wired-AND together when the INT/$\overline{\text{INT}}$ pin is active low. Use C6 of the Control Configuration 1 Register to set the active polarity of the INT/$\overline{\text{INT}}$ output. The power-up default is active low. The INT/$\overline{\text{INT}}$ output can be disabled or enabled by setting C5 of Control Configuration 1 register to a 1 or 0, respectively.

The INT/$\overline{\text{INT}}$ output becomes active when either the internal temperature value, the external temperature value, or the V_{DD} value exceeds the values in their corresponding T_{HIGH}/V_{HIGH} or T_{LOW}/V_{LOW} registers. The INT/$\overline{\text{INT}}$ output goes inactive again when a conversion result indicates that all measurement channels are within their trip limits, and when the status register associated with the out-of-limit event is read. The two interrupt status registers show which event caused the INT/$\overline{\text{INT}}$ pin to go active.

The INT/$\overline{\text{INT}}$ output requires an external pull-up resistor. This can be connected to a voltage different from V_{DD} provided that the maximum voltage rating of the INT/$\overline{\text{INT}}$ output pin is not exceeded. The value of the pull-up resistor depends on the application but should be large enough to avoid excessive sink currents at the INT/$\overline{\text{INT}}$ output, which can heat the chip and affect the temperature reading.

SMBUS Alert Response

The INT/$\overline{\text{INT}}$ pin behaves the same way as an SMBus alert pin when the SMBus/I²C interface is selected. It is an open-drain output and requires a pull-up to V_{DD}. Several INT/$\overline{\text{INT}}$ outputs can be wire-AND together so that the common line will go low if one or more of the INT/$\overline{\text{INT}}$ outputs goes low. The polarity of the INT/$\overline{\text{INT}}$ pin must be set for active low for a number of outputs to be wire-AND together. The INT/$\overline{\text{INT}}$ output can operate as an $\overline{\text{SMBALERT}}$ function. Slave devices on the SMBus can normally not signal to the master that they want to talk, but the $\overline{\text{SMBALERT}}$ function allows them to do so. $\overline{\text{SMBALERT}}$ is used in conjunction with the SMBus general call address.

One or more INT/$\overline{\text{INT}}$ outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. When $\overline{\text{SMBALERT}}$ line is pulled low by one of the devices, the following procedure occurs (see Figure 59).
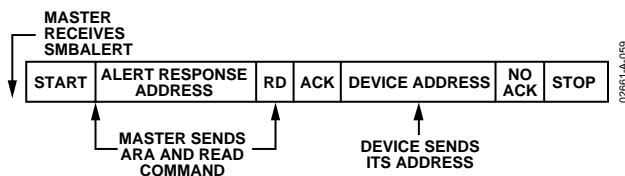

Figure 59. INT/$\overline{\text{INT}}$ Responds to $\overline{\text{SMBALERT}}$ ARA

1. $\overline{\text{SMBALERT}}$ pulled low.

2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.

3. The devices whose INT/$\overline{\text{INT}}$ output is low responds to the alert response address and the master reads its device address. Since the device address is seven bits long, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.

4. If more than one devices INT/$\overline{\text{INT}}$ output is low, the one with the lowest device address will have priority, in accordance with normal SMBus specifications.

5. Once the ADT7316/ADT7317/ADT7318 has responded to the alert response address, it will reset its INT/$\overline{\text{INT}}$ output, provided that the condition that caused the out-of-limit event no longer exists and the status register associated with the out-of-limit event is read. If the $\overline{\text{SMBALERT}}$ line remains low, the master will send the ARA again. It will continue to do this until all devices whose $\overline{\text{SMBALERT}}$ outputs were low have responded.
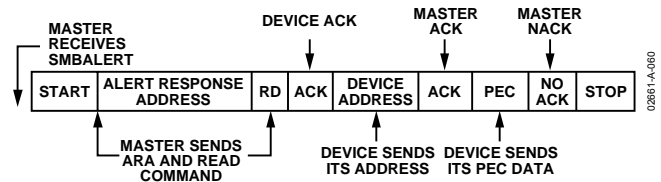

Figure 60. INT/$\overline{\text{INT}}$ Responds to $\overline{\text{SMBALERT}}$ ARA with Packet Error Checking (PEC)

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADT7316/ADT7317/ADT7318 as close as possible to the remote sensing diode. Provided that the worst noise sources, such as clock generators, data/address buses and CRTs, are avoided, this distance can be 4 inches to 8 inches.
2. Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended.
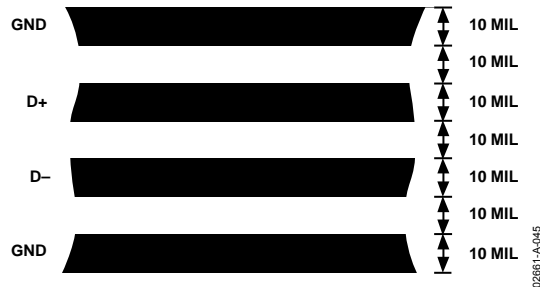

Figure 61. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and at the same temperature. Thermocouple effects should not be a major problem as 1°C corresponds to about 240 µV, and thermocouple voltages are about 3 µV/°C of the temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.
5. Place 0.1 µF bypass and 2200 pF input filter capacitors close to the ADT7316/ADT7317/ADT7318.
6. If the distance to the remote sensor is more than 8 inches, the use of the twisted pair cable is recommended. This will work up to about 6 feet to 12 feet.
7. For really long distances (up to 100 feet), use shielded twisted pair, such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND close to the ADT7316/ADT7317/ADT7318. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. Series resistance of 1 Ω introduces about 0.5°C error.

OUTLINE DIMENSIONS
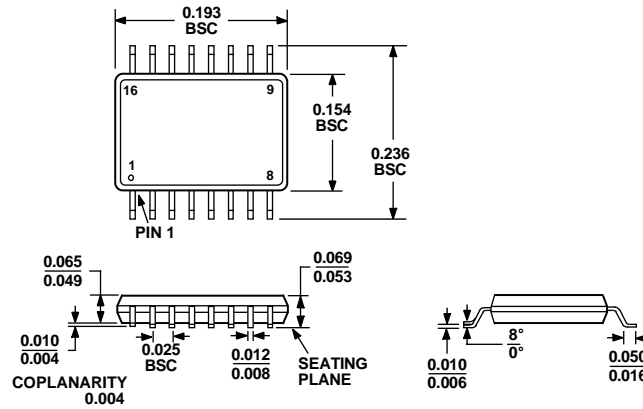
COMPLIANT TO JEDEC STANDARDS MO-137AB

Figure 62. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and millimeters

ORDERING GUIDE

Model[1]	Temperature Range	DAC Resolution	Package Description	Minimum Quantities/Reel
ADT7318ARQ	−40°C to +120°C	8-Bits	16-Lead QSOP	N/A
ADT7318ARQ-REEL	−40°C to +120°C	8-Bits	16-Lead QSOP	2500
ADT7318ARQ-REEL7	−40°C to +120°C	8-Bits	16-Lead QSOP	1000
ADT7317ARQ	−40°C to +120°C	10-Bits	16-Lead QSOP	N/A
ADT7317ARQ-REEL	−40°C to +120°C	10-Bits	16-Lead QSOP	2500
ADT7317ARQ-REEL7	−40°C to +120°C	10-Bits	16-Lead QSOP	1000
ADT7316ARQ	−40°C to +120°C	12-Bits	16-Lead QSOP	N/A
ADT7316ARQ-REEL	−40°C to +120°C	12-Bits	16-Lead QSOP	2500
ADT7316ARQ-REEL7	−40°C to +120°C	12-Bits	16-Lead QSOP	1000

[1] Devices that have date codes before 0414 have an internal reference of 2.25 V. Devices manufactured after this data code have the internal reference at 2.28 V.

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