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SSD1828

Advanced Information

LCD Segment / Common Driver with Controller
CMOS

1 General Description

SSD1828 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. SSD1828 consists of 162 high voltage driving output pins for driving 96 Segments, 64 Commons and 1 icon driving with dual Common outputs.

SSD1828 displays data directly from its internal 96x65 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through hardware selectable 6800-/8080-series compatible Parallel Interface or 3/4 wires Serial Peripheral Interface.

SSD1828 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die layout, SSD1828 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

This document contains information on a new product. Specification and information herein are subject to change without notice.

2 FEATURES

96x64 Graphic Display with a Icon Line

Programmable Multiplex ratio [16Mux - 65Mux]

Single Supply Operation, 1.8 V - 3.3V

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On-Chip 96 x 65 Graphic Display Data RAM

On-Chip Voltage Generator / External Power Supply

On-Chip Oscillator

Software Selectable On-Chip Bias Dividers, with No External Capacitors required

Hardware pin selectable for 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, 3-wire Serial Peripheral Interface or 4-wire Serial Peripheral Interface

Maximum 17MHz SPI or 15MHz PPI operation

Software selectable 2X / 3X / 4X / 5X On-Chip DC-DC Converter

Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 bias ratio

Re-mapping of Row and Column Drivers

Vertical Scrolling

Display Offset Control

64 Levels Internal Contrast Control

External Contrast Control

Selectable LCD Driving Voltage Temperature Coefficients (4 settings)

3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Seg	Com	Package Form
SSD1828Z	96	64 + 1	Gold Bump Die

4 BLOCK DIAGRAM

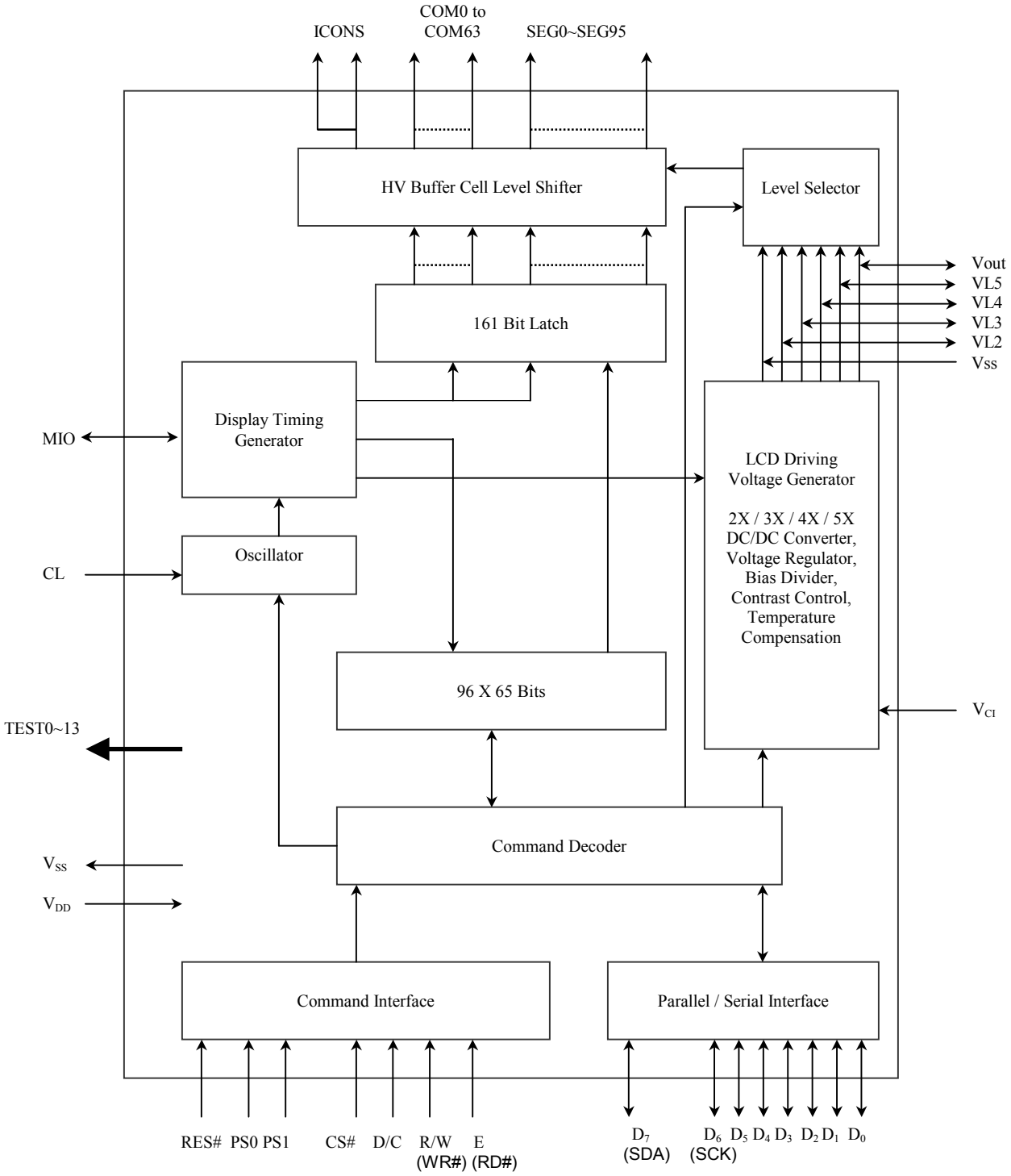
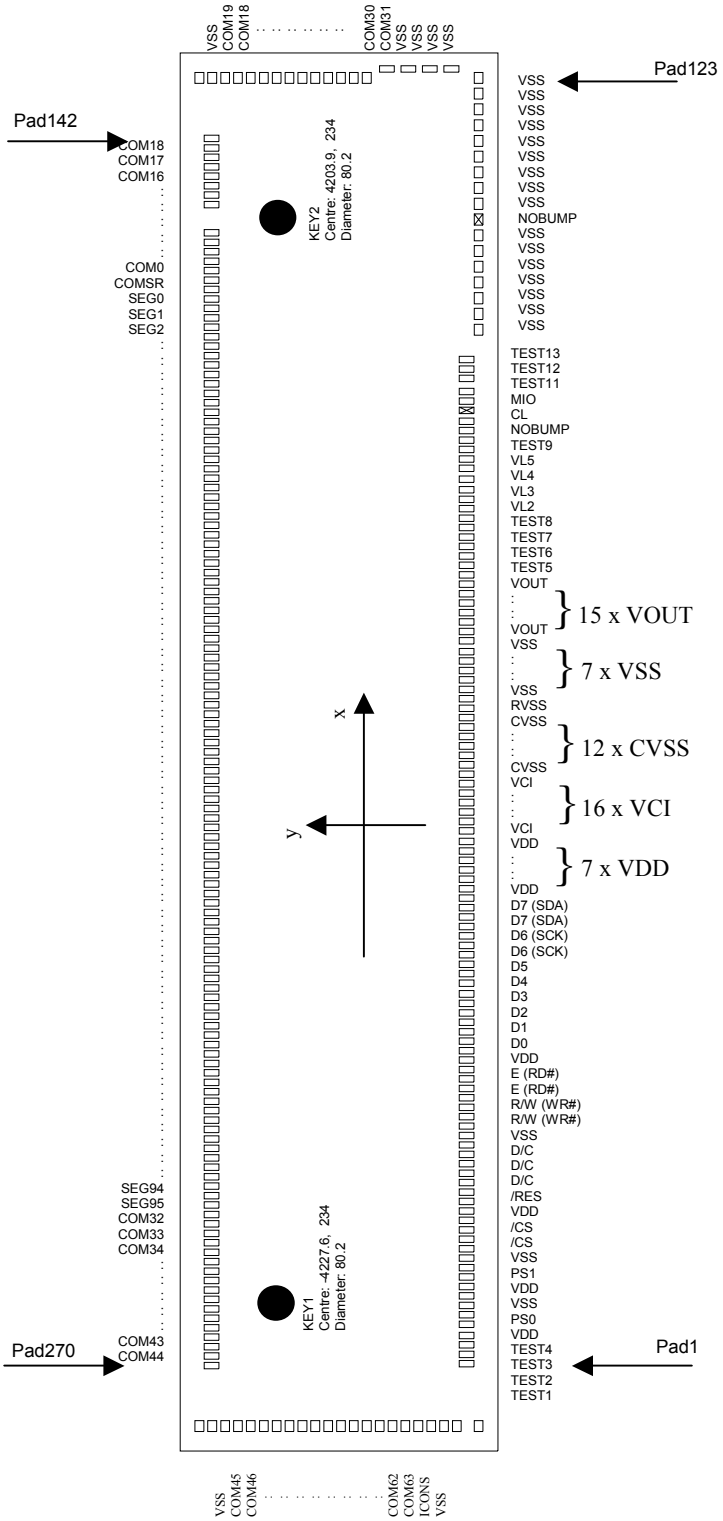


Figure 1 - Block Diagram

5 DIE Arrangement



Note:
1. Diagram showing the die face up.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.

Die size (with scribe): 9.6 x 1.6 mm^2
Die Thickness: 534±25µm
Bump Height: Typical 18µm
Bump co-planarity <3µm (within die)

Figure 2 – SSD1828 Pin Assignment

Table 2 - SSD1828 Series Die Pad Coordinates

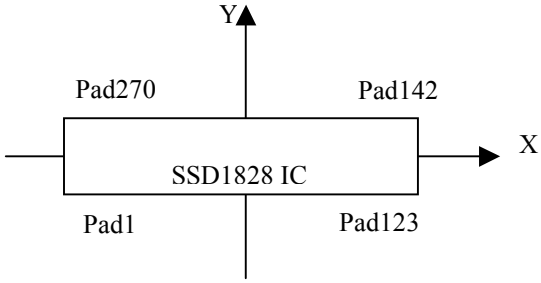
Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
1	TEST1	-4199.6	-642.0	51	VCI	-939.2	-642.0	101	NOBUMP	2344.4	-642.0
2	TEST2	-4134.8	-642.0	52	VCI	-874.4	-642.0	102	CL	2409.2	-642.0
3	TEST3	-4070.0	-642.0	53	VCI	-809.6	-642.0	103	MIO	2474.0	-642.0
4	TEST4	-4005.2	-642.0	54	VCI	-744.8	-642.0	104	TEST11	2564.4	-642.0
5	VDD	-3928.7	-642.0	55	VCI	-680.0	-642.0	105	TEST12	2629.2	-642.0
6	PS0	-3863.9	-642.0	56	VCI	-615.2	-642.0	106	TEST13	2694.0	-642.0
7	VSS	-3799.1	-642.0	57	CVSS	-541.7	-642.0	107	VSS	2899.2	-702.9
8	VDD	-3734.3	-642.0	58	CVSS	-476.9	-642.0	108	VSS	3007.2	-702.9
9	PS1	-3669.5	-642.0	59	CVSS	-412.1	-642.0	109	VSS	3115.2	-702.9
10	VSS	-3604.7	-642.0	60	CVSS	-347.3	-642.0	110	VSS	3223.2	-702.9
11	/CS	-3539.9	-642.0	61	CVSS	-282.5	-642.0	111	VSS	3331.2	-702.9
12	/CS	-3475.1	-642.0	62	CVSS	-217.7	-642.0	112	VSS	3439.2	-702.9
13	VDD	-3410.3	-642.0	63	CVSS	-152.9	-642.0	113	VSS	3547.2	-702.9
14	/RES	-3345.5	-642.0	64	CVSS	-88.1	-642.0	114	NOBUMP	3655.2	-702.9
15	D/C	-3280.7	-642.0	65	CVSS	-23.3	-642.0	115	VSS	3763.2	-702.9
16	D/C	-3215.9	-642.0	66	CVSS	41.6	-642.0	116	VSS	3871.2	-702.9
17	D/C	-3151.1	-642.0	67	CVSS	106.4	-642.0	117	VSS	3979.2	-702.9
18	VSS	-3086.3	-642.0	68	CVSS	171.2	-642.0	118	VSS	4087.2	-702.9
19	R/W (RW#)	-3021.5	-642.0	69	RVSS	236.0	-642.0	119	VSS	4195.2	-702.9
20	R/W (RW#)	-2956.7	-642.0	70	VSS	300.8	-642.0	120	VSS	4303.2	-702.9
21	E (RD#)	-2891.9	-642.0	71	VSS	365.6	-642.0	121	VSS	4411.2	-702.9
22	E (RD#)	-2827.1	-642.0	72	VSS	430.4	-642.0	122	VSS	4519.2	-702.9
23	VDD	-2762.3	-642.0	73	VSS	495.2	-642.0	123	VSS	4627.2	-702.9
24	D0	-2697.5	-642.0	74	VSS	560.0	-642.0	124	VSS	4688.1	-564.9
25	D1	-2632.7	-642.0	75	VSS	624.8	-642.0	125	VSS	4688.1	-456.9
26	D2	-2567.9	-642.0	76	VSS	689.6	-642.0	126	VSS	4688.1	-348.9
27	D3	-2503.1	-642.0	77	VOUT	763.1	-642.0	127	VSS	4688.1	-240.9
28	D4	-2438.3	-642.0	78	VOUT	827.9	-642.0	128	COM31	4627.2	-139.5
29	D5	-2373.5	-642.0	79	VOUT	892.7	-642.0	129	COM30	4627.2	-74.7
30	D6 (SCK)	-2308.7	-642.0	80	VOUT	957.5	-642.0	130	COM29	4627.2	-9.9
31	D6 (SCK)	-2243.9	-642.0	81	VOUT	1022.3	-642.0	131	COM28	4627.2	54.9
32	D7 (SDA)	-2179.1	-642.0	82	VOUT	1087.1	-642.0	132	COM27	4627.2	119.7
33	D7 (SDA)	-2114.3	-642.0	83	VOUT	1151.9	-642.0	133	COM26	4627.2	184.5
34	VDD	-2049.5	-642.0	84	VOUT	1216.7	-642.0	134	COM25	4627.2	249.3
35	VDD	-1984.7	-642.0	85	VOUT	1281.5	-642.0	135	COM24	4627.2	314.1
36	VDD	-1919.9	-642.0	86	VOUT	1346.3	-642.0	136	COM23	4627.2	378.9
37	VDD	-1855.1	-642.0	87	VOUT	1411.1	-642.0	137	COM22	4627.2	443.7
38	VDD	-1790.3	-642.0	88	VOUT	1475.9	-642.0	138	COM21	4627.2	508.5
39	VDD	-1725.5	-642.0	89	VOUT	1540.7	-642.0	139	COM20	4627.2	573.3
40	VDD	-1660.7	-642.0	90	VOUT	1605.5	-642.0	140	COM19	4627.2	638.1
41	VCI	-1587.2	-642.0	91	VOUT	1670.3	-642.0	141	VSS	4627.2	702.9
42	VCI	-1522.4	-642.0	92	TEST5	1735.1	-642.0	142	COM18	4212.0	642.0
43	VCI	-1457.6	-642.0	93	TEST6	1799.9	-642.0	143	COM17	4147.2	642.0
44	VCI	-1392.8	-642.0	94	TEST7	1873.4	-642.0	144	COM16	4082.4	642.0
45	VCI	-1328.0	-642.0	95	TEST8	1946.9	-642.0	145	COM15	4017.6	642.0
46	VCI	-1263.2	-642.0	96	VL2	2011.7	-642.0	146	COM14	3952.8	642.0
47	VCI	-1198.4	-642.0	97	VL3	2076.5	-642.0	147	COM13	3888.0	642.0
48	VCI	-1133.6	-642.0	98	VL4	2141.3	-642.0	148	COM12	3823.2	642.0
49	VCI	-1068.8	-642.0	99	VL5	2206.1	-642.0	149	COM11	3758.4	642.0
50	VCI	-1004.0	-642.0	100	TEST9	2270.9	-642.0	150	COM10	3564.0	642.0

Pad #	Pad Name	X-pos	Y-pos	Pad #	Pad Name	X-pos	Y-pos
151	COM9	3499.2	642.0	201	SEG39	259.2	642.0
152	COM8	3434.4	642.0	202	SEG40	194.4	642.0
153	COM7	3369.6	642.0	203	SEG41	129.6	642.0
154	COM6	3304.8	642.0	204	SEG42	64.8	642.0
155	COM5	3240.0	642.0	205	SEG43	0.0	642.0
156	COM4	3175.2	642.0	206	SEG44	-64.8	642.0
157	COM3	3110.4	642.0	207	SEG45	-129.6	642.0
158	COM2	3045.6	642.0	208	SEG46	-194.4	642.0
159	COM1	2980.8	642.0	209	SEG47	-259.2	642.0
160	COM0	2916.0	642.0	210	SEG48	-324.0	642.0
161	ICONS	2851.2	642.0	211	SEG49	-388.8	642.0
162	SEG0	2786.4	642.0	212	SEG50	-453.6	642.0
163	SEG1	2721.6	642.0	213	SEG51	-518.4	642.0
164	SEG2	2656.8	642.0	214	SEG52	-583.2	642.0
165	SEG3	2592.0	642.0	215	SEG53	-648.0	642.0
166	SEG4	2527.2	642.0	216	SEG54	-712.8	642.0
167	SEG5	2462.4	642.0	217	SEG55	-777.6	642.0
168	SEG6	2397.6	642.0	218	SEG56	-842.4	642.0
169	SEG7	2332.8	642.0	219	SEG57	-907.2	642.0
170	SEG8	2268.0	642.0	220	SEG58	-972.0	642.0
171	SEG9	2203.2	642.0	221	SEG59	-1036.8	642.0
172	SEG10	2138.4	642.0	222	SEG60	-1101.6	642.0
173	SEG11	2073.6	642.0	223	SEG61	-1166.4	642.0
174	SEG12	2008.8	642.0	224	SEG62	-1231.2	642.0
175	SEG13	1944.0	642.0	225	SEG63	-1296.0	642.0
176	SEG14	1879.2	642.0	226	SEG64	-1360.8	642.0
177	SEG15	1814.4	642.0	227	SEG65	-1425.6	642.0
178	SEG16	1749.6	642.0	228	SEG66	-1490.4	642.0
179	SEG17	1684.8	642.0	229	SEG67	-1555.2	642.0
180	SEG18	1620.0	642.0	230	SEG68	-1620.0	642.0
181	SEG19	1555.2	642.0	231	SEG69	-1684.8	642.0
182	SEG20	1490.4	642.0	232	SEG70	-1749.6	642.0
183	SEG21	1425.6	642.0	233	SEG71	-1814.4	642.0
184	SEG22	1360.8	642.0	234	SEG72	-1879.2	642.0
185	SEG23	1296.0	642.0	235	SEG73	-1944.0	642.0
186	SEG24	1231.2	642.0	236	SEG74	-2008.8	642.0
187	SEG25	1166.4	642.0	237	SEG75	-2073.6	642.0
188	SEG26	1101.6	642.0	238	SEG76	-2138.4	642.0
189	SEG27	1036.8	642.0	239	SEG77	-2203.2	642.0
190	SEG28	972.0	642.0	240	SEG78	-2268.0	642.0
191	SEG29	907.2	642.0	241	SEG79	-2332.8	642.0
192	SEG30	842.4	642.0	242	SEG80	-2397.6	642.0
193	SEG31	777.6	642.0	243	SEG81	-2462.4	642.0
194	SEG32	712.8	642.0	244	SEG82	-2527.2	642.0
195	SEG33	648.0	642.0	245	SEG83	-2592.0	642.0
196	SEG34	583.2	642.0	246	SEG84	-2656.8	642.0
197	SEG35	518.4	642.0	247	SEG85	-2721.6	642.0
198	SEG36	453.6	642.0	248	SEG86	-2786.4	642.0
199	SEG37	388.8	642.0	249	SEG87	-2851.2	642.0
200	SEG38	324.0	642.0	250	SEG88	-2916.0	642.0

Pad #	Pad Name	X-pos	Y-pos
251	SEG89	-2980.8	642.0
252	SEG90	-3045.6	642.0
253	SEG91	-3110.4	642.0
254	SEG92	-3175.2	642.0
255	SEG93	-3240.0	642.0
256	SEG94	-3304.8	642.0
257	SEG95	-3369.6	642.0
258	COM32	-3434.4	642.0
259	COM33	-3499.2	642.0
260	COM34	-3564.0	642.0
261	COM35	-3628.8	642.0
262	COM36	-3693.6	642.0
263	COM37	-3758.4	642.0
264	COM38	-3823.2	642.0
265	COM39	-3888.0	642.0
266	COM40	-3952.8	642.0
267	COM41	-4017.6	642.0
268	COM42	-4082.4	642.0
269	COM43	-4147.2	642.0
270	COM44	-4212.0	642.0
271	VSS	-4627.2	702.9
272	COM45	-4627.2	638.1
273	COM46	-4627.2	573.3
274	COM47	-4627.2	508.5
275	COM48	-4627.2	443.7
276	COM49	-4627.2	378.9
277	COM50	-4627.2	314.1
278	COM51	-4627.2	249.3
279	COM52	-4627.2	184.5
280	COM53	-4627.2	119.7
281	COM54	-4627.2	54.9
282	COM55	-4627.2	-9.9
283	COM56	-4627.2	-74.7
284	COM57	-4627.2	-139.5
285	COM58	-4627.2	-204.3
286	COM59	-4627.2	-269.1
287	COM60	-4627.2	-333.9
288	COM61	-4627.2	-398.7
289	COM62	-4627.2	-463.5
290	COM63	-4627.2	-528.3
291	ICONS	-4627.2	-593.1
292	VSS	-4627.2	-702.9

	X	Y	Unit	Remark
Pad Pitch	64.8	64.8	um	Min.
Pad Space	20.8	20.8	um	Min.

	Pad #	X	Y	Unit
Pad Size	1 - 100	44	75	um
	101	-	-	um
	102 - 106	44	75	um
	107 - 113	75	44	um
	114	-	-	um
	115 - 123	75	44	um
	124 - 127	44	75	um
	128 - 141	75	44	um
	142 - 270	44	75	um
	271 - 292	75	44	um



6 PIN DESCRIPTION

6.1 RES

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

6.2 PS0

This pin pair with PS1 to determine the interface protocol between the driver and MCU. Refer to PS1 pin descriptions for more details.

6.3 PS1

This pin pair with PS0 to determine the interface protocol between the driver and MCU, according to the following table.

Table 3 - PS0 & PS1 Interface

PS0	PS1	Interface
L	L	3-wire SPI (write only)
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

6.4 CS#

This pin is chip select input. The chip is enabled for display data/command transfer only when CS is low.

6.5 D/C

This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpreted as command. This pin must be connected to V_{SS} when 3-lines SPI interface is used. .

6.6 R/W(WR#)

This pin is microprocessor interface signal. When interfacing to a 6800-series microprocessor, the signal indicates read mode when high and write mode when low. When interfacing to an 8080-microprocessor, a data write operation is initiated when R/W(WR) is low and the chip is selected.

6.7 E(RD#)

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, a data operation is initiated when E(RD) is high and the chip is selected. When interfacing to an 8080-microprocessor, a data read operation is initiated when E(RD) is low and the chip is selected.

6.8 D_0 -D_7

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

6.9 V_{DD}

Power supply pin.

6.10 RV_{SS}

Ground reference of Vref.

6.11 CV_{SS}

Ground reference of analog circuitry.

6.12 V_{SS}

Ground reference of logic circuitry.

6.13 V_{CI}

Reference voltage input for internal DC-DC converter. The voltage of generated V_{CC} equals to the multiple factor (2X, 3X, 4X or 5X) times V_{CI} with respect to V_{SS}.
Note: Voltage at this input pin must be larger than or equal to V_{DD}.

6.14 V_{out}

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal regulator.

6.15 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:
$V_{out} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$

Table 4 - $V_{out} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

	1 : a bias
V_{L5}	(a-1)/a * V_{out}
V_{L4}	(a-2)/a * V_{out}
V_{L3}	2/a * V_{out}
V_{L2}	1/a * V_{out}

a is equals to 9 at POR.

6.16 COM0 – COM63

These pins provide the row driving signal COM0 - COM63 to the LCD panel. See Figure 5 or Figure 7 about the COM signal mapping in different multiplex ratio N.

6.17 ICONS

This pin is the special icons line COM signal output.

6.18 SEG0 – SEG95

These pins provide the LCD column driving signal. Their voltage level is V_{SS} during sleep mode.

6.19 CL

This pin is the external clock input for the device, which is enabled by using an extended command. Under normal operation, this pin should be left opened and internal oscillator will be used after power on reset.

6.20 MIO

This pin is used for cascade purpose only. Under normal operation, it should be left open.

6.21 TEST0~13

These pins is used for internal only and should be left open, any connection is not allowed.

6.22 NOBUMP

These pins are AL metal pads only, without any gold bump on the top. They should be left open, any connection is not allowed.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C is high, data is written to Graphic Display Data RAM (GDDRAM). If D/C is low, the input at D_0 -D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once RES# receives a negative reset pulse of about 1us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

7.2 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/W(WR#), D/C, E(RD#) and CS#. R/W(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD#) and CS# input serves as data latch signal (clock) when they are high and low respectively. Refer to Figure 10 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

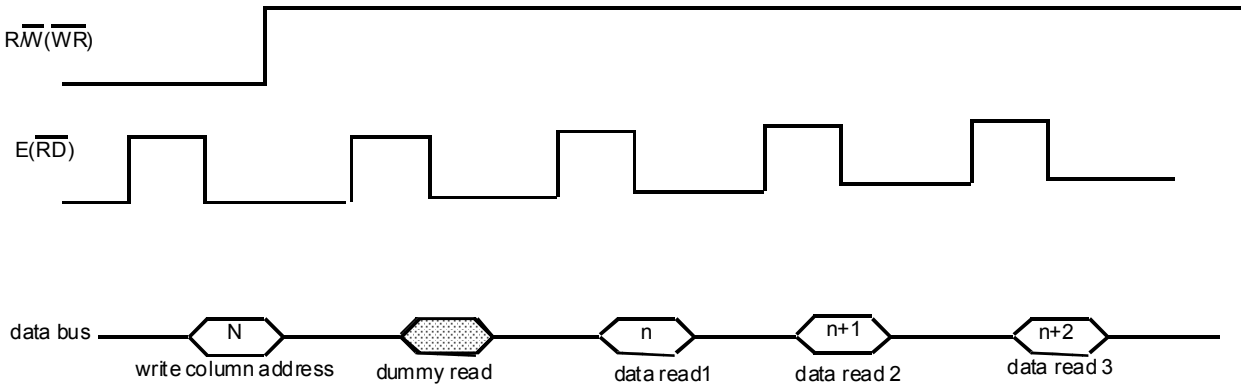


Figure 3 – Display Data Read with the insertion of Dummy Read

7.3 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/W(WR#), E(RD#), D/C and CS#. The CS# input serves as data latch signal (clock) when it is low. Whether it is display data or status register read is controlled by D/C. R/W(WR#) and E(RD#) input indicates a write or read cycle when CS is low. Refer to Figure 12 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

7.4 MPU Serial 4-wire Interface

The serial interface consists of serial clock SCK, serial data SDA, D/C and CS#. SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock. No extra clock or command is required to end the transmission.

7.5 MPU Serial 3-wire interface

Operation is similar to 4-wire serial interface while D/C is not been used. The Display Data Length instruction is used to indicate that a specified number display data byte(s) (1-256) are to be transmitted. Next byte after the display data string is handled as a command.

It should be noted that if there is a signal glitch at SCK that causing an out of synchronization in the serial communication, a hardware reset pulse at RES# pin is required to initialize the chip for re-synchronization.

Table 5 -Modes of Operation

	6800 Parallel	8080 Parallel	Serial
Data Read	Yes	Yes	No
Data Write	Yes	Yes	Yes
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

7.6 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 96 x 65 = 6,240bits for SSD1828. Figure 5 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data mapped to the display. Figure 5 shows the case in which the display start line register is set at 30H.

For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

7.7 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

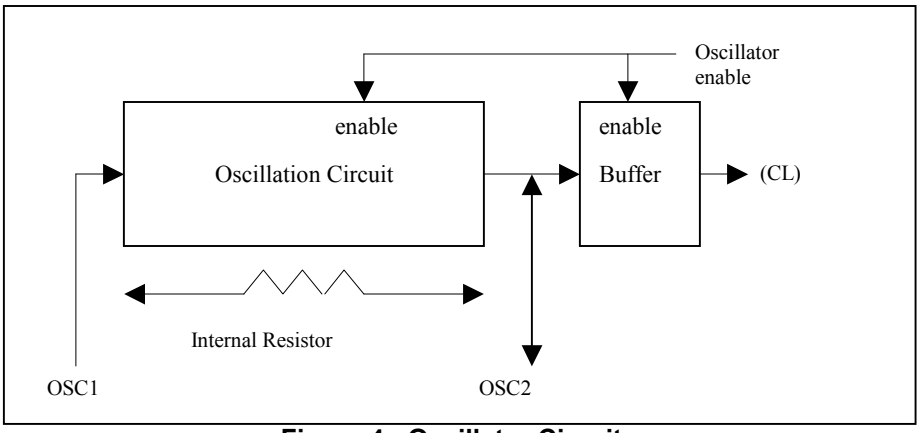


Figure 4 - Oscillator Circuitry

7.8 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages.

It consists of:

1. 2X, 3X, 4X and 5X DC-DC voltage converter
2. Bias Divider
   If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{out}) to give the LCD driving levels (V_{L2} - V_{L5}).
   The divider does not require external capacitors to reduce the external hardware and pin counts.
3. Contrast Control
   Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry
   Software control of 1/4 to 1/9 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (PTC3) value is -0.05%/°C.

7.9 161 Bit Latch

A register carries the display signal information. In 96 X 65 display-mode, data will be fed to the HV-buffer Cell and level-shifted to the required level.

7.10 Level selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

7.11 HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter, which translated the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.12 Default Value after hardware reset

When RES input is low, the chip is initialized to the following:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display ON/OFF	0	Display OFF
Display Start Line	0	GDDRAM page 0,D0
Display Offset	0	COM0 is mapped to ROW0
Mux Ratio	40H	64 Mux
Normal/Reverse Display	0	Normal Display
N-line Inversion	0	No N-line Inversion
Entire Display	0	Entire Display is OFF
DC-DC booster	3	2X booster is selected
Internal Resistor Ratio	0	Gain = 2.3 (IR0)
Contrast	20H	
LCD Bias Ratio	5	1/9 Bias Ratio
Scan direction of COM	0	Normal Scan direction
Segment Remap	0	Segment remap is disabled
Internal oscillator	0	Internal oscillator is OFF
Temperature coefficient	2	PTC3 (-0.05%/^{o}C)
Icon display	0	Icon display line is OFF
Frame frequency	2	Frame frequency = 75Hz
Power control	0,0,0	Booster, regulator & divider are both disabled

When RESET command is issued, the following parameters are initialized only:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 2.3 (IR0)
Contrast	20H	

7.13 LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 6and Figure 7 illustrate the desired multiplex scheme with N-line inversion feature is disabled (default).

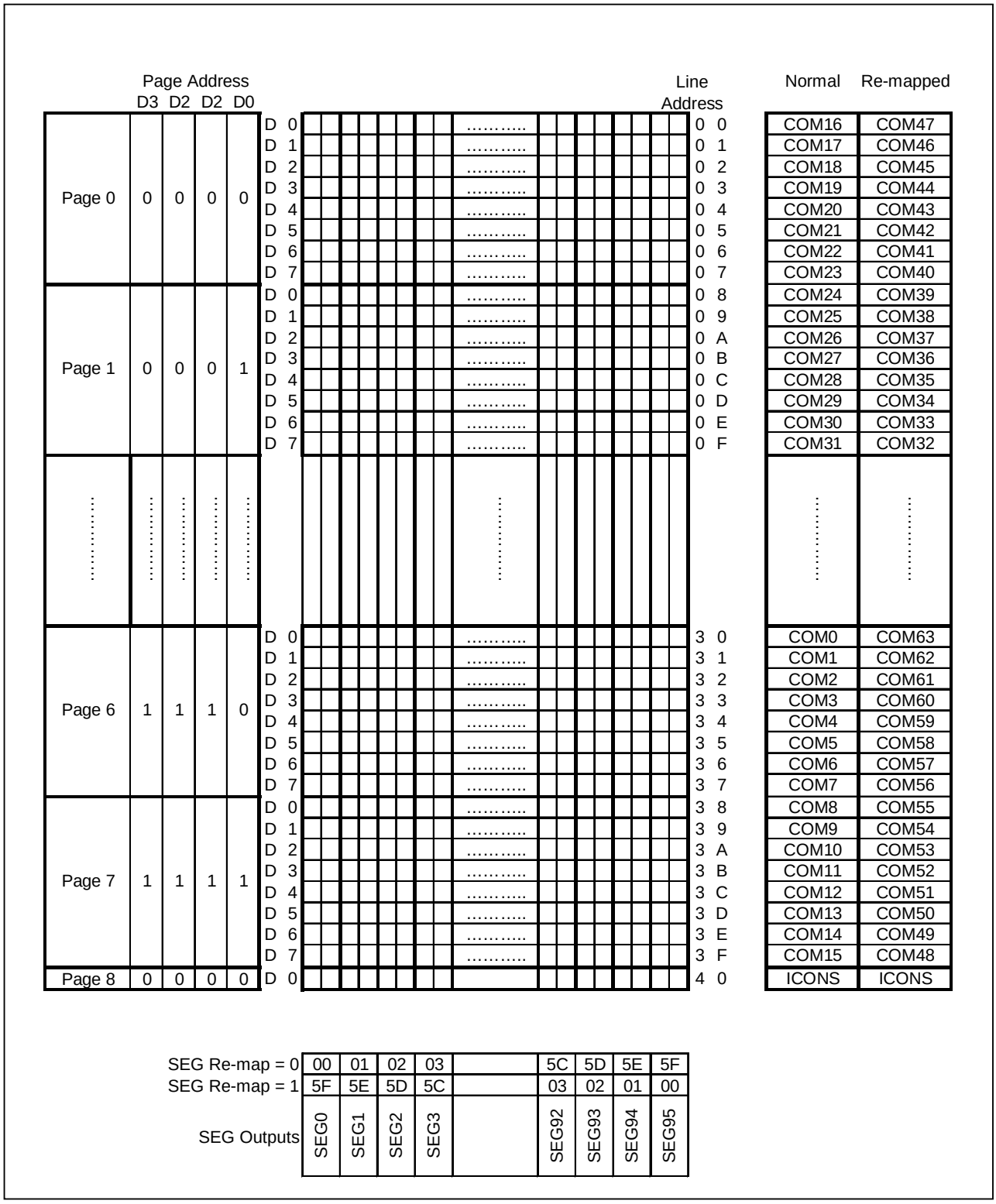


Figure 5 - SSD1828 Graphic Display Data RAM (GDDRAM) Address Map (with vertical scroll value 30H)

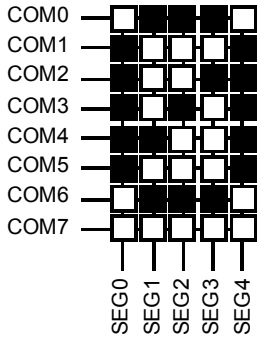
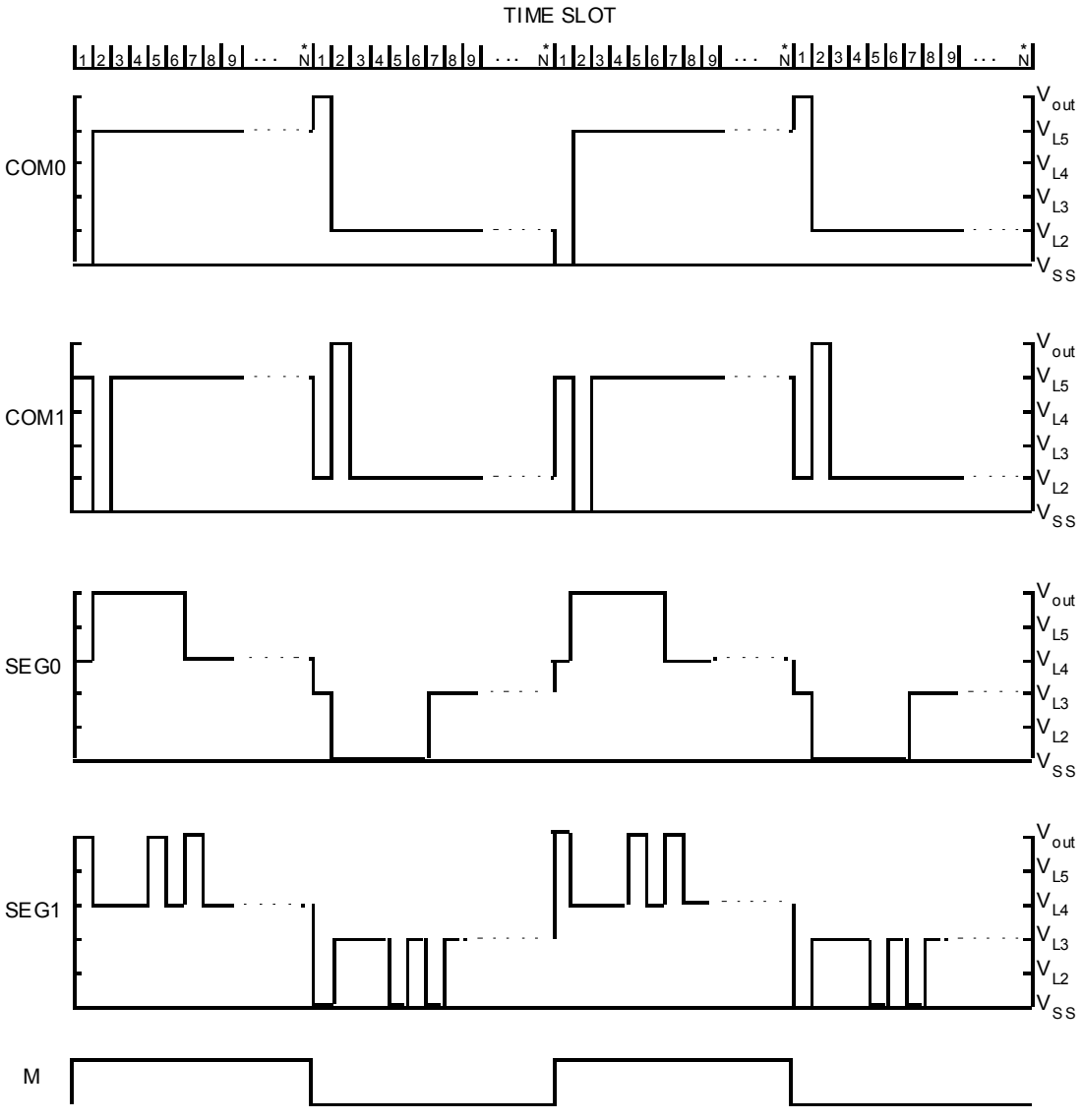


Figure 6 - LCD Display Example "0"



* Note : N is the number of multiplex ratio including Icon line if it is enabled, N is equal to 64 on POR.

Figure 7 - LCD Driving Signal from SSD1828

COMMAND TABLE

Table 6 - COMMAND TABLE

Bit Pattern	Command	Description
0000 $C_3C_2C_1C_0$	Set Column LSB	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0001 $0C_6C_5C_4$	Set Column MSB	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
0010 $0R_2R_1R_0$	Set Internal Resistor Ratio	The internal regulator gain ($1+R_2/R_1$) Vout increases as $R_2R_1R_0$ is increased from 000b to 111b. The factor, $1+R_2/R_1$, is given by: $R_2R_1R_0$ = 000: 2.3 (POR) $R_2R_1R_0$ = 001: 3.0 $R_2R_1R_0$ = 010: 3.7 $R_2R_1R_0$ = 011: 4.4 $R_2R_1R_0$ = 100: 5.1 $R_2R_1R_0$ = 101: 5.8 $R_2R_1R_0$ = 110: Reserved $R_2R_1R_0$ = 111: Reserved (Refer to 8.14)
0010 1VC VR VF	Set Voltage Control	VC VR = 00: turn OFF the internal voltage booster & regulator (POR) VC VR = 01,10,11: turn ON the internal voltage booster & regulator VF=0: turn OFF the output op-amp buffer (POR) VF=1: turn ON the output op-amp buffer
0011 $1T_2T_1T_0$	Set TC value	This command set the Temperature Coefficient $T_2T_1T_0$: 001: -0.035%/^{o}C 010: -0.035%/^{o}C 011: -0.05%/^{o}C (POR) 100: -0.083%/^{o}C
0100 00XX $XL_6L_5L_4$ $L_3L_2L_1L_0$	Set Initial Display Line	The second command specifies the row address pointer (0-63) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
0100 01XX XXC_5C_4 $C_3C_2C_1C_0$	Set Initial COM0	The second command specifies the mapping of first display line (COM0) to one of ROW0~63. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

Bit Pattern	Command	Description
0100 10XX $XD_6D_5D_4$ $D_3D_2D_1D_0$	Set Multiplex Ratio (partial display)	The second command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), 16~64 mux could be selected. With Icon enabled, the available mux are 17~ 65. D6 – D0 Mux (Icon disable) Mux (Icon enable) 000000 invalid invalid … 0001111 invalid invalid 0010000 16 17 0010001 17 18 … 1000000 64 65 1000001 invalid invalid 1000010 invalid invalid … 1111111 invalid invalid
0100 11XX $XXXN_4$ $N_3N_2N_1N_0$	Set N-line Inversion	The second command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
0101 $0B_2B_1B_0$	Set LCD Bias	Sets the LCD bias from 1/4 ~ 1/9 according to $B_2B_1B_0$: 000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7 bias 100: 1/8 bias 101: 1/9 bias (POR) 110: 1/9 bias 111: 1/9 bias
0110 $01B_1B_0$	Set Boost Level	Set the DC-DC multiplying factor from 2X to 5X B_1B_0: 00: 3X 01: 4X 10: 5X 11: 2X (POR)
1000 0001 XXC_5C_4 $C_3C_2C_1C_0$	Set Contrast Level	The second command sets one of the 64 contrast levels. The darkness increase as the contrast level increase.
1010 $000S_0$	Set Segment Re-map	S_0=0: column address 00H is mapped to SEG0 (POR) S_0=1: column address 5FH is mapped to SEG0
1010 $001C_0$	Icon Control Register ON/OFF	C_0=0: Disable icon row (Mux = 16 to 64, POR) C_0=1: Enable icon row (Mux = 17 to 65)
1010 $010E_0$	Entire Display Select	E_0=0: Normal display (display according to RAM contents, POR) E_0=1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of “Set Normal/Invert Display”
1010 $011R_0$	Invert Display Select	R_0=0: Normal display (display according to RAM contents, POR) R_0=1: Invert display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon lines

Bit Pattern	Command	Description
1010 1000	NOP	No operation
1010 1001	Power Save Mode	Sleep Mode: Oscillator: OFF LCD Power Supply: OFF COM/SEG Outputs: V_{SS}
1010 1011	Start Internal Oscillator	This command starts the internal oscillator. Note that the oscillator is OFF after reset, so this instruction must be executed for initialization
1010 111D_0	Display On/Off	Turn the display on and off without modifying the content of the RAM. (0: off, 1: on) This command has priority over Entire Display On/Off and Invert Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.
1011 $P_3P_2P_1P_0$	Set Page Address	Set GDDRAM page address (0~8) using $P_3P_2P_1P_0$ for RAM access. The page address is sets to 0 after reset.
1100 S_0XXX	Set COM Scan Direction	Set the COM (row) scanning direction. (0: COM0 →COM63, 1: COM63 →COM0)
1101 1$F_2F_1F_0$	Set Frame Frequency	This command is used to set the frame frequency. $F_2F_1F_0$ Frame Frequency 000 68 001 73 010 75 (POR) 011 80 100 80 101 86 110 90 111 100
1110 0001	Exit Power-save Mode	DC-DC converter, regulator and divider status before entering the power-save mode is restored. At POR, Power-save Mode is released.
1110 0010	Software Reset	Reset some functions of the driver/controller. See Reset Section below for more details.
1110 0100	Release N-line Inversion Mode	Release the driver/controller from N-line inversion mode. The frame will be inverted once per frame
1110 1000 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	Display Data Length	This command is used in 3-line SPI mode (without D/C line) to specify that the controller is about to send display data to the display RAM. Eight bits are used to specify the number of bytes to be sent (1 to 256 bytes). The second command received after the display data is transmitted is assumed to be command data.

Table 7 – Extended Command Table

Bit Pattern	Command	Comment
1111 0010 0000 $X_0$000	Enable external oscillator input	Select external oscillator input form CL pin. X_0 = 0 : (POR) internal RC oscillator X_0 = 1 : external square wave
Other than above	Reserved	

7.14 Read Status Byte

A 8 bits status byte will be placed to the data bus if a read operation is performed if D/C is low. The status byte is defined as follow.

Table 8 - Read Status Byte

Bit Pattern	Command	Comment
BUSY ON RES 0 1000	Read Status	BUSY=0: Chip is idle BUSY=1: Chip is executing instruction ON=0: Display is OFF ON=1: Display is ON RES=0: Chip is idle RES=1: Chip is executing reset

7.15 Data Read / Write

To read data from the GDDRAM, input High to R/W(WR#) pin and D/C pin for 6800-series parallel mode. Low to E(RD#) pin and High to D/C pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W(WR#) pin and High to D/C pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. The address will be reset to 0 in next data read/write operation is executed when it is 95.

Table 9 - Address Increment Table

D/C	R/W (WR)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM is also affected. It will be reset to 0 in next data read/write operation is executed when it is 95.

Table 10 - Commands Required for R/W (WR#) Actions on RAM

R/W (WR) Actions on RAMs	Commands Required	
Read/write Data from/to GDDRAM	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	(1011$X_3X_2X_1X_0$)* (0001$X_3X_2X_1X_0$)* (0000$X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$)

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

8 COMMAND DESCRIPTIONS

8.1 Set Display On/Off

This command turns the display on/off, by the value of the LSB.

8.2 Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

8.3 Set Page Address

This command positions the page address to 0 to 8 possible positions in GDDRAM. Refer to Figure 5.

8.4 Set Higher Column Address

This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95).

8.5 Set Lower Column Address

This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>95).

8.6 Set Temperature Coefficient (TC) Value

This command is to set 1 out of 4 different temperature coefficients in order to match various liquid crystal temperature grades.

8.7 Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to Figure 5.

8.8 Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an “ON” pixel while in reverse display; a RAM data of 0 indicates an “ON” pixel. The icon line is not affected by this command.

8.9 Set Entire Display On/Off

This command forces the entire display, including the icon row, to be “ON” regardless of the contents of the display data RAM. This command has priority over normal/reverse display. To execute this command, Set Display On command must be sent in advance.

8.10 Set LCD Bias

This command selects a suitable bias ratio (1/4 to 1/9) required for driving the particular LCD panel in use. The POR is set to 1/9 bias.

8.11 Software Reset

This command causes some of the internal status of the chip to be initialized:

Register	Default Value	Remarks:
Page address	0	
Column address	0	
Display Start Line	0	GDDRAM page 0,D0
Internal Resistor Ratio	0	Gain = 2.3 (IR0)
Contrast	20H	

8.12 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

8.13 Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power relating sub-circuits could be turned on/off by this command.

Internal voltage booster is used to generate the highest positive voltage supply internally from the voltage input (V_{CI} -V_{SS}).

Internal regulator is used to generate the LCD driving voltage.

Output op-amp buffer is the internal divider for dividing the different voltage levels (V_{L2}, V_{L3}, V_{L4}, V_{L5}) from the internal regulator output, V_{out}. External voltage sources should be fed into this driver if this circuit is turned off.

8.14 Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref} \qquad , where\ Vref = 2.1V$$

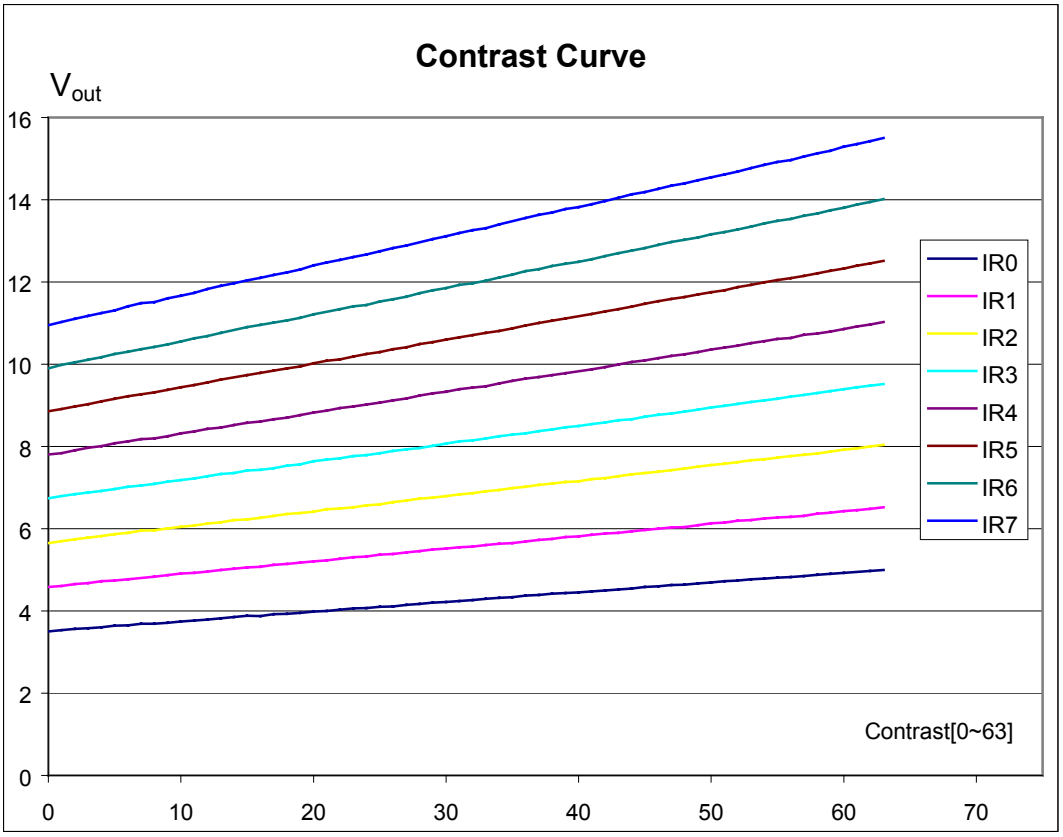


Figure 8 - Contrast Control Voltage Range Curve (V_{DD}=2.775V; V_{CI}=3.5V; TC=-0.05%/°C)

8.15 Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing V_{out} of the LCD drive voltage provided by the On-Chip power circuits. V_{out} is set with 64 steps (6-bit) contrast control register. It is a compound commands:

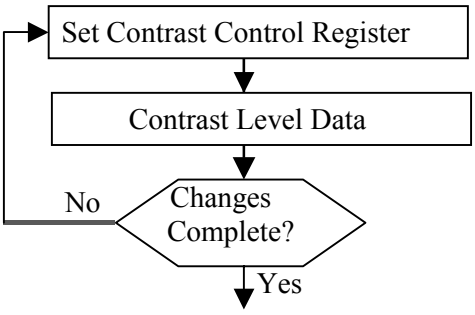


Figure 9 - Contrast Control Flow Set Segment Re-map

8.16 Set Frame Frequency

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 75Hz at 64 mux after POR.

8.17 Set Multiplex Ratio

This command switches default 64 multiplex modes to any multiplex from 16 to 64, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 65. The chip pads ROW0-ROW63 will be switched to corresponding COM signal output as specified in Table 2.

8.18 Set Power Save Mode

Force the chip to enter Standby or Sleep Mode. LSB of the command will define which mode will be entered.

8.19 Exit Power Save Mode

This command releases the chip from Sleep Mode and return to normal operation.

8.20 Set N-line Inversion

Number of line inversion is set by this command for reducing crosstalk noise. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.
It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

8.21 Exit N-line Inversion

This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

8.22 Set DC-DC Converter Factor

Internal DC-DC converter factor is set by this command. For SSD1828, 2X to 5X multiplying factors could be selected. 2X to 5X factors are selected using this command.

8.23 Set Icon Enable

This command enable/disable the Icon displays.

8.24 Start Internal Oscillator

After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

8.25 Set Display Data Length

This two-bytes command only valid when 3-wire SPI configuration is set by H/W input (PS0=PS1=L). The second 8-bit is used to indicate that a specified number display data byte(s) (1-256) are to be transmitted. Next byte after the display data string is handled as a command.

8.26 Set Test Mode

This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

8.27 Status Register Read

This command is issued by setting D/C Low during a data read (refer to figure 1 and 2 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to trigger the enhanced features, on top of general ones, designed for the chip.

8.28 Enable external oscillator input.

This command enables the external clock input from CL pin and expected external square wave is 58.5kHz.

9 MAXIMUM RATINGS

Table 11 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 5.5	V
V_{CC}		V_{SS} -0.3 to V_{SS} +12.0	V
V_{CI}	Booster Supply Voltage	V_{DD} to +5.5	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}). Unused outputs must be open. This device may be light sensitive. Caution should be taken to avoid exposure of this device any light source during normal operation. This device is not radiation protected.

10 DC CHARACTERISTICS

Table 12 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 1.8 to 3.3V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
V_{CI}	Booster Voltage Supply Pin	(Absolute value referenced to V_{SS})	V_{DD}	-	3.6	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X DC-DC Converter Enabled, Write accessing, T_{cyc} =3.3MHz, Osc. Freq.=58.5kHz, Display On.	-	600	800	uA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} & V_{CI} Pins)	V_{DD} =V_{CI} = 2.7V, Voltage Generator off, external V_{out} Divider Enable. Read/Write Halt, Osc. Freq. = 58.5kHz, Display On, V_{out} = 10.0V.	-	20	40	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} &V_{CI} Pins)	V_{DD} = 1.8V, V_{CI} = 2.5V, Voltage Generator ON, 5x DC-DC Converter Enabled, Internal V_{out} Divider Enable. Read/Write Halt, Osc Freq. = 58.5kHz, Display On, V_{out} = 10.0V, no panel loading.	-	100	150	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (VDD Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, Read/Write halt.	-	0.5	1	µA
V_{out}	LCD Driving Voltage Generator Output (V_{out} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Regulator Enabled, Osc. Freq. = 58.5kHz,	4.0	-	12.0	V
	DC-DC Converter Efficiency (Without loading)		-	95	-	%
V_{LCD}	LCD Driving Voltage Input (V_{out} Pin)	Voltage Generator Disabled	4.0	-	12.0	V
V_{OH1}	Output High Voltage (D_0-D_7)	I_{out} = +500µA	0.8*V_{DD}	-	V_{DD}	V_{LCD}
V_{OL1}	Out Low Voltage (D_0-D_7)	I_{out} = -500µA	0	-	0.2*V_{DD}	V
V_{out}	LCD Driving Voltage Source (V_{out} Pin)	Regulator Enabled (V_{out} voltage depends on Internal contrast Control)	V_{DD}	-	12.0	V
V_{out}	LCD Driving Voltage Source (V_{out} Pin)	Regulator Disable	-	Floating	-	V
V_{IH1}	Input high voltage (/RES, PS0, PS1, /CS, D/C, R/W, D_0-D_7)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input low voltage (/RES, PS0, PS1, /CS, D/C, R/W, D_0-D_7)		0	-	0.2*V_{DD}	V
V_{out}	LCD Display Voltage Output	Bias Divider Enabled, 1:a bias ratio	-	V_{out}	-	V
V_{L5}	(V_{out}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)\		-	(a-1)/a*V_{out}	-	V
V_{L4}			-	(a-2)/a*V_{out}	-	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{L3}			-	2/a* V_{out}	-	V
V_{L2}			-	1/a* V_{out}	-	V
V_{out}	LCD Display Voltage Input (V_{out}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Voltage reference to V_{SS}, External Voltage Generator, Bias Diver Disabled	V_{L5}	-		V
V_{L5}			V_{L4}	-	V_{out}	V
V_{L4}			V_{L3}	-	V_{L5}	V
V_{L3}			V_{L2}	-	V_{L4}	V
V_{L2}			V_{SS}		V_{L3}	V
I_{OH}	Output High Current Source (D_0-D_7)	Output Voltage=V DD -0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D_0-D_7)	Output Voltage = 0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Source (D_0-D_7)		-1	-	1	µA
I_{IL} /I_{IH}	Input Current (RES , PS0, PS1, CS , E, D/C, R/W, D_0-D_7		-1	-	1	µA
C_{IN}	Input Capacitance (all logic pins)		-	5	7.5	PF
ΔV_{out}	Variation of Vout Output (1.8V < V_{DD} < 3.3V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	±1	-	%
V_{ref}	Reference Voltage (T= 25ºC)		2.04	2.1	2.16	V
	Reference Voltage (T= -20ºC)		2.09	2.15	2.21	V
	Reference Voltage (T= 70ºC)		1.99	2.05	2.11	V
	Temperature Coefficient Compensation					
PTC1	Temperature Coefficient 1*	Voltage Regulator Enabled	0	-0.01	-0.02	%/°C
PTC2	Temperature Coefficient 2*	Voltage Regulator Enabled	-0.025	-0.035	-0.045	%/°C
PTC3	Temperature Coefficient 3*(POR)	Voltage Regulator Enabled	-0.04	-0.05	-0.06	%/°C
PTC4	Temperature Coefficient 4*	Voltage Regulator Enabled	-0.07	-0.083	-0.096	%/°C

* The formula for the temperature coefficient is:

$$TC(\%)= \frac{V_{out}\ 50ºC - V_{out}\ at\ 0ºC}{50ºC - 0ºC} \times \frac{1}{V_{out}\ at\ 25ºC} \times 100\%$$

11 AC CHARACTERISTICS

Table 13 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, $V_{DD} = V_{CI} = 2.7V$, $T_A = -40$ to $85°C$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{osc}	Oscillator frequency	Display ON, Set 96 x 64 Graphic Display Mode, Icon Line Disabled	50.7	58.5	78	kHz
F_{FRM}	Frame Frequency	Display ON, Set 96 x 64 Graphic Display Mode, Icon Line Disabled	65	75	100	Hz

Table 14 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 1.8V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	200	1000	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 200	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

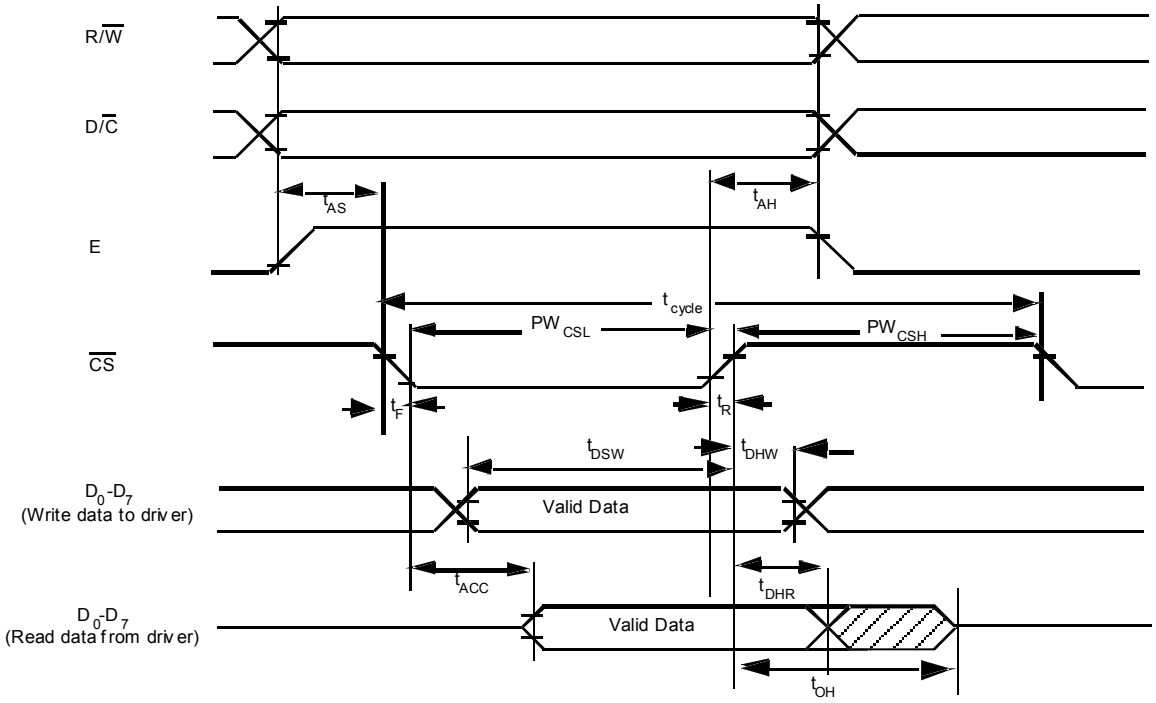


Figure 10 – Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 15 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.7, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	500	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 100	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

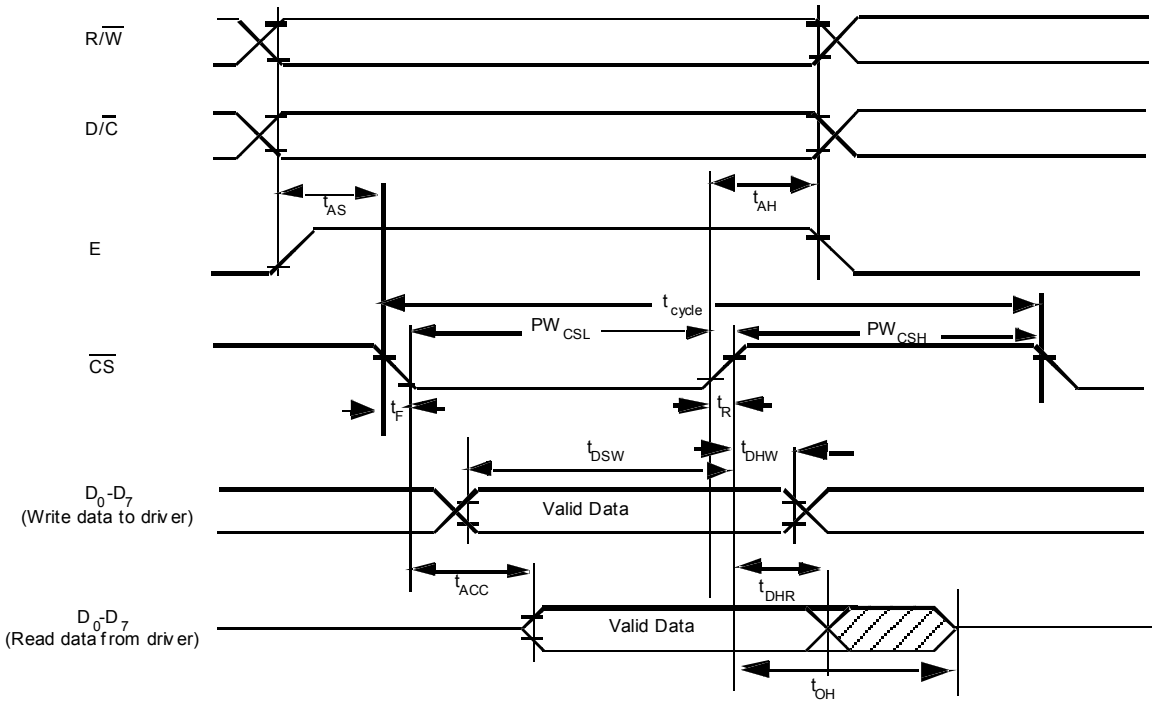


Figure 11 – Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 16 - Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 1.8V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	200	1000	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	500 500 100	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	200 200	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

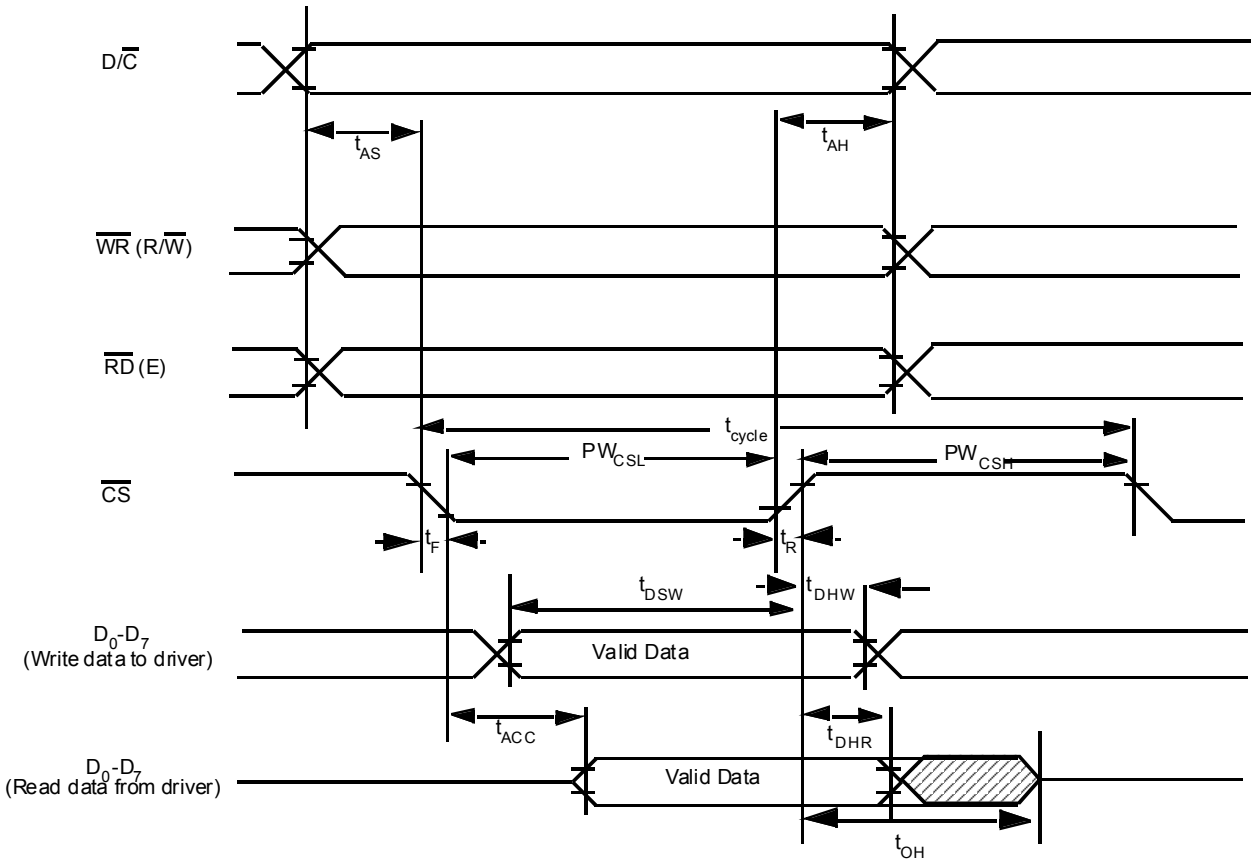


Figure 12 - Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 17 - Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.7V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	500	-	ns
t_{AS}	Address Setup Time	0	-	25	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	50	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (command)	15 15	- -	- -	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	100 100	- -	- -	ns ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

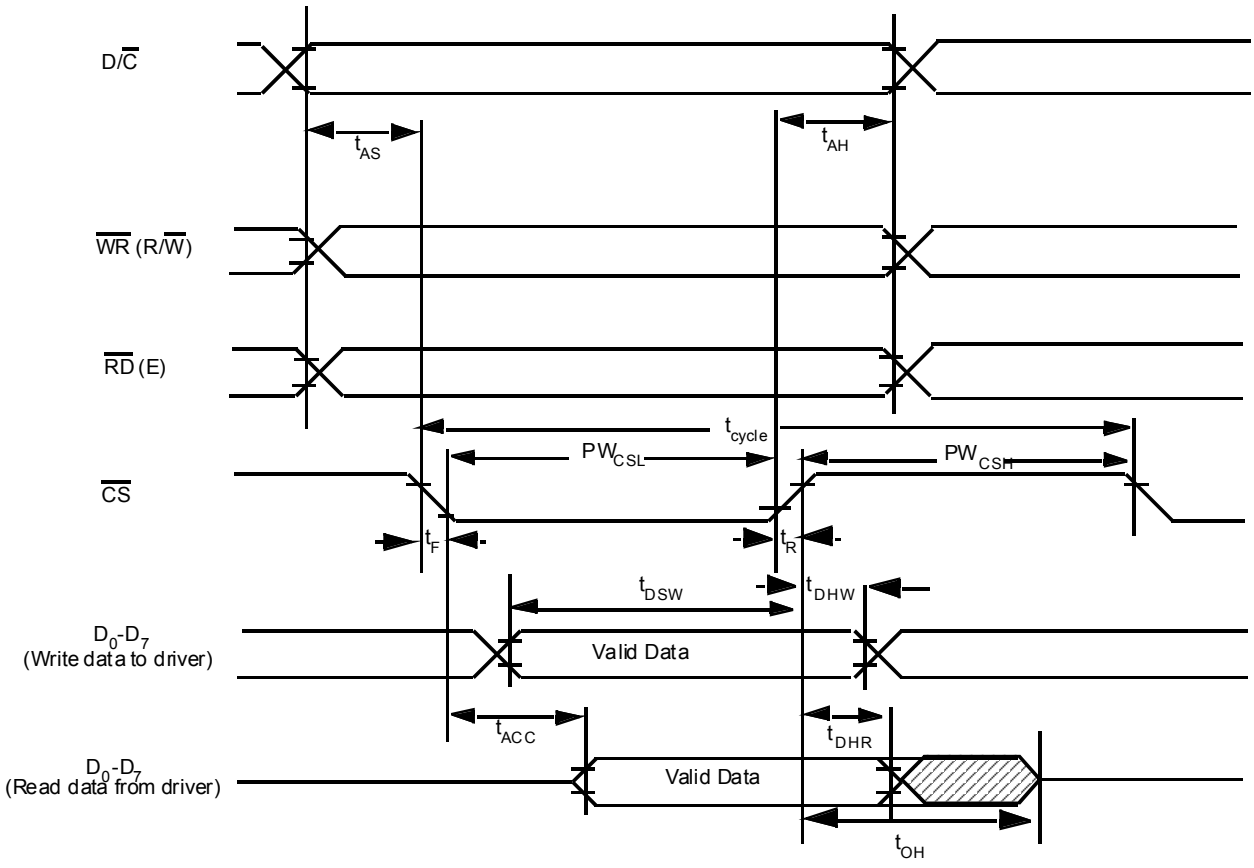


Figure 13 - Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 18 – Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.7V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	58.8	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	30	-	-	ns
t_{CSH}	Chip Select Hold Time	29.4	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{OHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	29.4	-	-	ns
t_{CLKH}	Clock High Time	29.4	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

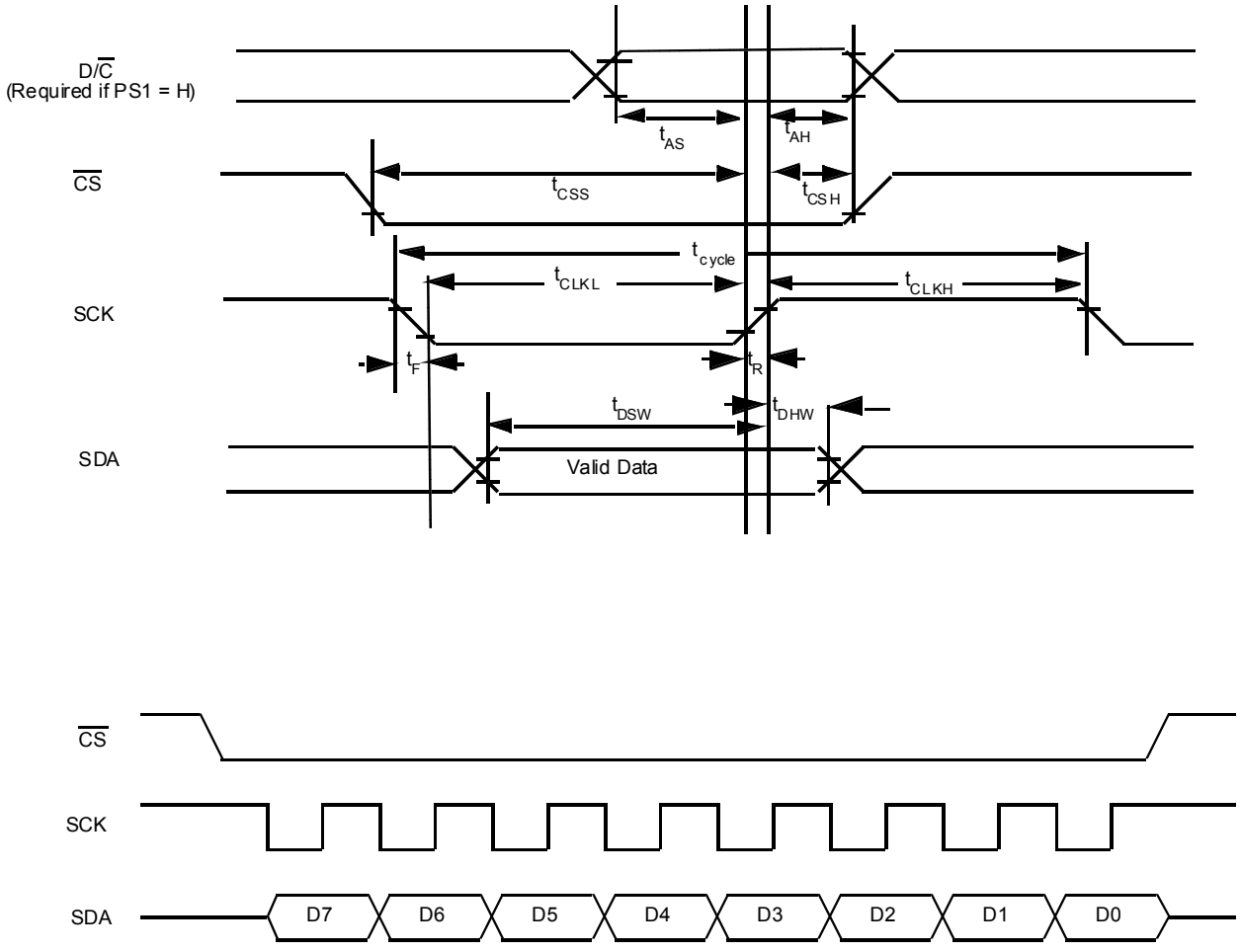


Figure 14- Serial Timing Characteristics (PS0 = L)

Table 19 – Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 1.8V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	111	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	60	-	-	ns
t_{CSH}	Chip Select Hold Time	55.5	-	-	ns
t_{DSW}	Write Data Setup Time	60	-	-	ns
t_{OHW}	Write Data Hold Time	60	-	-	ns
t_{CLKL}	Clock Low Time	55.5	-	-	ns
t_{CLKH}	Clock High Time	55.5	-		ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

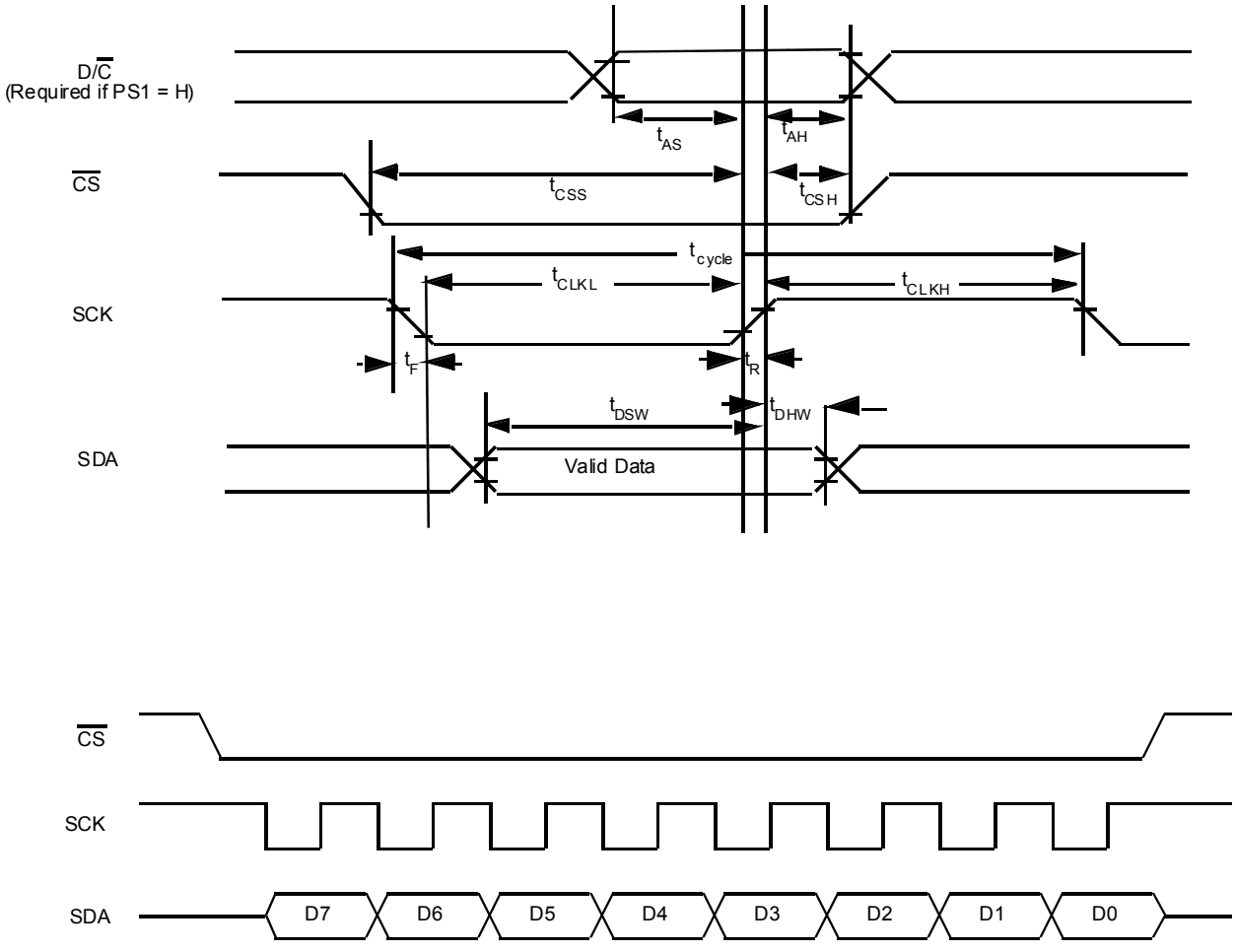
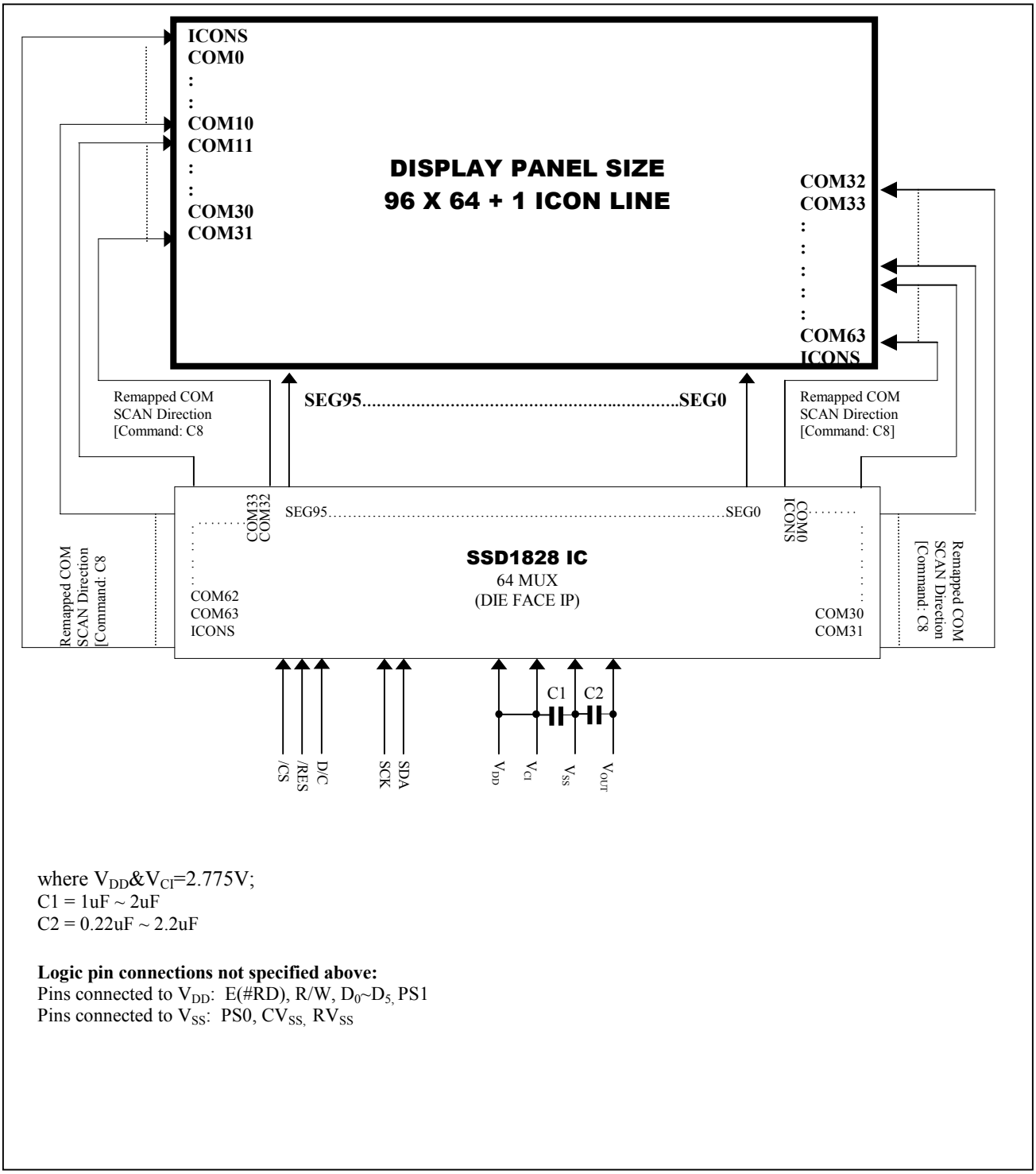


Figure 15 - Serial Timing Characteristics (PS0 = L)

12 APPLICATION EXAMPLES



where V_{DD}&V_{CI}=2.775V;
C1 = 1uF ~ 2uF
C2 = 0.22uF ~ 2.2uF

Logic pin connections not specified above:
Pins connected to V_{DD}: E(#RD), R/W, D_0~D_5, PS1
Pins connected to V_{SS}: PS0, CV_{SS}, RV_{SS}

Figure 16 - Typical Application (4-wires SPI mode)

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