OVERVIEW

The SM6150P/S is a successive-approximation 8-bit A/D converter, fabricated using the Molybdenum-gate CMOS process. It's low-voltage operation makes it ideal for battery-powered portable equipment.

The output comprises 8-bit parallel 3-state output pins for easy interface with a microprocessor. Also, it features an 8-channel analog multiplexer built-in.

It also features a power-save function which automatically reduces the supply current and reference voltage pin input current when no conversion is taking place.

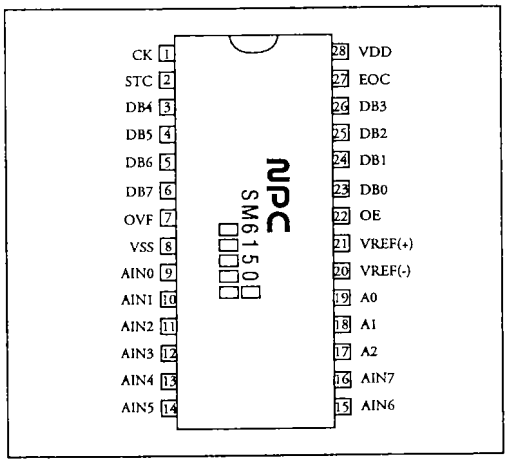
FEATURES

- Charge-redistribution method, successive-approximation A/D converter
- 8-bit resolution
- 19 µs conversion time (f_{CK} = 2 MHz)
- 2.8 to 5.5 V operating supply voltage range
- Low current consumption
  - ≤ 3 mA during conversion
  - Standby current
    - ≤ 100 µA (f_{CK} = 2 MHz)
    - ≤ 10 µA (with no input clock)
- High precision
  - ≤ ±0.75 LSB non-linearity error
- Easy interface with a microprocessor
- 8-channel analog multiplexer built-in
- Molybdenum-gate CMOS process
- 28-pin plastic SOP and DIP

APPLICATIONS

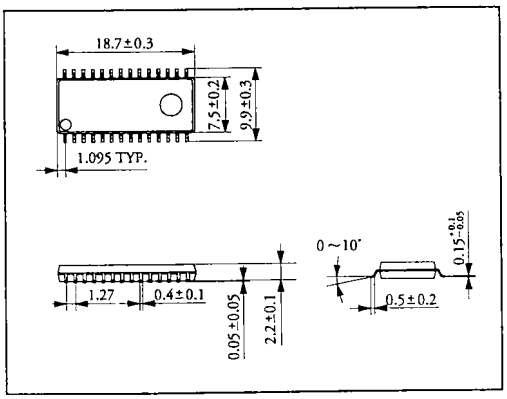
- Data acquisition systems
- Measurement equipment

PINOUT

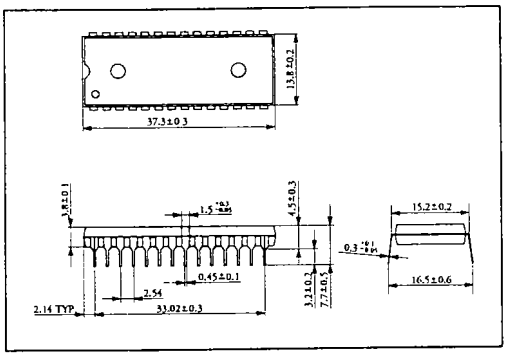


PACKAGE DIMENSIONS

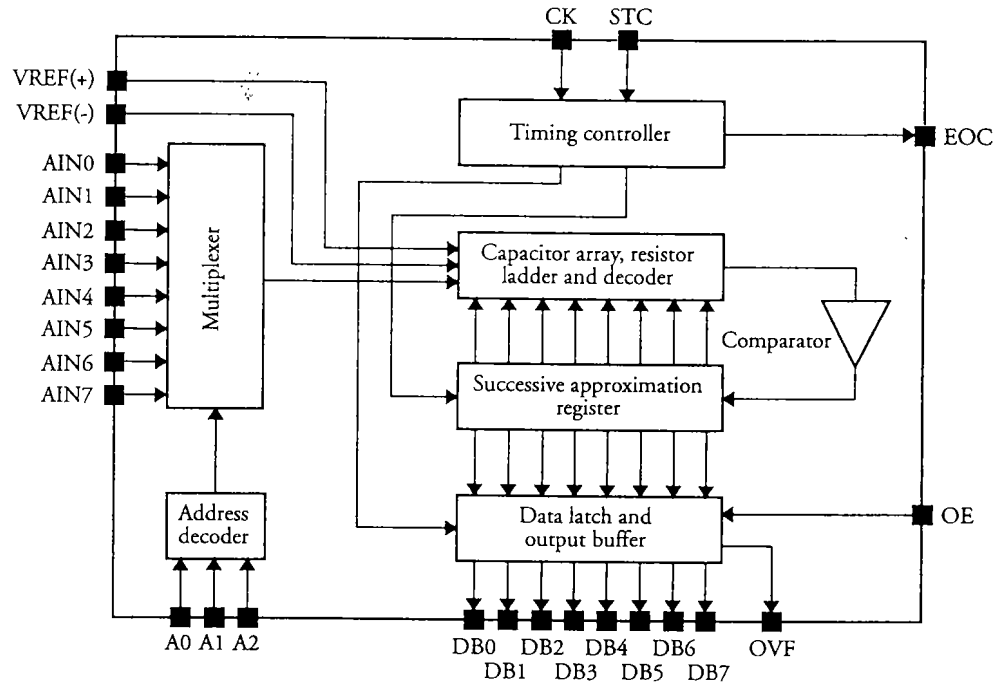
28-pin SOP (Unit: mm)



28-pin DIP (Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	CK	Conversion operation clock input
2	STC	Conversion start signal. Conversion starts on a LOW-to-HIGH transition.
3	DB4	3-state output bit 4
4	DB5	3-state output bit 5
5	DB6	3-state output bit 6
6	DB7	3-state output bit 7 (MSB)
7	OVF	Overflow indicator output pin. Overflow when HIGH.
8	VSS	Ground
9	AIN0	Analog input channel 0
10	AIN1	Analog input channel 1
11	AIN2	Analog input channel 2
12	AIN3	Analog input channel 3
13	AIN4	Analog input channel 4
14	AIN5	Analog input channel 5
15	AIN6	Analog input channel 6
16	AIN7	Analog input channel 7
17	A2	Analog input channel input select pins. Pull-down resistors built-in.
18	A1	
19	A0	

Number	Name	Description
20	VREF(–)	Reference voltage input pin (–)
21	VREF(+)	Reference voltage input pin (+)
22	OE	Data output enable signal. DB0 to DB7 are output when HIGH, and high-impedance when LOW.
23	DB0	Three-state output bit 0 (LSB)
24	DB1	Three-state output bit 1
25	DB2	Three-state output bit 2
26	DB3	Three-state output bit 3
27	EOC	End-of-conversion signal. LOW when STC goes HIGH. Returns HIGH when conversion ends.
28	VDD	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0$ V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	– 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	250	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

$V_{SS} = 0$ V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.8	–	5.5	V
VREF(+)-to-VREF(–) voltage	V_{REF}		2.0	–	V_{DD}	V
Clock frequency	f_{CK}		0.01	–	2.0	MHz
Operating temperature	T_{opr}		–20	–	70	°c

DC Electrical Characteristics

V_{DD} = 2.8 to 5.5 V, T_a = –20 to 70 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CK, STC, OE and A0 to A2 HIGH-level input voltage	V_{IH}		$0.7V_{DD}$	–	–	V
CK, STC, OE and A0 to A2 LOW-level input voltage	V_{IL}		–	–	$0.3V_{DD}$	V

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
CK, STC and OE HIGH-level input current	I_{IH1}	$V_{IH} = V_{DD}$		–	–	1	μA
A0 to A2 HIGH-level input current	I_{IH2}			–	60	–	μA
CK, STC, OE and A0 to A2 LOW-level input current	I_{IL}	$V_{IL} = V_{SS}$		–1	–	–	μA
DB0 to DB7, OVF and EOC HIGH-level output voltage	V_{OH}	I_{source} = 0.8 mA		V_{DD} – 0.4	–	–	V
DB0 to DB7, OVF and EOC LOW-level output voltage	V_{OL}	I_{sink} = 0.8 mA		–	–	0.4	V
DB0 to DB7 high-impedance leakage current	I_{leak}	$V_{OUT} = V_{DD}$		–	–	3	μA
		$V_{OUT} = V_{SS}$		–3	–	–	μA
AIN0 to AIN7 analog input current	I_{AIN}	$V_{AIN} = V_{DD}$		–	–	3	μA
		$V_{AIN} = V_{SS}$		–3	–	–	μA
Operating current consumption	I_{DD}	f_{CK} = 2 MHz	V_{DD} = 5.5 V	–	1.5	3.0	mA
			V_{DD} = 2.8 V	–	0.3	–	mA
Standby current	I_{DS1}	f_{CK} = 2 MHz		–	1	100	μA
	I_{DS2}	$V_{CK} = V_{SS}$ or V_{DD}		–	1	10	μA
VREF(+)-to-VREF(–) reference resistance	R_{REF}	Conversion operation		–	16	–	kΩ
		In standby mode		10	–	–	MΩ

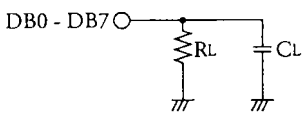
AC Electrical Characteristics

V_{DD} = 2.8 to 5.5 V, T_a = –20 to 70 °C unless otherwise noted

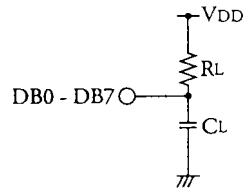
Parameter[1]	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time[2]	t_{TLH}	C_L = 20 pF	–	–	100	ns
Output fall time[2]	t_{THL}	C_L = 20 pF	–	–	100	ns
3-state output enable time[3]	t_{PZH}, t_{PZL}	C_L = 20 pF, R_L = 10 kΩ	–	–	200	ns
3-state output disable time[4]	t_{PHZ}, t_{PLZ}	C_L = 20 pF, R_L = 10 kΩ	–	–	200	ns
STC pulsewidth	t_{WSTC}		150	–	–	ns
STC to EOC propagation delay	t_{SE}	C_L = 20 pF	–	–	150	ns
Data to EOC propagation delay	t_{DE}	C_L = 20 pF	0	1	–	clock cycle

1. All times are measured from when the input control signal output level reaches the 50% point.
2. Rise and fall times are measured between the output level 10% and 90% points.
3. Measured with the following load circuit, when the data output has been 50% converted.
4. Measured with the following load circuit, when the data output has been 10% converted.

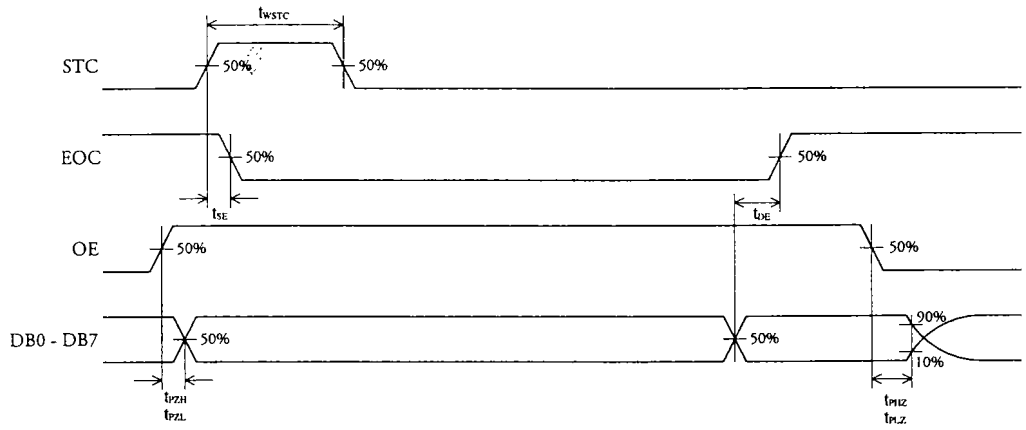
t_{PHZ}, t_{PZH} load circuit



t_{PLZ}, t_{PZL} load circuit



AC Timing



Conversion Characteristics

V_{DD} = 2.8 to 5.5 V, VREF(+) = V_{DD}, VREF(−) = V_{SS}, T_a = −20 to 70 °C unless otherwise noted

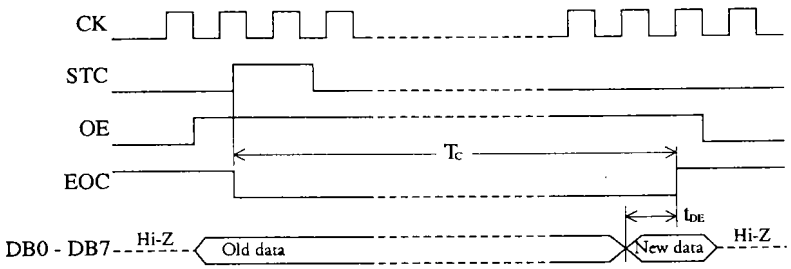
Parameter	Condition	Rating			Unit
		min	typ	max	
Resolution		–	–	8	bits
Non-linearity error		–	–	±0.75	LSB
Differential non-linearity error		–	–	±0.75	LSB
Offset error[1]		–	–	±0.75	LSB
Full-scale error[1]		–	–	±0.75	LSB
Conversion time	f_{CK} = 2 MHz	–	19	–	µs
		37.5	–	38.5	clock cycles

1. The offset error and full-scale error represent the error from the ideal transition points of 0.5 LSB and 254.5 LSB, respectively.

FUNCTIONAL DESCRIPTION

Conversion Operation

When STC goes HIGH, EOC goes LOW and conversion starts. After the conversion time T_C has elapsed, EOC goes HIGH to indicate the end-of-conversion. The data on the output data bus is replaced with the new data a time t_{DE} before EOC goes HIGH. The data bus becomes high impedance when OE goes LOW.



Power-save Function

The device automatically enters power-save mode when there is no conversion operation. At this point, the circuit between the reference voltage inputs VREF(+) and VREF(−) becomes high resistance. In power-save mode, the standby supply current reduces to ≤ 100 µA when the conversion clock frequency is 2 MHz and to ≤ 10 µA when the clock is stopped.

Internal Initialization

When power is first applied, a minimum of 40 conversion clock cycles are required to initialize the internal IC states. The device enters power-save mode when initialization ends.

8-channel Analog Multiplexer Switching

The input channel is selected on the rising edge of STC by the analog input channel select signals A0, A1 and A2.

Input channel select truth table

A2	A1	A0	Channel
0	0	0	AIN0
0	0	1	AIN1
0	1	0	AIN2
0	1	1	AIN3
1	0	0	AIN4
1	0	1	AIN5
1	1	0	AIN6
1	1	1	AIN7