NT56V1616A0T
DATA SHEET

1Mx16
Synchronous DRAM

REV 1.2

August , 2000

Revision History

Revision 1.2 (August, 2000)

- Changed data sheet format
- Changed package dimension format
- Changed

Item		From	To
Voltage on Any Pin Relative to Vss	V_{IN},V_{OUT}	-0.5 to Vcc +0.5 (V)	-1.0 to 4.6 (V)
Voltage on Vcc Supply Relative to Vss	V_{CC}, V_{CCQ}	-0.5 to 4.5 (V)	-1.0 to 4.6 (V)
Input Leakage Current	I_{IL}	-10 ~ +10 µA	-5 ~ +5 µA
Ambient Temperature	Ta	0~65°C	0~70°C

Revision 1.1 (May, 2000)

- Add Timing waveform chart

Revision 1.0 (May, 2000)

- First Version

DESCRIPTION

The NTC 16Meg SDRAM is a high-speed CMOS dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual memory array (512K x 16) with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the two internal banks is organized with 2,048 rows and with either 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command which will then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed (A11 selects the bank, A0-10 selects the row). The address bits coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The NTC 16Meg SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provides seamless high-speed random access operation. The NTC 16Meg SDRAM is designed to comply with the Intel PC (66MHz) and Intel PC/100 (100MHz) specifications.

The NTC 16Meg SDRAM is designed to operate in 3.3V, low-power memory systems. An AUTO REFRESH mode is provided along with a power saving Power-Down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

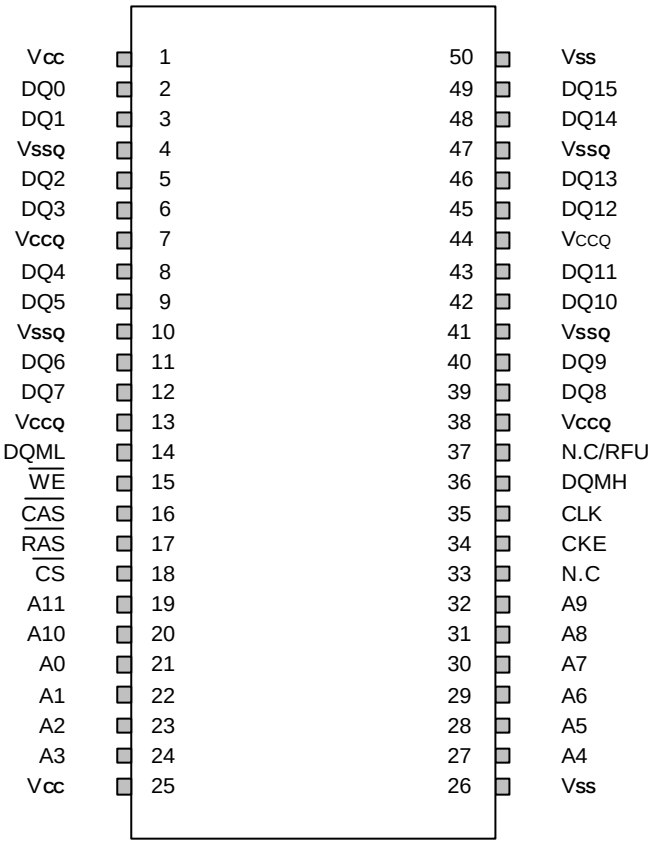
FEATURE

- PC100 compliant functionality and performance.
- JEDEC standard 3.3 V ± 10% power supply.
- LVTTL compatible inputs and outputs.
- All inputs are sampled on positive edge of system clock.
- Dual Banks for hidden row access/precharge.
- Internal pipeline operation, column addresses can be changed every cycle.
- MRS cycle with address key programmability for:
  - CAS latency (2 , 3)
  - Burst Length (1 , 2 , 4 , 8 or full page)
  - Burst Type (Sequential & Interleave)
- DQM for masking.
- Auto Precharge and Auto Refresh modes.
- Self Refresh Mode.
- 64ms , 4096 cycle refresh (15.6 us/row)
- 50–pin 400 mil plastic TSOP (type II) package.

PRODUCT FAMILY

Part NO.	Max Freq.	CL	tAC	Organization	Interface	Package
NT56V1616A0T-7	143 MHz	3	5.5 ns	2Banks x 512Kbits x 16	LVTTL	400mil 50pin TSOP II
NT56V1616A0T-8	125 MHz	3	6 ns			

PIN ASSIGNMENT (Top View)

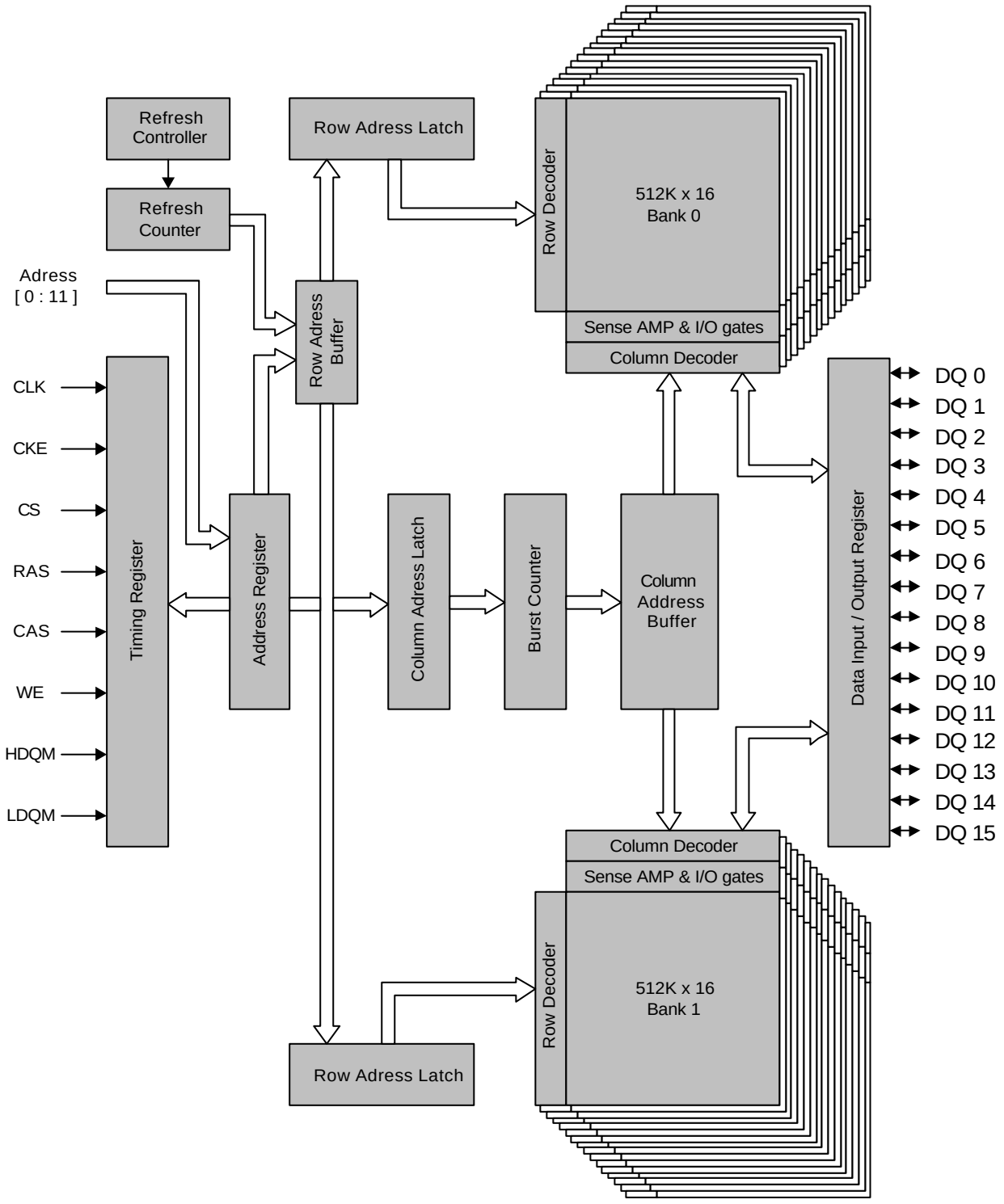


50-pin Plastic TSOP-II

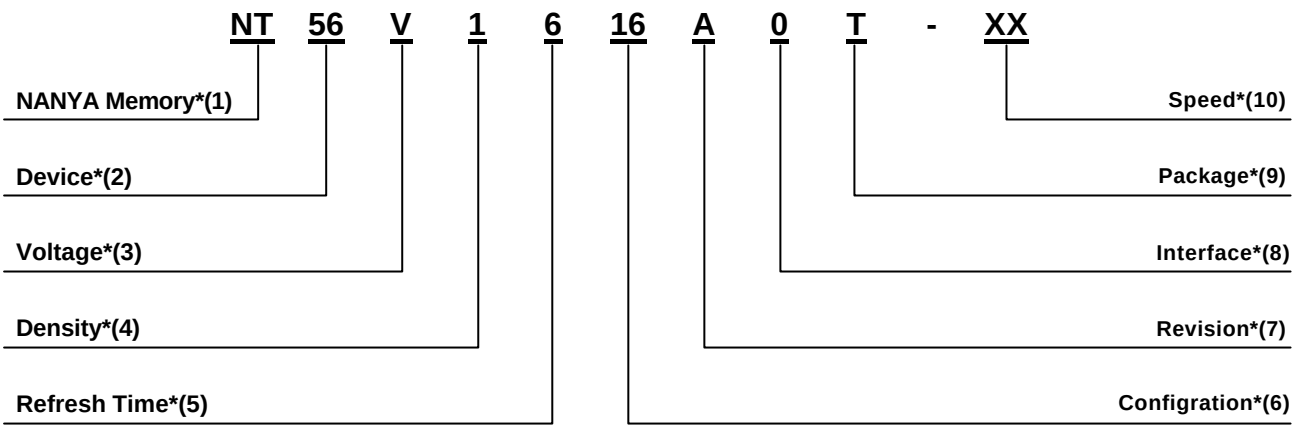
PIN FUNCTIONAL DESCRIPTION

Symbol	Function	Description
A0 – A10 / A11	Address	Row address:RA0 – RA10 ; Column address: CA0 –CA7 ; Bank selection: A11
CLK	System Clock	Fetches all input at the "H" edge.
CKE	Clock Enable	Master system clock to deactivate the subsequent CLK operation.
$\overline{RAS}$	Row address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all controls except CLK, CKE and DQM.L(H)
DQML, DQMH	Data input/output Mask	Active high. Controls the data output buffers in read mode. In write mode it masks the data from being written to the memory array. DQML corresponds to DQ0-DQ7 DQMH corresponds to DQ8-DQ15.
DQi	Data Input/Output	Data I/O are multiplexed on the same table.
NC/RFU	No connect/ Reserved for Future Use	This pin should be left No Connect on the device so that the normal functionality of the device is not effected by the external connection to this pin.
Vcc, Vss	Power supply , Ground	Supply pins for the core.
VccQ, VssQ	Data output power supply , Ground.	Supply pins for the output buffers.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION



(1) NANYA Memory

(2) Device

56 - - - - - - - - SDRAM

(3) Voltage

V - - - - - - - - 3.3V

(4) Density

1 - - - - - - - - 16M
6 - - - - - - - - 64M
2 - - - - - - - - 128M

(5) Refresh Time

7 - - - - - - - - 2K/32ms
6 - - - - - - - - 4K/64ms

(6) Configuration

40 - - - - - - - - 2 bank, x 4
80 - - - - - - - - 2 bank, x 8
16 - - - - - - - - 2 bank, x 16
10 - - - - - - - - 4 bank, x 8

(7) Revision

A - - - - - - - - 1st version
B - - - - - - - - 2nd version
C - - - - - - - - 3rd version
D - - - - - - - - 4th version

(8) Interface

0 - - - - - - - - LVTTL
1 - - - - - - - - SSTL

(9) Package

T - - - - - - - -TSOP II
F - - - - - - - -TQFP
Q - - - - - - - -QFP

(10) Speed

6 - - - - - - - -166MHz
7 - - - - - - - -143MHz
8 - - - - - - - -125MHz
10 - - - - - - - 100MHz

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN},V_{OUT}	-1.0 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}, V_{CCQ}	-1.0 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Ambient Temperature	Ta	0 to 70	°C
Storage Temperature	Tstg	-55 to 150	°C

❖ Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect reliability.

Recommended Operating Condition (Ta=0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}, V_{CCQ}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{cc}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Output High Voltage	V_{OH}	2.4		-	V	I_{OH} =-4.0 mA
Output Low Voltage	V_{OL}	-		0.4	V	I_{OL} = 4.0 mA
Input Leakage Current	I_{IL}	-5		5	uA	1

1. 0<Vln< Vcc Input leakage current includes hi-Z output leakage for all bi-directional buffers with tri-state outputs.

Capacitance

Parameter	Symbol	Min.	Max.	Unit
Input Pin Capacitance	C_{IN}	2.5	5.0	pF
I/O Pin Capacitance	$C_{I/O}$	4.0	6.5	pF
Clock Pin Capacitance	C_{CLK}	2.5	4.0	pF

The Capacitance parameters are sampled by Vcc=3.3V ± 10% , Ta =25°C,f =1 MHZ

DC CHARACTERISTICS

(Vcc=3.3V ± 10% , Ta=0°C to 70°C)

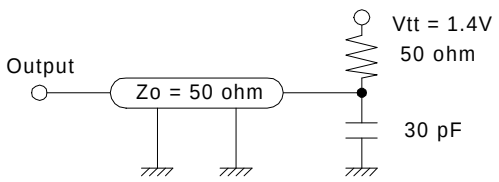
Parameter	Symbol	Test condition	Version		Unit
			- 7	- 8	
Operating current (One bank active)	ICC1	Burst length=1, tRC >= tRC(mim), IOL=0mA tCLK =7ns	90	80	mA
Precharge standby current in power-down mode	ICC2P	CKE <= VIL(max), tCLK= 7ns	2		mA
	ICC2PS	CKE & CLK <= VIL(max), tCC=∞	2		
Precharge standby current in non power-down mode	ICC2N	CKE >= VIH(min), /CS >= VIH(min), tCLK=7ns input singles are changed one time during 7ns	50		mA
	ICC2NS	CKE >= VIH(min),CLK <= VIL(min), tCC =∞ input singles are stable	30		
Active standby current in power-down mode	ICC3P	CKE<=VIL(max), tCLK=7ns	5		mA
	ICC3PS	CKE & CLK <= VIL(max), tCC=∞	3		
Active standby current in non power-down mode (Two bank active)	ICC3N	CKE >=VIH(min), /CS >= VIH(min), tCLK=7ns input singles are changed one time during 7ns	65		mA
	ICC3NS	CKE >= VIH(min), CLK <= VIL(min), tCC=∞ input singles are stable	25		
Operating current (Burst mode)	ICC4	IOL=0mA;2 banks active; BL=4,tCLK=7ns	150	140	mA
Refresh current	ICC5	tRC >= tRC(min) ; tCLK=7ns	90	80	mA
Self refresh current	ICC6	CKE <= VIL(max), tCLK=7ns	2		mA

AC OPERATING TEST CONDITIONS

(Vcc=3.3V ± 10% , Ta=0°C to 70°C)

Parameter	Value	Unit
Input levels (V_{IH} / V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 1	

AC Output Load Circuit.



(Fig.1) AC Output Load Circuit

AC TIMING PARAMETERS (Ta=0-70°C, Vcc=3v-3.6v)

Parameter		Symbol	- 7		- 8		Unit	Notes
			Min	Max	Min	Max		
Clock cycle time	CL = 3	tCK	7		8		ns	
	CL = 2		12		12			
Clock high time		tCH	3		3		ns	
Clock low time		tCL	3		3		ns	
Input setup time		tSS	2		2		ns	
Input hold time		tSH	1		1		ns	
Output valid from clock	CL = 3	tAC	-	5.5	-	6	ns	
	CL = 2			6		6	ns	
Output hold from clock		tOH	2		2		ns	
CAS to CAS delay		tCCD	1		1		CLK	
RAS to RAS bank active delay		tRRD	2		2		CLK	
DQM to input data delay		tDQD	0		0		CLK	
Write command to data-in delay		tDWD	0		0		CLK	
MRS to active delay		tMRD	2		2		CLK	
Precharge to O/P in Hi-Z		tROH	CL		CL		CLK	1
DQM to data in Hi-Z for read		tDQZ	2		2		CLK	
DQM to data mask for write		tDQM	0		0		CLK	
Data-in to precharge command		tDPL	2		2		CLK	
Data-in to active command		tDAL	5		5		CLK	
Power down mode entry		tSB		1		1	CLK	
Self refresh exit time		tSRX	1		1		CLK	
Power down exit setup time		tPDE	1		1		CLK	

Note:
1. CL=CAS Latency

FREQUENCY vs AC PARAMETERS

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(Unit: number of clock)

Frequency	CL	tRC	tRAS	TRP	tRCD
143Mhz (7ns)	3	10	7	3	3
125MHz(8ns)	3	9	6	3	3
100Mhz (10ns)	3	7	5	2	2
83Mhz (12ns)	2	6	4	2	2

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(Unit: number of clock)

Frequency	CL	tRC	tRAS	tRP	tRCD
125Mhz (8ns)	3	9	6	3	3
100Mhz (10ns)	3	7	5	2	2
83Mhz (12ns)	2	6	4	2	2

COMMAND TRUTH TABLE

Function	Symbol	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
Device Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read w/ auto precharge	READAP	H	X	L	H	L	H	V	H	V
Write	WRITE	H	X	L	H	L	L	V	L	V
Write w/ auto precharge	WRITEAP	H	X	L	H	L	L	V	H	V
Bank Active	ACT	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Auto refresh	CBR	H	H	L	L	L	H	X	X	X
Self refresh entry from IDLE	SLFRSH	H	L	L	L	L	H	X	X	X
Self refresh exit	SLFRSHX	L	H	H	X	X	X	X	X	X
Power Down entry from IDLE	PWRDN	H	L	X	X	X	X	X	X	X
Power Down exit	PWRDNX	L	H	H	X	X	X	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Burst Stop	BST	H	X	L	H	H	L	X	X	X

DQM TRUTH TABLE

Function	CKE n-1	CKE n	DQML / DQMH
Data write/output enable	H	X	L
Data mask/output disable	H	X	H

H: High Level, L: Low Level, X: don’ t care, V: Valid data input.

OPERATIVE COMMAND TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Bank Address	Action	Notes
Idle	H	X	X	X	X	X	No Operation command	
	L	H	H	H	X	X	No Operation command	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA,A10	BA	ILLEGAL	2
	L	L	H	H	RA	BA	Row Active	
	L	L	H	L	A10	BA	No Operation command	4
	L	L	L	H	X	X	Auto Refresh or Self refresh	5
	L	L	L	L	Op Code	L	Mode Register Access	5
Row Active	H	X	X	X	X	X	No Operation command	
	L	H	H	X	X	X	No Operation command	
	L	H	L	H	CA,A10	BA	Read	
	L	H	L	L	CA,A10	BA	Write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Read	H	X	X	X	X	X	Continue burst to end, row active	
	L	H	H	H	X	X	Continue burst to end, row active	
	L	H	L	H	CA,A10	BA	Term burst, start new burst read	
	L	H	L	L	CA,A10	BA	Term burst, start new burst write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Term burst, precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
	L	H	H	L	X	X	Burst Stop	6
Write	H	X	X	X	X	X	Continue burst to end, row active	
	L	H	H	H	X	X	Continue burst to end, row active	
	L	H	L	H	CA,A10	BA	Term burst start read	
	L	H	L	L	CA,A10	BA	Term burst, new write	
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	Term burst precharge	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
	L	H	H	L	X	X	Burst Stop	6
Read with Auto Precharge	H	X	X	X	X	X	Continue burst to end and enter Row precharge	
	L	H	H	H	X	X	Continue burst to end and enter Row precharge	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	H	CA,A10	BA	ILLEGAL	2
	L	H	L	L	X	X	ILLEGAL	
	L	L	H	X	RA,A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	Continue burst to end and enter Row precharge	
	L	H	H	H	X	X	Continue burst to end and enter Row precharge	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	H	CA,A10	BA	ILLEGAL	2
	L	H	L	L	X	X	ILLEGAL	
	L	L	H	X	RA,A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	L	ILLEGAL	

OPERATIVE COMMAND TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Bank Address	Action	Notes
Precharge	H	X	X	X	X	X	NOP-enter idle after tRP	
	L	H	H	H	X		NOP-enter idle after tRP	
	L	H	L	H	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	NOP-enter idle after tRP	4
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Row Active	H	X	X	X	X	X	NOP-enter idle after tRCD	
	L	H	H	H	X	X	NOP-enter idle after tRCD	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Write Recovery	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	BA	ILLEGAL	2
	L	H	L	X	CA	BA	ILLEGAL	2
	L	L	H	H	RA	BA	ILLEGAL	2
	L	L	H	L	A10	BA	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	L	Op-code	X	ILLEGAL	
Refresh	H	X	X	X	X	X	NOP – enter idle after tRC	
	L	H	H	H	X	X	NOP – enter idle after tRC	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Set	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Note:

1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of tCCD and tWR (Write Recovery Time)to prevent bus contention.
4. NOP to bank precharge or in idle state. Precharge activated bank by BA or A10.
5. Illegal if any bank is not idle.
6. Not bank-specific ; BURST STOP affects the most recent READ or WRITE burst, regardless of bank.

OPERATIVE COMMAND TABLE (TABLE 2)

Current State(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh-Idle after tRFC(ABI)	7
	L	H	L	H	H	H	X	Exit Self Refresh-Idle after tRFC(ABI)	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP	
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down - ABI	
	L	H	L	H	H	H	X	Exit Power Down - ABI	8
	L	H	L	H	H	L	X	ILLEGAL	8
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP	
All Banks Idle (ABI)	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	H	H	X	X	Enter Power Down	
	H	L	L	H	H	X	X	Enter Power Down	9
	H	L	L	H	L	L	X	ILLEGAL	9
	H	L	L	L	H	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (&bank) A ctive	
	H	L	L	L	L	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	9
	H	L	L	L	X	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	10
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	10
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Note:

7. CKE low to high transition is asynchronous.
8. CKE low to high transition is asynchronous if restart internal clock.
   A minimum setup time 1CLK + tSI must be satisfied before any command other than exit.
9. Power down and self refresh can be entered only from the both banks idle state.
10. Must be a legal command.

1. When $\overline{CS}$ is set ' High ' at a clock transition from ' Low' to ' high' , all inputs except CKE and DQM are invalid.
2. When issuing an active, read or write command, the bank is selected by A11

A11	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enable or disable by the A10 input when the read and write command is issued.

A10	A11	Operation
0	0	After the end of burst, bank A holds the idle status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the idle status.
1	1	After the end of burst, bank B is precharged automatically.

4. when issuing a precharge command, the bank to be precharged is selected by the A10 and A11 input.

A10	A11	Operation
0	0	Bank A is precharge.
0	1	Bank B is Precharge.
1	x	Both banks A & B are precharged.

Device Operation

Power Up Sequence

- Apply power and start clock, attempt to maintain CKE= "H", DQM= "H". Other pins are NOP condition at their inputs.
- Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

Initialization Sequence

After the following initialization sequence, the device is ready for full functionality:

- Precharge both banks.
- Issue 2 or more Auto refresh (CBR) commands to the device.
- Issue a mode register set (MRS) command to set the device mode of operation.
- After tRMD (3 clocks) is met. The device is ready for operation.

  ** Step 2 and 3 are interchangeable.

Precharge Select bank (PRE)

The precharge operation will be performed on the active bank when the precharge selected bank command is issued. When the precharge command is issued with address A10 low, A11 selects the bank to be precharged. At the end of the precharge selected bank command the selected bank will be in idle state after the minimum tRP is met.

Precharge All (PALL)

Both banks are precharged at the same time when this command is issued. When the precharge command is issued with address A10 high then all banks will be precharged. At the end of the precharge all command both banks will be in idle state after the minimum tRP is met.

Auto Precharge

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

AUTO PRECHARGE ensures that the PRECHARGE is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

Burst Terminate

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WEITE command prior to the BURST TERMINATE command will be truncated as shown in the Operation section of this data sheet.

NOP and Device Deselect (NOP, DSEL)

The device is deselected by deactivating the $\overline{CS}$ signal. In this mode the device ignores all the control inputs. The SDRAMs are put in NOP mode when $\overline{CS}$ is active and by deactivating, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP the device will finish the current operation when this command is issued.

Row Activate (ACT)

This command is used to select a row in a specified bank of the device. Read and write operation can only be initiated on this activated bank after the minimum tRCD time has elapsed from the activate command.

Read Bank (READ)

This command is issued after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CS}$, $\overline{CAS}$ and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank (WRITE)

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Functionality of SDRAM device:

The following operations are supported by SDRAM:

- Burst Read
- Burst Write
- Multi bank Ping-Pong access
- Burst Read with Autoprecharge
- Burst Write with Autoprecharge
- Burst Read terminated with precharge
- Burst Write terminated with precharge
- Burst Read terminated with another Burst Read/Write
- Burst Write terminated with another Burst Write/Read
- DQM masking
- Fastest command to command delay of 1 clock
- Precharge All command
- Auto Refresh
- CL=2,3
- Burst Length 1,2,4, 8 and full page (256)
- Self Refresh Command
- Power down
- Terminating a read burst
- Terminating a write burst

Mode Register Set (MRS)

This command is used to program the SDRAM for the desired operating mode. This command is normally used after power up as defined in the power up sequence before the actual operation of the SDRAM is initiated. The functionality of the SDRAM device can be altered by re-programming the mode register through the execution of Mode Register Set command. Both banks must be precharged (i.e. in idle state) before the MRS command can be issued.

Mode Register Definition

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A9, A8, A7: (OP Mode):

The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and burst write:

Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

Burst read and single write:

Data is only written to the column address specified during the write cycle, regardless of the burst length.

A6, A5, A4: (CAS Latency):

These pins specify the CAS latency.

A3: (BT):

A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (Burst Length):

These pins specify the burst length.

Mode Register set: (Programming mode)

BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
11	10	9	8	7	6	5	4	3	2	1	0	Mode Register (Mx)
Reserved		OP Mode			CAS Latency			BT	Burst Length			

CAS Latency				Burst Type		Burst Length				
A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	0	1	Reserved	1	Interleave	0	0	1	2	2
0	1	0	2			0	1	0	4	4
0	1	1	3			0	1	1	8	8
1	0	0	Reserved			1	0	0	Reserved	Reserved
1	0	1	Reserved			1	0	1	Reserved	Reserved
1	1	0	Reserved			1	1	0	Reserved	Reserved
1	1	1	Reserved			1	1	1	Full Page (256)	Reserved

OP Mode			
A9	A8	A7	Mode
0	0	0	Normal (Burst read and burst write)
1	0	0	Single write and burst read

Burst Length	Starting Bit			Interleave	Sequential
2	A0				
	0			0-1	0-1
	1			1-0	1-0
4	A1		A0		
	0		0	0-1-2-3	0-1-2-3
	0		1	1-0-3-2	1-2-3-0
	1		0	2-3-0-1	2-3-0-1
	1		1	3-2-1-0	3-0-1-2
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-0
	0	1	0	2-3-0-1-6-7-4-5	2-3-4-5-6-7-0-1
	0	1	1	3-2-1-0-7-6-5-4	3-4-5-6-7-0-1-2
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-4-7-6-1-0-3-2	5-6-7-0-1-2-3-4
	1	1	0	6-7-4-5-2-3-0-1	6-7-0-1-2-3-4-5
	1	1	1	7-6-5-4-3-2-1-0	7-0-1-2-3-4-5-6
Full Page (256)	n = A0-A7 (location0-255)			Not supported	Cn, Cn+1,Cn+2 Cn+3, Cn+4… …Cn-1, Cn ….

Multi-bank ping pong access

Two-bank Ping-Pong accesses are described in the following diagram. Another bank can be activated while the first bank is being accessed as shown. RAS to RAS delay tRRD must be met while activating another bank.

Read and Write with Autoprecharge

Burst reads and writes with auto precharge commands are initiated with Autoprecharge if A10 is at a high state while the read or write commands are issued.

Precharge Termination of Burst

Burst reads and writes without Autoprecharge can be terminated prematurely by a precharge command. If the burst read or write command was issued in auto precharge mode then the commands may not be terminated prematurely for that bank.

Precharge Command After a Burst Read

The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL – 2 clocks. The precharge command can be issued as soon as the tRAS time is met. The earliest time that precharge can be issued is shown for the CAS Latency = 3 device.

Precharge Termination of a Burst Read

Burst Read (with no Autoprecharge) can be terminated earlier using a precharge command along with the DQM . It allows starting the precharge early. The remaining data is undefined. DQM should be used to mask the invalid data.

Precharge Termination of a Burst Write

To terminate Burst Write early with precharge command the DQM signal must be used as shown. Data sampled tDPL clocks before precharge command will be written correctly. Data sampled afterward and before the precharge command is undefined. DQM must be used to prevent the location from being corrupted. DQM must be asserted active to prevent location (A3 and A4 in this case) from being corrupted. DQ(A2) will be written correctly as tDPL is met.

Read Terminated by Read

A Read command will terminate the previous read command and the data will be available after CAS Latency for the new command. Fastest command to command delay is determined by tCCD (1 clock as shown).

Write Terminated by Write

A Write command will terminate the previous write command and the new burst write command will start with the new command as shown. Fastest command to command delay is determined by tCCD (1 clock as shown).

Read Terminated by Write

A Write command terminates the previous read command and the new burst write will start . The minimum command delay for valid operation (i.e. read-modified-write) = CAS Latency + 2. The DQM must be held active for 3 clocks to keep the output buffer in HiZ as shown to prevent an internal IO buffer conflict between the read data (in pipe) and the write data driven on the input pins.

Write Terminated by Read

A Read command terminates the previous write command and the new burst read will start as shown. In case of tCCD=1, CL=3, and tDQZ=2, there is no loss of data bandwidth even if DQM is activated to mask the write data.

The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with, $\overline{CAS}$ and $\overline{WE}$ low at the rising edge of the clock. When using the Burst Stop Command during a burst read cycle, it should be issued x cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency minus one.

When using the Burst Stop Command during a burst write cycle, the input data applied coincident with the Burst Stop Command will be ignored. The last data written (provided that DQM is low at that time) will be the input data applied one clock previous to the Burst Stop Command.

SDRAM commands to two banks in consecutive clocks

Given COMMAND1 detected by SDRAM component (to bank(i)), it will handle correctly COMMAND2 (to bank(j)) that is detected in the next clock or later clock.
Also, note that COMMAND1 (or COMMAND2) can be: Precharge-Bank, Internally-Scheduled_Auto-Precharge, Activate, Read or Write. Command1/2 cannot be a Precharge-All. Next command to same bank after Precharge

Precharge-Bank

If a Precharge-Bank command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+tRP).

Precharge-All

If a Precharge-All command is detected by SDRAM component in CLK(n), then there can be no commands presented to this component until CLK(n+tRP).

Read-Auto Precharge

If a Read with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+CL+BL-2+tRP).

Write-Auto Precharge

If a Write with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+BL+Tdal-1).

Back to back command with Auto precharge

Read or write burst initiated with auto precharge (A10=high during read or write) will execute the read or write normally with the exception that after the burst operation is over the accessed bank will start precharge. To access the bank again the user must reactivate with an active bank command.
The commands initiated with auto-precharge cannot be terminated with any other commands for that bank.

Auto Refresh (CBR) Command

An auto refresh (CBR) refreshes the SDRAM array. Refresh addresses are generated internally by the SDRAM device and incremented after each auto refresh automatically. No commands (including another auto refresh) can be issued until a minimum tRC is satisfied.

Self Refresh Entry/Exit

The self refresh mode is entered by holding $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$,CKE low and $\overline{WE}$ high at the rising edge of the clock. Once the SDRAM enters the Self Refresh mode, all inputs except CKE will be in a don' t care state and outputs will be tri-stated. The external clock may be halted while the device is in Self Refresh mode, however, the clock must be restarted 200 cycles before CKE is high. The self refresh command is exited by asserting CKE high. A new command may be given tRC clocks after CKE is high.

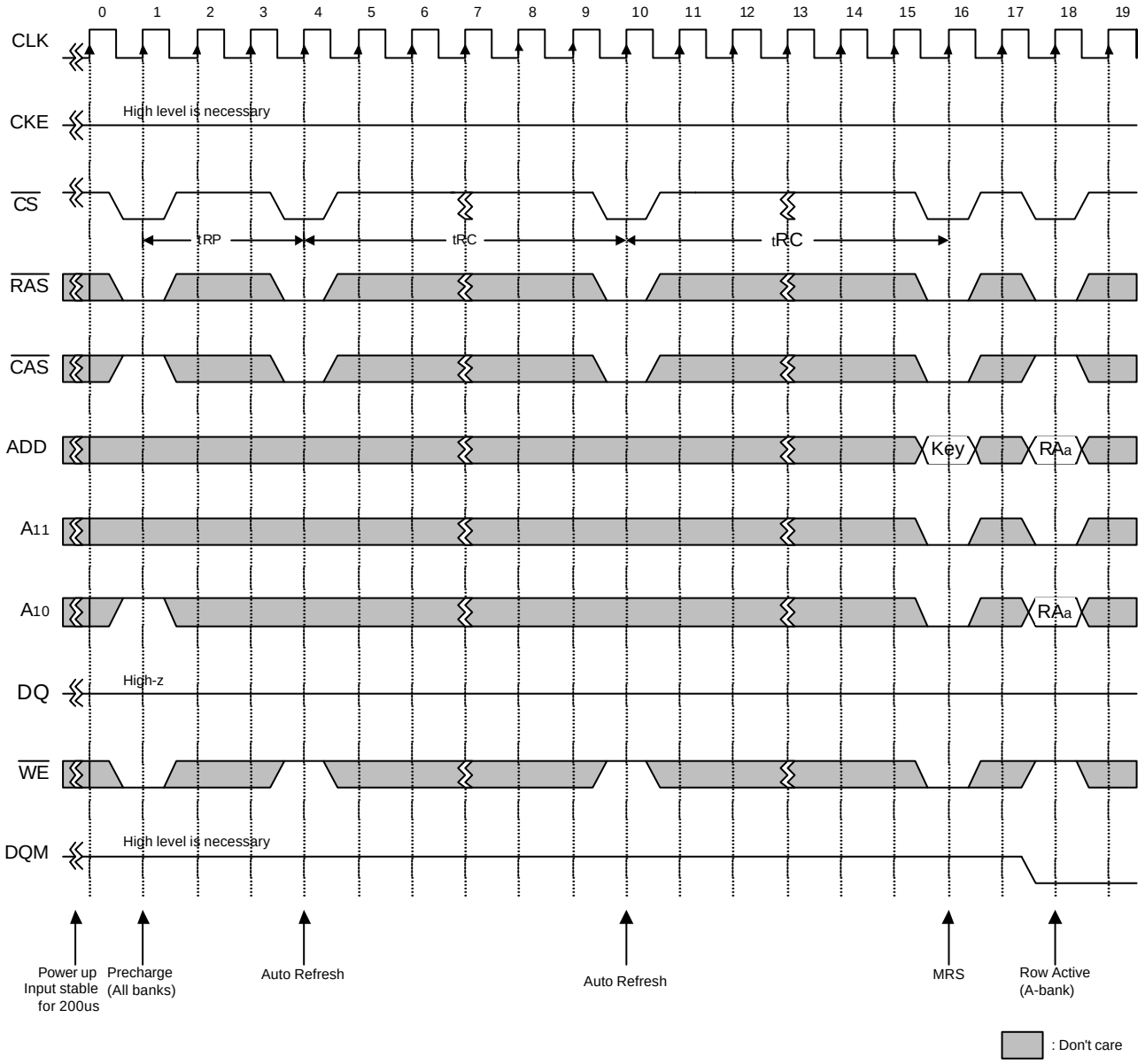
Multibank Operation

The following table specifies some of the timing parameters used for the timing diagrams. CL, tRCD and tRP can all have values of 2 or 3.

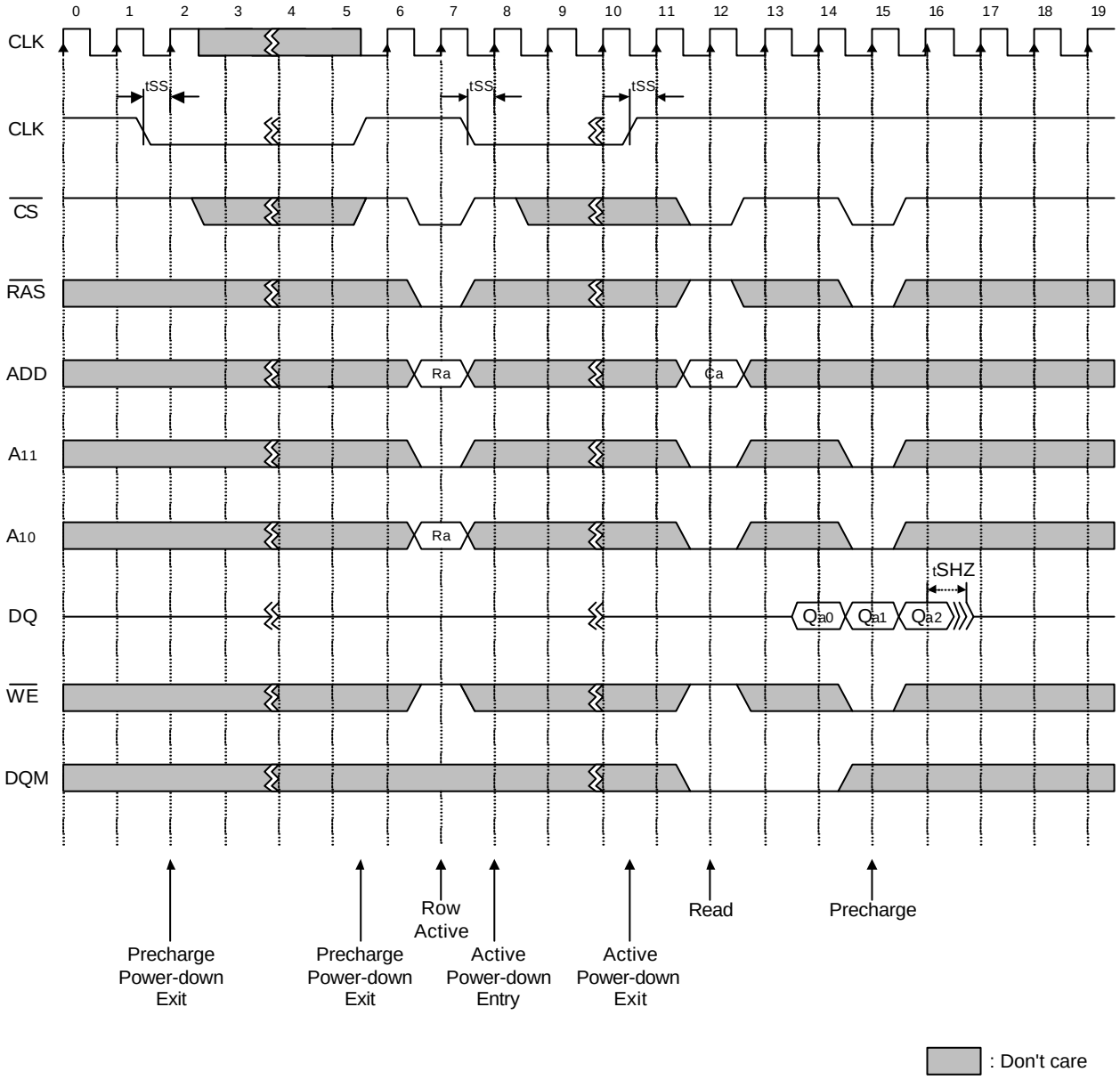
CL	CAS latency	3 clocks
BL	Burst Length	4
tRP	RAS Precharge	3 clocks
tRAS	RAS active time	5 clocks
tRCD	RAS to CAS delay	3 clocks

TIMING WAVEFORM

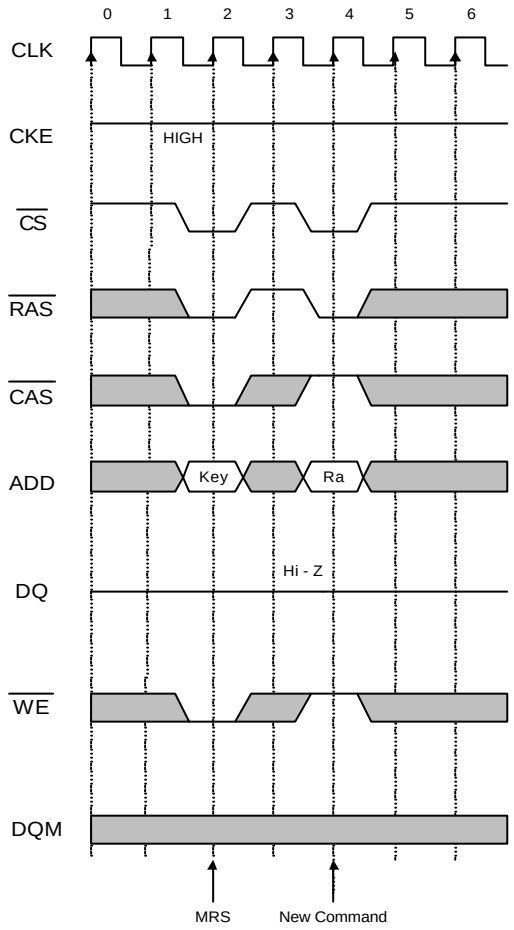
Power Up Initialization Sequence



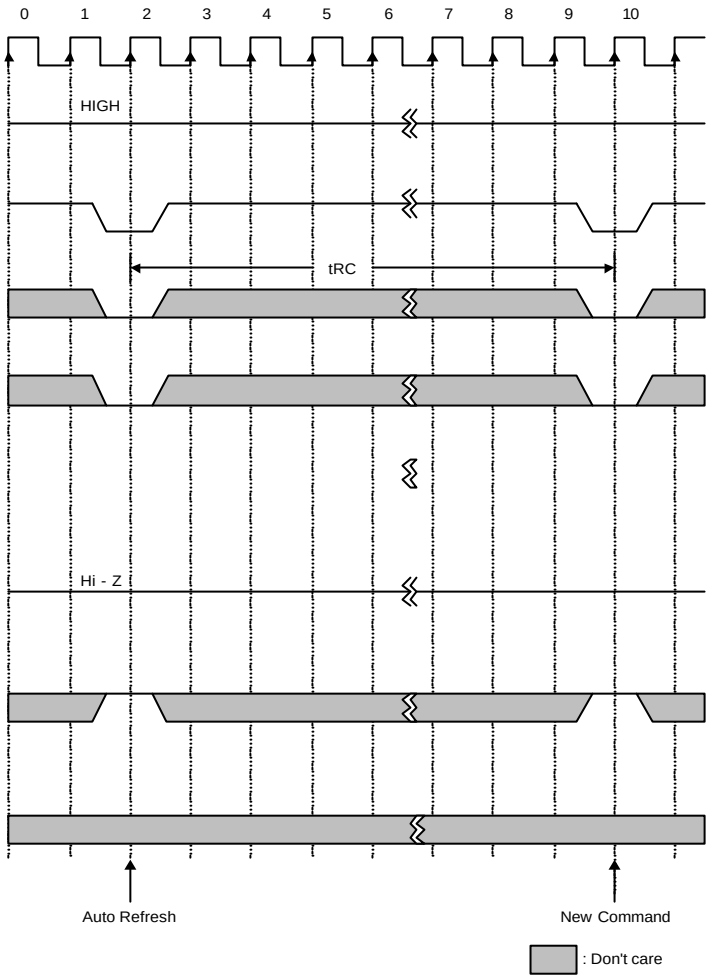
Active / Precharge Power Down Mode (CL =2 , BL =4)



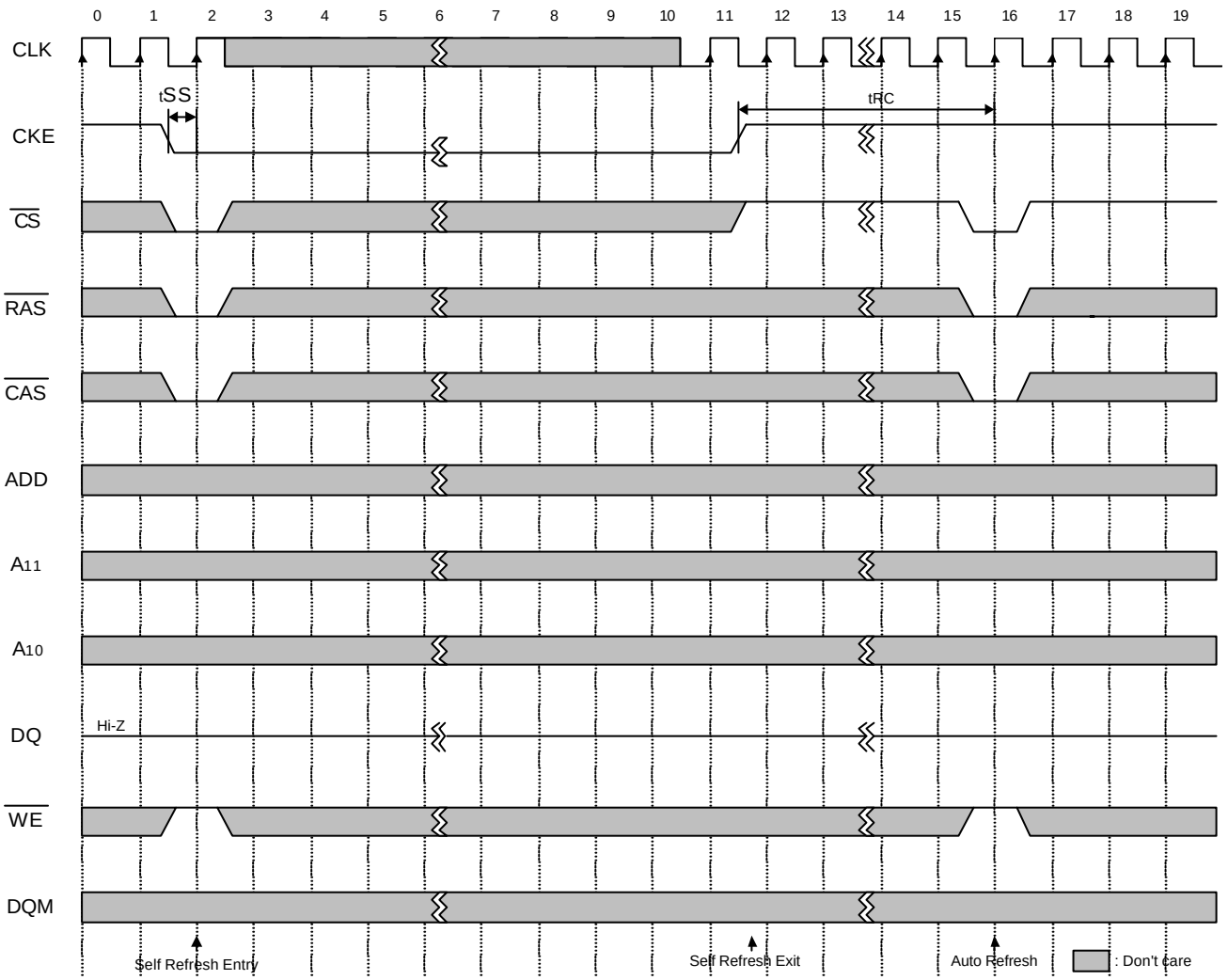
Mode Register Set Cycle



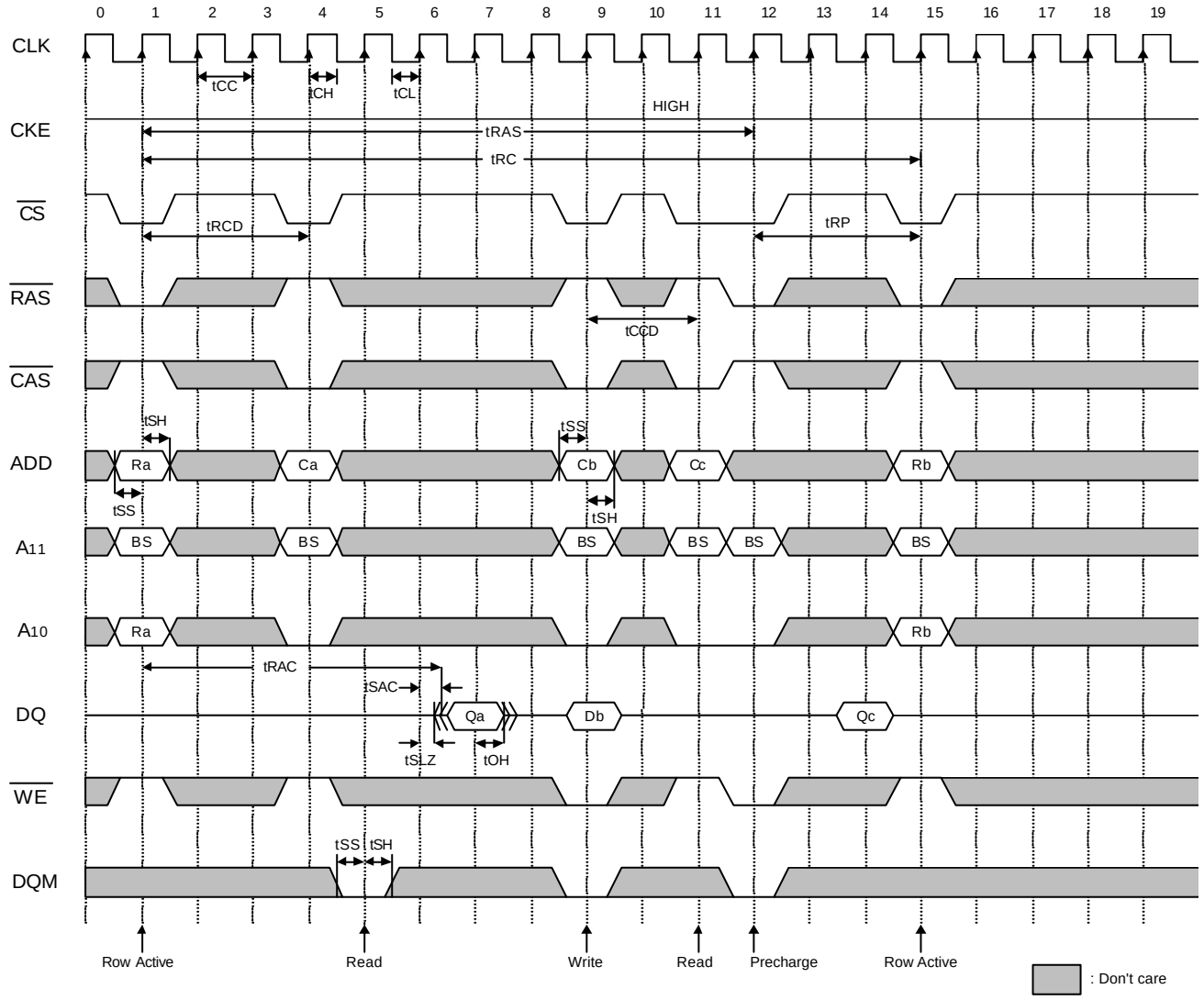
Auto Refresh Cycle



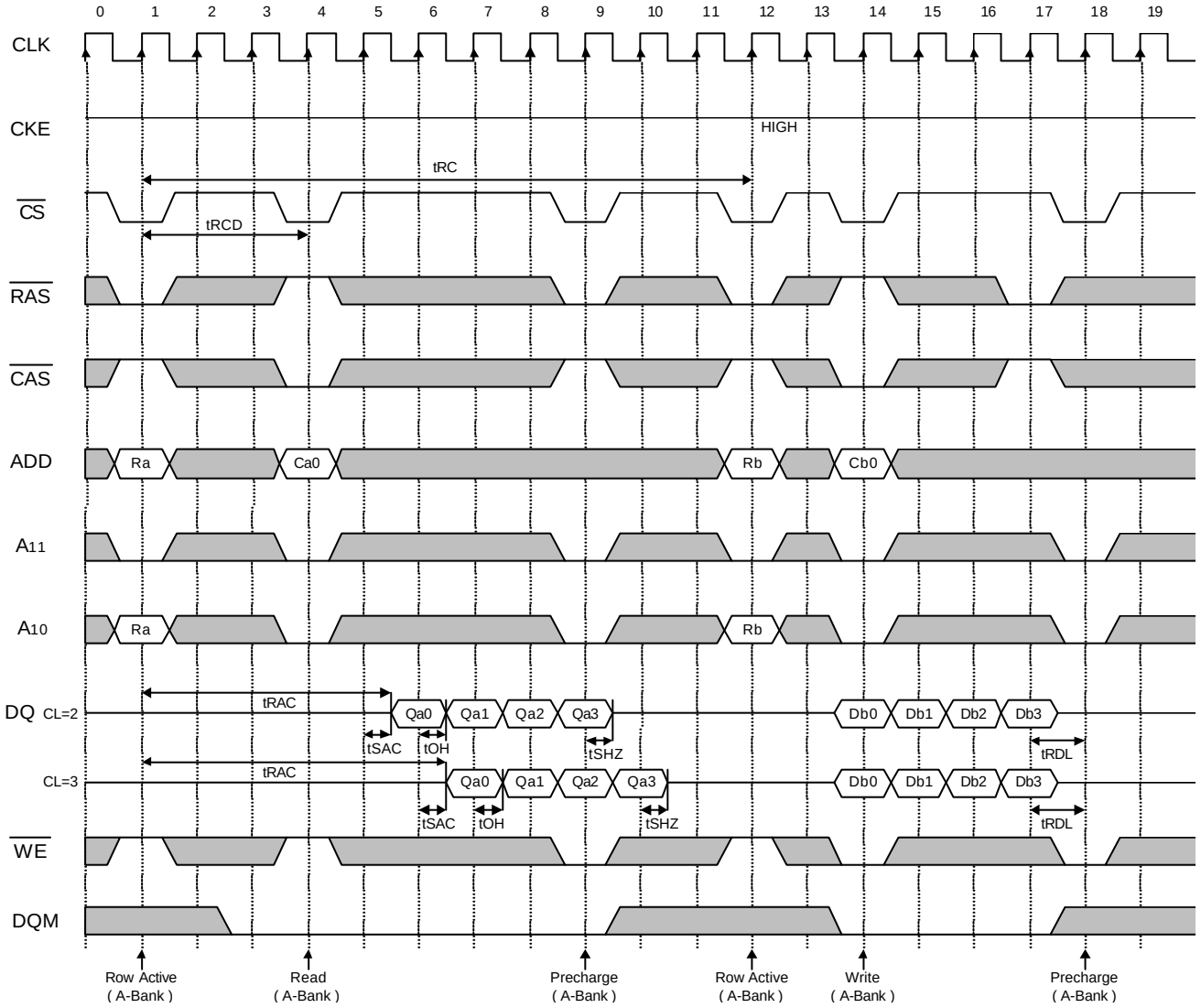
Self Refresh Entry & Exit Cycle



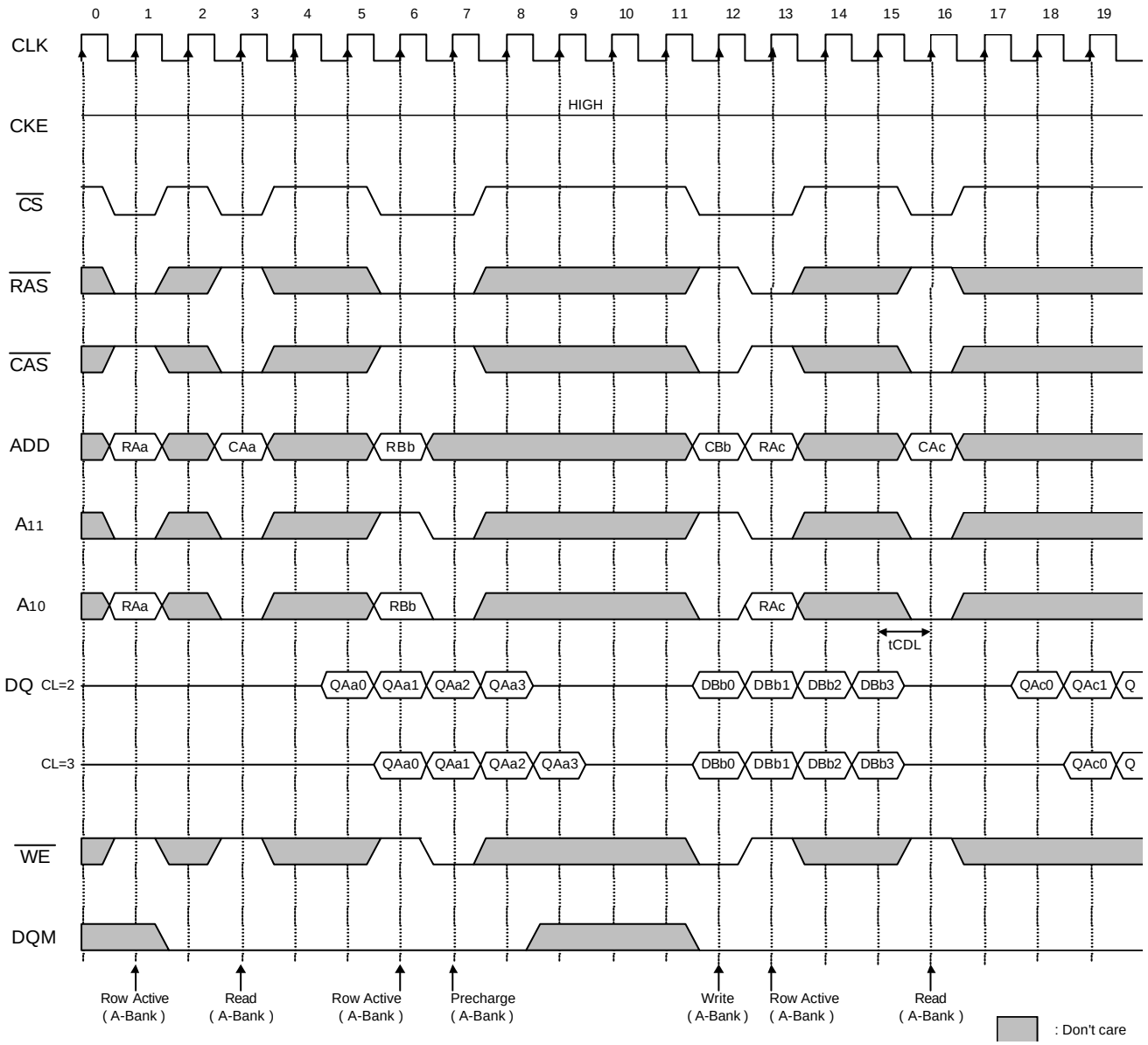
Single Bit Read-Write-Read Cycle at same page (CL = 3 , BL = 1)



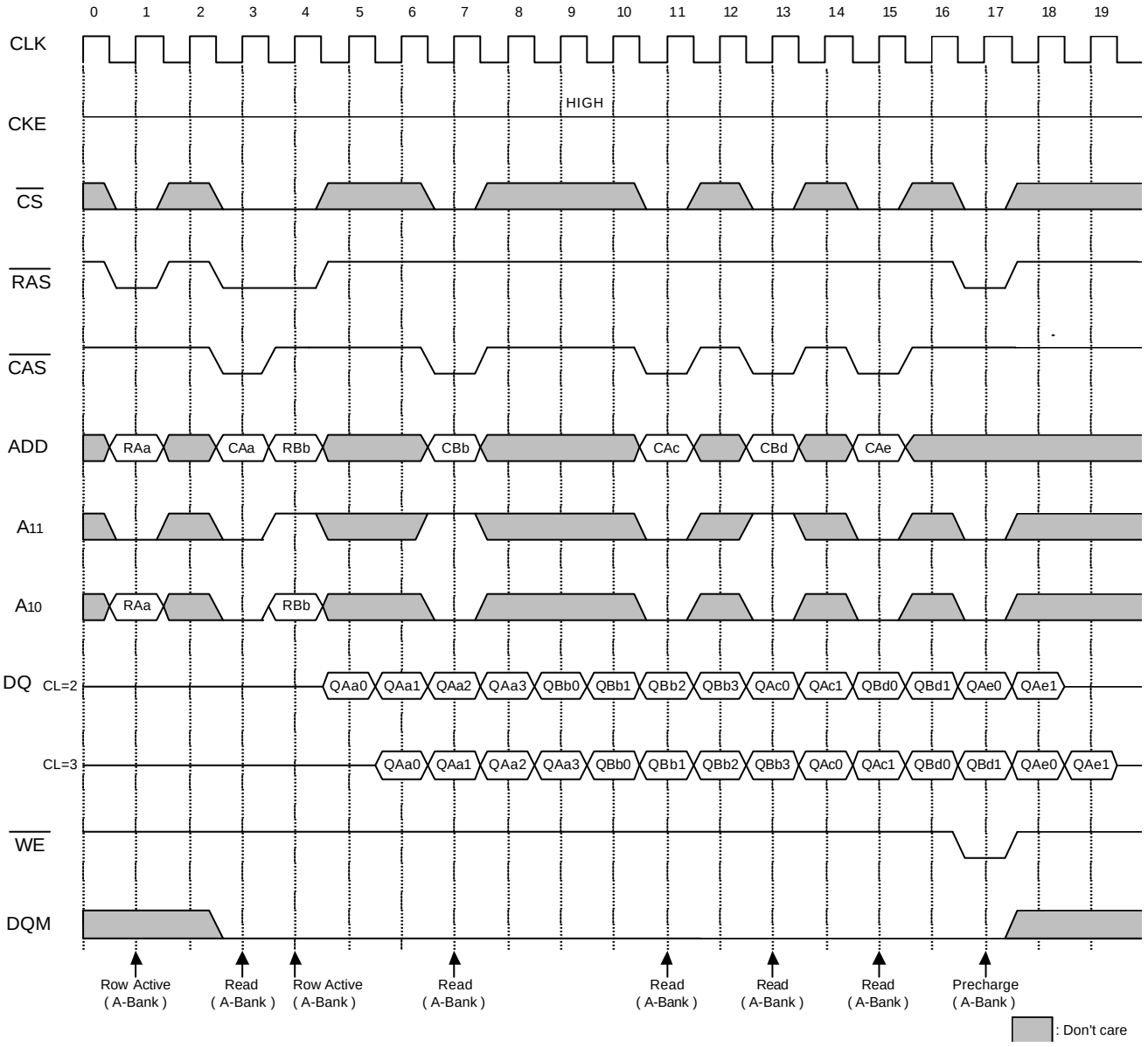
Read & Write Cycle at Same Bank (BL = 4)



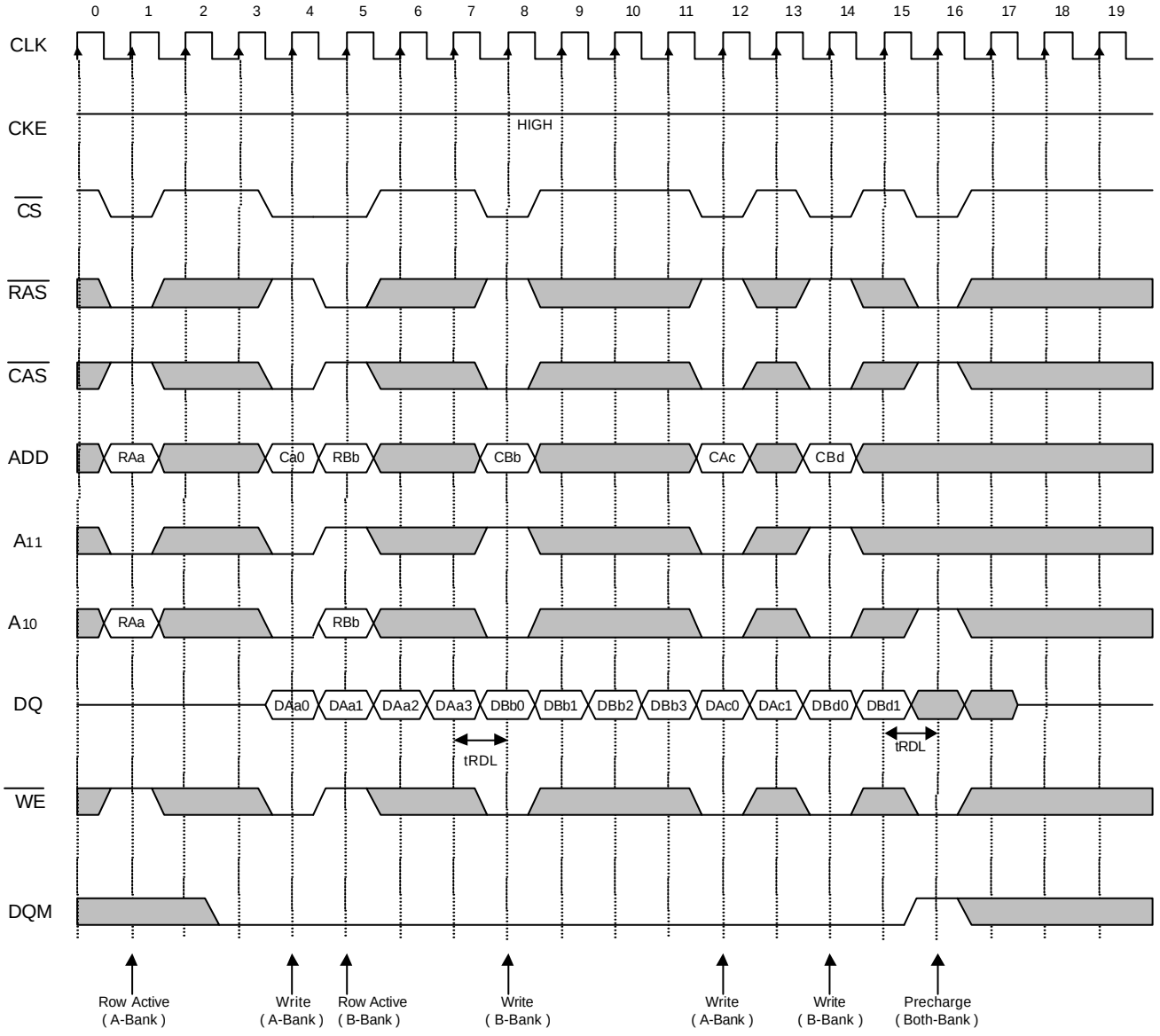
Read & Write Cycle with Random Row at Different Bank (BL = 4)



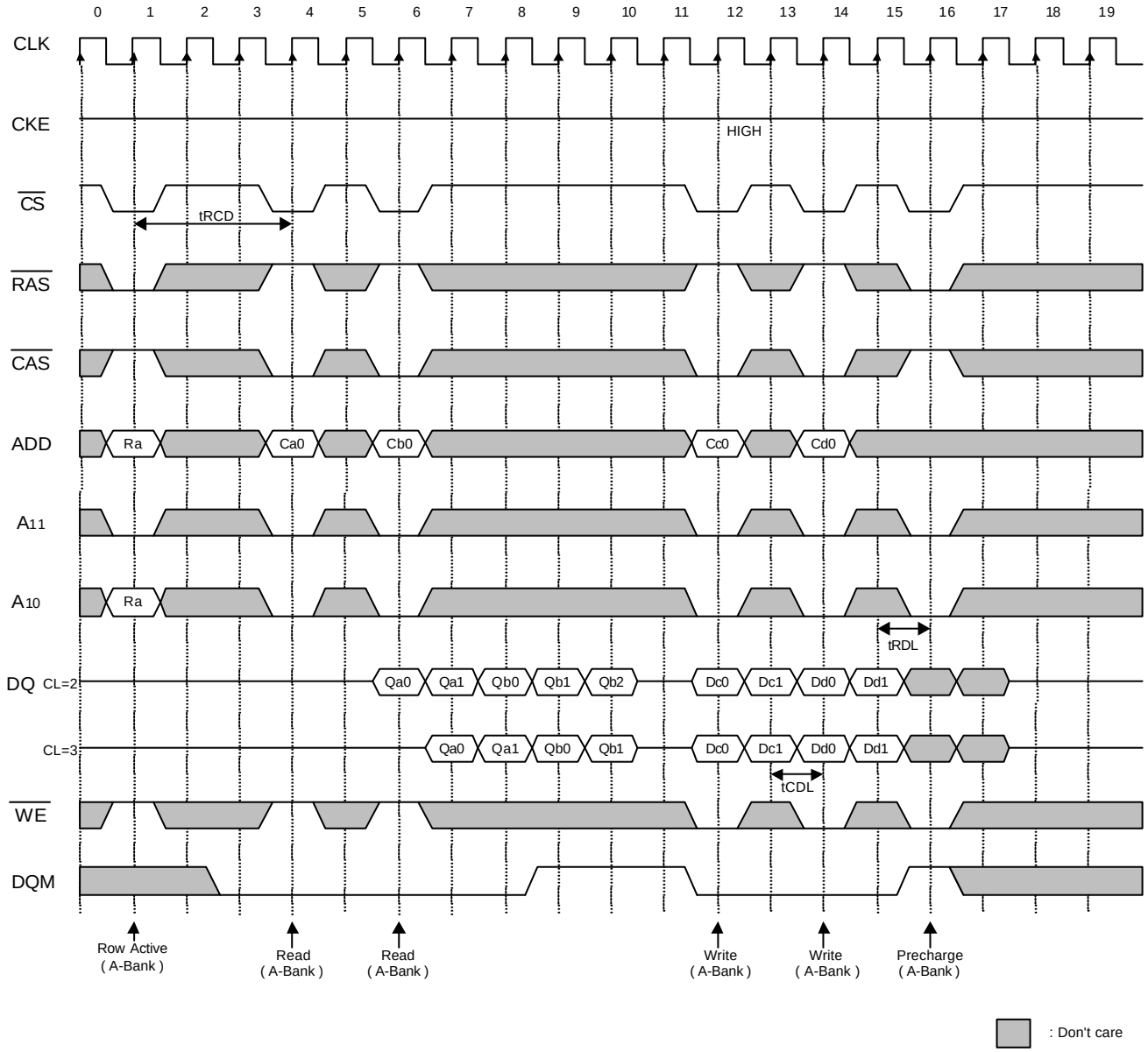
Page Read Cycle at Different Bank (BL = 4)



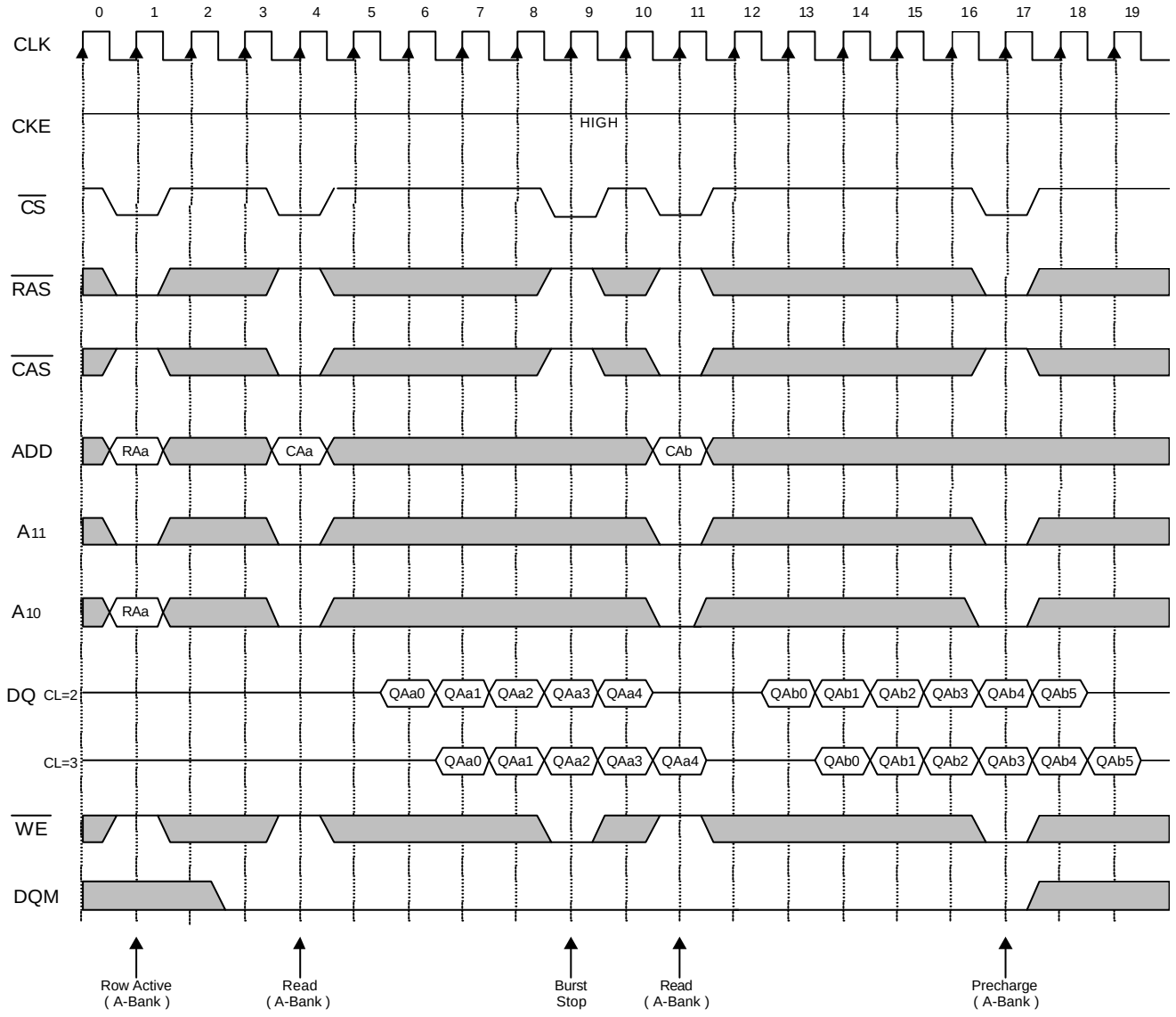
Page Write Cycle at Different Bank (BL = 4)



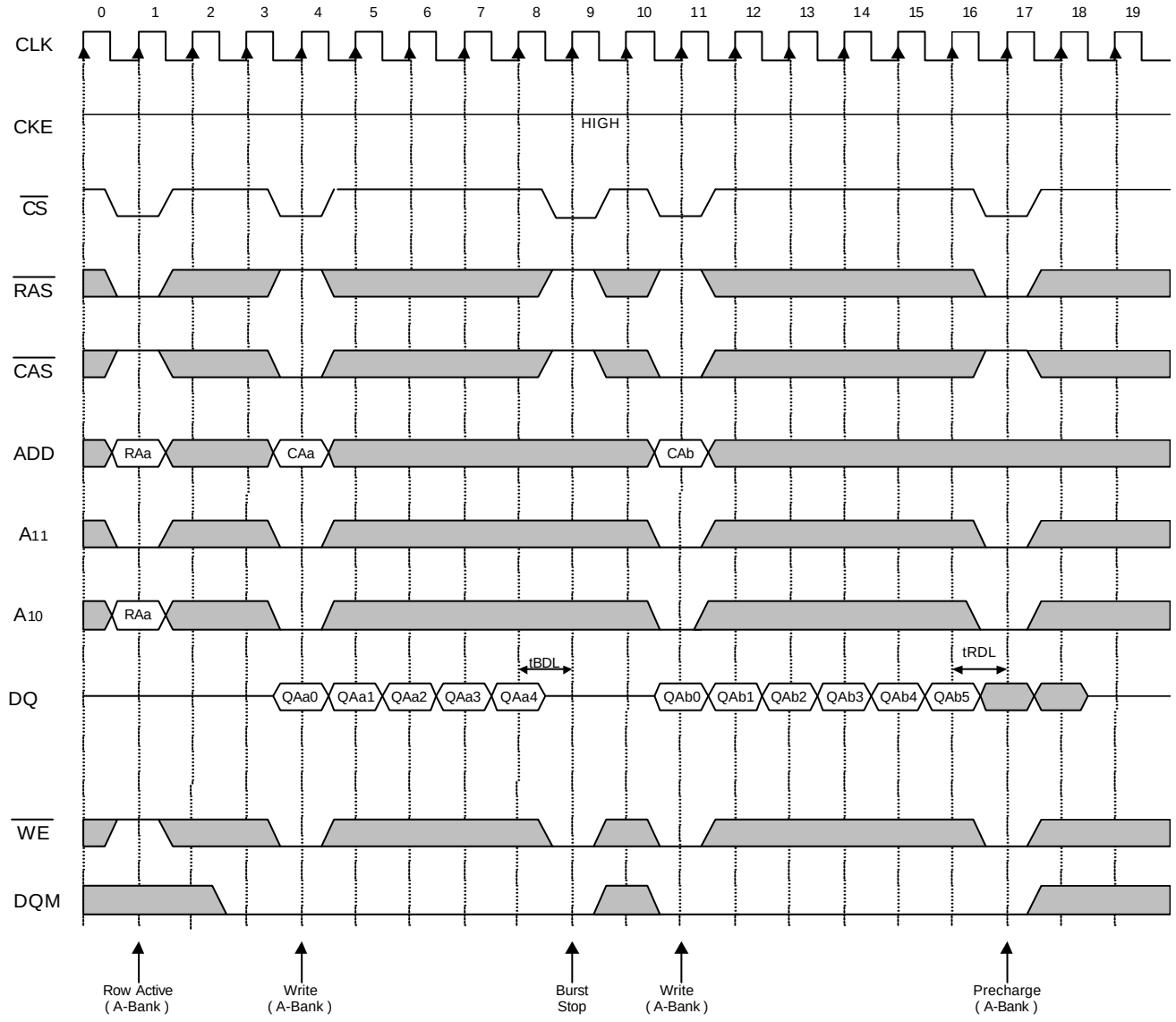
Page Read & Write Cycle at Same Bank (CL = 2 , BL = 4)



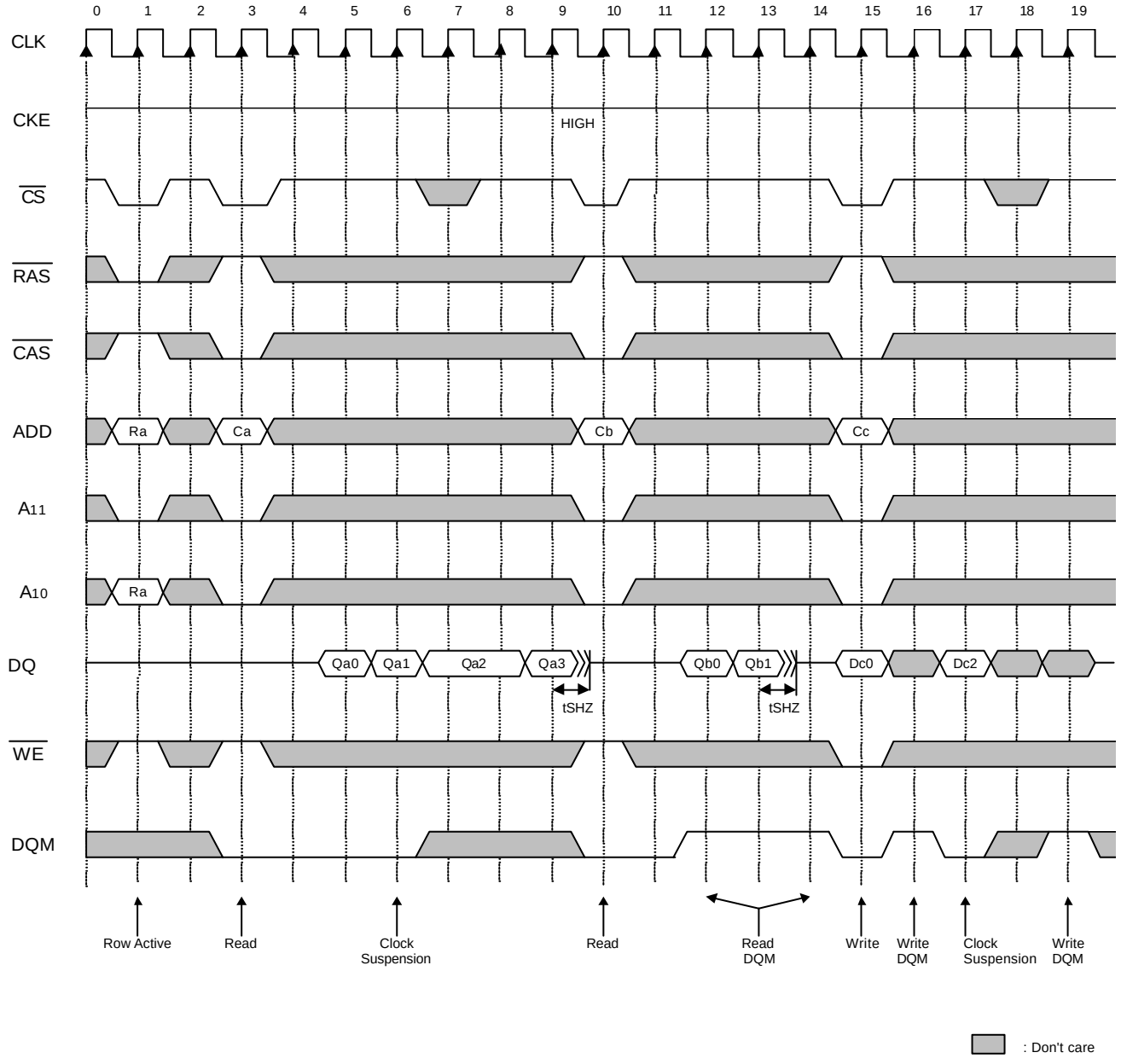
Read Interruption by Precharge Command & Read Burst Stop Cycle
(BL = Full Page)



Write Interruption by Precharge Command & Write Burst Stop Cycle (BL = Full Page)

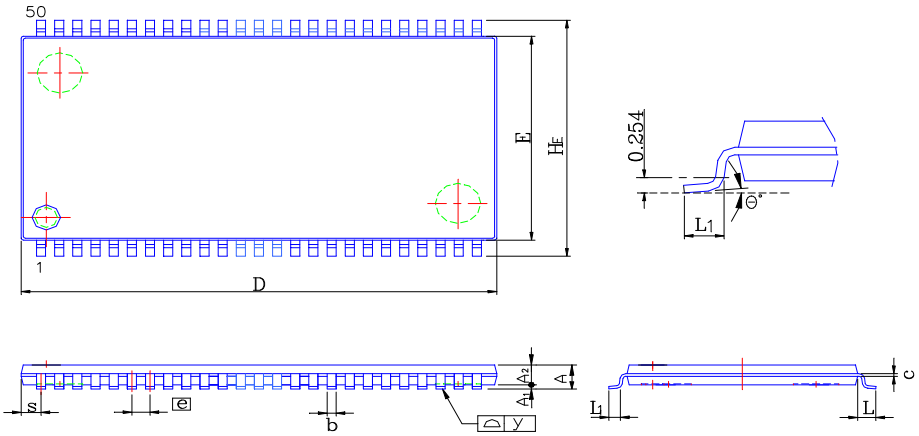


Clock Suspension & DQM Operation Cycle (CL = 2 , BL = 4)



PACKAGE DIMENSIONS

(400mil; 50-Pin; Thin Small Outline Package)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.010	0.014	0.018	0.25	0.35	0.45
c	0.005	0.006	0.008	0.12	0.15	0.21
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.396	0.400	0.405	10.06	10.16	10.29
e	-	0.031	-	-	0.80	-
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	-	0.031	-	-	0.80	-
L_1	0.016	0.020	0.024	0.40	0.50	0.60
S	-	-	0.040	-	-	1.03
y	-	-	0.004	-	-	0.10
θ	0 º	-	5 º	0 º	-	5 º

Note:

1. Dimension D&E do not include interlead flash.
2. Dimension S includes end flash.
3. Controlling dimension : MM