16 V Quad Operational Amplifier

ADD8704

FEATURES

Single-supply operation: 4.5 V to 16.5 V
Upper/lower buffers swing to V_{DD}/GND
Continuous output current: 35 mA
V_{COM} peak output current: 250 mA
Offset voltage: 15 mV
Slew rate: 6 V/µs
Unity gain stable with large capacitive loads
Supply current: 700 µA per amplifier
Drop-in replacement for EL5420

APPLICATIONS

TFT LCD monitor panels
TFT LCD notebook panels
Communications equipment
Portable instrumentation
Electronic games

GENERAL DESCRIPTION

The ADD8704 is a single-supply quad operational amplifier that has been optimized for today's low cost TFT LCD notebook and monitor panels. Output channels A and D swing to the rail for use as end-point gamma references. Output channels B and C provide high continuous and peak current drive for use as V_{COM} or repair amplifiers; they can also be used as midpoint gamma references. All four amplifiers have excellent transient response and have high slew rate and capacitive load drive capability. The ADD8704 is specified over the –40°C to +85°C temperature range and is available in either a 14-lead TSSOP or a 16-lead LFCSP package for thin, portable applications.

Table 1. Input/Output Characteristics

Channel	V_{IH}	V_{IL}	I_O (mA)	I_{SC} (mA)
A	V_{DD} – 1.7 V	GND	15	150
B	V_{DD} – 1.7 V	GND	35	250
C	V_{DD}	GND	35	250
D	V_{DD}	GND + 1.7 V	15	150

PIN CONFIGURATIONS

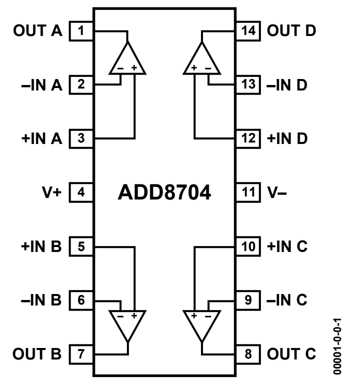

Figure 1. 14-Lead TSSOP (RU Suffix)

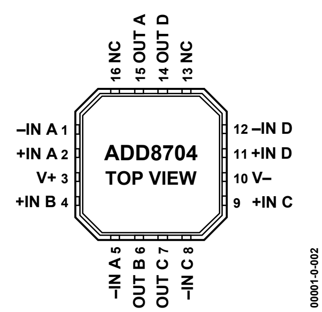

Figure 2. 16-Lead CSP (CP Suffix)

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Table 2. V_S = 16 V, V_{CM} = V_S/2, T_A @ 25°C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		10		μV/°C
Input Bias Current	I_B			200	1100	nA
		−40°C ≤ T_A ≤ +85°C			1500	nA
Input Offset Current	I_{OS}			10	100	nA
		−40°C ≤ T_A ≤ +85°C			250	nA
Common-Mode Rejection Ratio	CMRR	−40°C ≤ T_A ≤ +85°C				
Amp A		V_{CM} = 0 to (V_S – 1.7 V)	54	95		dB
Amp B		V_{CM} = 0 to (V_S – 1.7 V)	54	95		dB
Amp C		V_{CM} = 0 to V_S	54	95		dB
Amp D		V_{CM} = 1.7 V to V_S	54	95		dB
Large Signal Voltage Gain	AVO	R_L = 10 kΩ, V_O = 0.5 to (V_S – 0.5 V)	1	10		V/mV
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTIS						
Output Voltage High (A)	V_{OH}	I_L = 100 μA		15.985		V
Optimized for Low Swing		I_L = 5 mA	15.6	15.75		V
		−40°C ≤ T_A ≤ +85°C	15.5			V
Output Voltage High (B)	V_{OH}	I_L = 100 μA		15.995		V
Optimized for V_{COM}		I_L = 5 mA	15.8	15.9		V
		−40°C ≤ T_A ≤ +85°C	15.75			V
Output Voltage High (C)	V_{OH}	I_L = 100 μA		15.995		V
Optimized for Midrange		I_L = 5 mA	15.8	15.9		V
		−40°C ≤ T_A ≤ +85°C	15.75			V
Output Voltage High (D)	V_{OH}	I_L = 100 μA		15.99		V
Optimized for High Swing		I_L = 5 mA	15.75	15.85		V
		−40°C ≤ T_A ≤ +85°C	15.65			V
Output Voltage Low (A)	V_{OL}	I_L = 100 μA		20		mV
Optimized for Low Swing		I_L = 5 mA		80	200	mV
		−40°C ≤ T_A ≤ +85°C			300	mV
Output Voltage Low (B)	V_{OL}	I_L = 100 μA		5		mV
Optimized for V_{COM}		I_L = 5 mA		50	150	mV
		−40°C ≤ T_A ≤ +85°C			250	mV
Output Voltage Low (C)	V_{OL}	I_L = 100 μA		5		mV
Optimized for Midrange		I_L = 5 mA		50	150	mV
		−40°C ≤ T_A ≤ +85°C			250	mV
Output Voltage Low (D)	V_{OL}	I_L = 100 μA		50		mV
Optimized for High Swing		I_L = 5 mA		375	500	mV
		−40°C ≤ T_A ≤ +85°C			600	mV
Continuous Output Current (A and D)	I_{OUT}			15		mA
Continuous Output Current (B and C)	I_{OUT}			35		mA
Peak Output Current (A and D)	I_{PK}	V_S = 16 V		50		mA
Peak Output Current (B and C)	I_{PK}	V_S = 16 V		200		mA
SUPPLY CHARACTERISTICS						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 17 V, −40°C ≤ T_A ≤ +85°C	70	90		dB
Total Supply Current	I_{SY}	V_O = V_S/2, No Load		2.8	3.4	mA
		−40°C ≤ T_A ≤ +85°C			4	mA

ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	4	6		V/μs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, C_L = 40 pF		5.8		MHz
−3 dB Bandwidth	BW	R_L = 10 kΩ, C_L = 40 pF		6.8		MHz
Phase Margin	Øo	R_L = 10 kΩ, C_L = 40 pF		55		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density (A, B, and C)	e_n	f = 1 kHz		26		nV/√Hz
	e_n	f = 10 kHz		25		nV/√Hz
Voltage Noise Density (D)	e_n	f = 1 kHz		36		nV/√Hz
	e_n	f = 10 kHz		35		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		0.8		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3. ADD8704 Stress Ratings[1]

Parameter	Rating
Supply Voltage (V_S)	18 V
Input Voltage	–0.5 V to V_S + 0.5 V
Differential Input Voltage	V_S
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature Range	300°C
ESD Tolerance (HBM)	±1500 V
ESD Tolerance (MM)	175 V

Table 4. Package Characteristics

Package Type	θ_{JA}[2]	θ_{JC}	Unit
14-Lead TSSOP (RU)	180	35	°C/W
16-Lead LFCSP (CP)	38[3]	30[3]	°C/W

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for devices soldered onto a circuit board for surface-mount packages.

[3] DAP is soldered down to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this part features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

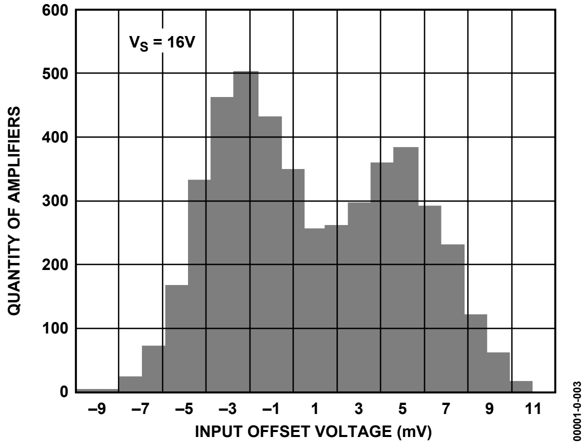

Figure 3. Input Offset Voltage, $V_S = 16$ V

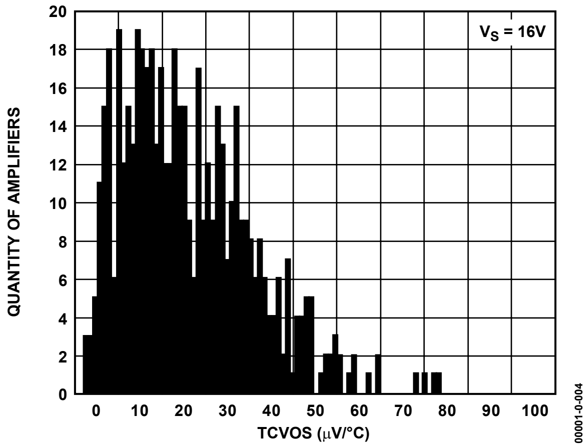

Figure 4. Input Offset Voltage Drift, $V_S = 16$ V

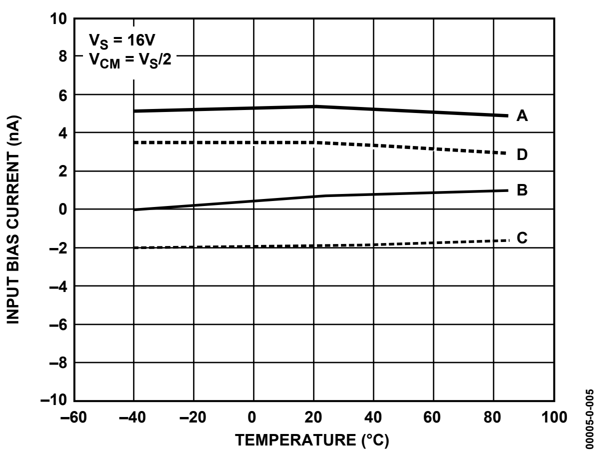

Figure 5. Input Bias Current vs. Temperature

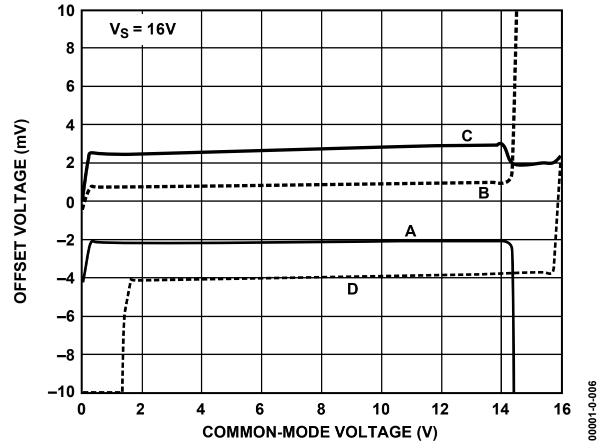

Figure 6. Offset Voltage vs. Common-Mode Voltage

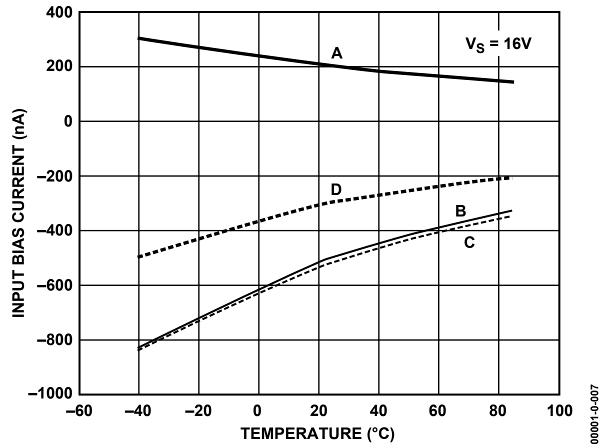

Figure 7. Input Bias Current vs. Temperature

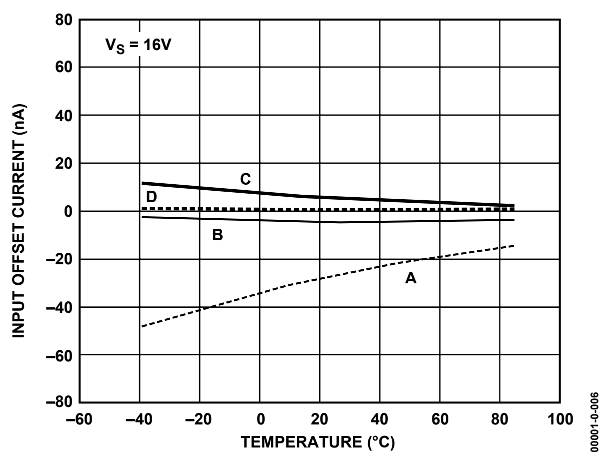

Figure 8. Input Offset Current vs. Temperature

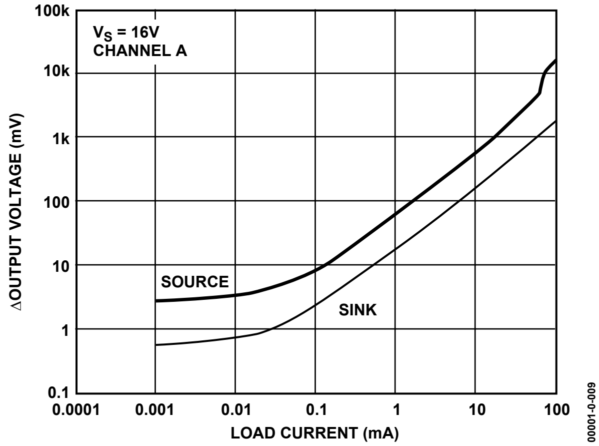

Figure 9. Channel A Output Voltage vs. Load Current

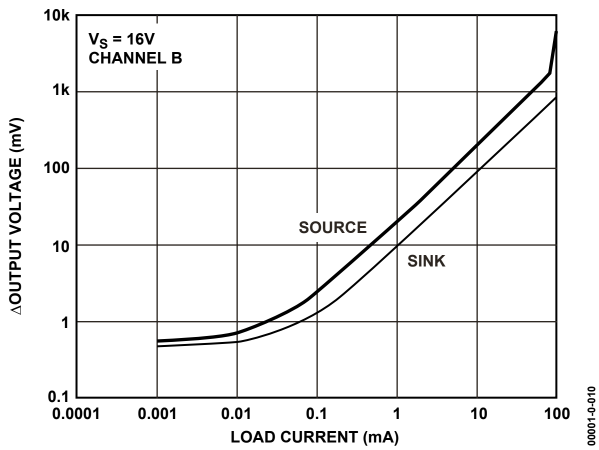

Figure 10. Channel B Output Voltage vs. Load Current

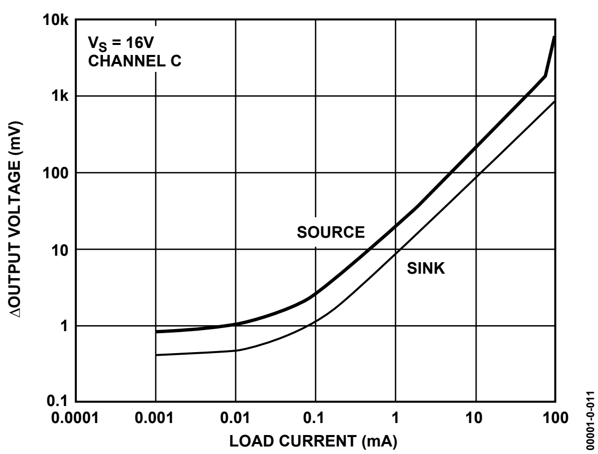

Figure 11. Channel C Output Voltage vs. Load Current

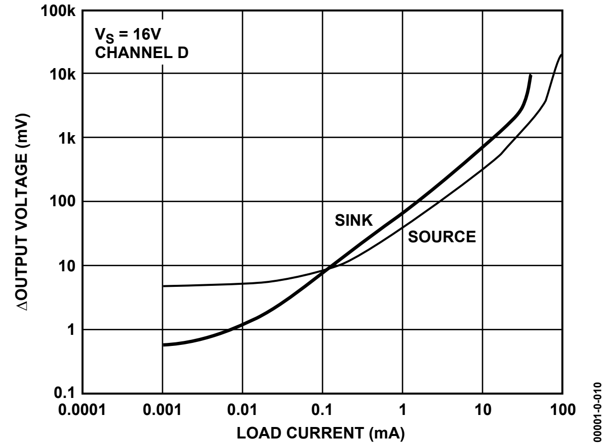

Figure 12. Channel D Output Voltage vs. Load Current

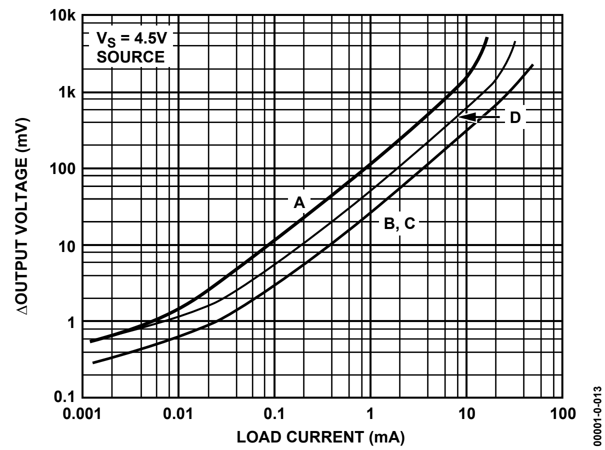

Figure 13. Output Source Voltage vs. Load Current, All Channels

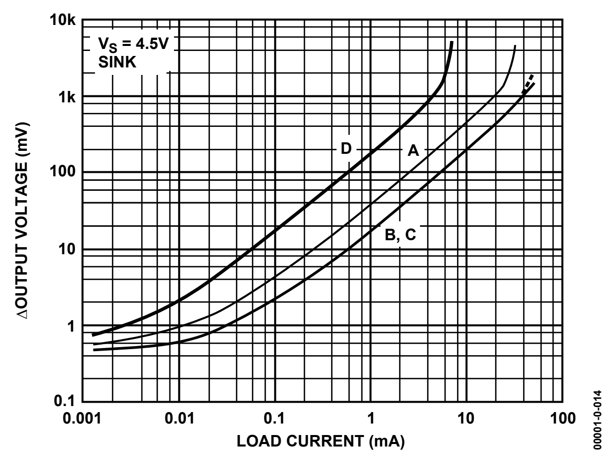

Figure 14. Output Sink Voltage vs. Load Current, All Channels

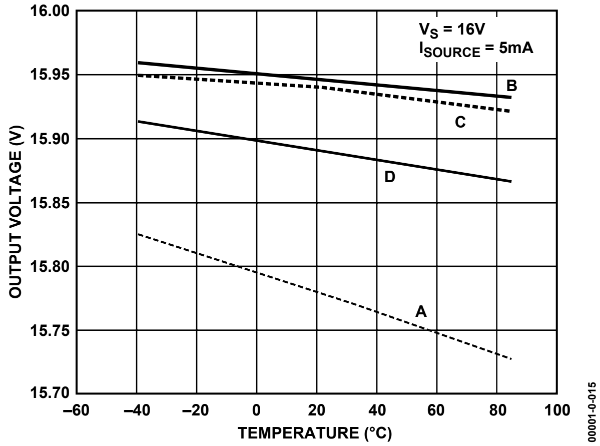

Figure 15. Output Source Voltage vs. Temperature

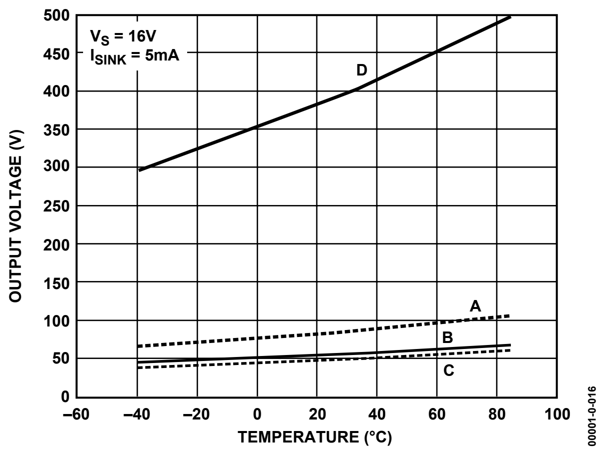

Figure 16. Output Sink Voltage vs. Temperature

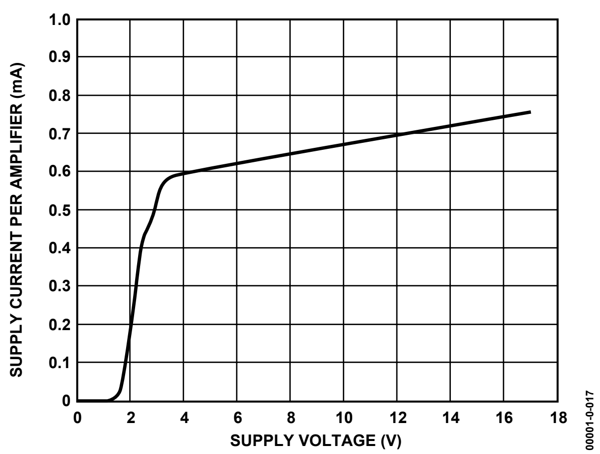

Figure 17. Supply Current vs. Supply Voltage

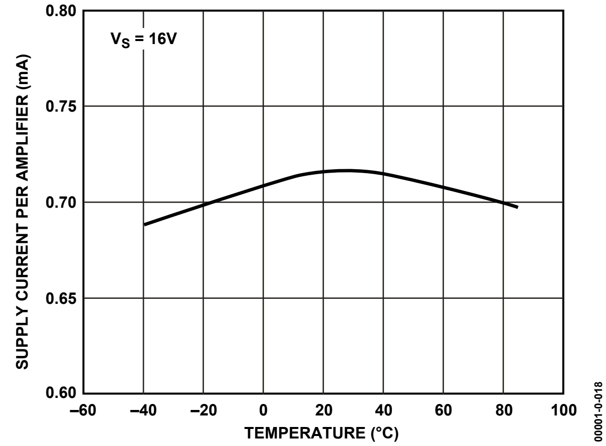

Figure 18. Supply Current vs. Temperature

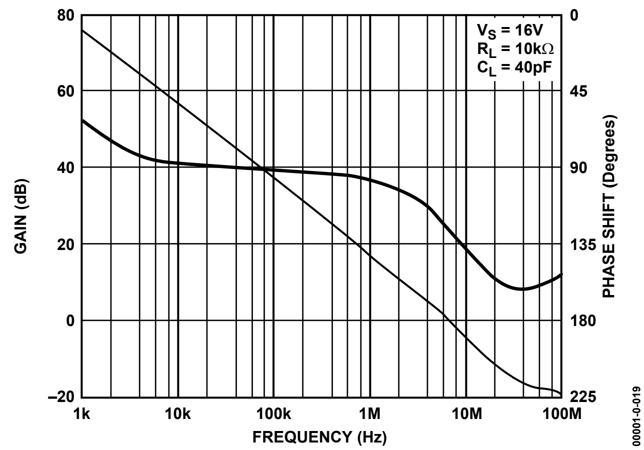

Figure 19. Frequency vs. Gain and Shift

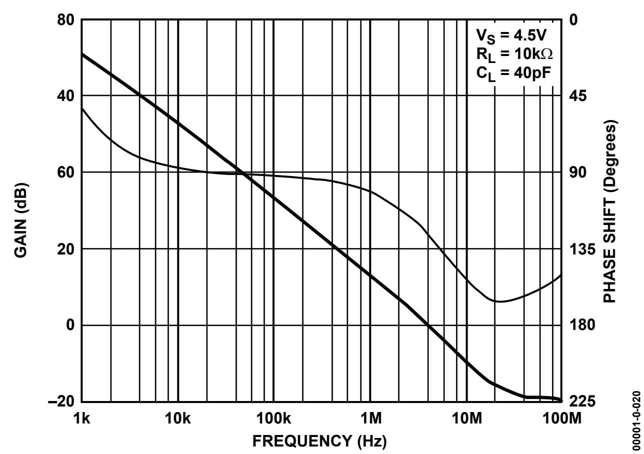

Figure 20. Frequency vs. Gain and Shift

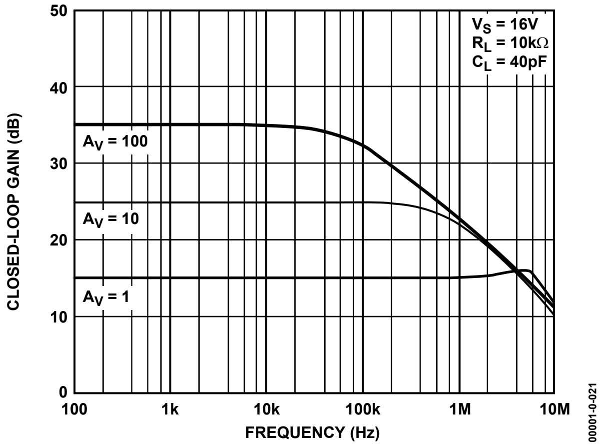

Figure 21. Closed-Loop Gain vs. Frequency

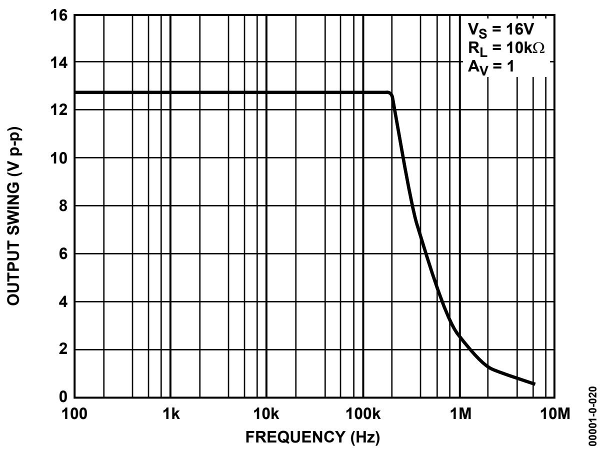

Figure 22. Output Swing vs. Frequency

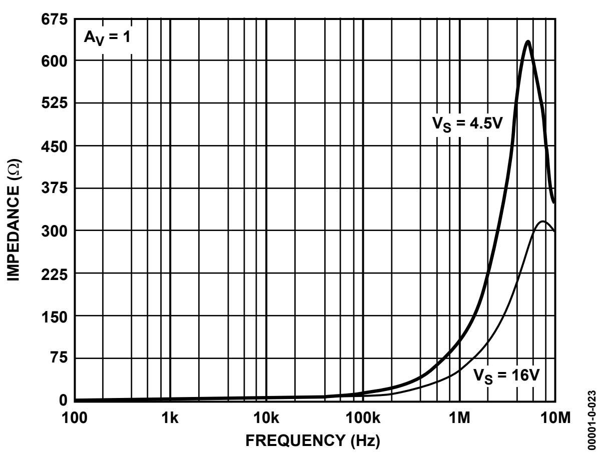

Figure 23. Impedance vs. Frequency

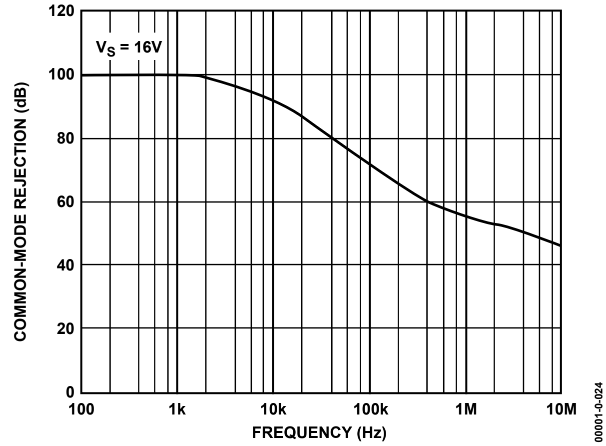

Figure 24. Common-Mode Rejection vs. Frequency

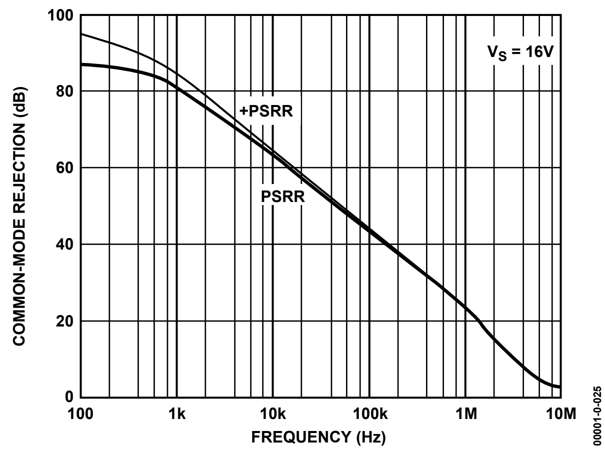

Figure 25. Common-Mode Rejection vs. Frequency

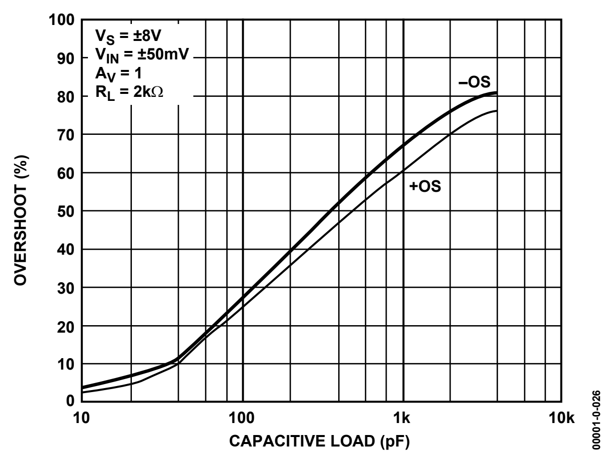

Figure 26. Overshoot vs. Capacitive Load

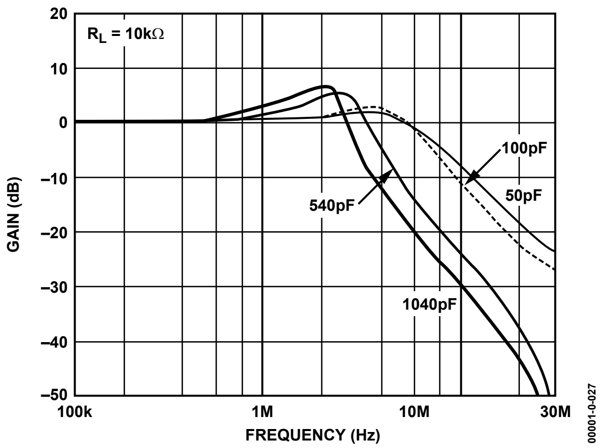

Figure 27.Gain vs. Capacitive Load

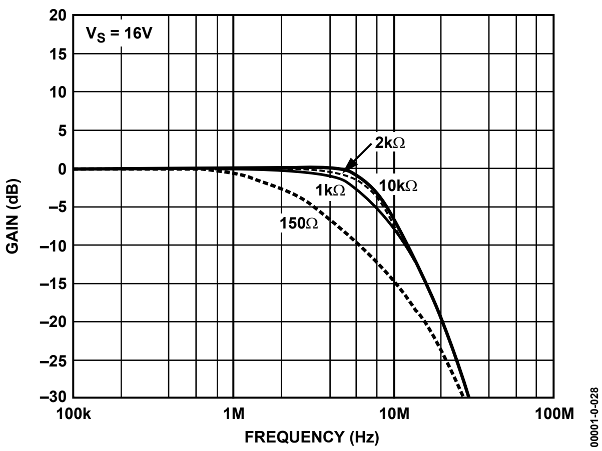

Figure 28. Gain vs. Resistive Load

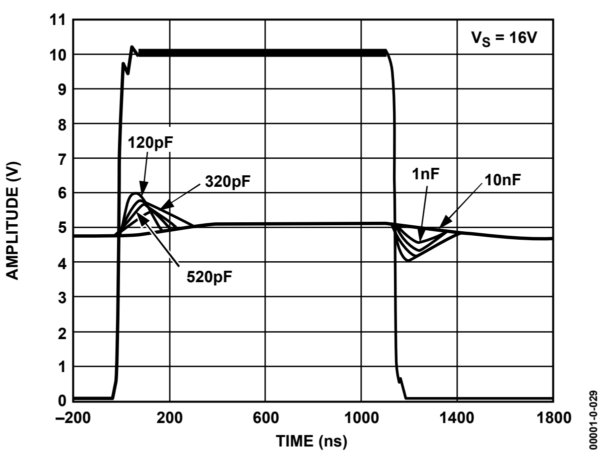

Figure 29. Transient Load Response

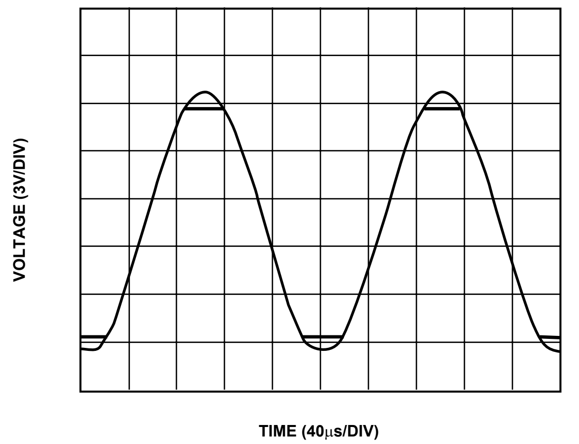

Figure 30. No Phase Reversal

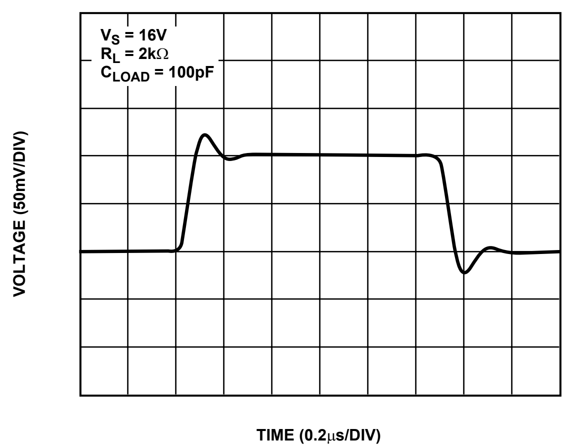

Figure 31. Small-Signal Transient Response

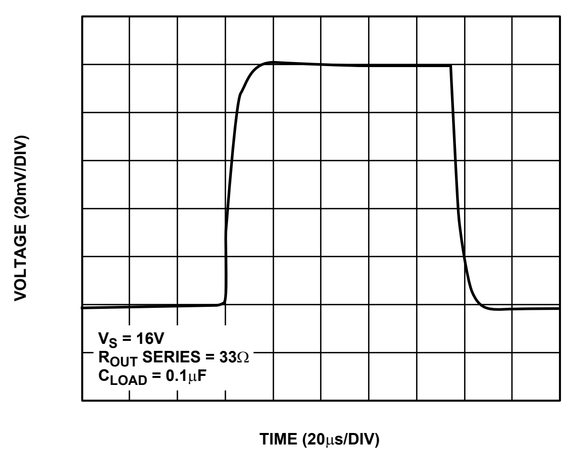

Figure 32. Small-Signal Transient Response

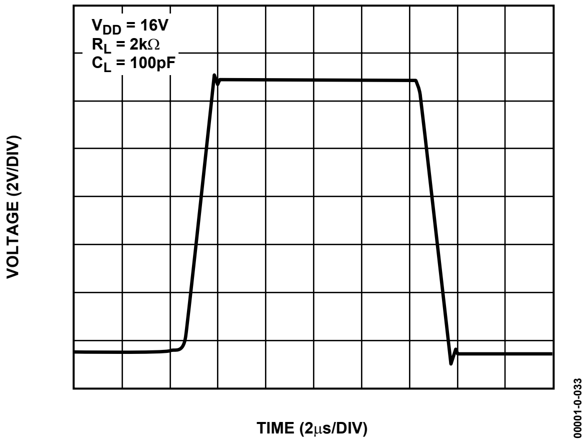

Figure 33. Large Signal Transient Response

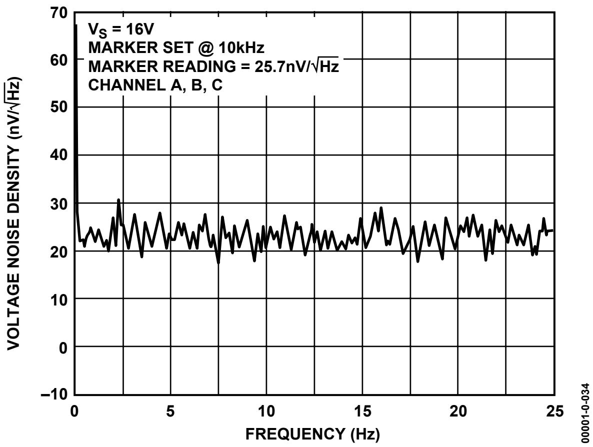

Figure 34. Voltage Noise Density vs. Frequency

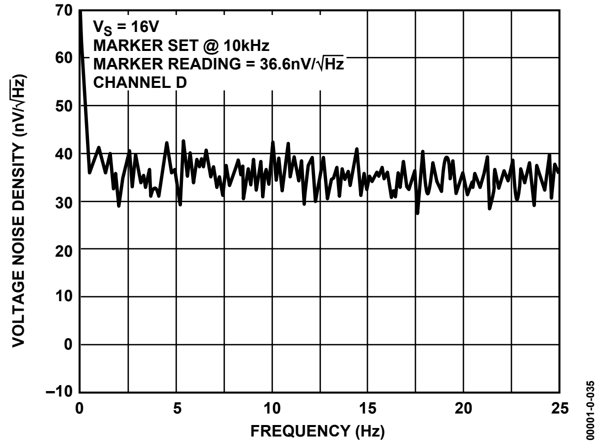

Figure 35. Voltage Noise Density vs. Frequency

APPLICATION INFORMATION

THEORY

The ADD8704 is designed for use in LCD gamma correction circuits. Depending on the panel architecture, between 4 and 18 different gamma voltages may be needed. These gamma voltages provide the reference voltages for the column driver RDACs. Due to the capacitive nature of LCD panels, it is necessary for these drivers to provide high capacitive load drive.

In addition to providing gamma reference voltages, these parts are also capable of providing the V_{COM} voltage. V_{COM} is the center voltage common to all the LCD pixels. Since the V_{COM} circuit is common to all the pixels in the panel, the V_{COM} driver is designed to supply continuous currents up to 35 mA.

INPUT

The ADD8704 has four amplifiers specifically designed for the needs of an LCD panel. Figure 36 shows a typical gamma correction curve for a normally white twisted nematic LCD panel. The symmetric curve comes from the need to reverse the polarity on the LC pixels to avoid "burning" in the image. The application therefore requires gamma voltages that come close to both supply rails. To accommodate this transfer function, the ADD8704 has been designed to have four different amplifiers in one package.

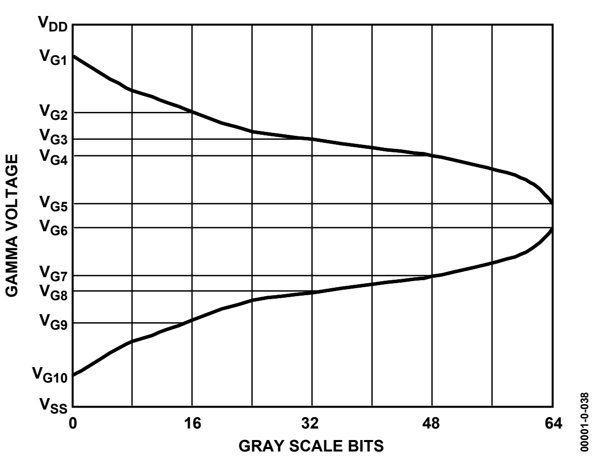

Figure 36. LCD Gamma Correction Curve

Amplifier A has a single-supply PNP input stage followed by a folded cascode stage. This provides an input range that goes to the bottom rail. This amplifier can therefore be used to provide the bottom voltage on the RDAC string.

Amplifier B (PNP folded cascode) swings to the low rail as well, but it provides 35 mA continuous output current versus 15 mA. This buffer is suitable for lower RDAC range, middle RDAC range, or V_{COM} applications.

Amplifier C is a rail-to-rail input range that makes the ADD8704 suitable for use anywhere on the RDAC as well as for V_{COM} applications.

Amplifier D has an NPN follower input stage. This covers the upper rail to GND plus 1.7 V. This amplifier is suitable for the upper range of the RDAC.

OUTPUT

The outputs of the amplifiers have been designed to match the performance needs of the gamma correction circuit. All four of the amplifiers have rail-to-rail outputs, but the current drive capabilities differ. Since amplifier A is suited for voltages close to V_{SS} (GND), the output is designed to sink more current than it sources; it can sink 15 mA of continuous current. Likewise, since amplifier D is primarily used for voltages close to V_{DD}, it sources more current. Amplifier D can source 15 mA of continuous current. Amplifiers B and C are designed for use as either midrange gamma or V_{COM} amplifiers. They therefore sink and source equal amounts of current. Since they are used as V_{COM} amplifiers, they have a drive capability of up to 35 mA of continuous current.

The nature of LCD panels introduces a large amount of parasitic capacitance from the column drivers as well as the capacitance associated with the liquid crystals via the common plane. This makes capacitive drive capability an important factor when designing the gamma correction circuit.

IMPORTANT NOTE

Because of the asymmetric nature of amplifiers A and D, care must be taken to connect an input that forces the amplifiers to operate in their most productive output states. Amplifier D has very limited sink capabilities, while amplifier A does not source well. If more than one ADD8704 is used, set the amplifier D input to enable the amplifier output to source current and set the amplifier A input to force a sinking output current. This means making sure the input is above the midpoint of the common-mode input range for amplifier D and below the midpoint for amplifier A. Mathematically speaking, make sure $V_{IN} > V_S/2$ for amplifier D and $V_{IN} < V_S/2$ for amplifier A.

Figure 37 shows an example using 4 ADD8704s to generate 10 gamma outputs. Note that the top three resistor tap-points are connected to the amplifier D inputs, thus assuring these channels will source current. Likewise, the bottom three resistor tap-points are connected to the amplifier A inputs to provide sinking output currents.

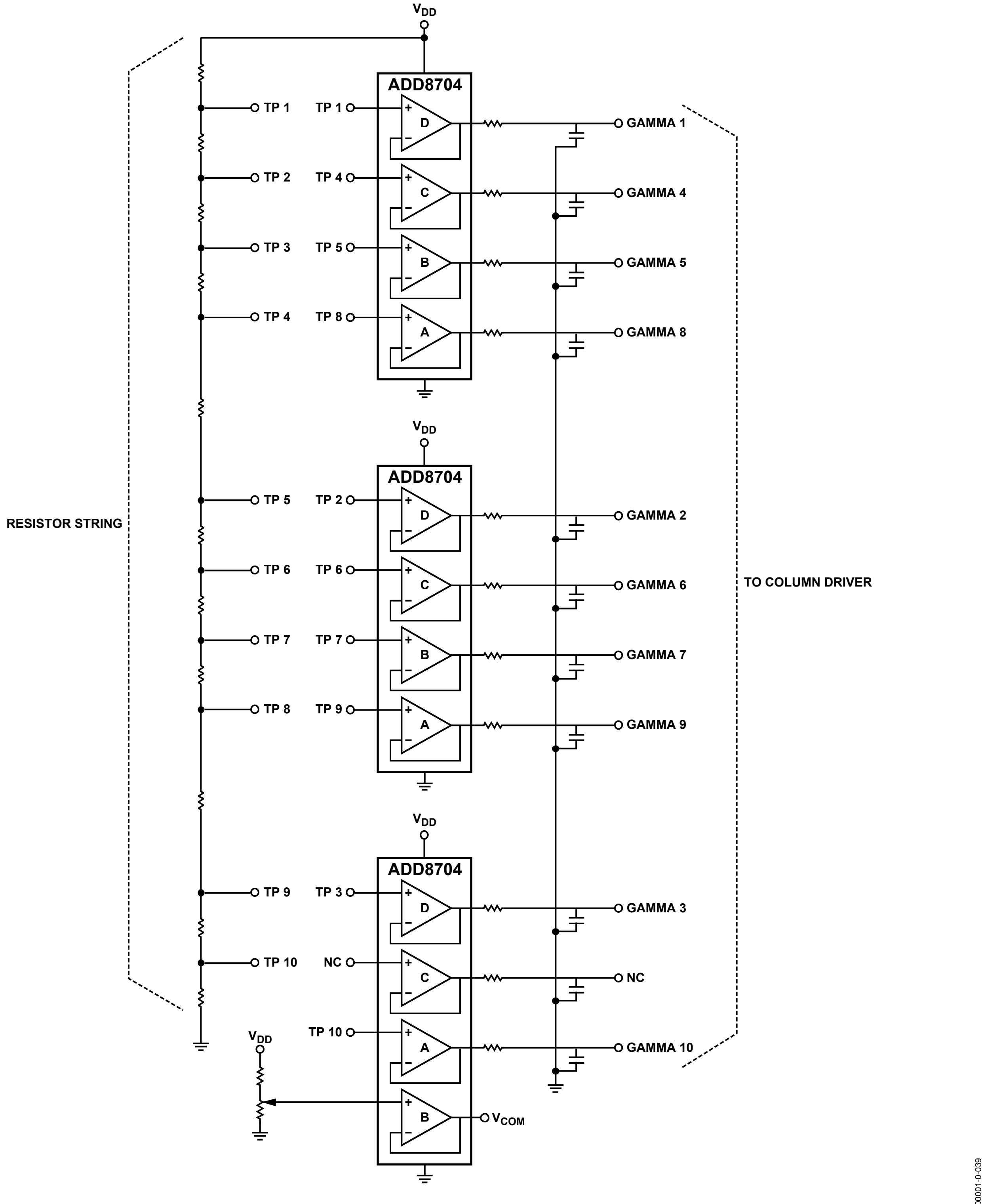

Figure 37. Using Four ADD8704s to Generate 10 Gamma Outputs

OUTLINE DIMENSIONS

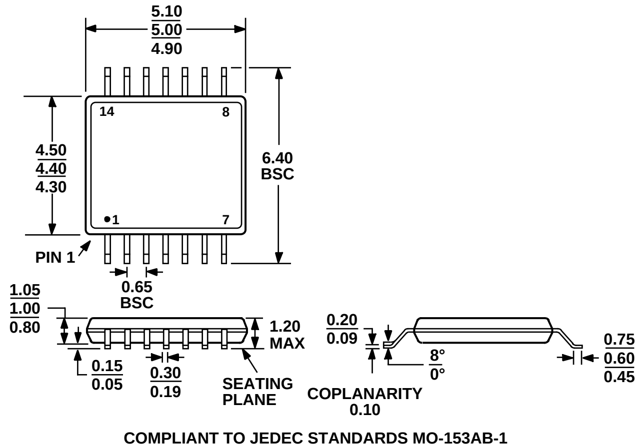

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU)
Dimensions shown in millimeters

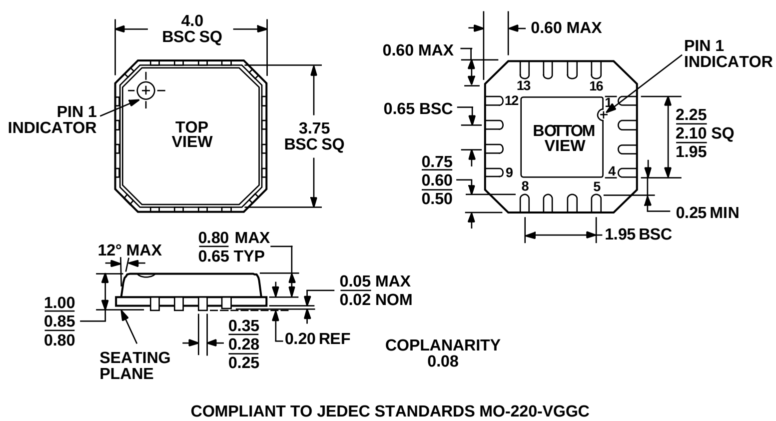

Figure 39. 16-Terminal Leadless Frame Chip Scale Package [LFCSP] (CP)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8704ARU	−40°C to +85°C	14-Lead Thin Shrink SOIC	RU-14
ADD8704ARU-REEL	−40°C to +85°C	14-Lead Thin Shrink SOIC	RU-14
ADD8704ARUZ[1]	−40°C to +85°C	14-Lead Thin Shrink SOIC	RU-14
ADD8704ARUZ-REEL[1]	−40°C to +85°C	14-Lead Thin Shrink SOIC	RU-14
ADD8704ACPZ-R2[1]	−40°C to +85°C	16-Terminal Leadless Frame Chip Scale	CP-16
ADD8704ACPZ-REEL7[1]	−40°C to +85°C	16-Terminal Leadless Frame Chip Scale	CP-16

[1] Z = Pb-free part.

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