PBL 403 09

3.6 V Differential Power Amplifier for DECT Telecommunications system

Description.

The PBL 403 09 is a differential two stage silicon MMIC power amplifier intended for use in handheld cordless terminals in the 1900 MHz band. It can deliver more than 27 dBm at 1900 MHz into a balanced 50 Ω load using a single 3.6 V supply. The circuit has a logic input to control transmit on/off and can be operated up to 100 % duty cycle with minimum performance degradation. The circuit is housed in a specially designed QSOP16 (150 mil body) package and the implementation requires only few external components.

25 GHz f_t state-of-the-art deep trench isolated double-poly silicon bipolar process with additional features for improved wireless performance has been used. On-chip capacitors and inductors are used for the integrated internal matching network. Special front-side metallized substrate contacts provide excellent ground paths from active devices to the highly doped semiconductor substrate and package ground.

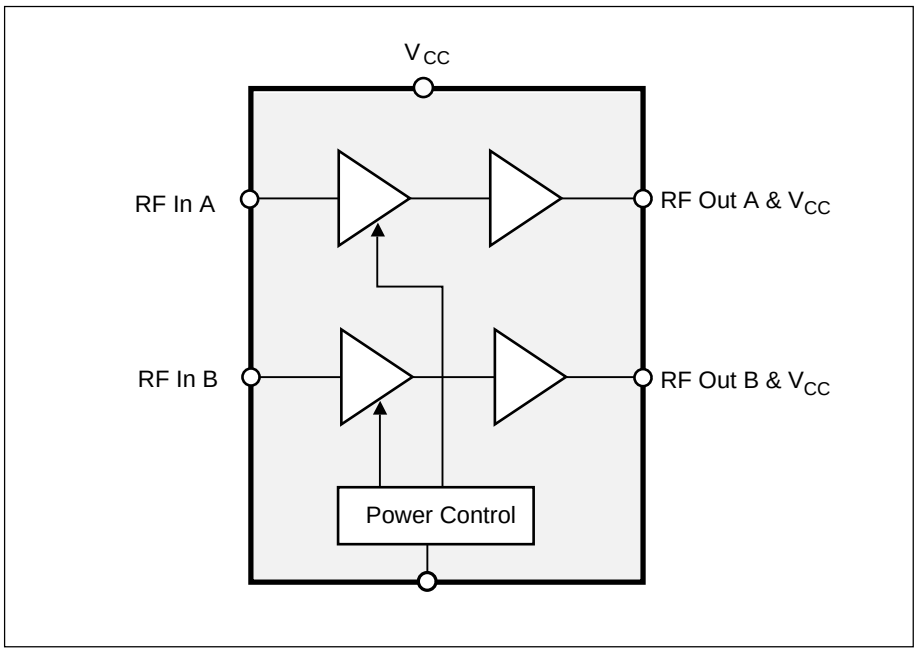


Figure 1. Block diagram.

Key features.

- 27 dBm output power
- 25 dB small signal gain
- 50 % Power Added Efficiency
- Simple logic on/off power control
- Battery charging conditions to 5.0 V
- ESD protected
- Excellent ruggedness
- On-chip input and interstage matching
- Differential input matched to 50 Ω
- Easy implementation with a simple output matching network
- Proven RF Silicon Technology Reliability
- Low overall solution cost

Applications.

- DECT

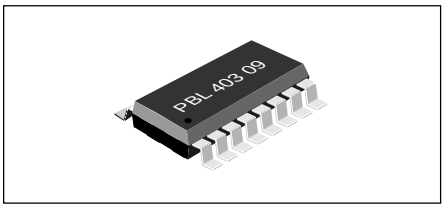


Figure 2. Package outlook.

Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage, continuous	Vcc	-	5.2	V
All inputs (zener protection)			6.5	V
Operating case temperature	T_{op}	-25	+80	°C
Storage temperature range	T_{Stg}	-30	+100	°C

Electrical Characteristics at room temperature

Unless otherwise stated the values below are valid for Vcc = 3.6 V, P_{in} = 4dBm, Z_L = 50 Ω and f = 1900 MHz, pulsed mode t = 417 µs, duty cycle 1/24. All data as measured in the recommended typical application circuit.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Frequency range		f	1880		1930	MHz
Power output	PA - ON = low	P	27	29	-	dBm
Power Added Efficiency	P_{in} = 10 dBm	PAE	45	50	-	%
Power Added Efficiency	P_{in} = 4 dBm	PAE	35	43	-	%
Small signal Gain	P_{in} = -10 dBm	G		25.5	-	dB
Isolation	PA - ON = high, P_{in} = 4 dBm			-35	-30	dB
2 nd and 3 rd harmonics	PA - ON = low, P_{in} < 4 dBm			-35		dBc
Input VSWR				1.6:1	3:1	
Load Mismatch	P_{in} = 4-10 dBm, Vcc = 5.2 V, Load VSWR = 6:1 all phases		no damage for 10 sec.			
Stability and spurious	P_{in} = 4-10 dBm, Vcc = 3.0-5.2 V, Load VSWR = 5:1 all phases		All spurious below - 36 dBm			
Supply current	No input signal present, PA - ON = low	I_{DC}		135		mA
Supply current	P_{in} = 4 dBm	I_{DC}		550		mA
Supply current	PA - ON = high	I_{DC}		1	10	µA
Rise time	P_{out} to 1dB from final value. Measure time from switch to low.	t_r			1	µA
Fall time	P_{out} to less than -20 dB measured from PA - ON pulse switched to high	t_f			2	µs
PA - ON = low			-0.5		0.5	V
PA - ON = high			Vcc -0.5		Vcc +0.5	V
I (PA - ON) low				110	130	µA

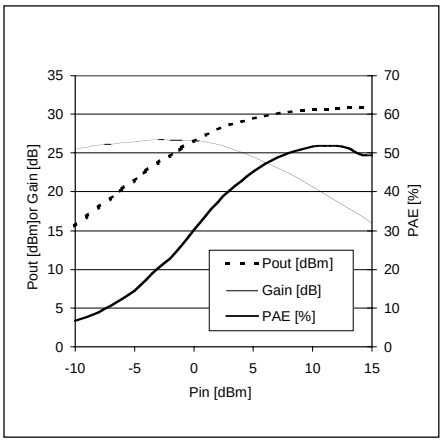


Figure 3. P_{out}, Gain and PAE vs. P_{in} V_{cc} = 3.6 V

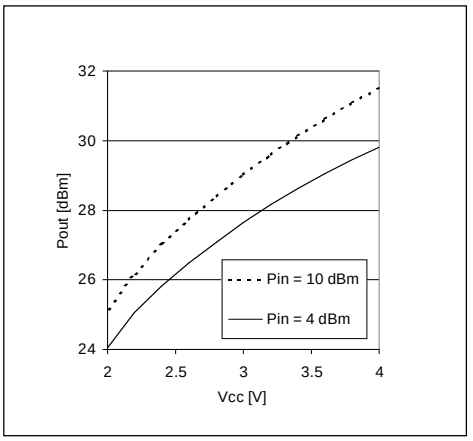


Figure 4. P_{out} vs. V_{cc} for P_{in} = 4 dBm and 10 dBm

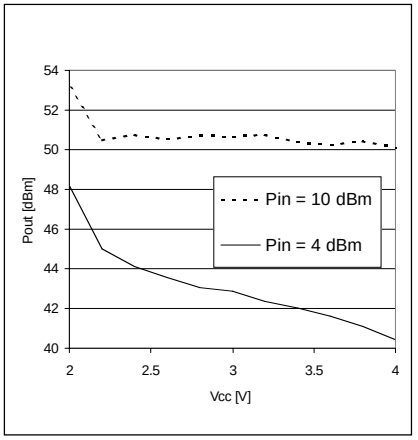


Figure 5. PAE vs.V_{cc} for P_{in} = 4 dBm and 10 dBm

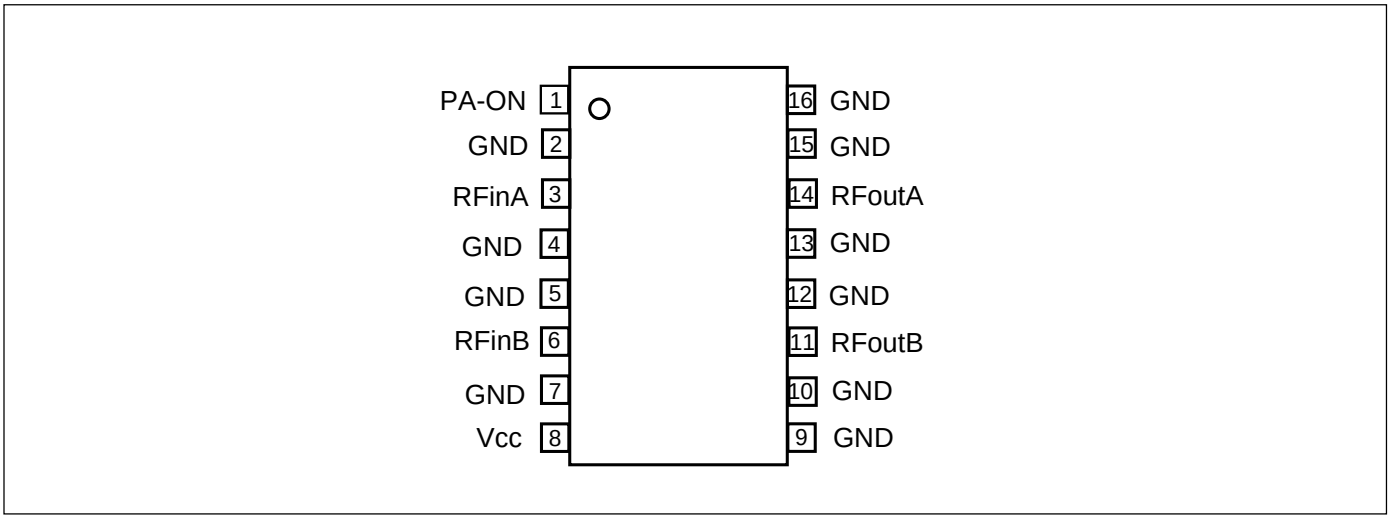


Figure 6. Pin configuration.

Pin Descriptions:

Refer to pin configuration.

SO	Name	Function	SO	Name	Function
1	PA-ON	PA On/Off Control pin (active low)	9	GND	Common ground
2	GND	Common ground	10	GND	Common ground
3	RFinA	RF input	11	RFoutB	RF output
4	GND	Common ground	12	GND	Common ground
5	GND	Common ground	13	GND	Common ground
6	RFinB	RF input	14	RFoutA	RF output
7	GND	Common ground	15	GND	Common ground
8	Vcc	Supply voltage	16	GND	Common ground

Functional description.

PBL403 09 is a differential two stage integrated power amplifier intended for DECT. The circuit is manufactured in a bipolar 5.0 V technology with additional features for improved wireless performance. Input and interstage matching is done completely on-chip, tuned to 1.9 GHz, and only normal supply decoupling plus output matching is necessary. If the device is used in a single ended environment, input and output transformers need to be added to the external circuitry.
PBL403 09 is optimized to work at a supply voltage of 3.6 V, but is able to operate between 2.7 and 5.2 V. At 3.6 V it can deliver up to 31 dBm when driven into compression, while 27 dBm is guaranteed with an input power of 4 dBm. Best Power Added Efficiency (PAE) is obtained close to maximum output power where PAE exeeds 50 %. Small signal gain is 25-26 dB. In a DECT handset with the duty cycle 1/24, the average power dissipation in the circuit is low, normally between 30 to 40 mW. In the base station, the duty cycle can increase and PBL403 09 can be operated at CW with a small penalty in power gain and output power (< 0.5 dB).
Operation is controlled through a power-on pin which is active low. When active, the current consumption is typically 135 mA without any input signal present. When not active, current consumption is less than 10 μA.

Application information.

DECT SINGLE ENDED POWER AMPLIFIER

When used as a single ended power amplifier, please refer to fig.7 and the test board fig. 8.

The 50 Ω source impedance is converted to 50 Ω differential with an LC-CL structure. Two series capacitors AC-couples the signal to the input of PBL403 09. Suitable value of the capacitors is 1 to 5 pF in order to compensate for series inductance of the PCB and package. Input impedance of the PBL403 09 is 50 Ω differential.
The ideal collector load of the open collector RF output of PBL403 09 is about 11 Ω per side. A matching and combination network to 50 Ω single ended case is shown in fig. 7. A shunt capacitor (2.7 pF) transforms each output to 50 Ω. Both 50 Ω outputs are AC coupled and then combined with an LC-CL structure to a 50 Ω single ended output.

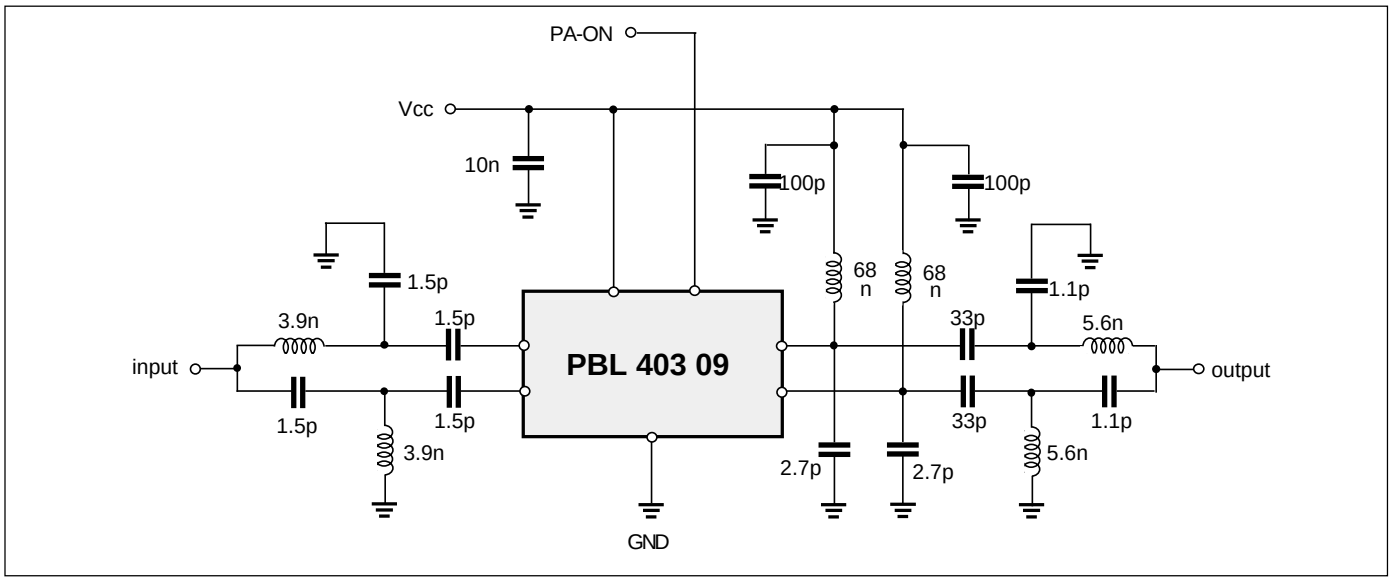


Figure 7. Evaluation setup including networks for unbalanced input/output.

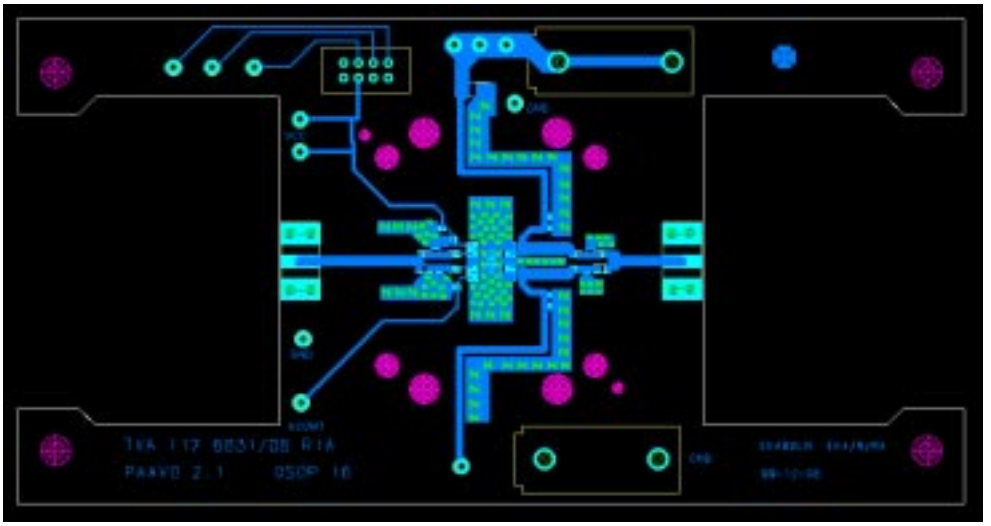


Figure 8. Evaluation testboard.

DECT RADIO WITH PBL402 15 TRANSCEIVER

PBL403 09 together with the transceiver chip PBL402 15 form the base of the radio platform for DECT systems. The transmission part of the chip PBL402 15 has a differential output which can deliver up to 7 dBm. The output power can be programmed in steps. The outputs are of open-collector type. Suitable network between PBL402 15 and PBL403 09 is therefore shunt inductors from the open-collectors to V_{cc} and series capacitors to the RF inputs of PBL403 09. Suitable value of the capacitors is 1 to 5 pF in order to compensate for the series inductance of the PCB and package. Input impedance of the PBL403 09 is 50 Ω differential.

The ideal collector load of the open collector RF output of PBL403 09 is about 11 Ω per side. A matching and combination network to 50 Ω single ended case is shown in fig.9. A shunt capacitor (2.7 pF) transforms each output to 50 Ω. Both 50 Ω outputs are AC coupled and then combined with an LC-CL structure to a 50 Ω single ended output.

A power control signal with active low is received from PBL402 15. This signal controls power up/down of the PBL403 09.

Supply decoupling consists of high frequency and low frequency decoupling capacitors. The high frequency decoupling capacitor should be placed close to the V_{cc} pin.

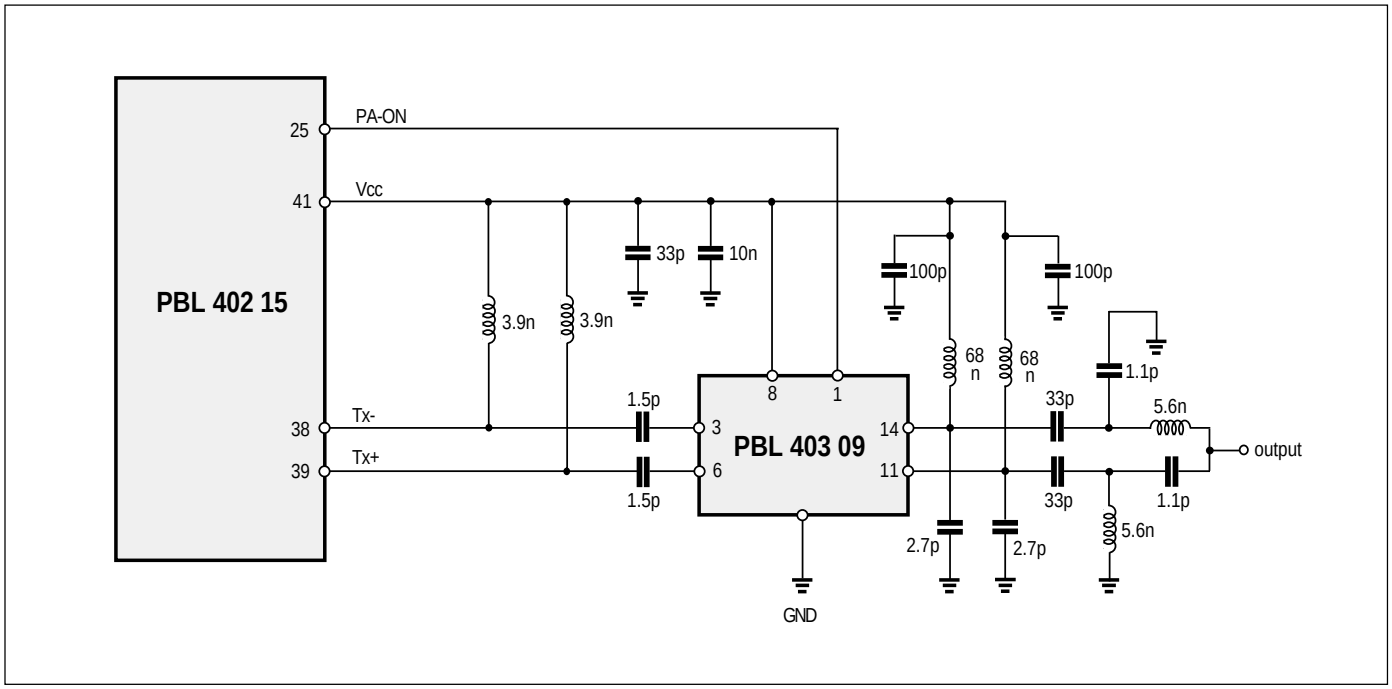
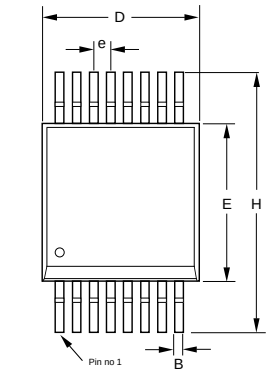
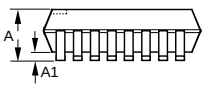


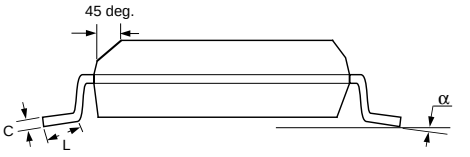
Figure 9. DECT radio with PBL402 015 transceiver and PA.

Package drawing, QSOP 16



Dim.	millimeters min.	max.	inches min.	max.
A	1.35	1.75	0.532	0.688
A1	0.10	0.25	0.004	0.0098
B	0.20	0.30	0.008	0.012
C	0.15	0.25	0.006	0.01
D	4.80	4.98	0.189	0.i96
E	3.81	3.99	0.150	0.157
e	0.635mm		0.025 inch ref.	
H	5.70	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
$\alpha = 0–8$ deg.				
h	0.22	0.49	0.009	0.019





Specifications subject to change without notice.

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Ordering Information

Package	Temp. Range	Part No.
16 pin plastic QSOP	-25 to 80°C	PBL 403 09