FUJITSU

CMOS 262,144-BIT STATIC RANDOM ACCESS MEMORY

MB 81C86-55
MB 81C86-70

September 1986
Edition 1.0

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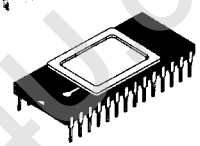
64K x 4 BIT(262,144-BIT) HIGH SPEED STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

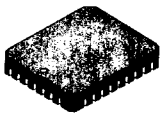
The Fujitsu MB 81C86 is a 65,536-words by 4-bits static random access memory fabricated with a CMOS silicon gate process. To make power dissipation lower, peripheral circuits consist of CMOS technology, and to obtain smaller chip size, cells consist of NMOS transistors and resistors. The memory utilizes asynchronous and requires single +5V power supply. All pins are TTL compatible.

The MB 81C86 is ideally suited for use in large computer systems and other applications where fast access time, large capacity and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization: 65,536 words x 4 bits
- Fast access time: $t_{AA} = t_{ACS}$ = 55 ns max. (MB 81C86-55)
  $t_{AA} = t_{ACS}$ = 70 ns max. (MB 81C86-70)
- Completely static operation: No clock required
- TTL compatible inputs/outputs
- Three-state output
- Separate data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 550 mW max. (Active)
  55 mW max. (Standby)
- Standard 28-pin DIP: (Suffix: -C)
- Standard 32-pad LCC: (Suffix: -CV)

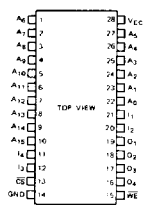


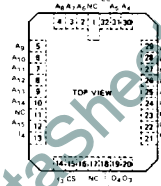
CERAMIC PACKAGE
DIP-28C-A07



CERAMIC PACKAGE
LCC-32C-A02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−3.0 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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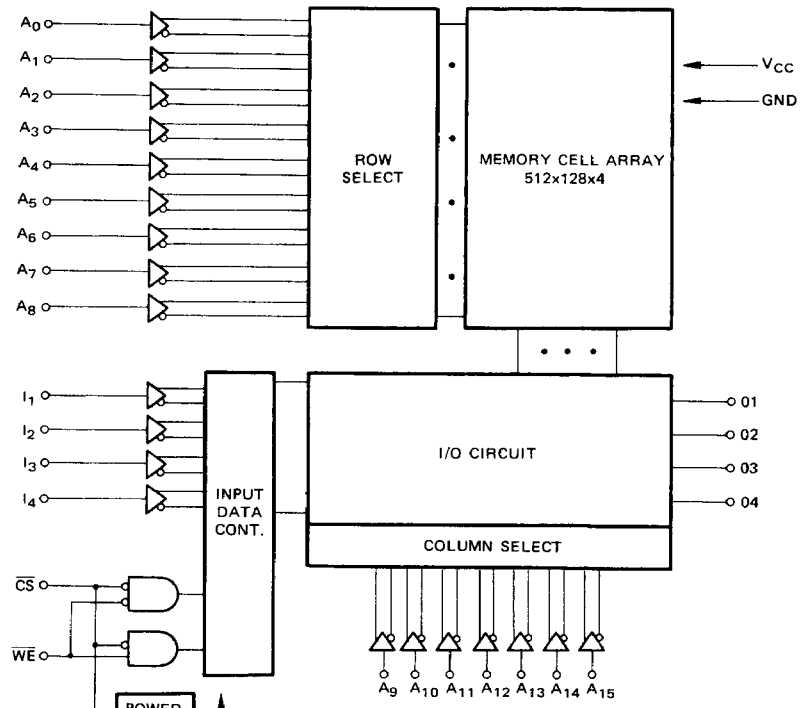
Fig. 1 – MB 81C86 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			8	pF
Input Capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

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RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*1		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

*1 -3.0 V Min. for pulse width less than 20 ns. (V_{IL} min. = -0.5 V at DC level)

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB}		10	mA	$\overline{CS} = V_{IH}$ V_{IN} = 0 V to V_{CC}
Operating Supply Current	I_{CC}		100	mA	Cycle = Min., I_{OUT} = 0 mA $\overline{CS} = V_{IL}$
Input Leakage Current	I_{LI}	-5	5	μA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-5	5	μA	$\overline{CS} = V_{IH}$ V_{OUT} = 0 V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 mA
Peak Power-on Current	I_{PO}		40	mA	V_{CC} = 0V to V_{CC} MAX. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.

Note: All voltages are referenced to GND

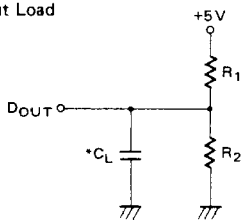
Fig. 2 – AC TEST CONDITIONS

Input Pulse Levels: 0.6V to 2.4V

Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)

Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.2V

Output Load



*Including Scope and Jig Capacitance

	R_1	R_2	C_L	Parameters Measured
Load I	480Ω	255Ω	30pF	except t_{LZ}, t_{HZ}, t_{WZ}, and t_{OW}
Load II	480Ω	255Ω	5pF	t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}

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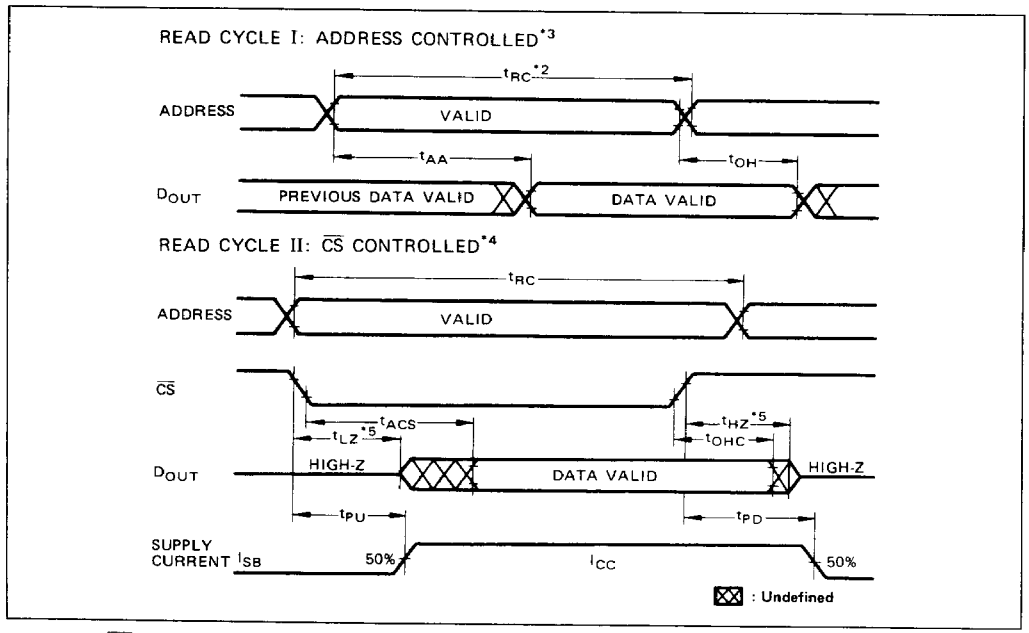
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE[*1]

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Read Cycle Time[*2]	t_{RC}	55		70		ns
Address Access Time[*3]	t_{AA}		55		70	ns
$\overline{CS}$ Access Time[*4]	t_{ACS}		55		70	ns
Output Hold from Address Change	t_{OH}	5		5		ns
Output Hold from $\overline{CS}$	t_{OHC}	5		5		ns
Chip Selection to Output Low-Z[*5]	t_{LZ}	10		10		ns
Chip Deselection to Output High-Z[*5]	t_{HZ}	5	25	5	25	ns
Power Up from $\overline{CS}$	t_{PU}	0		0		ns
Power Down from $\overline{CS}$	t_{PD}		40		40	ns

READ CYCLE TIMING DIAGRAM[*1]



Note: *1 $\overline{WE}$ is high for Read cycle.
*2 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*3 Device is continuously selected, $\overline{CS} = V_{IL}$.
*4 Address valid prior to or coincident with $\overline{CS}$ transition low.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

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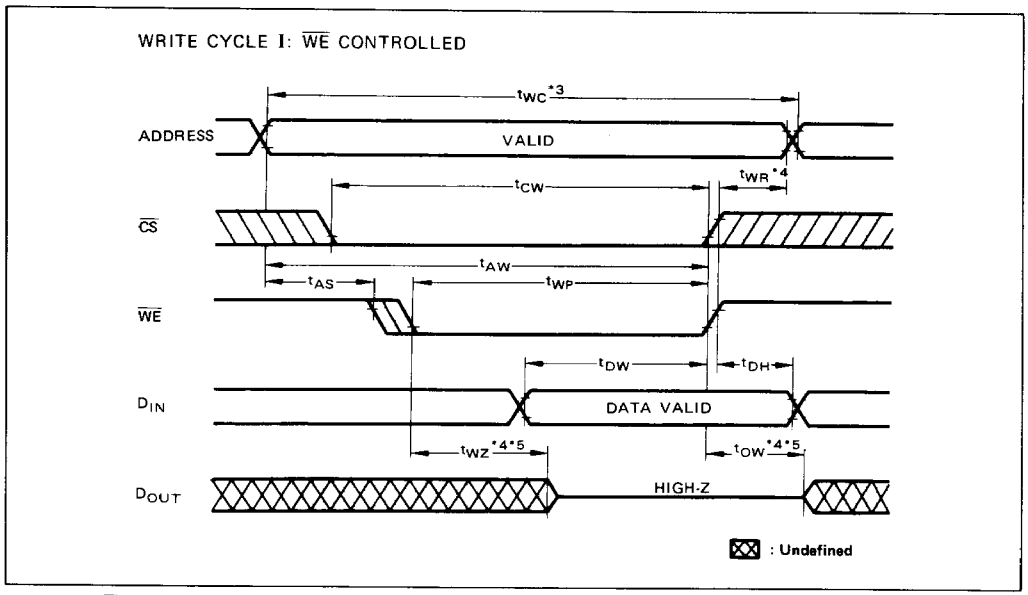
WRITE CYCLE *1*2

Parameter	Symbol	MB 81C86-55		MB 81C86-70		Unit
		Min	Max	Min	Max	
Write Cycle Time*3	t_{WC}	55		70		ns
Address Valid to End of Write	t_{AW}	45		50		ns
Chip Select to End of Write	t_{CW}	45		50		ns
Data Valid to End of Write	t_{DW}	25		30		ns
Data Hold Time	t_{DH}	5		5		ns
Write Pulse Width	t_{WP}	30		35		ns
Address Setup Time	t_{AS}	5		5		ns
Write Recovery Time*4	t_{WR}	5		5		ns
Output High-Z from $\overline{WE}$*5	t_{WZ}	0	25	0	25	ns
Output Low-Z from $\overline{WE}$*5	t_{OW}	5	30	5	35	ns

WRITE CYCLE TIMING DIAGRAM *1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Read cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified load II in Fig. 2.

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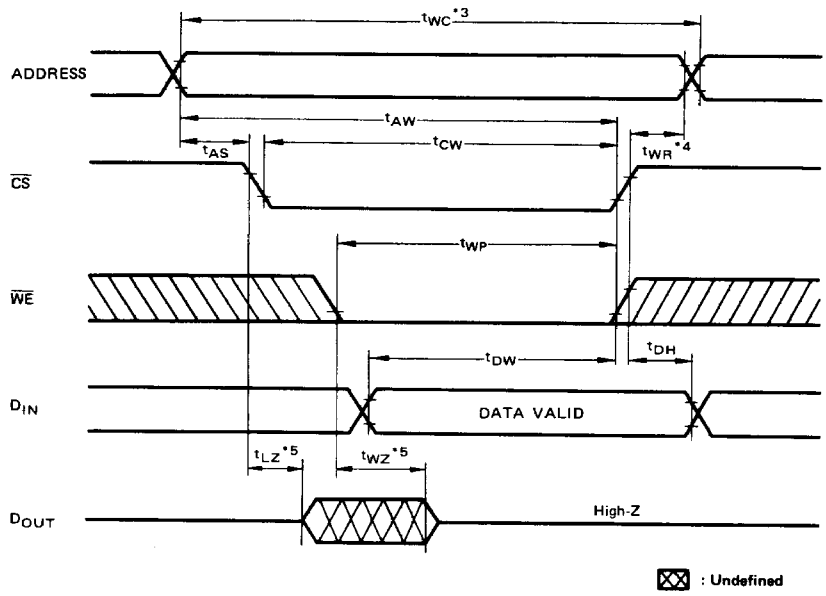
WRITE CYCLE II: $\overline{CS}$ CONTROLLED*1*2



Note: *1 $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
*2 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*3 All Write cycle timings are referenced from the last valid address to the first transitioning address.
*4 t_{WR} is defined from the end point of WRITE Mode.
*5 Transition is specified ±500mV from steady state voltage with specified Load II in Fig.2.

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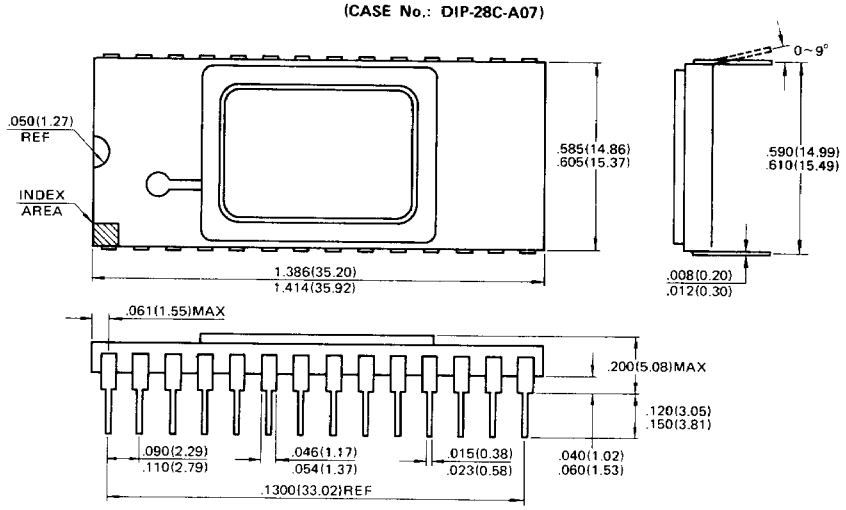
PACKAGE DIMENSIONS

(Suffix: -C)

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A07)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -CV)

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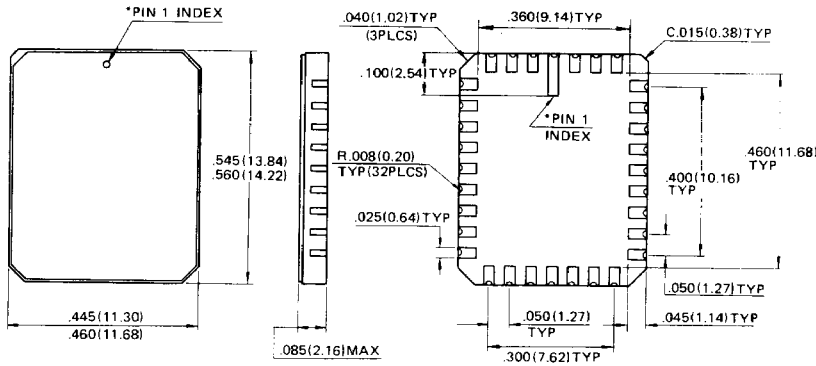
32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice