M36DR232A
M36DR232B

32 Mbit (2Mb x16, Dual Bank, Page) Flash Memory and 2 Mbit (128K x16) SRAM, Multiple Memory Product

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DDF} = V_{DDS} =1.65V to 2.2V
  - V_{PPF} = 12V for Fast Program (optional)
- ACCESS TIME: 100,120ns
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M36DR232A: 00A0h
  - Bottom Device Code, M36DR232B: 00A1h

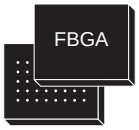
FLASH MEMORY

- 32 Mbit (2Mb x16) BOOT BLOCK
  - Parameter Blocks (Top or Bottom Location)
- PROGRAMMING TIME
  - 10µs typical
  - Double Word Programming Option
- ASYNCRONOUS PAGE MODE READ
  - Page width: 4 Word
  - Page Mode Access Time: 35ns
- DUAL BANK OPERATION
  - Read within one Bank while Program or Erase within the other
  - No Delay between Read and Write Operations
- BLOCK PROTECTION ON ALL BLOCKS
  - $\overline{WPF}$ for Block Locking
- COMMON FLASH INTERFACE
  - 64 bit Security Code

SRAM

- 2 Mbit (128K x 16 bit)
- LOW V_{DDS} DATA RETENTION: 1V
- POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS

Figure 1. Packages



Stacked LFBGA66 (ZA)
8 x 8 ball array

DESCRIPTION

The M36DR232 is a multichip memory device containing a 32 Mbit boot block Flash memory and a 4 Mbit of SRAM. The device is offered in a Stacked LFBGA66 (0.8 mm pitch) package.

The two components are distinguished by use with three chip enable inputs: $\overline{EF}$ for the Flash memory and, $\overline{E1S}$ and E2S for the SRAM. The two components are also separately power supplied and grounded.

Figure 2. Logic Diagram

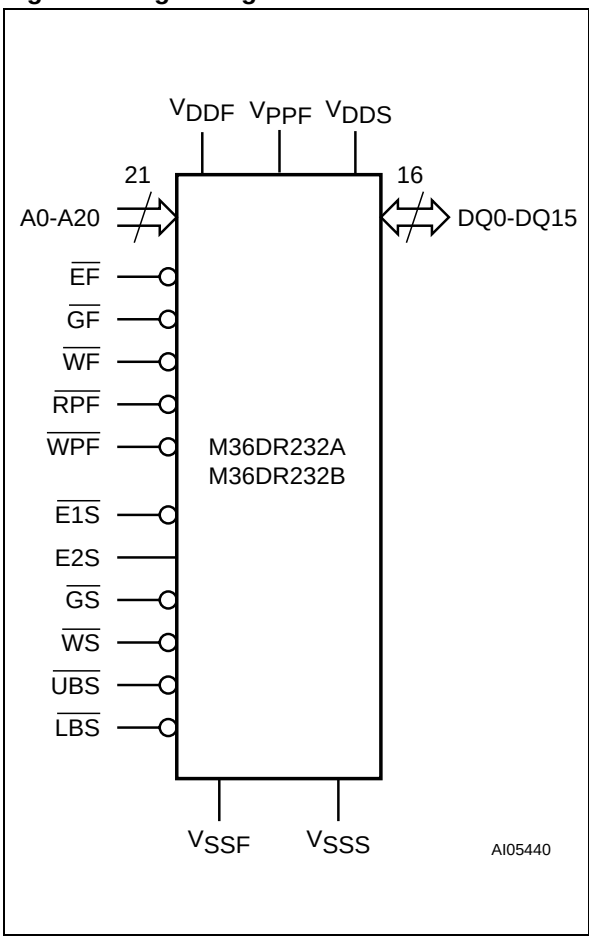


Table 1. Signal Names

A0-A16	Address Inputs
A17-A20	Address Inputs for Flash Chip only
DQ0-DQ15	Data Input/Output
V_{DDF}	Flash Power Supply
V_{PPF}	Flash Optional Supply Voltage for Fast Program & Erase
V_{SSF}	Flash Ground
V_{DDS}	SRAM Power Supply
V_{SSS}	SRAM Ground
NC	Not Connected Internally
Flash control functions	
$\overline{EF}$	Chip Enable input
$\overline{GF}$	Output Enable input
$\overline{WF}$	Write Enable input
$\overline{RPF}$	Reset input
$\overline{WPF}$	Write Protect input
SRAM control functions	
$\overline{E1S}$, E2S	Chip Enable input
$\overline{GS}$	Output Enable input
$\overline{WS}$	Write Enable input
$\overline{UBS}$	Upper Byte Enable input
$\overline{LBS}$	Lower Byte Enable input

Figure 3. LFBGA Connections (Top view through package)

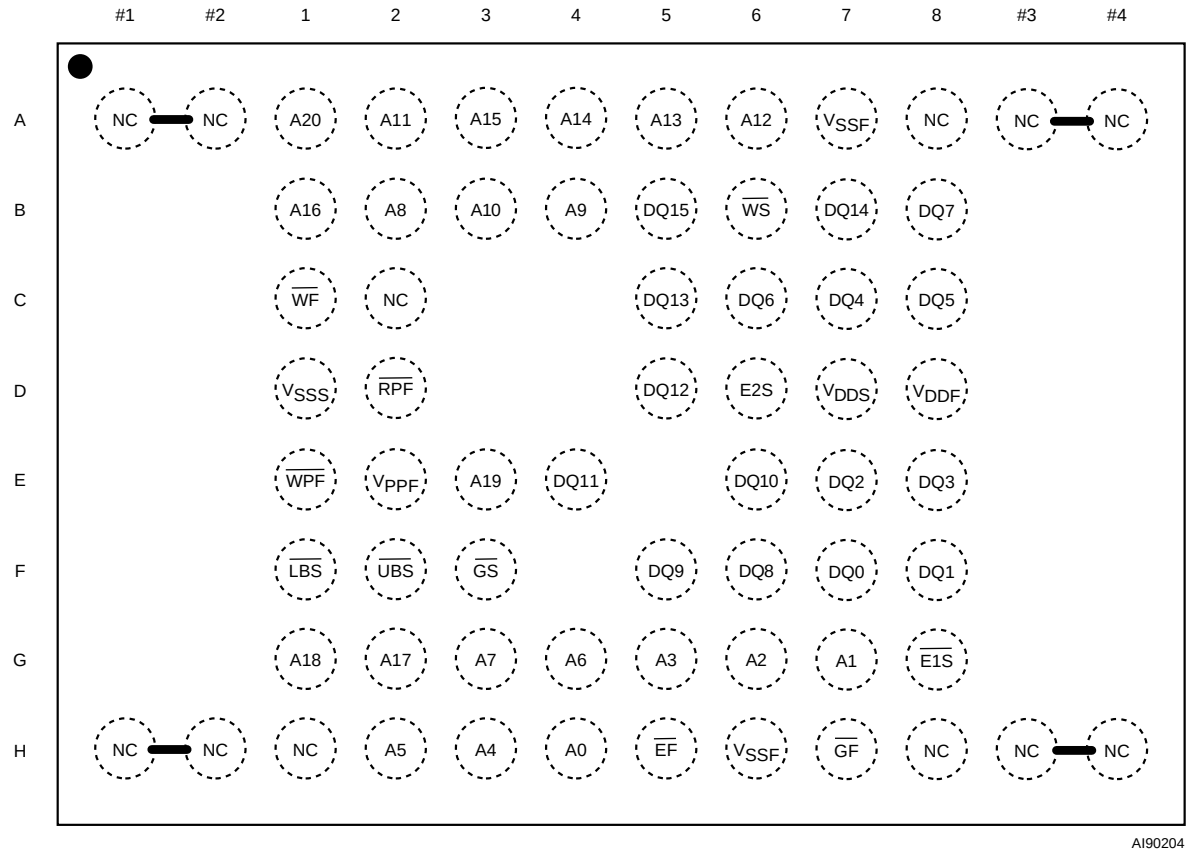
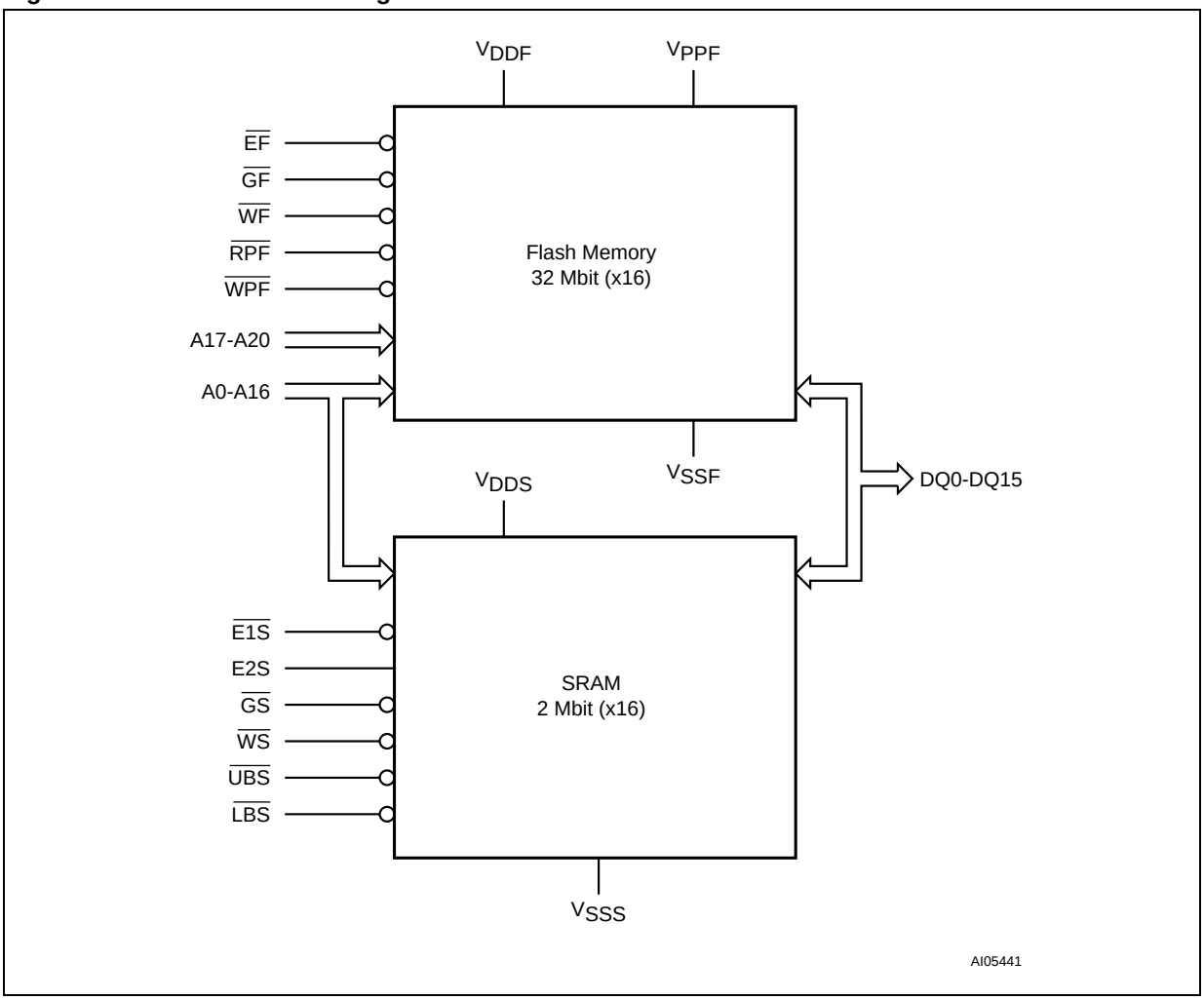


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IO} (2)	Input or Output Voltage	–0.2 to V_{DD}(4) + 0.3	V
V_{DDF}	Flash Chip Supply Voltage	–0.5 to 2.7	V
V_{DDS}	SRAM Chip Supply Voltage	–0.2 to 2.6	V
V_{PPF}	Program Voltage	–0.5 to 13.0	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum voltage may undershoot to –2V during transition and for less than 20ns.
3. Depends on range.
4. $V_{DD} = V_{DDS} = V_{DDF}$.

Figure 4. Functional Block Diagram



SIGNAL DESCRIPTIONS

See Figure 2 and Table 1.

Address Inputs (A0-A16). Addresses A0 to A16 are common inputs for the Flash chip and the SRAM chip. The address inputs for the Flash memory are latched during a write operation on the falling edge of the Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{WF}$), while address inputs for the SRAM array are latched during a write operation on the falling edge of the SRAM Chip Enable lines ($\overline{E1S}$ or E2S) or Write Enable ($\overline{WS}$).

Address Inputs (A17-A20). Address A17 to A20 are address inputs for the Flash chip. They are latched during a write operation on the falling edge of Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{WF}$).

Data Input/Outputs (DQ0-DQ15). The input is data to be programmed in the Flash or SRAM memory array or a command to be written to the C.I. of the Flash chip. Both are latched on the rising edge of Flash Chip Enable ($\overline{EF}$) or Write Enable ($\overline{WF}$) and, SRAM Chip Enable lines ($\overline{E1S}$ or E2S) or Write Enable ($\overline{WS}$). The output is data from the Flash memory or SRAM array, the Electronic Signature Manufacturer or Device codes or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Flash Chip Enable ($\overline{EF}$) and Output Enable ($\overline{GF}$) or SRAM Chip Enable lines ($\overline{E1S}$ or E2S) and Output Enable ($\overline{GS}$) are active. The output is high impedance when the both the Flash chip and the SRAM chip are deselected or the outputs are disabled and when Reset ($\overline{RPF}$) is at a V_{IL}.

Flash Chip Enable ($\overline{EF}$). The Chip Enable input for Flash activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{EF}$ at V_{IH} deselects the memory and reduces the power consumption to the standby level and output do Hi-Z. $\overline{EF}$ can also be used to control writing to the command register and to the Flash memory array, while $\overline{WF}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL}, $\overline{E1S}$ at V_{IL} and E2S at V_{IH} at the same time.

Flash Write Enable ($\overline{WF}$). The Write Enable input controls writing to the Command Register of the Flash chip and Address/Data latches. Data are latched on the rising edge of $\overline{WF}$.

Flash Output Enable ($\overline{GF}$). The Output Enable gates the outputs through the data buffers during a read operation of the Flash chip. When $\overline{GF}$ and $\overline{WF}$ are High the outputs are High impedance.

Flash Reset/Power Down Input ($\overline{RPF}$). The $\overline{RPF}$ input provides hardware reset of the memory (without affecting the Configuration Register status), and/or Power Down functions, depending on the Configuration Register status. Reset/Power Down of the memory is achieved by pulling $\overline{RPF}$ to V_{IL} for at least t_{PLPH}. When the reset pulse is given, if the memory is in Read, Erase Suspend Read or Standby, it will output new valid data in t_{PHQ7V1} after the rising edge of $\overline{RPF}$. If the memory is in Erase or Program modes, the operation will be aborted and the reset recovery will take a maximum of t_{PLQ7V}. The memory will recover from Power Down (when enabled) in t_{PHQ7V2} after the rising edge of $\overline{RPF}$. See Tables 1, 26 and Figure 11.

Flash Write Protect ($\overline{WPF}$). Write Protect is an input to protect or unprotect the two lockable parameter blocks of the Flash memory. When $\overline{WPF}$ is at V_{IL}, the lockable blocks are protected. Program or erase operations are not achievable. When $\overline{WPF}$ is at V_{IH}, the lockable blocks are unprotected and they can be programmed or erased (refer to Table 17).

SRAM Chip Enable ($\overline{E1S}$, E2S). The Chip Enable inputs for SRAM activate the memory control logic, input buffers and decoders. $\overline{E1S}$ at V_{IH} or E2S at V_{IL} deselects the memory and reduces the power consumption to the standby level. $\overline{E1S}$ and E2S can also be used to control writing to the SRAM memory array, while $\overline{WS}$ remains at V_{IL}. It is not allowed to set $\overline{EF}$ at V_{IL}, $\overline{E1S}$ at V_{IL} and E2S at V_{IH} at the same time.

SRAM Write Enable ($\overline{WS}$). The Write Enable input controls writing to the SRAM memory array. $\overline{WS}$ is active low.

SRAM Output Enable ($\overline{GS}$). The Output Enable gates the outputs through the data buffers during a read operation of the SRAM chip. $\overline{GS}$ is active low.

SRAM Upper Byte Enable ($\overline{UBS}$). Enable the upper bytes for SRAM (DQ8-DQ15). $\overline{UBS}$ is active low.

SRAM Lower Byte Enable ($\overline{LBS}$). Enable the lower bytes for SRAM (DQ0-DQ7). $\overline{LBS}$ is active low.

V_{DDF} Supply Voltage (1.65V to 2.2V). Flash memory power supply for all operations (Read, Program and Erase).

V_{PPF} Programming Voltage (11.4V to 12.6V). Used to provide high voltage for fast factory programming. High voltage on V_{PPF} pin is required to use the Double Word Program instruction. It is also possible to perform word program or erase instructions with V_{PPF} pin grounded.

V_{DDS} Supply Voltage (1.65V to 2.2V). SRAM power supply for all operations (Read, Program).

V_{SSF} and V_{SSS} Ground. V_{SSF} and V_{SSS} are the reference for all voltage measurements respectively in the Flash and SRAM chips.

Table 3. Main Operation Modes

Operation Mode		$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	$\overline{RPF}$	$\overline{WPF}$	V_{PPF}	$\overline{E1S}$	E2S	$\overline{GS}$	$\overline{WS}$	$\overline{UBS}$, $\overline{LBS}$ (1)	DQ15-DQ0
Flash Memory	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Don't care	SRAM must be disabled					Data Output
	Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{CCF} or V_{PPFH}	SRAM must be disabled					Data Input
	Block Locking	V_{IL}	X	X	V_{IH}	V_{IL}	Don't care	SRAM must be disabled					X
	Standby	V_{IH}	X	X	V_{IH}	X	Don't care	Any SRAM mode is allowable					Hi-Z
	Reset	X	X	X	V_{IL}	X	Don't care	Any SRAM mode is allowable					Hi-Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Don't care	Any SRAM mode is allowable					Hi-Z
SRAM	Read	Flash must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data out Word Read
	Write	Flash must be disabled						V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data in Word Write
	Standby/ Power Down	Any Flash mode is allowable						V_{IH}	X	X	X	X	Hi-Z
								X	V_{IL}	X	X	X	Hi-Z
								X	X	X	X	V_{IH}	Hi-Z
	Data Retention	Any Flash mode is allowable						V_{IH}	X	X	X	X	Hi-Z
								X	V_{IL}	X	X	X	Hi-Z
								X	X	X	X	V_{IH}	Hi-Z
	Output Disable	Any Flash mode is allowable						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PPFH} = 12V ± 5%.

1. If $\overline{UBS}$ and $\overline{LBS}$ are tied together the bus is at 16 bit. For an 8 bit bus configuration use $\overline{UBS}$ and $\overline{LBS}$ separately.

FLASH MEMORY COMPONENT

Organization

The Flash Chip is organized as 2Mb x16 bits. A0-A20 are the address lines, DQ0-DQ15 are the Data Input/Output. Memory control is provided by Chip Enable $\overline{EF}$, Output Enable $\overline{GF}$ and Write Enable $\overline{WF}$ inputs.

Reset $\overline{RPF}$ is used to reset all the memory circuitry and to set the chip in power down mode if this function is enabled by a proper setting of the Configuration Register. Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on DQ7 provides a Data Polling signal, DQ6 and DQ2 provide Toggle signals and DQ5 provides error bit to indicate the state of the P/E.C operations.

Memory Blocks

The device features asymmetrically blocked architecture. The Flash Chip has an array of 71 blocks and is divided into two banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible into Bank B or vice versa. The memory also features an erase suspend allowing to read or program in another block within the same bank. Once suspended the erase can be resumed. The Bank Size and Sectorization are summarized in Table 4. Parameter Blocks are located at the top of the memory address space for the Top version, and at the bottom for the Bottom version. The memory maps are shown in Tables 5, 6, 7 and 8.

The Program and Erase operations are managed automatically by the P/E.C. Block protection against Program or Erase provides additional data security. All blocks are protected at Power Up. Instructions are provided to protect or unprotect any block in the application. A second register locks the protection status while $\overline{WPF}$ is low (see Block Locking description). The Reset command does not affect the configuration of unprotected blocks and the Configuration Register status.

Device Operations

The following operations can be performed using the appropriate bus cycles: Read Array (Random, and Page Modes), Write command, Output Disable, Standby, Reset/Power Down and Block Locking. See Table 9.

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the CFI, the Block Protection Status or the Configuration Register status. Read operation of the memory array is performed in asynchronous page mode, that provides fast access time. Data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by A0-A1 address inputs. Read operations of the Electronic Signature, the Status Register, the CFI, the Block Protection Status, the Configuration Register status and the Security Code are performed as single asynchronous read cycles (Random Read). Both Chip Enable $\overline{EF}$ and Output Enable $\overline{GF}$ must be at V_{IL} in order to read the output of the memory.

Write. Write operations are used to give Instruction Commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{EF}$ and Write Enable $\overline{WF}$ are at V_{IL} with Output Enable $\overline{GF}$ at V_{IH}. Addresses are latched on the falling edge of $\overline{WF}$ or $\overline{EF}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{WF}$ or $\overline{EF}$ whichever occurs first. Noise pulses of less than 5ns typical on $\overline{EF}$, $\overline{WF}$ and $\overline{GF}$ signals do not start a write cycle.

Dual Bank Operations. The Dual Bank allows to read data from one bank of memory while a program or erase operation is in progress in the other bank of the memory. Read and Write cycles can be initiated for simultaneous operations in different banks without any delay. Status Register during Program or Erase must be monitored using an address within the bank being modified.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{GF}$ is at V_{IH} with Write Enable $\overline{WF}$ at V_{IH}.

Standby. The memory is in standby when Chip Enable $\overline{EF}$ is at V_{IH} and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{GF}$ or Write Enable $\overline{WF}$ inputs.

Automatic Standby. When in Read mode, after 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus.

Power Down. The memory is in Power Down when the Configuration Register is set for Power Down and $\overline{RPF}$ is at V_{IL}. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independent of the Chip Enable $\overline{EF}$, Output Enable $\overline{GF}$ or Write Enable $\overline{WF}$ inputs.

Block Locking. Any combination of blocks can be temporarily protected against Program or Erase by setting the lock register and pulling $\overline{WPF}$ to V_{IL} (see Block Lock instruction).

Table 4. Bank Size and Sectorization

	Bank Size	Parameter Blocks	Main Blocks
Bank A	4 Mbit	8 blocks of 4 KWord	7 blocks of 32 KWord
Bank B	28 Mbit	-	56 blocks of 32 KWord

Table 5. Bank A, Top Boot Block Addresses M36DR232A

#	Size (KWord)	Address Range
0	4	1FF000h-1FFFFFh
1	4	1FE000h-1FEFFFh
2	4	1FD000h-1FDFFFh
3	4	1FC000h-1FCFFFh
4	4	1FB000h-1FBFFFh
5	4	1FA000h-1FAFFFh
6	4	1F9000h-1F9FFFh
7	4	1F8000h-1F8FFFh
8	32	1F0000h-1F7FFFh
9	32	1E8000h-1EFFFFh
10	32	1E0000h-1E7FFFh
11	32	1D8000h-1DFFFFh
12	32	1D0000h-1D7FFFh
13	32	1C8000h-1CFFFFh
14	32	1C0000h-1C7FFFh

Table 6. Bank B, Top Boot Block Addresses M36DR232A

#	Size (KWord)	Address Range
0	32	1B8000h-1BFFFFh
1	32	1B0000h-1B7FFFh
2	32	1A8000h-1AFFFFh
3	32	1A0000h-1A7FFFh
4	32	198000h-19FFFFh
5	32	190000h-197FFFh
6	32	188000h-18FFFFh
7	32	180000h-187FFFh
8	32	178000h-17FFFFh
9	32	170000h-177FFFh
10	32	168000h-16FFFFh
11	32	160000h-167FFFh
12	32	158000h-15FFFFh
13	32	150000h-157FFFh
14	32	148000h-14FFFFh
15	32	140000h-147FFFh
16	32	138000h-13FFFFh
17	32	130000h-137FFFh
18	32	128000h-12FFFFh
19	32	120000h-127FFFh
20	32	118000h-11FFFFh
21	32	110000h-117FFFh
22	32	108000h-10FFFFh
23	32	100000h-107FFFh
24	32	0F8000h-0FFFFFh
25	32	0F0000h-0F7FFFh
26	32	0E8000h-0EFFFFh
27	32	0E0000h-0E7FFFh
28	32	0D8000h-0DFFFFh
29	32	0D0000h-0D7FFFh
30	32	0C8000h-0CFFFFh
31	32	0C0000h-0C7FFFh
32	32	0B8000h-0BFFFFh
33	32	0B0000h-0B7FFFh
34	32	0A8000h-0AFFFFh
35	32	0A0000h-0A7FFFh
36	32	098000h-09FFFFh
37	32	090000h-097FFFh
38	32	088000h-08FFFFh
39	32	080000h-087FFFh
40	32	078000h-07FFFFh
41	32	070000h-077FFFh
42	32	068000h-06FFFFh
43	32	060000h-067FFFh
44	32	058000h-05FFFFh
45	32	050000h-057FFFh
46	32	048000h-04FFFFh
47	32	040000h-047FFFh
48	32	038000h-03FFFFh
49	32	030000h-037FFFh
50	32	028000h-02FFFFh
51	32	020000h-027FFFh
52	32	018000h-01FFFFh
53	32	010000h-017FFFh
54	32	008000h-00FFFFh
55	32	000000h-007FFFh

Table 7. Bank B, Bottom Boot Block Addresses M36DR232B

#	Size (KWord)	Address Range
55	32	1F8000h-1FFFFFh
54	32	1F0000h-1F7FFFh
53	32	1E8000h-1EFFFFh
52	32	1E0000h-1E7FFFh
51	32	1D8000h-1DFFFFh
50	32	1D0000h-1D7FFFh
49	32	1C8000h-1CFFFFh
48	32	1C0000h-1C7FFFh
47	32	1B8000h-1BFFFFh
46	32	1B0000h-1B7FFFh
45	32	1A8000h-1AFFFFh
44	32	1A0000h-1A7FFFh
43	32	198000h-19FFFFh
42	32	190000h-197FFFh
41	32	188000h-18FFFFh
40	32	180000h-187FFFh
39	32	178000h-17FFFFh
38	32	170000h-177FFFh
37	32	168000h-16FFFFh
36	32	160000h-167FFFh
35	32	158000h-15FFFFh
34	32	150000h-157FFFh
33	32	148000h-14FFFFh
32	32	140000h-147FFFh
31	32	138000h-13FFFFh
30	32	130000h-137FFFh
29	32	128000h-12FFFFh
28	32	120000h-127FFFh
27	32	118000h-11FFFFh
26	32	110000h-117FFFh
25	32	108000h-10FFFFh
24	32	100000h-107FFFh
23	32	0F8000h-0FFFFFh
22	32	0F0000h-0F7FFFh
21	32	0E8000h-0EFFFFh
20	32	0E0000h-0E7FFFh
19	32	0D8000h-0DFFFFh
18	32	0D0000h-0D7FFFh
17	32	0C8000h-0CFFFFh
16	32	0C0000h-0C7FFFh
15	32	0B8000h-0BFFFFh
14	32	0B0000h-0B7FFFh
13	32	0A8000h-0AFFFFh
12	32	0A0000h-0A7FFFh
11	32	098000h-09FFFFh
10	32	090000h-097FFFh
9	32	088000h-08FFFFh
8	32	080000h-087FFFh
7	32	078000h-07FFFFh
6	32	070000h-077FFFh
5	32	068000h-06FFFFh
4	32	060000h-067FFFh
3	32	058000h-05FFFFh
2	32	050000h-057FFFh
1	32	048000h-04FFFFh
0	32	040000h-047FFFh

Table 8. Bank A, Bottom Boot Block Addresses M36DR232B

#	Size (KWord)	Address Range
14	32	038000h-03FFFFh
13	32	030000h-037FFFh
12	32	028000h-02FFFFh
11	32	020000h-027FFFh
10	32	018000h-01FFFFh
9	32	010000h-017FFFh
8	32	008000h-00FFFFh
7	4	007000h-007FFFh
6	4	006000h-006FFFh
5	4	005000h-005FFFh
4	4	004000h-004FFFh
3	4	003000h-003FFFh
2	4	002000h-002FFFh
1	4	001000h-001FFFh
0	4	000000h-000FFFh

Table 9. User Bus Operations (1)

Operation	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	$\overline{RPF}$	$\overline{WPF}$	DQ0-DQ15
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	Hi-Z
Reset / Power Down	X	X	X	V_{IL}	V_{IH}	Hi-Z
Block Locking	V_{IL}	X	X	V_{IH}	V_{IL}	X

Note: 1. X = Don't care.

Table 10. Read Electronic Signature (AS and Read CFI instructions)

Code	Device	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A2-A7	Other Addresses	DQ0-DQ7	DQ8-DQ15
Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	Don't Care	20h	00h
Device Code	M36DR232A	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	A0h	00h
	M36DR232B	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	A1h	00h

Table 11. Read Block Protection (AS and Read CFI instructions)

Block Status	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A2-A7	Other Addresses	A12-A20	DQ0	DQ1	DQ2-DQ15
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	1	0	0000h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	0	0	0000h
Locked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	0	Don't Care	Block Address	X	1	0000h

Table 12. Read Configuration Register (AS and Read CFI instructions)

$\overline{RPF}$ Function	$\overline{EF}$	$\overline{GF}$	$\overline{WF}$	A0	A1	A2-A7	Other Addresses	DQ10	DQ0-DQ9 DQ11-DQ15
Reset	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	0	Don't Care	0	Don't Care
Reset/Power Down	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	0	Don't Care	1	Don't Care

INSTRUCTIONS AND COMMANDS

Seventeen instructions are defined (see Table 15), and the internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle, Error bits can be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions, made up of one or more commands written in cycles, can be given to the Program/ Erase Controller through a Command Interface (C.I.). The C.I. latches commands written to the memory. Commands are made of address and data sequences. Two Coded Cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The Coded Sequence consists of writing the data AAh at the address 555h during the first cycle and the data 55h at the address 2AAh during the second cycle.

Instructions are composed of up to six cycles. The first two cycles input a Coded Sequence to the Command Interface which is common to all instructions (see Table 15). The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data, Electronic Signature, Block Protection, Configuration Register Status or CFI Query for Read operations. In order to give additional data protection, the instructions for Block Erase and Bank Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For a Double Word Programming instruction, the fourth and fifth command cycles input the address and data to be programmed. For a Block Erase and Bank Erase instructions, the fourth and fifth cycles input a further Coded Sequence before the Erase confirm command on the sixth cycle. Any combination of blocks of the same memory bank can be erased. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed. When power is first applied the command interface is reset to Read Array.

Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to ensure maximum data security.

Table 13. Commands

Hex Code	Command
00h	Bypass Reset
10h	Bank Erase Confirm
20h	Unlock Bypass
30h	Block Erase Resume/Confirm
40h	Double Word Program
60h	Block Protect, or Block Unprotect, or Block Lock, or Write Configuration Register
80h	Set-up Erase
90h	Read Electronic Signature, or Block Protection Status, or Configuration Register Status
98h	CFI Query
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded Cycles. Subsequent read operations will read the memory array addressed and output the data read.

CFI Query (RCFI) Instruction. Common Flash Interface Query mode is entered writing 98h at address 55h. The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. Table 18, 19, 20 and 21 show the addresses used to retrieve each data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 80h. This area can be accessed only in read mode by the final user and there are no ways of changing the code after it has been written by ST. Write a read instruction (RD) to return to Read mode.

Auto Select (AS) Instruction. This instruction uses two Coded Cycles followed by one write cycle giving the command 90h to address 555h for command set-up. A subsequent read will output the Manufacturer or the Device Code (Electronic Signature), the Block Protection status or the Configuration Register status depending on the levels of A0 and A1 (see Table 10, 11 and 12). A7-A2 must be at V_{IL}, while other address input are ignored.

The bank address is don't care for this instruction. The Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of Flash Chip. The Manufacturer Code is output when the address lines A0 and A1 are at V_{IL}, the Device Code is output when A0 is at V_{IH} with A1 at V_{IL}.

The codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h. The AS instruction also allows the access to the Block Protection Status. After giving the AS instruction, A0 is set to V_{IL} with A1 at V_{IH}, while A12-A20 define the address of the block to be verified. A read in these conditions will output a 01h if the block is protected and a 00h if the block is not protected.

The AS Instruction finally allows the access to the Configuration Register status if both A0 and A1 are set to V_{IH}. If DQ10 is '0' only the Reset function is active as RPF is set to V_{IL} (default at power-up). If DQ10 is '1' both the Reset and the Power Down functions will be achieved by pulling RPF to V_{IL}. The other bits of the Configuration Register are reserved and must be ignored. A reset command puts the device in read array mode.

Write Configuration Register (CR) Instruction. This instruction uses two Coded Cycles followed by one write cycle giving the command 60h to address 555h. A further write cycle giving the command 03h writes the contents of address bits A0-A15 to the 16 bits configuration register. Bits written by inputs A0-A9 and A11-A15 are reserved for future use. Address input A10 defines the status of the Reset/Power Down functions. It must be set to V_{IL} to enable only the Reset function and to V_{IH} to enable also the Power Down function. At Power Up all the Configuration Register bits are reset to '0'.

Enter Bypass Mode (EBY) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 20h to address 555h for mode set-up. Once in Bypass mode, the device will accept the Exit Bypass (XBY) and Program or Double Word Program in Bypass mode (PGBY, DPGBY) commands. The Bypass mode allows to reduce the overall programming time when large memory arrays need to be programmed.

Exit Bypass Mode (XBY) Instruction. This instruction uses two write cycles. The first inputs to the memory the command 90h and the second inputs the Exit Bypass mode confirm (00h). After the XBY instruction, the device resets to Read Memory Array mode.

Program in Bypass Mode (PGBY) Instruction. This instruction uses two write cycles. The Program command A0h is written to any Address on the first cycle and the second write cycle latches the Address on the falling edge of $\overline{WF}$ or $\overline{EF}$ and the Data to be written on the rising edge and starts the P/E.C. Read operations within the same bank output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error.

Program (PG) Instruction. This instruction uses four write cycles. The Program command A0h is written to address 555h on the third cycle after two Coded Cycles. A fourth write operation latches the Address and the Data to be written and starts the P/E.C. Read operations within the same bank output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend.

Double Word Program (DPG) Instruction. This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel. High voltage (11.4V to 12.6V) on V_{PP} pin is required. This instruction uses five write cycles. The double word program command 40h is written to address 555h on the third cycle after two Coded Cycles. A fourth write cycle latches the address and data to be written to the first location. A fifth write cycle latches the new data to be written to the second location and starts the P/E.C.. Note that the two locations must have the same address except for the address bit A0. The Double Word Program can be executed in Bypass mode (DPGBY) to skip the two coded cycles at the beginning of each command.

Block Protect (BP), Block Unprotect (BU), Block Lock (BL) Instructions. All blocks are protected at power-up. Each block of the array has two levels of protection against program or erase operation. The first level is set by the Block Protect instruction; a protected block cannot be programmed or erased until a Block Unprotect instruction is given for that block. A second level of protection is set by the Block Lock instruction, and requires the use of the WPF pin, according to the following scheme:

– when $\overline{WPF}$ is at V_{IH}, the Lock status is overridden and all blocks can be protected or unprotected;
– when $\overline{WPF}$ is at V_{IL}, Lock status is enabled; the locked blocks are protected, regardless of their previous protect state, and protection status cannot be changed. Blocks that are not locked can still change their protection status, and program or erase accordingly;

– the lock status is cleared for all blocks at power up; once a block has been locked state can be cleared only with a reset command. The protection and lock status can be monitored for each block using the Autoselect (AS) instruction. Protected blocks will output a ‘1’ on DQ0 and locked blocks will output a ‘1’ on DQ1.

Refer to Table 14 for a list of the protection states.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 555h on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles and an address within the block to be erased is given and latched into the memory.

Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. All blocks must belong to the same bank of memory; if a new block belonging to the other bank is given, the operation is aborted. The erase will start after an erase timeout period of 100µs. Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C. is erasing the Block(s). If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before erasing to FFh. Read operations within the same bank, after the sixth rising edge of WF or EF, output the status register bits.

During the execution of the erase by the P/E.C., the memory accepts only the Erase Suspend ES instruction; the Read/Reset RD instruction is accepted during the 100µs time-out period. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit DQ6 toggles during the erase operation, and stops when erase is completed.

After completion the Status Register bit DQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit DQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the P/E.C.

Bank Erase (BKE) Instruction. This instruction uses six write cycles and is used to erase all the blocks belonging to the selected bank. The Erase Set-up command 80h is written to address 555h on the third cycle after the two Coded cycles. The Bank Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles at an address within the selected bank. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing it to FFh. Read operations within the same bank after the sixth rising edge of WF or EF output the Status Register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bit DQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure.

Erase Suspend (ES) Instruction. In a dual bank memory the Erase Suspend instruction is used to read data within the bank where erase is in progress. It is also possible to program data in blocks not being erased.

The Erase Suspend instruction consists of writing the command B0h without any specific address. No Coded Cycles are required. Erase suspend is accepted only during the Block Erase instruction execution. The Toggle bit DQ6 stops toggling when the P/E.C. is suspended within 15µs after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions. A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in DQ6 toggling when the data is being programmed.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at an address within the bank being erased and without any Coded Cycle.

Table 14. Protection States (1)

Current State (2) (WP, DQ1, DQ0)	Program/Erase Allowed	Next State After Event (3)			
		Protect	Unprotect	Lock	$\overline{WP}$ transition
100	yes	101	100	111	000
101	no	101	100	111	001
110	yes	111	110	111	011
111	no	111	110	111	011
000	yes	001	000	011	100
001	no	001	000	011	101
011	no	011	011	011	111 or 110 (4)

Note: 1. All blocks are protected at power-up, so the default configuration is 001 or 101 according to $\overline{WPF}$ status.
2. Current state and Next state gives the protection status of a block. The protection status is defined by the write protect pin and by DQ1 (= 1 for a locked block) and DQ0 (= 1 for a protected block) as read in the Autoselect instruction with A1 = V_{IH} and A0 = V_{IL}.
3. Next state is the protection status of a block after a Protect or Unprotect or Lock command has been issued or after $\overline{WPF}$ has changed its logic value.
4. A $\overline{WPF}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

Table 15. Instructions (1,2)

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.
RD (4)	Read/Reset Memory Array	1+	**Addr.** (3)	X	Read Memory Array until a new write cycle is initiated.				
			Data	F0h					
		3+	**Addr.**	555h	2AAh	555h	Read Memory Array until a new write cycle is initiated.		
			Data	AAh	55h	F0h			
RCFI	CFI Query	1+	**Addr.**	55h	Read CFI data until a new write cycle is initiated.				
			Data	98h					
AS (4)	Auto Select	3+	**Addr.**	555h	2AAh	555h	Read electronic Signature or Block Protection or Configuration Register Status until a new cycle is initiated.		
			Data	AAh	55h	90h			
CR	Configuration Register Write	4	**Addr.**	555h	2AAh	555h	Configura-tion Data		
			Data	AAh	55h	60h	03h		
PG	Program	4	**Addr.**	555h	2AAh	555h	Program Address	Read Data Polling or Toggle Bit until Program completes.	
			Data	AAh	55h	A0h	Program Data		
DPG	Double Word Program	5	**Addr.**	555h	2AAh	555h	Program Address 1	Program Address 2	Note 6, 7
			Data	AAh	55h	40h	Program Data 1	Program Data 2	
EBY	Enter Bypass Mode	3	**Addr.**	555h	2AAh	555h			
			Data	AAh	55h	20h			

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.
XBY	Exit Bypass Mode	2	**Addr.**	X	X				
			Data	90h	00h				
PGBY	Program in Bypass Mode	2	**Addr.**	X	Program Address	Read Data Polling or Toggle Bit until Program completes.			
			Data	A0h	Program Data				
DPGBY	Double Word Program in Bypass Mode	3	**Addr.**	X	Program Address 1	Program Address 2	Note 6, 7		
			Data	40h	Program Data 1	Program Data 2			
BP	Block Protect	4	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	01h		
BU	Block Unprotect	1	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	D0h		
BL	Block Lock	4	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	2Fh		
BE	Block Erase	6+	**Addr.**	555h	2AAh	555h	555h	2AAh	Block Address
			Data	AAh	55h	80h	AAh	55h	30h
BKE	Bank Erase	6	**Addr.**	555h	2AAh	555h	555h	2AAh	Bank Address
			Data	AAh	55h	80h	AAh	55h	10h
ES	Erase Suspend	1	**Addr.** (3)	X	Read until Toggle stops, then read all the data needed from any Blocks not being erased then Resume Erase.				
			Data	B0h					
ER	Erase Resume	1	**Addr.**	Bank Address	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time				
			Data	30h					

Note: 1. Commands not interpreted in this table will default to read array mode.
2. For Coded cycles address inputs A11-A20 are don't care.
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.
6. Program Address 1 and Program Address 2 must be consecutive addresses differing only for address bit A0.
7. High voltage on V_{PPF} (11.4V to 12.6V) is required for the proper execution of the Double Word Program instruction.

STATUS REGISTER BITS

P/E.C. status is indicated during execution by Data Polling on DQ7, detection of Toggle on DQ6 and DQ2, or Error on DQ5 bits. Any read attempt within the Bank being modified and during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits DQ2, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked (see Tables 17 and 16). Read attempts within the bank not being modified will output array data.

Data Polling Bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. In case of a double word program operation, the complement is done on DQ7 of the last word written to the command interface, i.e. the data written in the fifth cycle. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{WF}$ pulse for programming or after the sixth $\overline{WF}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. See Figure 25 for the Data Polling flowchart and Figure 12 for the Data Polling waveforms. DQ7 will also flag the Erase Suspend mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor DQ7 in the Erase Suspend mode an address within a block being erased must be provided. For a Read Operation in Suspend mode, DQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During Program operation in Erase Suspend Mode, DQ7 will have the same behavior as in the normal program execution outside of the suspend mode.

Toggle Bit (DQ6). When Programming or Erasing operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{GF}$, or $\overline{EF}$ when $\overline{GF}$ is at V_{IL}. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit DQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{WF}$ pulse for programming or after the sixth $\overline{WF}$ pulse for Erase. DQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend block. When erase is suspended DQ6 will toggle during programming operations in a block different from the block in Erase Suspend. Either $\overline{EF}$ or $\overline{GF}$ toggling will cause DQ6 to toggle. See Figure 25 for Toggle Bit flowchart and Figure 13 for Toggle Bit waveforms.

Toggle Bit (DQ2). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. During Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will output data. DQ2 will be set to '1' during program operation and to '0' in Erase operation. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Error Bit (DQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming or block erase, that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occurred or to which the programmed data belongs, must be discarded. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0'.

Erase Timer Bit (DQ3). This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, DQ3 returns to '1', in the range of 80µs to 120µs.

Table 16. Polling and Toggle Bits

Mode	DQ7	DQ6	DQ2
Program	$\overline{DQ7}$	Toggle	1
Erase	0	Toggle	N/A
Erase Suspend Read (in Erase Suspend block)	1	1	Toggle
Erase Suspend Read (outside Erase Suspend block)	DQ7	DQ6	DQ2
Erase Suspend Program	$\overline{DQ7}$	Toggle	1

Table 17. Status Register Bits (1)

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend.	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend.	
		$\overline{DQ}$	Program On-going (2)	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES)
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C:
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase Suspend read in the Erase Suspended Block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block.
		1	Program on-going or Erase Complete.	
		DQ	Erase Suspend read on non Erase Suspend block.	
1	Reserved			
0	Reserved			

Note: 1. Logic level '1' is High, '0' is Low. $\underline{-0-1}$-0-0-0-1-1-1-0- represent bit value in successive Read operations.
2. In case of double word program $\overline{DQ7}$ refers to the last word input.

POWER CONSUMPTION

Power Down

The memory provides Reset/Power Down control input RPF. The Power Down function can be activated only if the relevant Configuration Register bit is set to '1'. In this case, when the RPF signal is pulled at V_{SS} the supply current drops to typically I_{DDD} (see Table 24), the memory is deselected and the outputs are in high impedance.If RPF is pulled to V_{SS} during a Program or Erase operation, this operation is aborted in t_{PLQ7V} and the memory content is no longer valid (see Reset/ Power Down input description).

Power Up

The memory Command Interface is reset on Power Up to Read Array. Either EF or WF must be tied to V_{IH} during Power Up to allow maximum security and the possibility to write a command on the first rising edge of WF.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{CCF} rails decoupled with a 0.1µF capacitor close to the V_{CCF} and V_{SS} pins. The PCB trace widths should be sufficient to carry the required V_{CCF} program and erase currents.

COMMON FLASH INTERFACE (CFI)

The Common Flash Interface (CFI) specification is a JEDEC approved, standardised data structure that can be read from the Flash memory device. CFI allows a system software to query the flash device to determine various electrical and timing parameters, density information and functions supported by the device. CFI allows the system to easily interface to the Flash memory, to learn about its features and parameters, enabling the software to configure itself when necessary.

Tables 18, 19, 20, and 21 show the address used to retrieve each data.

The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. Tables 18, 19, 20, and 21 show the addresses used to retrieve each data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 81h. This area can be accessed only in read mode and there are no ways of changing the code after it has been written by ST. Write a read instruction to return to Read mode. Refer to the CFI Query instruction to understand how the M36DR232 enters the CFI Query mode.

Table 18. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables 19, 20 and 21. Query data are always presented on the lowest order data outputs.

Table 19. CFI Query Identification String

Offset	Data	Description
00h	0020h	Manufacturer Code
01h	00A0h - top 00A1h - bottom	Device Code
02h-0Fh	reserved	Reserved
10h	0051h	Query Unique ASCII String "QRY"
11h	0052h	Query Unique ASCII String "QRY"
12h	0059h	Query Unique ASCII String "QRY"
13h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm
14h	0000h	
15h	offset = P = 0040h	Address for Primary Algorithm extended Query table
16h	0000h	
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)
18h	0000h	
19h	value = A = 0000h	Address for Alternate Algorithm extended Query table note: 0000h means none exists
1Ah	0000h	

Note: 1. Query data are always presented on the lowest - order data outputs (DQ7-DQ0) only. DQ8-DQ15 are '0'.

Table 20. CFI Query System Interface Information

Offset	Data	Description
1Bh	0017h	V_{CCF} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Ch	0022h	V_{CCF} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Dh	0000h	V_{PPF} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PP} pin is present
1Eh	00C0h	V_{PPF} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PP} pin is present
1Fh	0004h	Typical timeout per single byte/word program (multi-byte program count = 1), 2^n µs (if supported; 0000h = not supported)
20h	0000h	Typical timeout for maximum-size multi-byte program or page write, 2^n µs (if supported; 0000h = not supported)
21h	000Ah	Typical timeout per individual block erase, 2^n ms (if supported; 0000h = not supported)
22h	0000h	Typical timeout for full chip erase, 2^n ms (if supported; 0000h = not supported)
23h	0004h	Maximum timeout for byte/word program, 2^n times typical (offset 1Fh) (0000h = not supported)
24h	0000h	Maximum timeout for multi-byte program or page write, 2^n times typical (offset 20h) (0000h = not supported)
25h	0004h	Maximum timeout per individual block erase, 2^n times typical (offset 21h) (0000h = not supported)
26h	0000h	Maximum timeout for chip erase, 2^n times typical (offset 22h) (0000h = not supported)

Table 21. Device Geometry Definition

Offset Word Mode	Data	Description
27h	0016h	Device Size = 2^n in number of bytes
28h	0001h	Flash Device Interface Code description: Asynchronous x16
29h	0000h	
2Ah	0000h	Maximum number of bytes in multi-byte program or page = 2^n
2Bh	0000h	
2Ch	0002h	Number of Erase Block Regions within device bit 7 to 0 = x = number of Erase Block Regions Note:1. x = 0 means no erase blocking, i.e. the device erases at once in "bulk." 2. x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128KB device (1Mb) having blocking of 16KB, 8KB, four 2KB, two 16KB, and one 64KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions. 3. By definition, symmetrically block devices have only one blocking region.
M36DR232A	M36DR232A	Erase Block Region Information bit 31 to 16 = z, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128 byte block size. e.g. for 64KB block size, z = 0100h = 256 => 256 * 256 = 64K bit 15 to 0 = y, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region: e.g. y = D15-D0 = FFFFh => y+1 = 64K blocks [maximum number] y = 0 means no blocking (# blocks = y+1 = "1 block") Note: y = 0 value must be used with number of block regions of one as indicated by (x) = 0
2Dh	003Eh	
2Eh	0000h	
2Fh	0000h	
30h	0001h	
31h	0007h	
32h	0000h	
33h	0020h	
34h	0000h	
M36DR232B	M36DR232B	
2Dh	0007h	
2Eh	0000h	
2Fh	0020h	
30h	0000h	
31h	003Eh	
32h	0000h	
33h	0000h	
34h	0001h	

SRAM COMPONENT

Device Operations

The following operations can be performed using the appropriate bus cycles: Read Array, Write Array, Output Disable, Power Down (see Table 3).

Read. Read operations are used to output the contents of the SRAM Array. The SRAM is in Read mode whenever Write Enable (WS) is at V_{IH} with Output Enable (GS) at V_{IL}, and both Chip Enables (E1S and E2S) and UBS, LBS combinations are asserted.

Valid data will be available at the output pins within t_{AVQV} after the last stable address, providing GS is Low, E1S is Low and E2S is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV} (see Table 31, Figures 16 and 17).

Write. Write operations are used to write data in the SRAM. The SRAM is in Write mode whenever the WS and E1S pins are at V_{IL}, with E2S at V_{IH}. Either the Chip Enable inputs (E1S and E2S) or the Write Enable input (WS) must be de-asserted during address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with WS at V_{IL}. A Write begins at the latest transition among E1S going to V_{IL}, E2S going to V_{IH} and WS going to V_{IL}. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge. The Write cycle can be terminated by the rising edge of E1S, the rising edge of WS or the falling edge of E2S, whichever occurs first. If the Output is enabled (E1S=V_{IL}, E2S=V_{IH} and GS=V_{IL}), then WS will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of E1S or for t_{DVE2L} before the falling edge of E2S, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HAX} or t_{E2LAX} (see Table 32, Figure 19, 21, 23).

Standby/Power-Down. The SRAM chip has a Chip Enable power-down feature which invokes an automatic standby mode (see Table 31, Figure 18) whenever either Chip Enable is de-asserted (E1S=V_{IH} or E2S=V_{IL}).

Data Retention

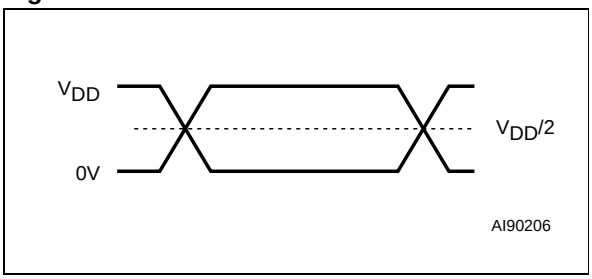
The SRAM data retention performances as V_{CCS} go down to V_{DR} are described in Table 33 and Figure 23, 24. In E1S controlled data retention mode, minimum standby current mode is entered when E1S ≥ V_{CCS} – 0.2V and E2S ≤ 0.2V or E2S ≥ V_{CCS} – 0.2V. In E2S controlled data retention mode, minimum standby current mode is entered when E2S ≤ 0.2V.

Output Disable. The data outputs are high impedance when the Output Enable (GS) is at V_{IH} with Write Enable (WS) at V_{IH}.

Table 22. AC Measurement Conditions

Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V_{DD}
Input and Output Timing Ref. Voltages	$V_{DD}/2$

Figure 5. AC Measurement Waveform



Note: V_{DD} means $V_{DDF} = V_{DDS}$

Figure 6. AC Measurement Load Circuit

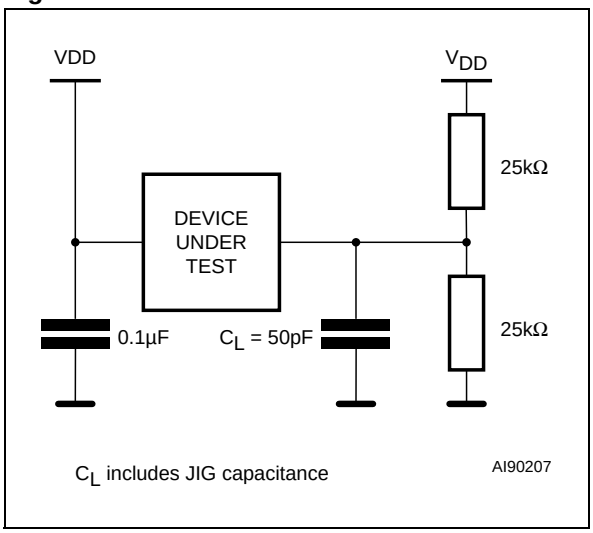


Table 23. Device Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 24. DC Characteristics
(T_A = –40 to 85°C; V_{DDF} = V_{DDS} = 1.65V to 2.2V)

Symbol	Parameter	Device	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	Flash & SRAM	$0V \le V_{IN} \le V_{DD}$			±2	µA
I_{LO}	Output Leakage Current	Flash & SRAM	$0V \le V_{OUT} \le V_{DD}$			±10	µA
I_{DDS}	V_{DD} Standby Current	Flash	$\overline{EF} = V_{DDF} \pm 0.2V$ $V_{DDF} = V_{DD}$ max		15	50	µA
		SRAM	$\overline{E1S} \ge V_{DDS} - 0.2V$, $E2S \le V_{DDS} - 0.2V$, $V_{IN} \ge V_{DDS} - 0.2V$ or $V_{IN} \le V_{DDS} - 0.2V$, f=0		10	50	µA
I_{DDD}	Supply Current (Reset)	Flash	$\overline{RPF} = V_{SSF} \pm 0.2V$		2	10	µA
I_{DD}	Supply Current	SRAM	I_{IO} = 0 mA, $\overline{E1S} = V_{IL}$, $E2S = \overline{WS} = V_{IH}$, $V_{IN} = V_{IL}$ or V_{IH}, $V_{DDS} = V_{DD}$ max, cycle time = 1µs		1	2	mA
			I_{IO} = 0 mA, $\overline{E1S} = V_{IL}$, $E2S = \overline{WS} = V_{IH}$, $V_{IN} = V_{IL}$ or V_{IH}, $V_{DDS} = V_{DD}$ max, min cycle time		3	7	mA
I_{DDR}	Supply Current (Read)	Flash	$\overline{EF} = V_{IL}$, $\overline{GF} = V_{IH}$, f = 5 MHz		10	20	mA
I_{DDW}	Supply Current (Program)	Flash	Program in progress		10	20	mA
I_{DDWD}	Supply Current (Dual Bank)	Flash	Program/Erase in progress in one bank Read in the other bank		20	40	mA
I_{DDE}	Supply Current (Erase)	Flash	Erase in progress		10	20	mA
I_{DDES}(1)	Supply Current (Erase Suspend)	Flash	Erase Suspend in progress			50	µA
I_{DDWS}(1)	Supply Current (Program Suspend)	Flash	Program Suspend in progress			50	µA
I_{PPS}	Program Current (Standby)	Flash	$V_{PPF} \le V_{DDS}$		0.2	5	µA
			V_{PPF} = 12V ± 0.6V		100	400	µA
I_{PPR}	Program Current (Read)	Flash	$V_{PPF} \le V_{DDS}$		0.2	5	µA
			V_{PPF} = 12V ± 0.6V		100	400	µA
I_{PPW}	Program Current (Program)	Flash	V_{PPF} = 12V ± 0.6V Program in progress		5	10	mA
I_{PPE}	Program Current (Erase)	Flash	V_{PPF} = 12V ± 0.6V Program in progress		5	10	mA
V_{IL}	Input Low Voltage	Flash & SRAM		–0.5		0.4	V
V_{IH}	Input High Voltage	Flash & SRAM		1.4		V_{DD} +0.2	V
V_{OL}	Output Low Voltage	Flash & SRAM	$V_{DDF} = V_{DDS} = V_{DD}$ min I_{OL} = 100µA			0.2	V
V_{OH}	Output High Voltage	Flash & SRAM	$V_{DDF} = V_{DDS} = V_{DD}$ min I_{OH} = –100µA	V_{DD} –0.1			V

Symbol	Parameter	Device	Test Condition	Min	Typ	Max	Unit
V_{PPL}	Program Voltage (Program or Erase operations)	Flash		1.65		2.2	V
V_{PPH}	Program Voltage (Program or Erase operations)	Flash		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)	Flash				1	V

Note: 1. I_{DDES} and I_{DDWS} are specified with device deselected. If device is read while in erase suspend, current draw is sum of I_{DDES} and I_{DDR}. If the device is read while in program suspend, current draw is the sum of I_{DDWS} and I_{DDR}.

Table 25. Flash Read AC Characteristics
(TA = –40 to 85°C; V_{DDF} = 1.65V to 2.2V)

Symbol	Alt	Parameter	Test Condition	Flash				Unit
				100		120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}	100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}		100		120	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}		35		45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{EF}$ = V_{IL}, $\overline{GF}$ = V_{IL}	0		0		ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{GF}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{GF}$ = V_{IL}		25		35	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{GF}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{GF}$ = V_{IL}	0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{EF}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{EF}$ = V_{IL}		25		35	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{EF}$ = V_{IL}		25		35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{EF}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{GF}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EF}$ without increasing t_{ELQV}

Figure 7. Flash Read AC Waveforms

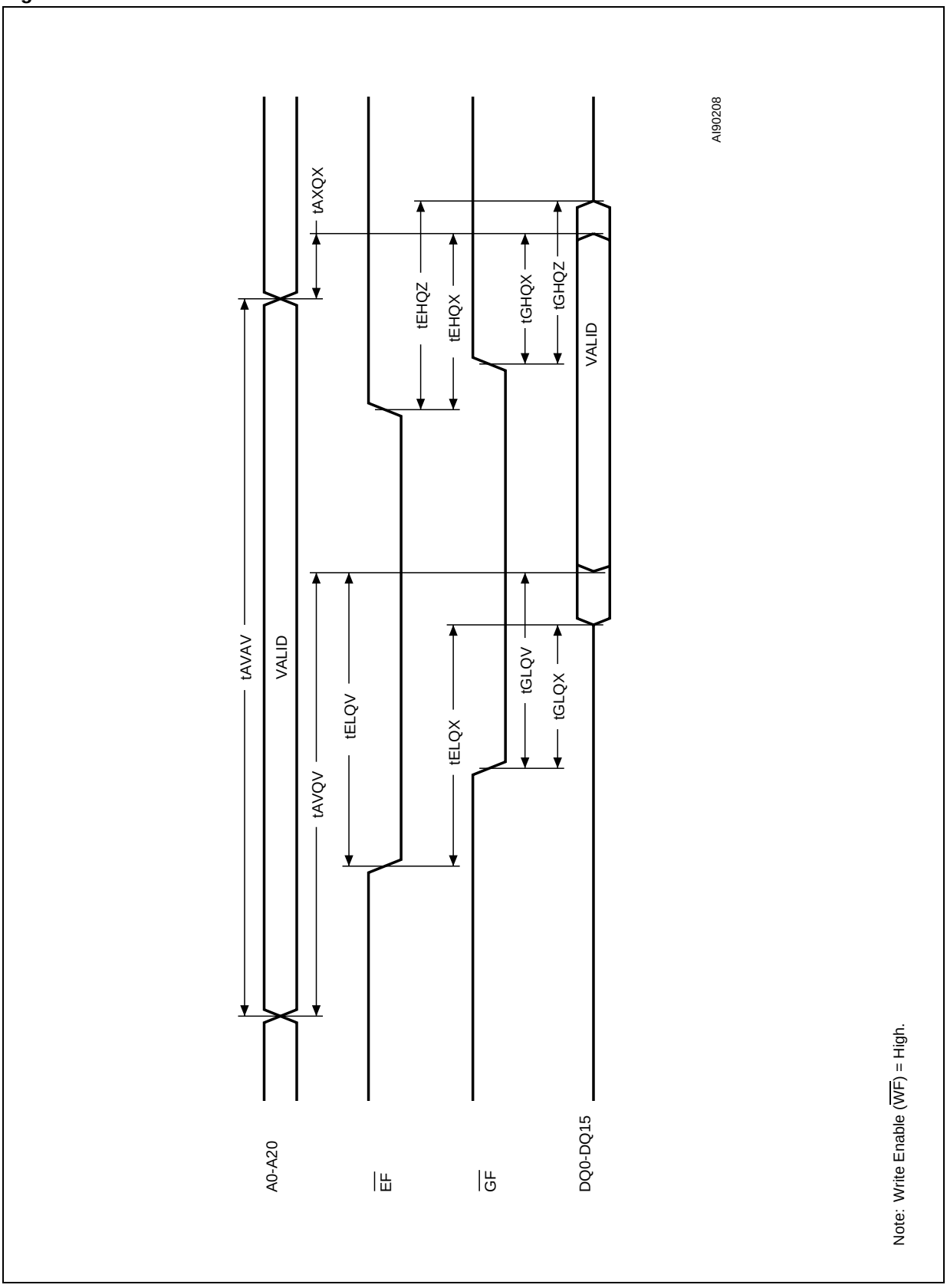


Figure 8. Flash Page Read AC Waveforms

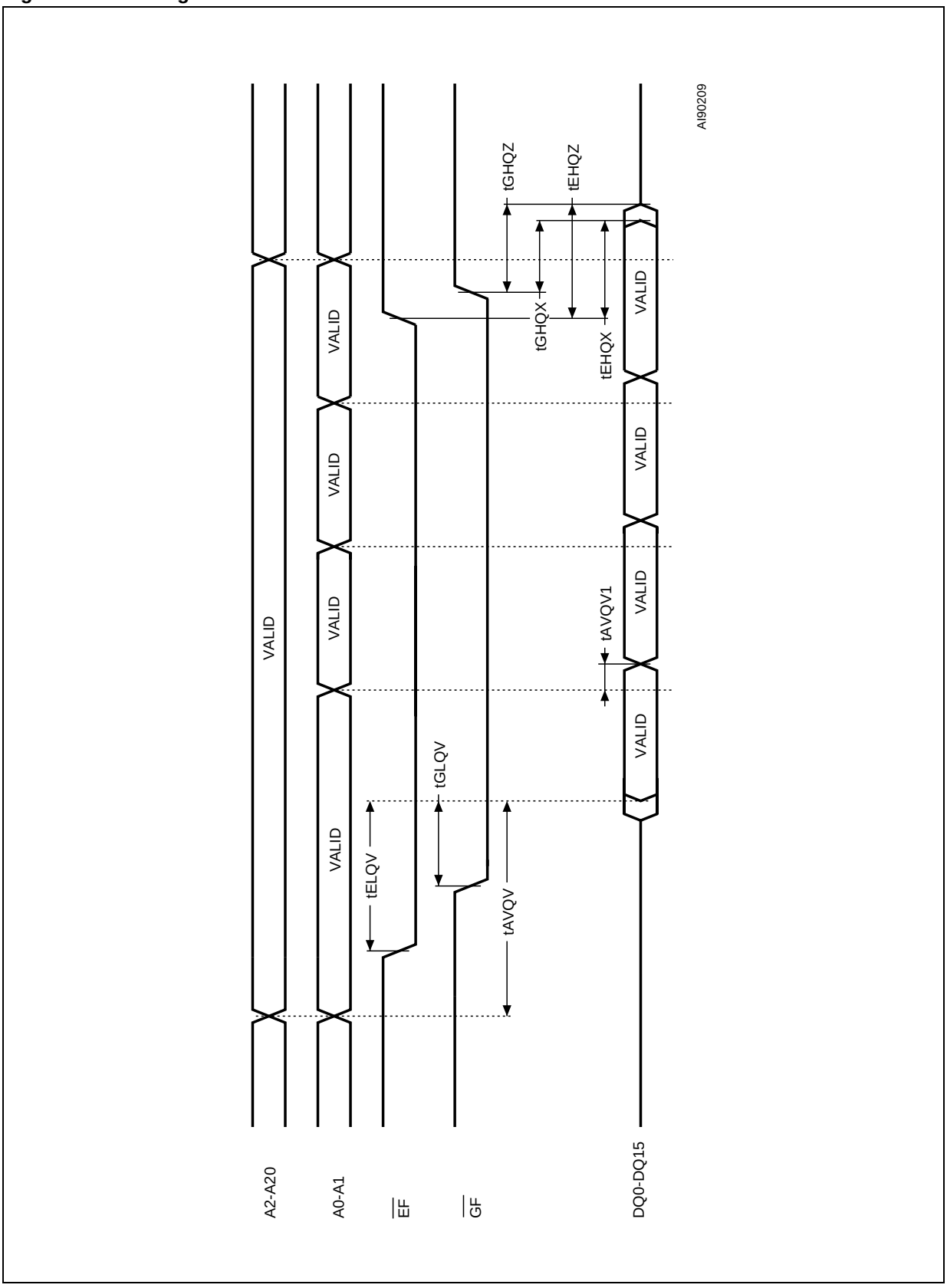
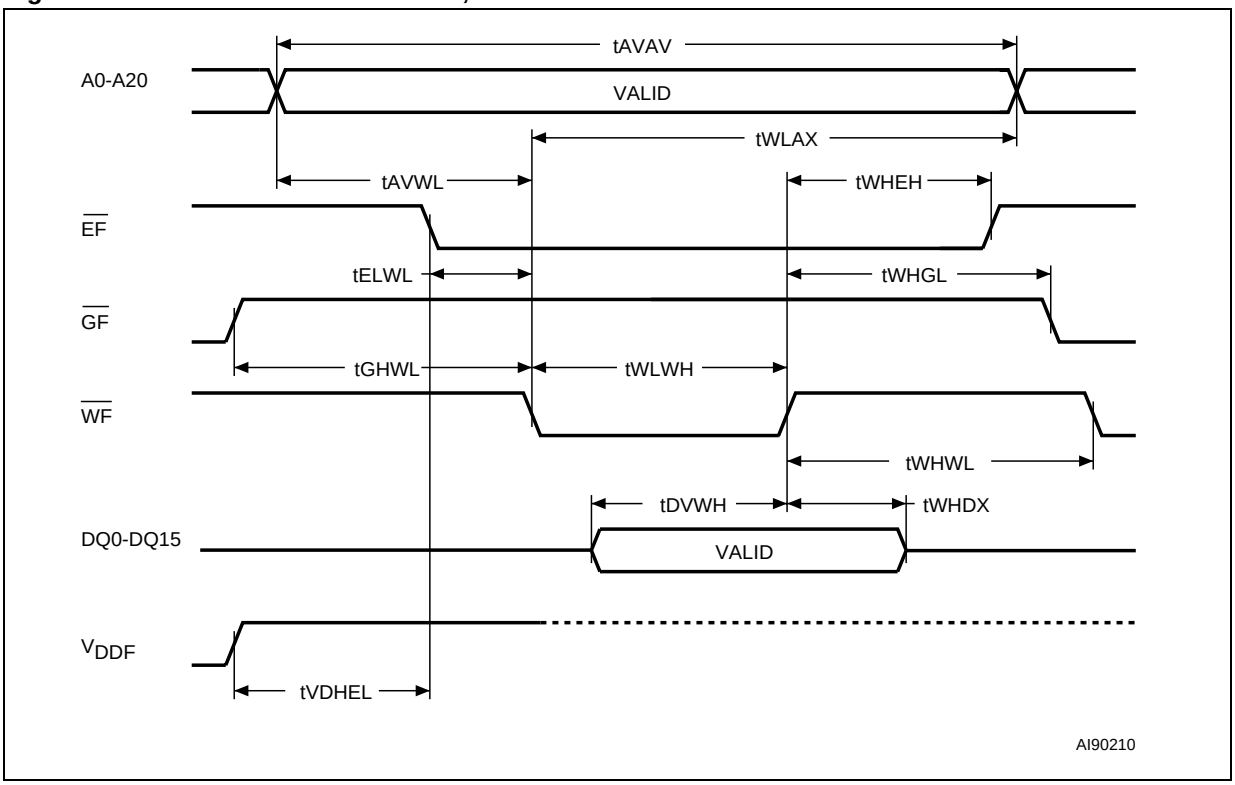


Table 26. Flash Write AC Characteristics, Write Enable Controlled
(T_A = –40 to 85 °C; V_{DDF} = 1.65V to 2.2V

Symbol	Alt	Parameter	Flash				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete During Program/Erase		15		15	µs
t_{VDHEL}	t_{VCS}	V_{CCF} High to Chip Enable Low	50		50		µs
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	30		30		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns

Figure 9. Flash Write AC Waveforms, $\overline{WF}$ Controlled

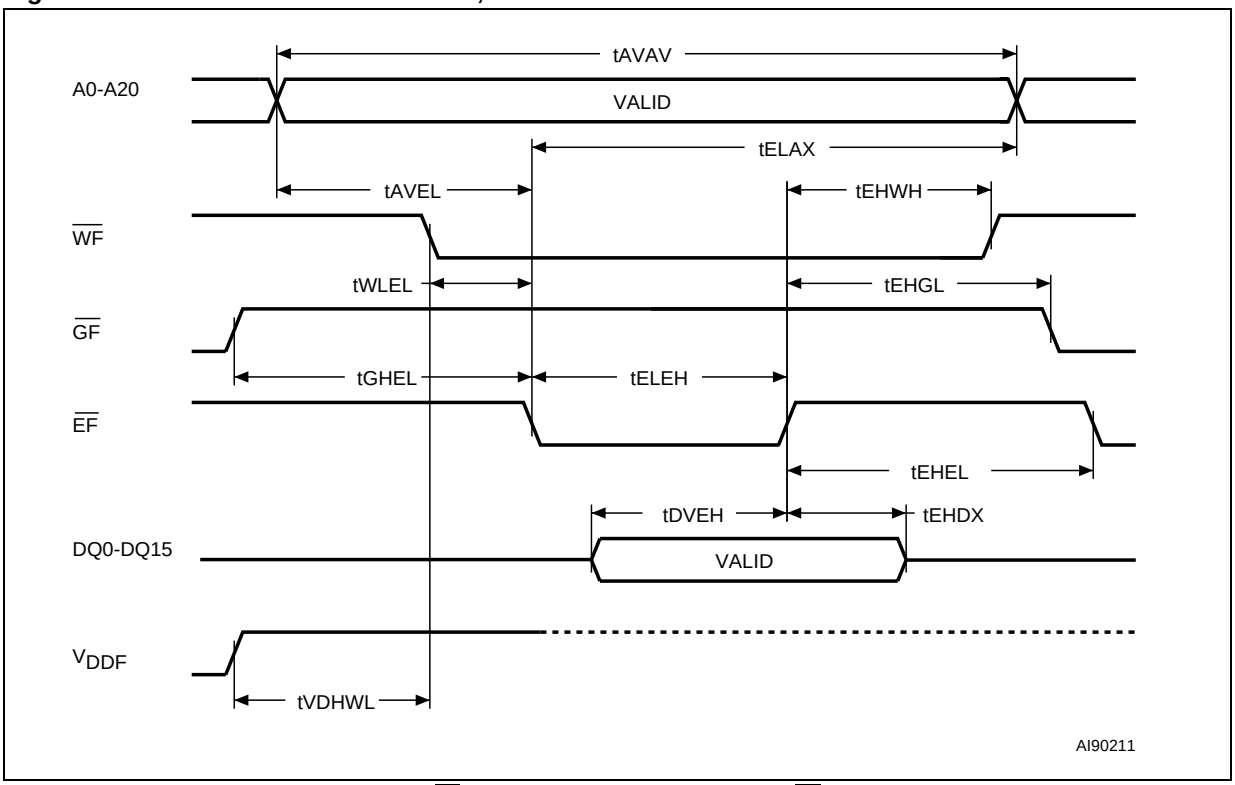


Note: 1. Address are latched on the falling edge of $\overline{WF}$, Data is latched on the rising edge of $\overline{WF}$.

Table 27. Flash Write AC Characteristics, Chip Enable Controlled
(T_A = –40 to 85 °C; V_{DDF} = 1.65V to 2.2V)

Symbol	Alt	Parameter	Flash				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	30		30		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete During Program/Erase		15		15	µs
t_{VDHWL}	t_{VCS}	V_{CCF} High to Write Enable Low	50		50		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns

Figure 10. Flash Write AC Waveforms, $\overline{EF}$ Controlled



Note: Address are latched on the falling edge of $\overline{EF}$, Data is latched on the rising edge of $\overline{EF}$.

Table 28. Flash Read and Write AC Characteristics, $\overline{RPF}$ Related
(T_A = –40 to 85°C; V_{DDF} = 1.65V to 2.2V)

Symbol	Alt	Parameter	Test Condition	Flash				Unit
				100		120		
				Min	Max	Min	Max	
t_{PHQ7V1}		$\overline{RPF}$ High to Data Valid (Read Mode)			150		150	ns
t_{PHQ7V2}		$\overline{RPF}$ High to Data Valid (Power Down enabled)			50		50	µs
t_{PLPH}	t_{RP}	$\overline{RPF}$ Pulse Width		100		100		ns
t_{PLQ7V}		$\overline{RPF}$ Low to Reset Complete During Program/Erase			15		15	µs

Figure 11. Flash Read and Write AC Waveforms, $\overline{RPF}$ Related

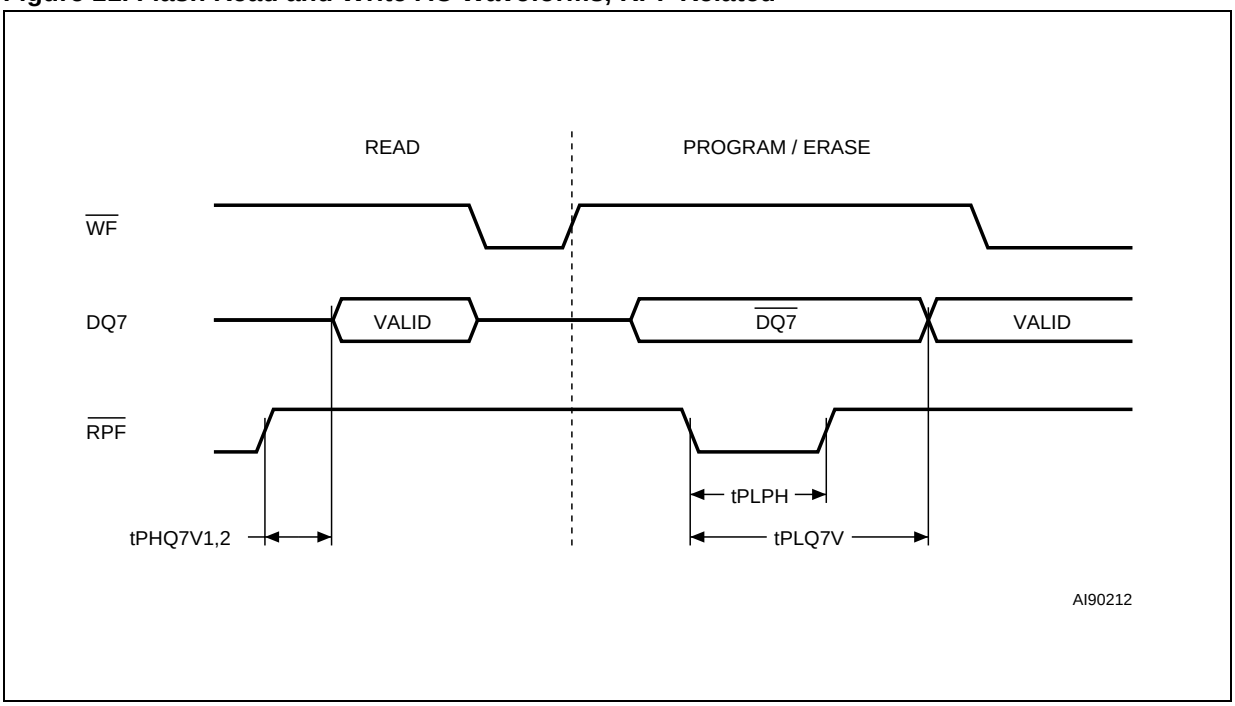


Table 29. Flash Program, Erase Times and Program, Erase Endurance Cycles
(T_A = –40 to 85°C; V_{DDF} = 1.65V to 2.2V, V_{PPF} = V_{DDF} unless otherwise specified)

Parameter	Min	Max (1)	Typ	Typical after 100k W/E Cycles	Unit
Parameter Block (4 KWord) Erase (Preprogrammed)		2.5	0.15	0.4	s
Main Block (32 KWord) Erase (Preprogrammed)		10	1	3	s
Bank Erase (Preprogrammed, Bank A)			2	6	s
Bank Erase (Preprogrammed, Bank B)			10	30	s
Chip Program (2)			20	25	s
Chip Program (DPG, V_{PP} = 12V) (2)			10		s
Word Program		200	10	10	µs
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. Max values refer to the maximum time allowed by the internal algorithm before error bit is set. Worst case conditions program or erase should perform significantly better.
2. Excludes the time needed to execute the sequence for program instruction.

Table 30. Flash Data Polling and Toggle Bits AC Characteristics (1)
(T_A = –40 to 85 °C; V_{DDF} = 1.65V to 2.2V)

Symbol	Parameter	Flash		Unit
		Min	Max	
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, $\overline{EF}$ Controlled)	10	200	µs
	Chip Enable High to DQ7 Valid (Block Erase, $\overline{EF}$ Controlled)	1	10	s
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	200	µs
	Chip Enable High to Output Valid (Block Erase)	1	10	s
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		0	ns
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, $\overline{WF}$ Controlled)	10	200	µs
	Write Enable High to DQ7 Valid (Block Erase, $\overline{WF}$ Controlled)	1	10	s
t_{WHQV}	Write Enable High to Output Valid (Program)	10	200	µs
	Write Enable High to Output Valid (Block Erase)	1	10	s

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 12. Flash Data Polling DQ7 AC Waveforms

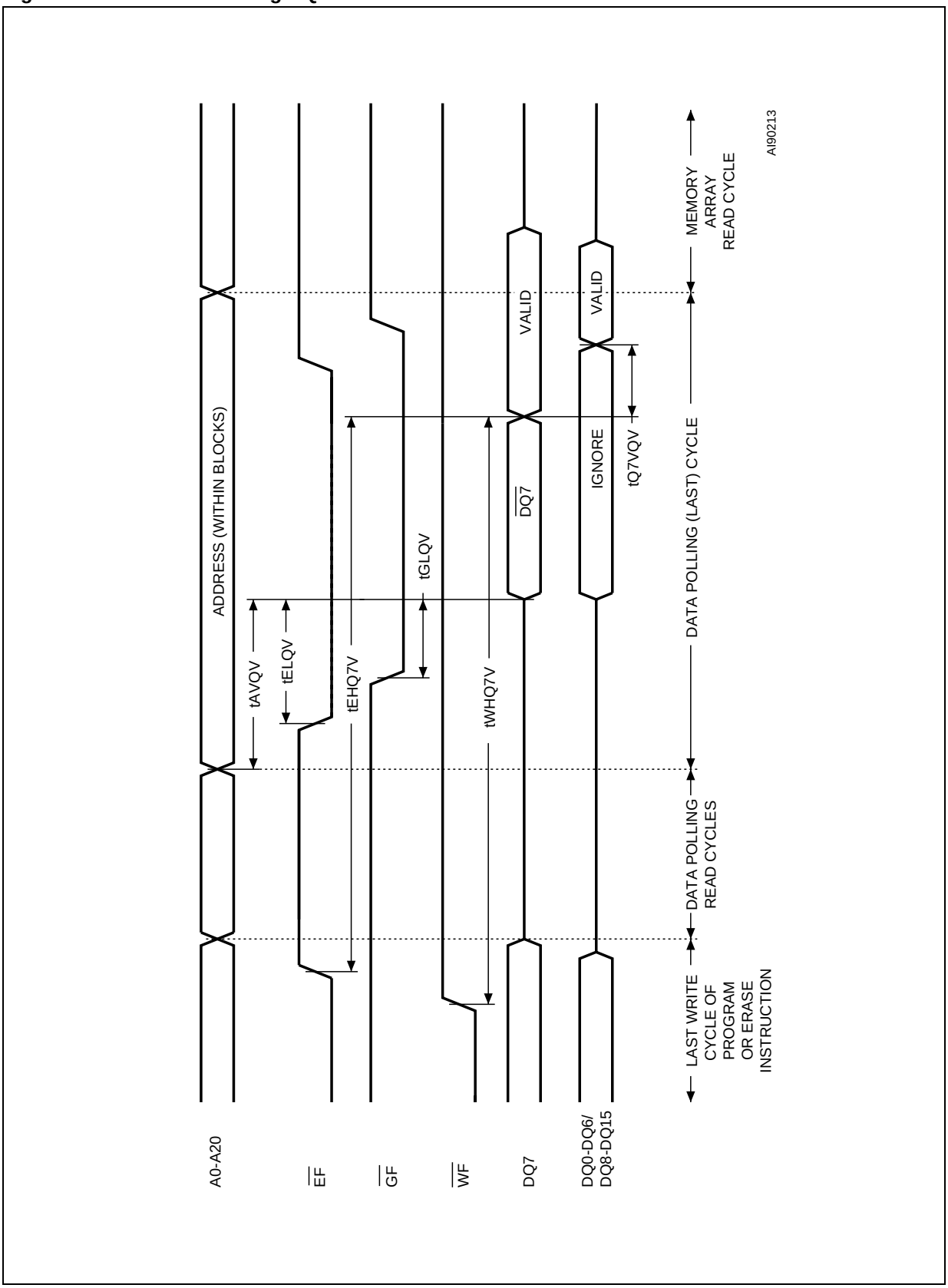


Figure 13. Flash Data Toggle DQ6, DQ2 AC Waveforms

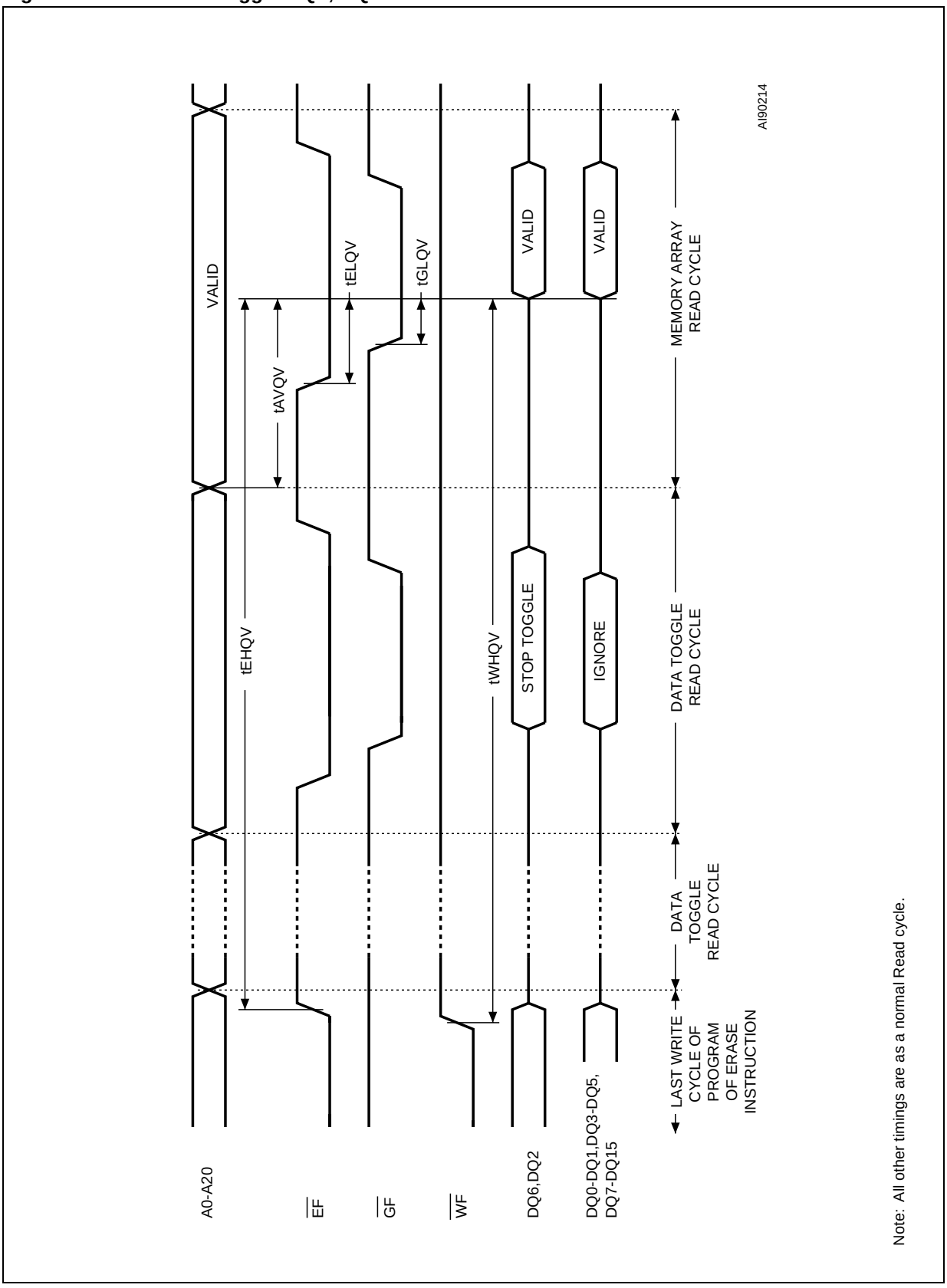


Figure 14. Flash Data Polling Flowchart

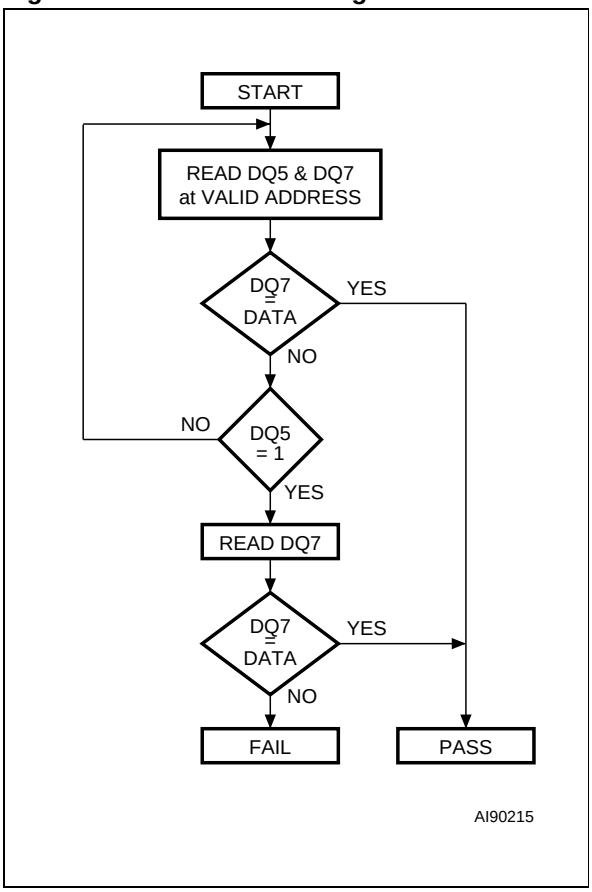


Figure 15. Flash Data Toggle Flowchart

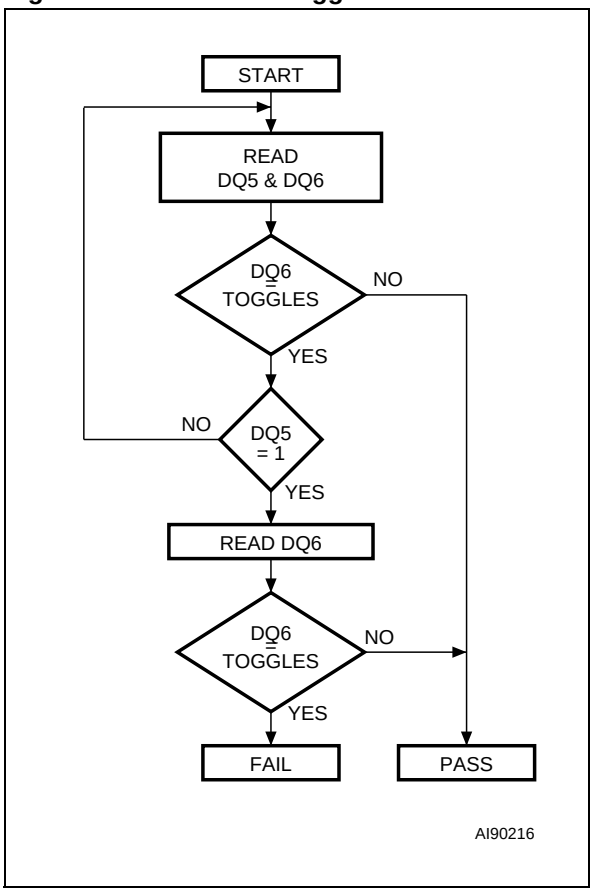
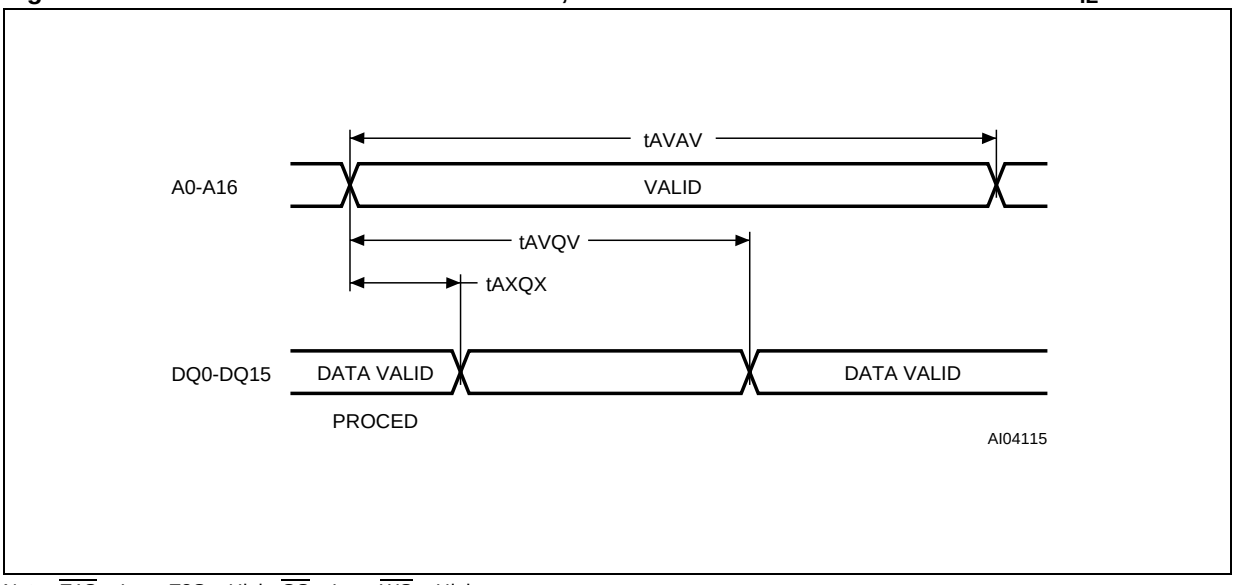


Table 31. SRAM Read AC Characteristics
(T_A = –40 to 85°C; V_{DDS} = 1.65V to 2.2V)

Symbol	Alt	Parameter	SRAM		Unit
			Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	70		ns
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	10		ns
t_{BHQZ}	t_{BHZ}	$\overline{UBS}$, $\overline{LBS}$ Disable to Hi-Z Output		25	ns
t_{BLQV}	t_{BA}	$\overline{UBS}$, $\overline{LBS}$ Access Time		70	ns
t_{BLQX}	t_{BLZ}	$\overline{UBS}$, $\overline{LBS}$ Enable to Low-Z Output	5		ns
t_{E1HQZ}	t_{HZ1}	Chip Enable 1 High to Output Hi-Z		25	ns
t_{E1LQV}	t_{CO1}	Chip Enable 1 Low to Output Valid		70	ns
t_{E1LQX}	t_{LZ1}	Chip Enable 1 Low to Output Transition	10		ns
t_{E2HQV}	t_{CO2}	Chip Enable 2 High to Output Valid		70	ns
t_{E2HQX}	t_{LZ2}	Chip Enable 2 High to Output Transition	10		ns
t_{E2LQZ}	t_{HZ2}	Chip Enable 2 Low to Output Hi-Z		25	ns
t_{GHQZ}	t_{OHZ}	Output Enable High to Output Hi-Z		25	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35	ns
t_{GLQX}	t_{OLZ}	Output Enable Low to Output Transition	5		ns
t_{PD} (1)		Chip Enable 1 High or Chip Enable 2 Low to Power Down		70	ns
t_{PU} (1)		Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns

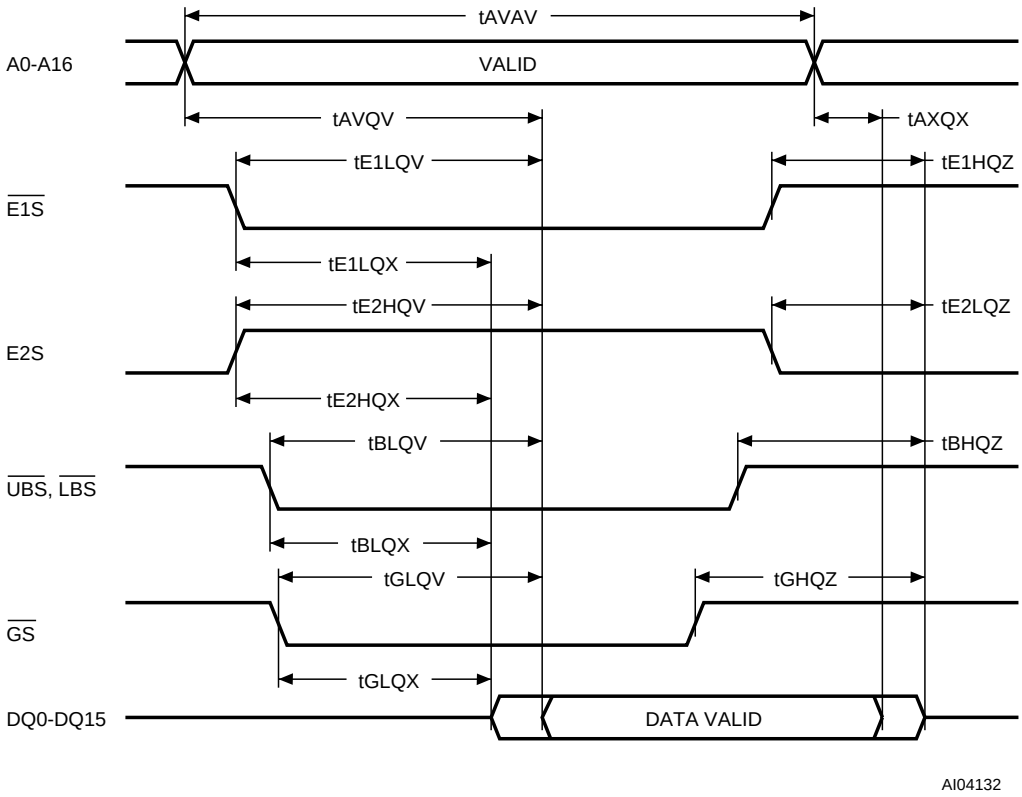
Note: 1. Sampled only. Not 100% tested.

Figure 16. SRAM Read Mode AC Waveforms, Address Controlled with $\overline{UBS}$ = $\overline{LBS}$ = V_{IL}



Note: $\overline{E1S}$ = Low, E2S = High, $\overline{GS}$ = Low, $\overline{WS}$ = High.

Figure 17. SRAM Read AC Waveforms, $\overline{E1S}$, E2S or $\overline{GS}$ Controlled



Note: Write Enable ($\overline{WS}$) = High.

Figure 18. SRAM Standby AC Waveforms

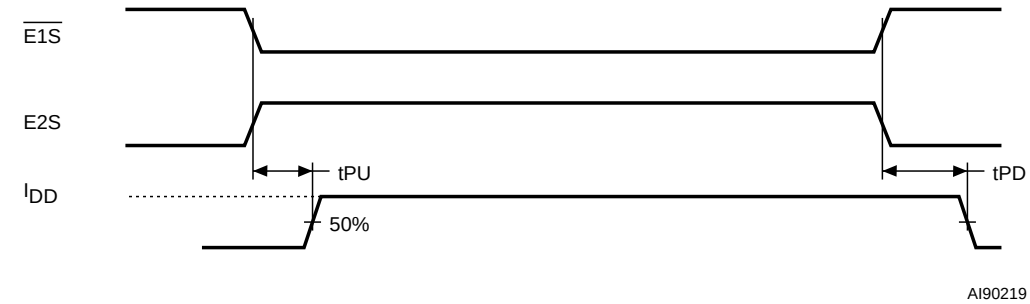
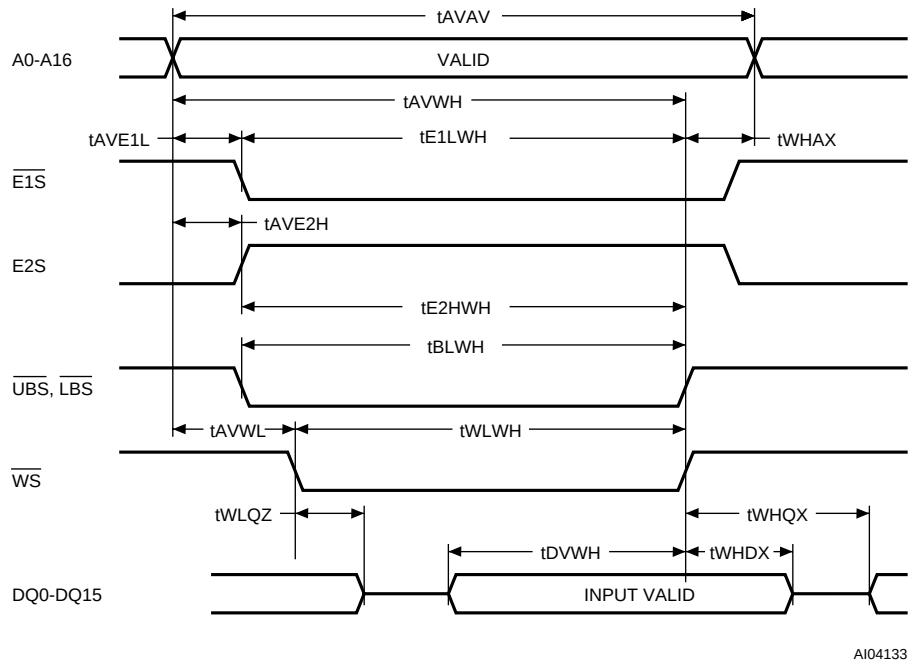


Table 32. SRAM Write AC Characteristics
(T_A = –40 to 85°C; V_{DDS} = 1.65V to 2.2V)

Symbol	Alt	Parameter	SRAM		Unit
			Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		ns
t_{AVE1L}	t_{AS} (1)	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	t_{AS} (1)	Address Valid to Chip Enable 2 High	0		ns
t_{AVWH}	t_{AW}	Address Valid to Write Enable High	60		ns
t_{AVWL}	t_{AS} (1)	Address Valid to Write Enable Low	0		ns
t_{BLWH}	t_{BW}	$\overline{UBS}$, $\overline{LBS}$ Valid to End of Write	60		ns
t_{DVE1H}	t_{DW}	Input Valid to Chip Enable 1 High	40		ns
t_{DVE2L}	t_{DW}	Input Valid to Chip Enable 2 Low	40		ns
t_{DVWH}	t_{DW}	Input Valid to Write Enable High	40		ns
t_{E1HAX}	t_{WR} (2)	Chip Enable 1 High to Address Transition	0		ns
t_{E1LWH}, t_{E2HWH}	t_{CW} (3)	Chip Select to End of Write	60		ns
t_{E2LAX}	t_{WR} (2)	Chip Enable 2 Low to Address Transition	0		ns
t_{GHQZ}	t_{GHZ}	Output Enable Higt to Output Hi-Z	0	25	ns
t_{WHAX}	t_{WR} (2)	Write Enable High to Address Transition	0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		ns
t_{WHQX}	t_{OW}	Write Enable High to Output Transition	5		ns
t_{WLQZ}	t_{WHZ}	Write Enable Low to Output Hi-Z	0	25	ns
t_{WLWH}	t_{WP} (4)	Write Enable Pulse Width	50		ns

Note: 1. t_{AS} is measured from the address valid to the beginning of write.
2. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{E1S}$ or $\overline{WS}$ going high.
3. t_{CW} is measured from $\overline{E1S}$ going low end of write.
4. A Write occurs during the overlap (t_{WP}) of low $\overline{E1S}$ and low $\overline{WS}$. A write begins when $\overline{E1S}$ goes low and $\overline{WS}$ goes low with asserting $\overline{UBS}$ or $\overline{LBS}$ for single byte operation or simultaneously asserting $\overline{UBS}$ and $\overline{LBS}$ for double byte operation. A write ends at the earliest transition when $\overline{E1S}$ goes high and $\overline{WS}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.

Figure 19. SRAM Write AC Waveforms, $\overline{WS}$ Controlled with $\overline{GS}$ Low



Note: Output Enable ($\overline{GS}$) = Low.

Figure 20. SRAM Write AC Waveforms, $\overline{WS}$ Controlled with $\overline{GS}$ High

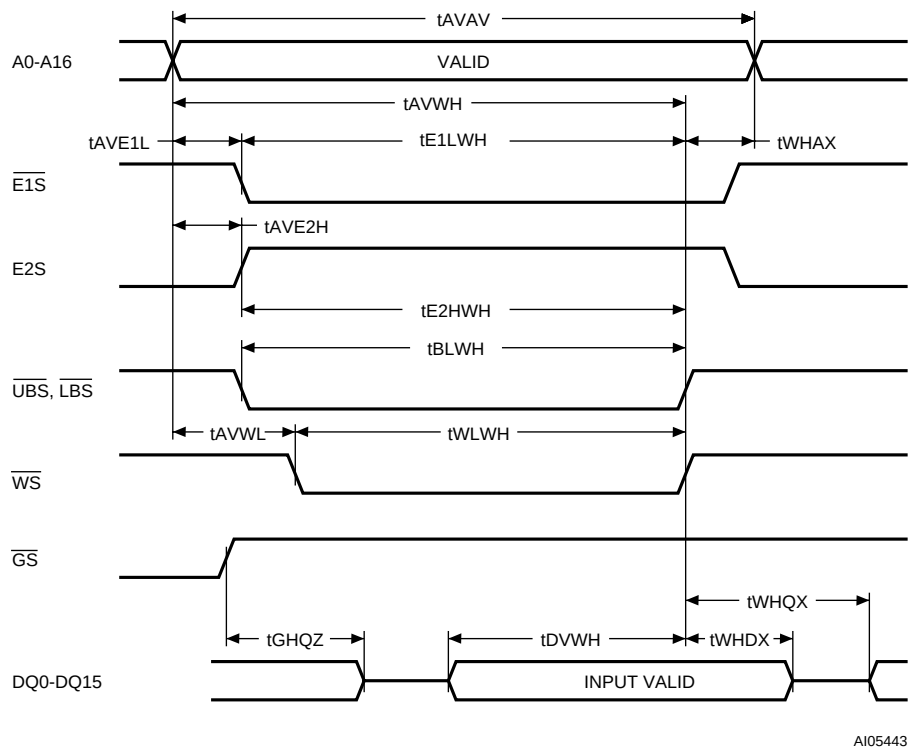


Figure 21. SRAM Write Cycle Waveform, $\overline{\text{UBS}}$ and $\overline{\text{LBS}}$ Controlled

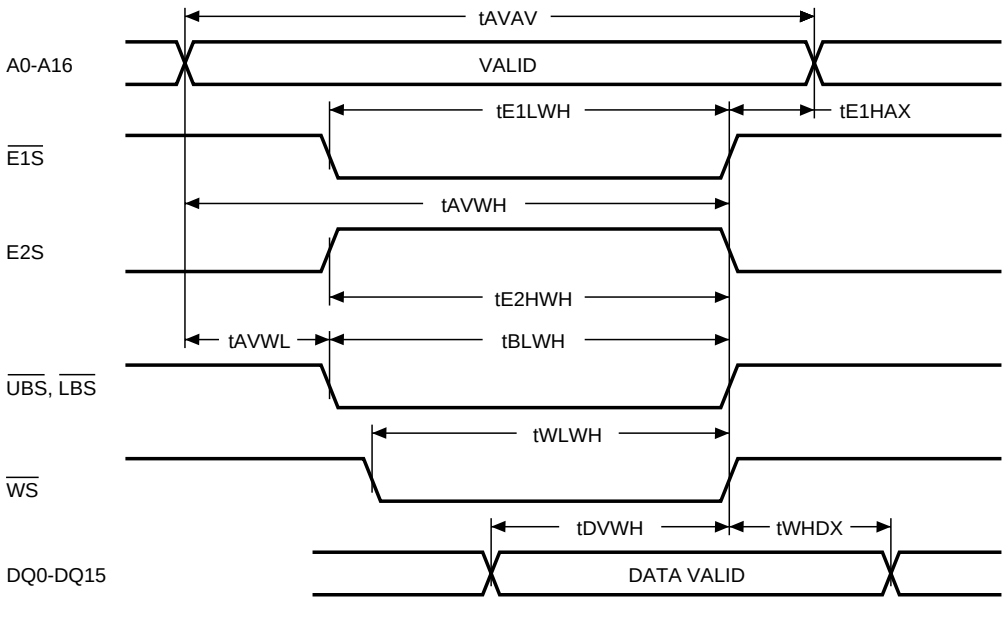
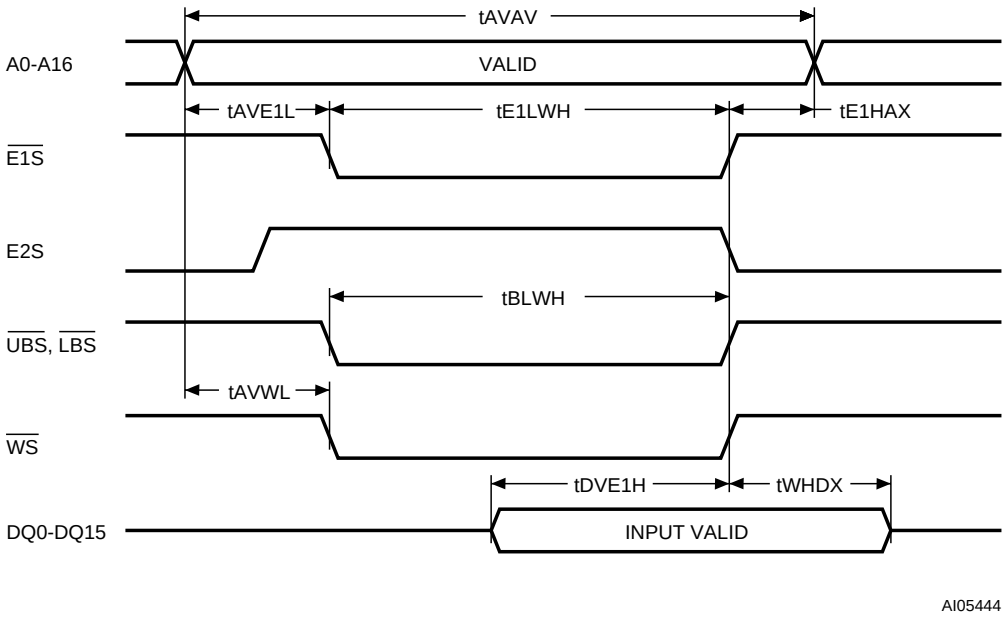


Figure 22. SRAM Write AC Waveforms, $\overline{\text{E1S}}$ Controlled



Note: Output Enable ($\overline{\text{GS}}$) = High.

Table 33. SRAM Low V_{CCS} Data Retention Characteristics (1, 2)
(T_A = –40 to 85°C; V_{DDS} = 1.65V to 2.2V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{DDDR}	Supply Current (Data Retention)	V_{DDS} = 1.0V, $\overline{E1S} \geq V_{DDS} - 0.2V$, E2S ≥ V_{DDS} – 0.2V or E2S ≤ 0.2V, f = 0		25	µA
V_{DR}	Supply Voltage (Data Retention)	$\overline{E1S} \geq V_{DDS} - 0.2V$, E2S ≤ 0.2V, f = 0	1	2.3	V
t_{CDR}	Chip Disable to Power Down	$\overline{E1S} \geq V_{CCS} - 0.2V$, E2S ≤ 0.2V, f = 0	0		ns
t_R	Operation Recovery Time		t_{RC}		ns

Note: 1. All other Inputs $V_{IH} \leq V_{DD} - 0.2V$ or $V_{IL} \leq 0.2V$.
2. Sampled only. Not 100% tested.

Figure 23. SRAM Low V_{DDS} Data Retention AC Waveforms, $\overline{E1S}$ Controlled

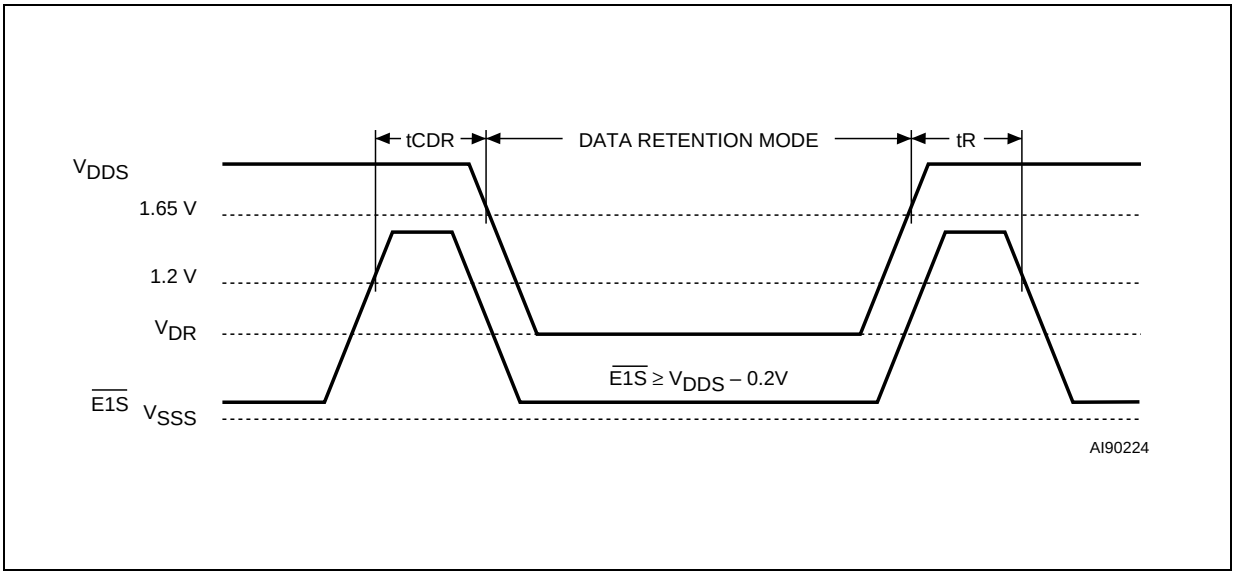


Figure 24. SRAM Low V_{DDS} Data Retention AC Waveforms, E2S Controlled

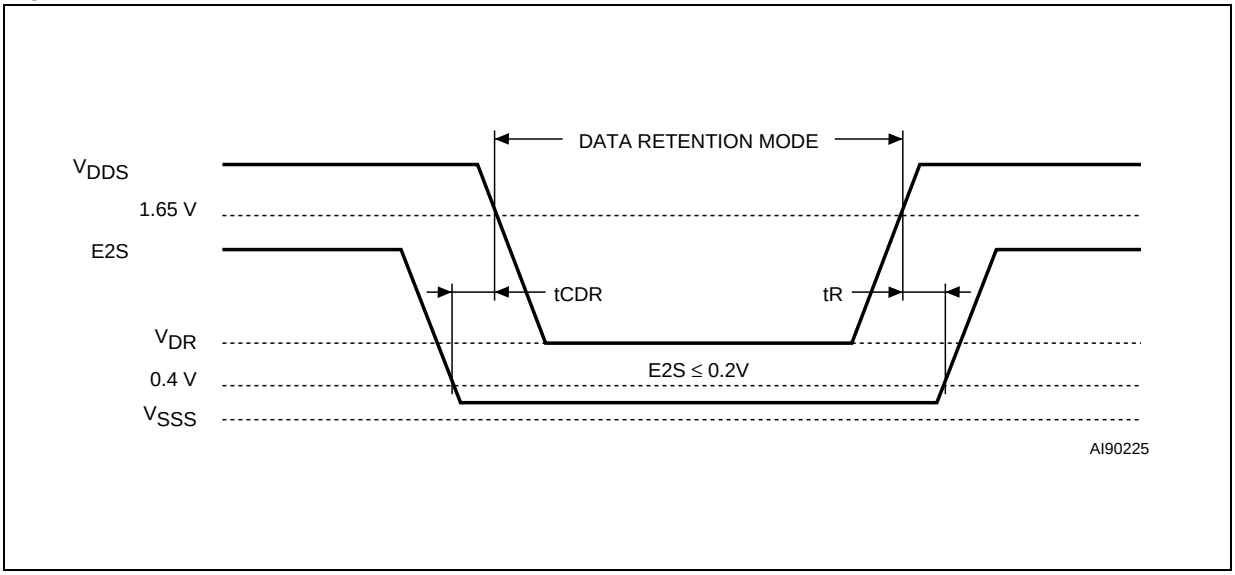


Table 34. Ordering Information Scheme

Example: M36DR232A 100 ZA 6 T

Device Type
M36 = MMP (Flash + SRAM)

Architecture
D = Dual Bank, Page Mode

Operating Voltage
R = V_{DDF} = V_{DDS} =1.65V to 2.2V

SRAM Chip Size & Organization
2 = 2 Mbit (256K x 16 bit)

Device Function
32A = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Top Boot
32B = 32 Mbit (x16), Dual Bank: 1/8-7/8 partitioning, Bottom Boot

Speed
100 = 100ns
120 = 120ns

Package
ZA = LFBGA66: 0.8mm pitch

Temperature Range
6 = –40 to 85°C

Option
T = Tape & Reel packing
C = Cypress's SRAM

Devices are shipped from the factory with the memory content bits erased to '1'.

Table 35. Daisy Chain Ordering Scheme

Example: M36DR232 -ZA T

Device Type
M36DR232

Daisy Chain
-ZA = LFBGA66: 0.8mm pitch

Option
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

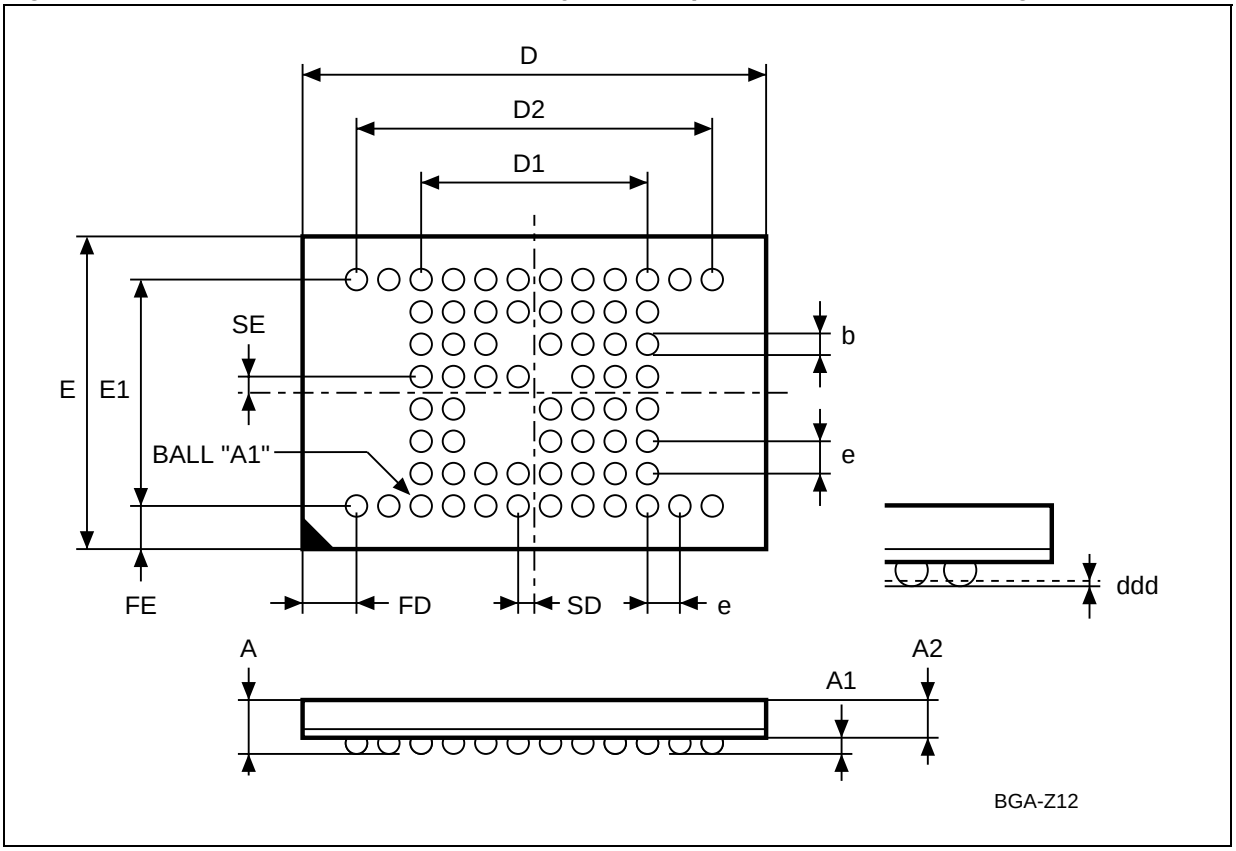
Table 36. Revision History

Date	Version	Revision Details
December 2000	-01	First Issue
6-March-2001	-02	Document type: from Preliminary Data to Data Sheet
26-July-2001	-03	Document Restructured DC Characteristics Table updated (Table 24) SRAM Write AC Waveforms, $\overline{WS}$ Controlled with $\overline{GS}$ High added (Figure 20)
19-Nov-2001	-04	LFBGA66 mechanical data updated (Table 37)

Table 37. Stacked LFBGA66 - 8 x 8 ball array, 0.8 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.250			0.0098	
A2			1.100			0.0433
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	12.000	–	–	0.4724	–	–
D1	5.600	–	–	0.2205	–	–
D2	8.800	–	–	0.3465	–	–
ddd			0.100			0.0039
E	8.000	–	–	0.3150	–	–
E1	5.600	–	–	0.2205	–	–
e	0.800	–	–	0.0315	–	–
FD	1.600	–	–	0.0630	–	–
FE	1.200	–	–	0.0472	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

Figure 25. Stacked LFBGA66 - 8 x 8 ball array, 0.8 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Figure 26. Stacked LFBGA66 Daisy Chain - Package Connections (Top view through package)

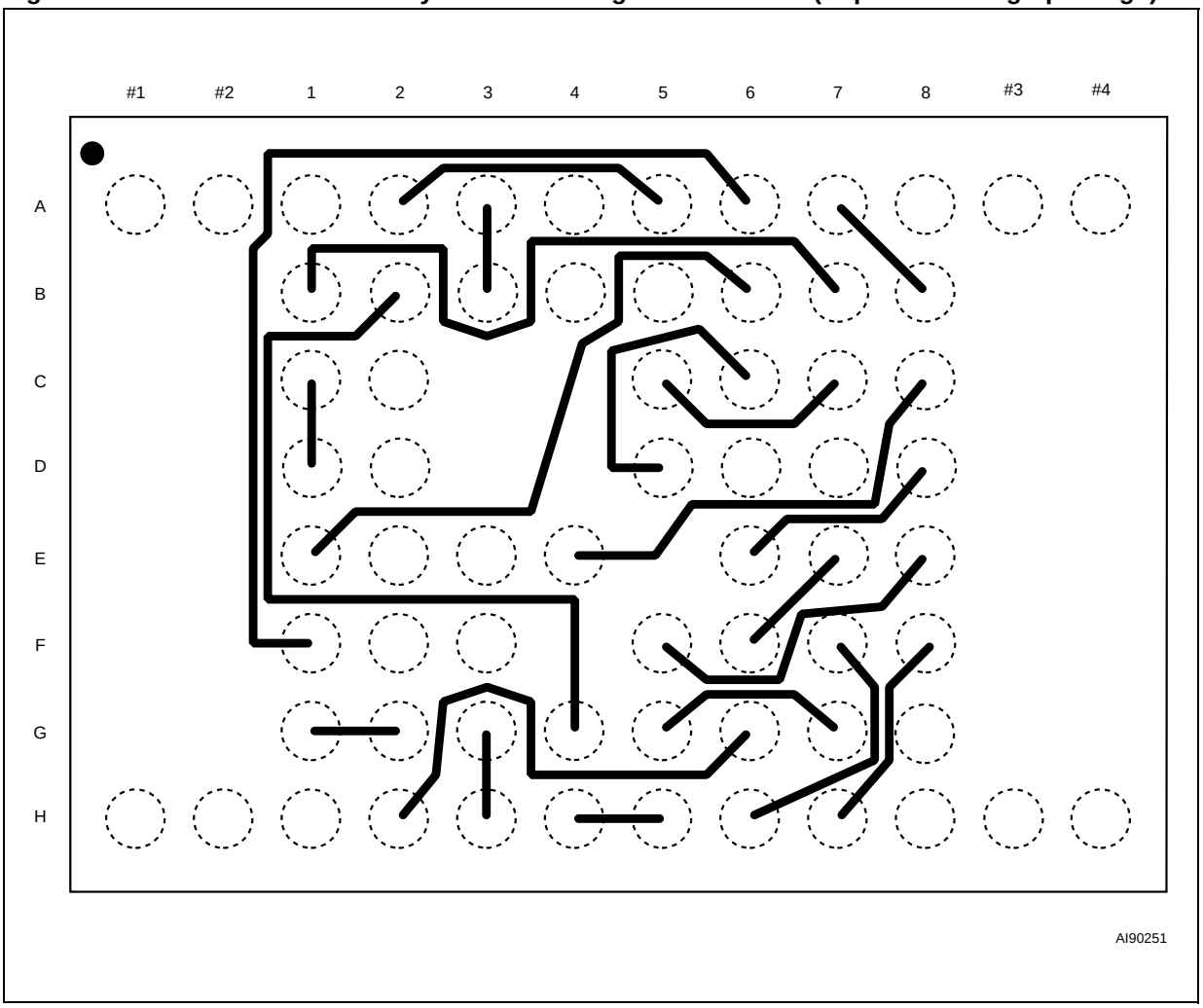


Figure 27. Stacked LFBGA66 Daisy Chain - PCB Connections proposal (Top view through package)