

# Preliminary

Notice: This is not a final specification.  
Some parametric limits are subject to change.

Renesas LSIs

## M6MGB/T331S8BKT

33,554,432-BIT (2,097,152 - WORD BY 16-BIT /4,194,304-WORD BY 8-BIT) CMOS  
FLASH MEMORY &  
8,388,608-BIT (524,288-WORD BY 16-BIT /1,048,576-WORD BY 8-BIT) CMOS SRAM  
Stacked -  $\mu$  MCP (micro Multi Chip Package)

### Description

The M6MGB/T331S8BKT is a Stacked micro Multi Chip Package (S- $\mu$ MCP) that contains 32M-bit Flash memory and 8M-bit Static RAM in a 52-pin TSOP for lead free use.

32M-bit Flash memory is a 4,194,304 bytes / 2,097,152 words, , single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is low. Using Software Lock Release function, program or erase operation can be executed.

8M-bit SRAM is a 1,048,576 bytes / 524,288 words asynchronous SRAM fabricated by CMOS technology for the peripheral circuit .

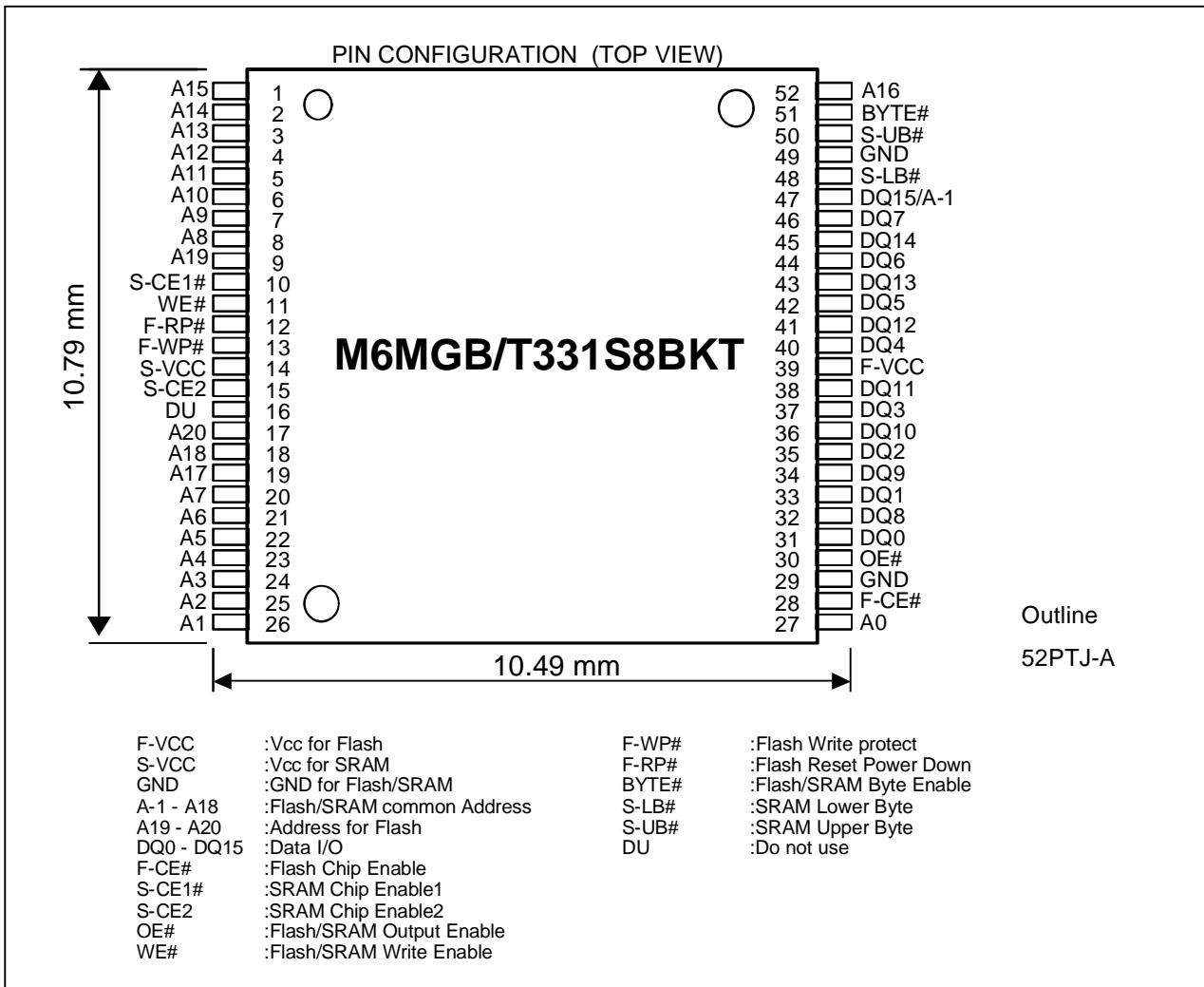
The M6MGB/T331S8BKT is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation

### Features

|                     |       |  |
|---------------------|-------|--|
| Access Time         | Flash | 70ns (Max.)  |
|                     | SRAM  | 85ns (Max.)  |
| Supply Voltage      |       | VCC=2.7 ~ 3.0V   |
| Ambient Temperature |       | Ta=-40 ~ 85 °C   |
| Package             |       | 52pin TSOP(Type-II),<br>Lead pitch 0.4mm<br>Outer-lead finishing:Sn-Cu |

### Application

Mobile communication products



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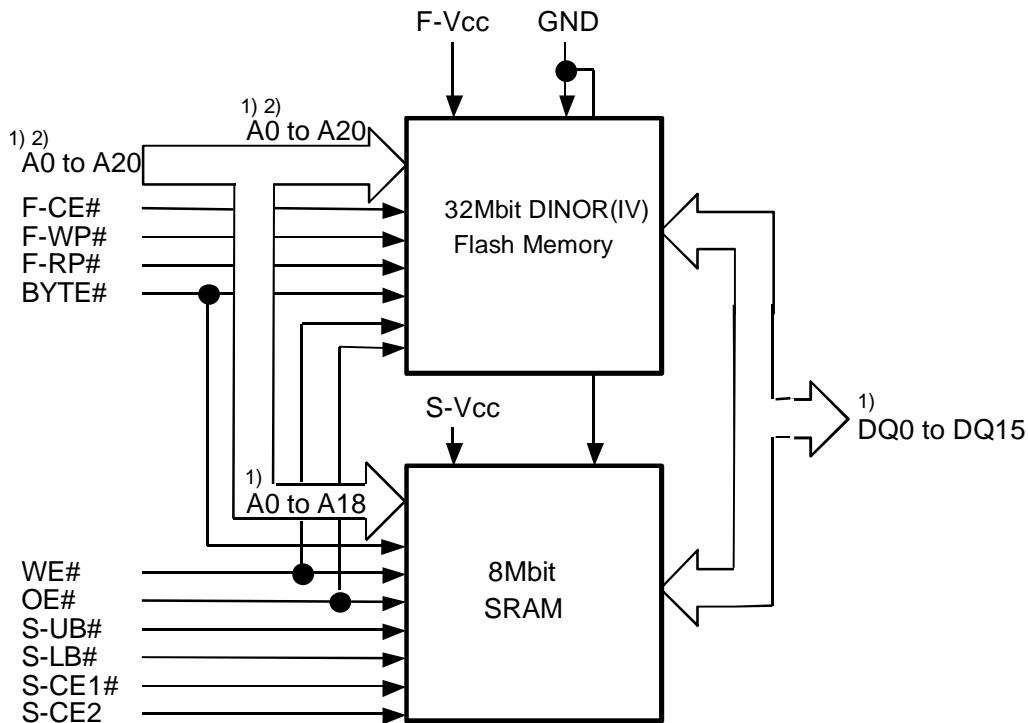
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### MCP Block Diagram



- Note 1): In case of x8 organization, A-1 is added, and only Lower Byte data(DQ0 to DQ7) are assigned to I/O and Upper Byte data(DQ8 to DQ15) are High-Z.  
Note 2): In the data sheet there are "VCC"s which mean "F-VCC" or "S-VCC". In the SRAM part there are "UB#" and "LB#" which mean "S-UB#" and "S-LB#", respectively.  
Note 3): "DU(Don't Use)" pin must be OPEN, otherwise be inputted within 0V ~ Vcc.

### Capacitance

| Symbol | Parameter          |   | Conditions                          | Limits |      |      | Unit |
|--------|--------------------|---|-------------------------------------|--------|------|------|------|
|        |                    |   |                                     | Min.   | Typ. | Max. |      |
| CIN    | Input capacitance  | A20-A0, OE#, WE#, F-CE#, F-WP#, F-RP#, S-CE1#, S-CE2, BYTE#, S-LB#, S-UB# | Ta=25 °C,<br>f=1MHz,<br>Vin=Vout=0V |        |      | 18   | pF   |
| COUT   | Output Capacitance | DQ15-DQ0  |                                     |        |      | 22   | pF   |

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3.0V-ONLY FLASH MEMORY &

8,388,608-BIT (524,288-WORD BY 16-BIT/1,048,576-WORD BY 8-BIT) CMOS SRAM  
Stacked -  $\mu$  MCP (micro Multi Chip Package)

## Renesas Technology Corp.

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