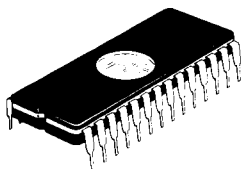


# M5L27128K, -2

**131 072-BIT (16384-WORD BY 8-BIT)  
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**



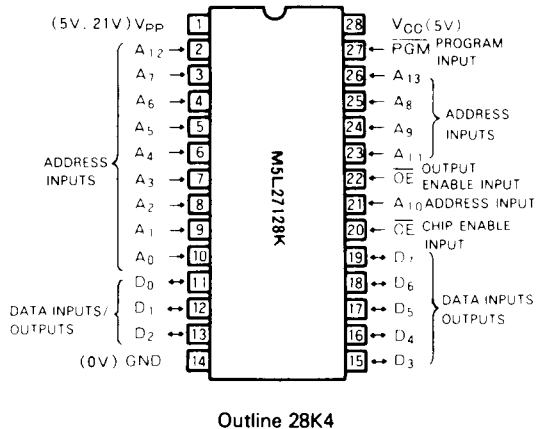
## DESCRIPTION

The Mitsubishi M5L27128K is a high-speed 131072-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27128K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIL package with a transparent lid.

## FEATURES

- 16384 word x 8 bit organization
- Access time M5L27128K-2 .....200ns (max.)  
M5L27128K .....250ns (max.)
- Two line control  $\overline{OE}$ ,  $\overline{CE}$
- Low power current ( $I_{CC}$ ): Active ..... 100mA (max.)  
Standby ..... 45mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIL package
- Fast programming algorithm
- Interchangeable with INTEL 27128

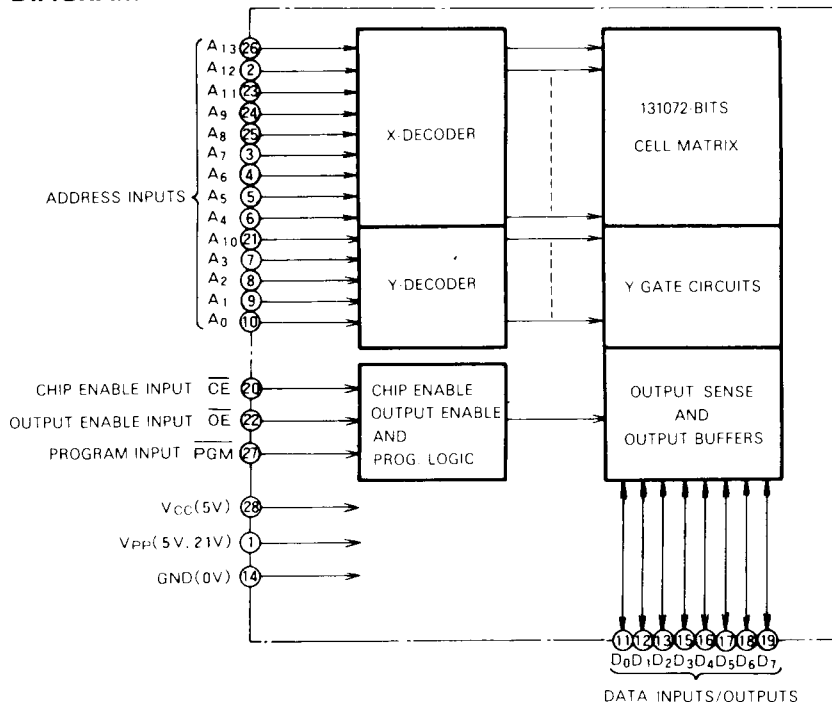
## PIN CONFIGURATION (TOP VIEW)



## APPLICATION

- Microcomputer systems and peripheral equipment

## BLOCK DIAGRAM



131 072-BIT(16384-WORD BY 8-BIT)  
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**FUNCTION**

**Read**

Set the  $\overline{CE}$  and  $\overline{OE}$  terminals to the read mode (low level). Low level input to  $\overline{CE}$  and  $\overline{OE}$  and address signals to the address inputs ( $A_0 \sim A_{13}$ ) make the data contents of the designated address location available at the data input/output ( $D_0 \sim D_7$ ). When the  $\overline{CE}$  or  $\overline{OE}$  signal is high, data input/output are in a floating state.

When the  $\overline{CE}$  signal is high, the device is in the standby mode or power-down mode.

**Programming**

**(Fast programming algorithm)**

First set  $V_{CC} = 6V$ ,  $V_{PP} = 21V$  and then set an address to first address to be programmed. After applying 1 ms program pulse ( $\overline{PGM}$ ) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1 ms program pulse. The programmer continues 1 ms pulse-then-verify routines until the device verify correctly or fifteen of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1 ms pulses applied to that address in register X. And then applied a program pulse 4 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. (See P.6-15)

**(Conventional programming algorithm)**

The device enters the programming mode when 21V is applied to the  $V_{PP}$  power supply input and  $\overline{CE}$  is at low level. A location is designated by address signals ( $A_0 \sim A_{13}$ ), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ( $D_0 \sim D_7$ ). A program pulse to the  $\overline{PGM}$  at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition  $45 \text{ ms} \leq t_{PW} \leq 55 \text{ ms}$ .

**Erase**

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm<sup>2</sup>. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

**MODE SELECTION**

Mode	Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	$V_{PP}$ (1)	$V_{CC}$ (28)	Outputs (11 ~ 13, 15 ~ 19)
Read		$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	Data out
Standby		$V_{IH}$	X*	X*	$V_{CC}$	$V_{CC}$	Floating
Program		$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{PP}$	$V_{CC}$	Data in
Program verify		$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	Data out
Program inhibit		$V_{IH}$	X*	X*	$V_{PP}$	$V_{CC}$	Floating

\*: X can be either  $V_{IL}$  or  $V_{IH}$ .

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Symbol	Parameter	Limits	Unit
$T_{opr}$	Temperature under bias	- 10 ~ 80	°C
$T_{stg}$	Storage temperature	- 65 ~ 125	°C
$V_{I1}$	All input or output voltage (Note 2)	0.6 ~ 7	V
$V_{I2}$	$V_{PP}$ supply voltage during programming (Note 2)	- 0.6 ~ 26.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

**131 072-BIT(16384-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**READ OPERATION**

**DC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, V<sub>CC</sub>=5V±5%, V<sub>PP</sub>=V<sub>CC</sub>, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input load current	V <sub>IN</sub> = 5.25V			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = 5.25V			10	μA
I <sub>PP1</sub>	V <sub>PP</sub> current read	V <sub>PP</sub> = 5.25V			5	mA
I <sub>CC1</sub>	V <sub>CC</sub> current standby	$\overline{CE} = V_{IH}$			45	mA
I <sub>CC2</sub>	V <sub>CC</sub> current Active	$\overline{CE} = \overline{OE} = V_{IL}$			100	mA
V <sub>IL</sub>	Input low voltage		0.1		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -400μA	2.4			V

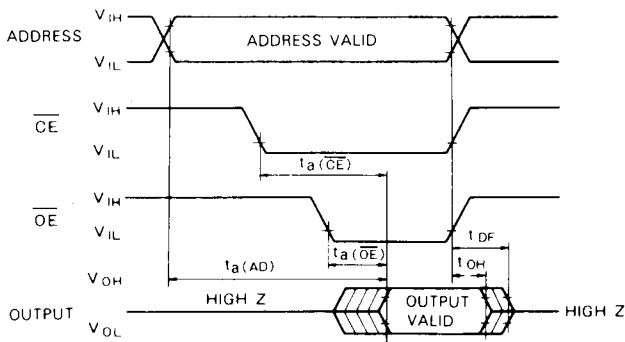
Note 3: Typical values are at Ta = 25°C and nominal supply voltages.

**AC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, V<sub>CC</sub>=5V±5%, V<sub>PP</sub>=V<sub>CC</sub>, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits				Unit
			M5L27128K-2		M5L27128K		
			Min	Max	Min	Max	
t <sub>a(AD)</sub>	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250	ns
t <sub>a(<math>\overline{CE}</math>)}</sub>	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		200		250	ns
t <sub>a(<math>\overline{OE}</math>)}</sub>	Output enable to output delay	$\overline{CE} = V_{IL}$		75		100	ns
t <sub>DF</sub>	Output enable high to output float	$\overline{CE} = V_{IL}$	0	60	0	85	ns
t <sub>OH</sub>	Output hold from $\overline{CE}$ or $\overline{OE}$	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

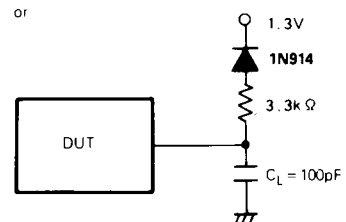
Note 4: V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>

**AC WAVEFORMS**



Test conditions for A.C. characteristics  
 Input voltage: V<sub>IL</sub> = 0.45V, V<sub>IH</sub> = 2.4V  
 Input rise and fall times: ≤ 20ns  
 Reference voltage at timing measurement: Inputs 1V and 2V Output 0.8V, and 2V

Output load: 1TTL gate + C<sub>L</sub>(100pF)



**CAPACITANCE**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>IN</sub>	Input capacitance (Address, $\overline{CE}$ , $\overline{OE}$ , PGM)	T <sub>a</sub> = 25°C, f = 1MHz, V <sub>I</sub> = V <sub>O</sub> = 0V		4	6	pF
C <sub>OUT</sub>	Output capacitance			8	12	pF

**131 072-BIT (16384-WORD BY 8-BIT)  
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**PROGRAM OPERATION**

**FAST PROGRAMMING ALGORITHM**

**DC ELECTRICAL CHARACTERISTICS**

( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input current	$V_{IN} = V_{IL}$ or $V_{IH}$			10	$\mu\text{A}$
$V_{OL}$	Output low voltage	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4			V
$V_{IL}$	Input low voltage		-0.1		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC}$	V
$I_{CC2}$	$V_{CC}$ supply current				100	mA
$I_{PP2}$	$V_{PP}$ supply current	$\overline{CE} = V_{IL} = \text{PGM}$			30	mA

**AC ELECTRICAL CHARACTERISTICS**

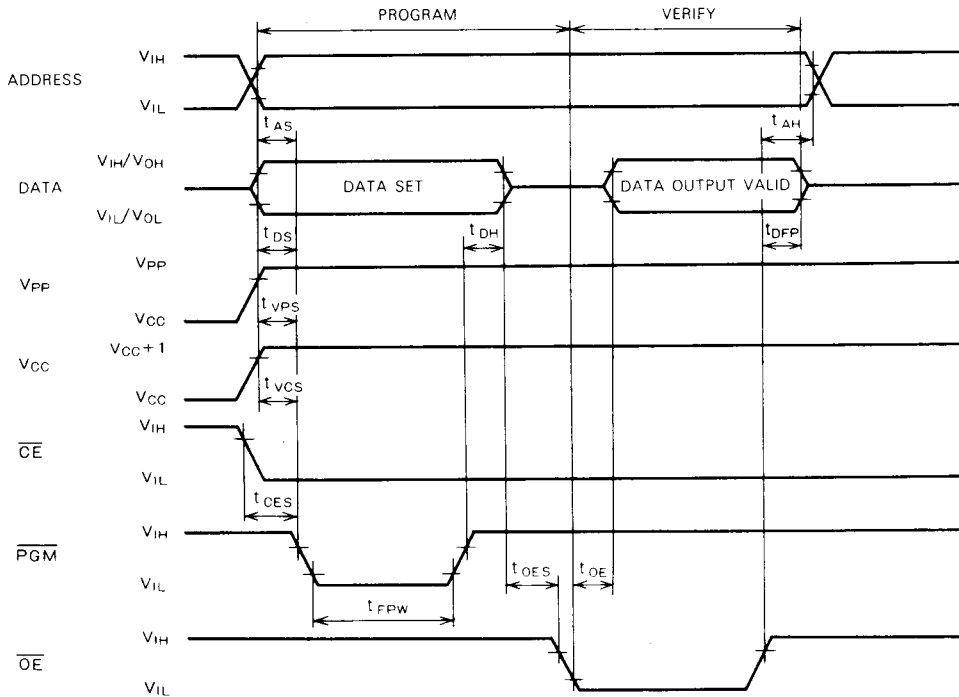
( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address setup time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ set up time		2			$\mu\text{s}$
$t_{DS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DFP}$	Output enable to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{FPW}$	PGM initial program pulse width		0.95	1	1.05	ms
$t_{OPW}$	PGM over program pulse width		3.8		63	ms
$t_{CES}$	$\overline{CE}$ setup time		2			$\mu\text{s}$
$t_{OE}$	Data valid from $\overline{OE}$				150	ns

Note 5:  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**131 072-BIT (16384-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

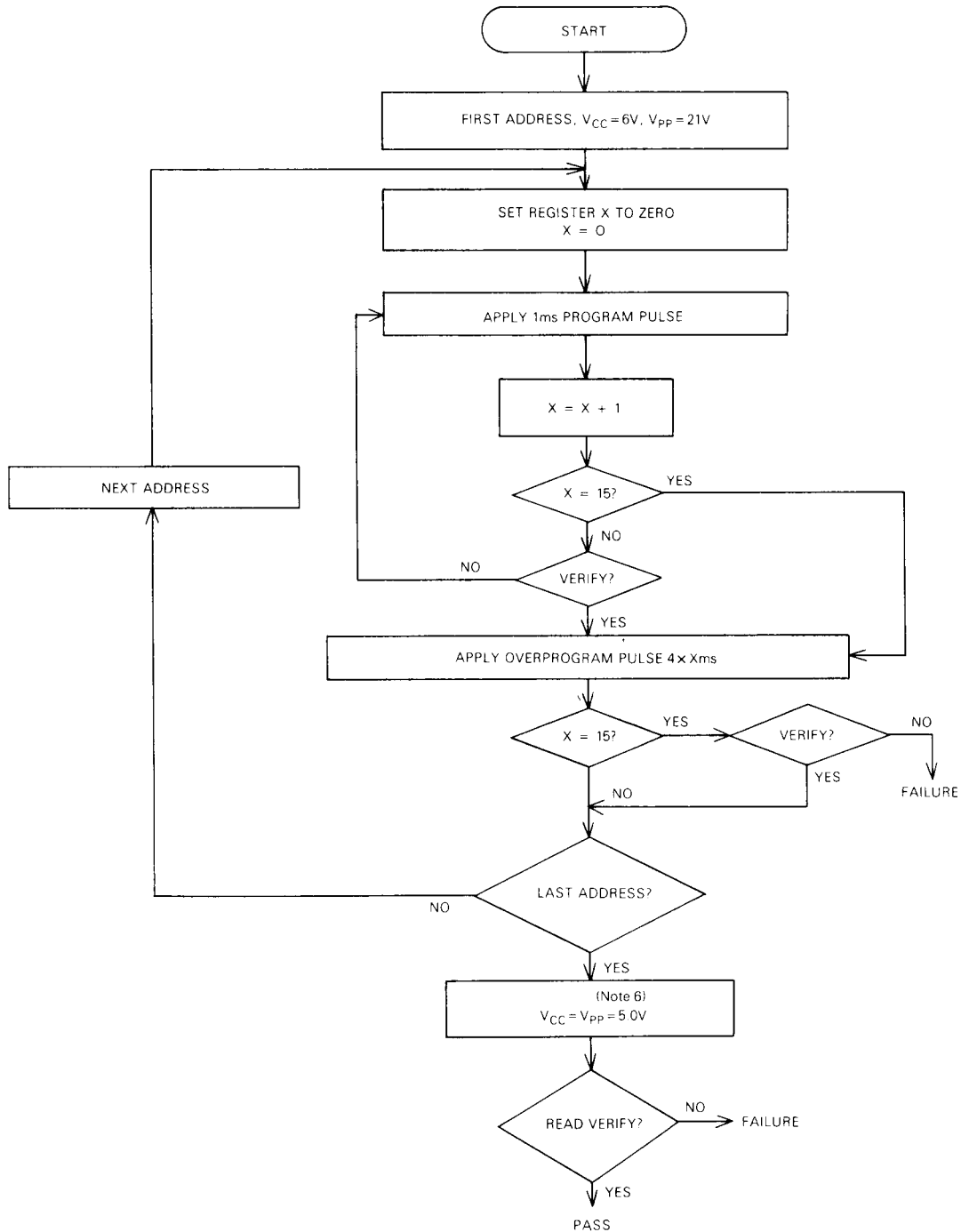
**AC WAVEFORMS**



Test conditions for A.C. characteristics  
 Input voltage:  $V_{IL} = 0.45V$ ,  $V_{IH} = 2.4V$   
 Input rise and fall times:  $\leq 20ns$   
 Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V

**131 072-BIT(16384-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**FAST PROGRAMMING ALGORITHM  
 FLOW CHART**



Note 6.  $4.75 \leq V_{CC} = V_{PP} \leq 5.25V$

**131 072-BIT(16384-WORD BY 8-BIT)**  
**ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**CONVENTIONAL PROGRAMMING ALGORITHM**

**DC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input current	$V_{IN} = V_{IL}$ or $V_{IH}$			10	$\mu\text{A}$
$V_{OL}$	Output low voltage	$I_{OL} = 2.1\text{mA}$			0.45	V
$V_{OH}$	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4			V
$V_{IL}$	Input low voltage		-0.1		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC} + 1$	V
$I_{CC2}$	$V_{CC}$ Supply current				100	mA
$I_{PP2}$	$V_{PP}$ Supply current	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

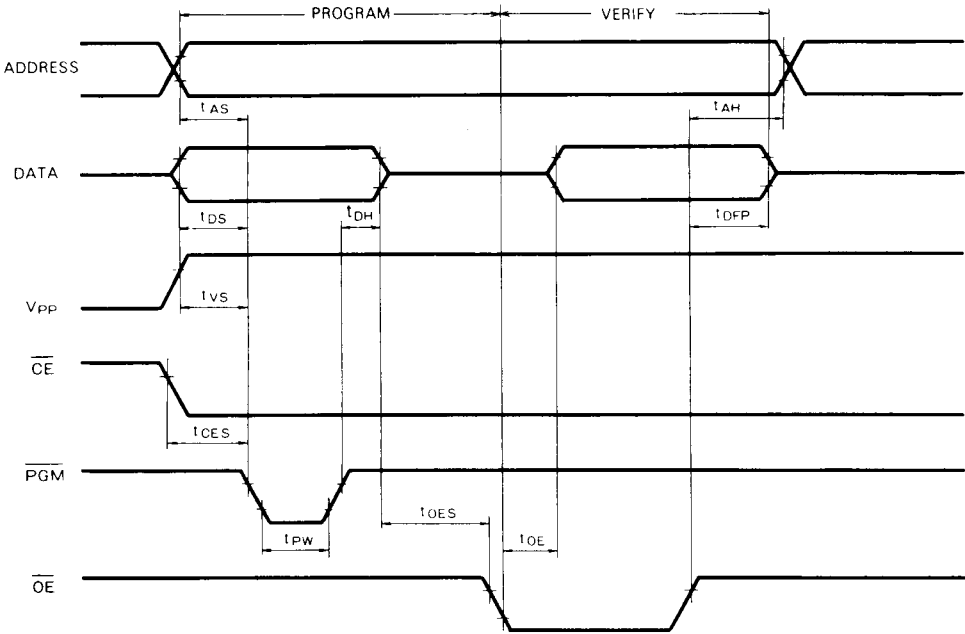
**AC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = 21V \pm 0.5V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address set up time		2			$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ setup time		2			$\mu\text{s}$
$t_{DS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DFP}$	Output enable to output delay		0		130	ns
$t_{VS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{PW}$	$\overline{PGM}$ Pulse width (during program)		45	50	55	ms
$t_{CES}$	$\overline{CE}$ setup time		2			$\mu\text{s}$
$t_{OE}$	Data valid from $\overline{OE}$				150	ns

Note 7:  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**131 072-BIT(16384-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**AC WAVEFORMS**



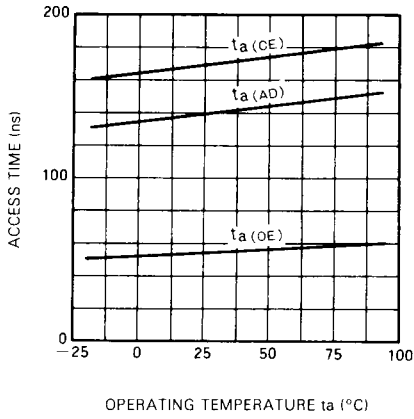
Test conditions for A.C. characteristics  
 Input rise and fall time:  $\leq 20\text{ns}$   
 Input voltage:  $V_{IL} = 0.45\text{V}$ ,  $V_{IH} = 2.4\text{V}$   
 Reference voltage at timing measurement: Input 0.8V and 2V  
 Outputs 0.8V and 2V



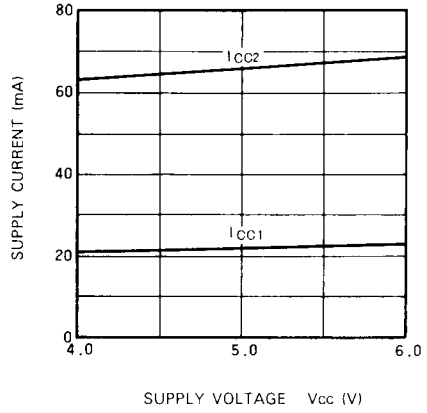
**131 072-BIT(16384-WORD BY 8-BIT)  
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**TYPICAL CHARACTERISTICS**

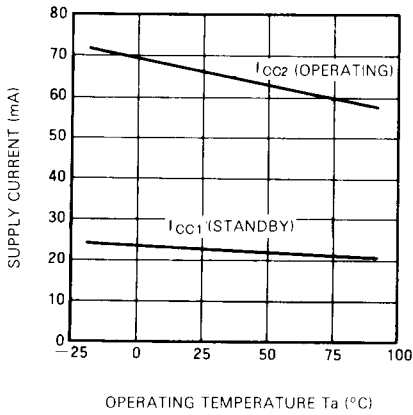
**ACCESS TIME VS  
 OPERATING TEMPERATURE**



**SUPPLY CURRENT VS  
 SUPPLY VOLTAGE**



**SUPPLY CURRENT VS  
 OPERATING TEMPERATURE**



**OUTPUT CHARACTERISTICS**

