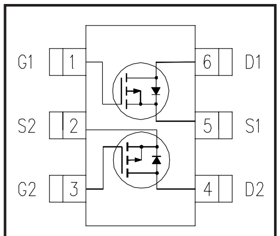
International
IOR Rectifier

IRF5850

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Low Gate Charge



Top View

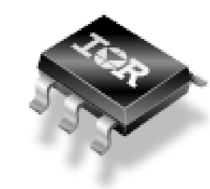
V_{DSS} = -20V

$R_{DS(on)}$ = 0.135Ω

Description

These P-channel MOSFETs from International Rectifier utilize advanced processing techniques to achieve the extremely low on-resistance per silicon area. This benefit provides the designer with an extremely efficient device for use in battery and load management applications.

This Dual TSOP-6 package is ideal for applications where printed circuit board space is at a premium and where maximum functionality is required. With two die per package, the IRF5850 can provide the functionality of two SOT-23 packages in a smaller footprint. Its unique thermal design and $R_{DS(on)}$ reduction enables an increase in current-handling capability.


TSOP-6

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ -4.5V	-2.2	A
I_D @ T_A= 70°C	Continuous Drain Current, V_{GS} @ -4.5V	-1.8	
I_{DM}	Pulsed Drain Current ①	-9.0	
P_D @T_A = 25°C	Power Dissipation	0.96	W
P_D @T_A = 70°C	Power Dissipation	0.62	
	Linear Derating Factor	7.7	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

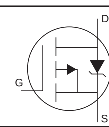
	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient③	130	°C/W

7/25/00

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	——	——	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.011	——	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.135	Ω	V_{GS} = -4.5V, I_D = -2.2A ②
		——	——	0.220		V_{GS} = -2.5V, I_D = -1.9A ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	——	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	3.5	——	——	S	V_{DS} = -10V, I_D = -2.2A
I_{DSS}	Drain-to-Source Leakage Current	——	——	-1.0	µA	V_{DS} = -16V, V_{GS} = 0V
		——	——	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	-100	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage	——	——	100		V_{GS} = 12V
Q_g	Total Gate Charge	——	3.6	5.4	nC	I_D = -2.2A
Q_{gs}	Gate-to-Source Charge	——	0.66	——		V_{DS} = -10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	0.83	——		V_{GS} = -4.5V ②
$t_{d(on)}$	Turn-On Delay Time	——	8.3	——	ns	V_{DD} = -10V ②
t_r	Rise Time	——	14	——		I_D = -1.0A
$t_{d(off)}$	Turn-Off Delay Time	——	31	——		R_G = 6.0Ω
t_f	Fall Time	——	28	——		V_{GS} = -4.5V
C_{iss}	Input Capacitance	——	320	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	56	——		V_{DS} = -15V
C_{rss}	Reverse Transfer Capacitance	——	40	——		f = 1.0kHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-0.96	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-9.0		
V_{SD}	Diode Forward Voltage	——	——	-1.2	V	T_J = 25°C, I_S = -0.96A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	——	23	35	ns	T_J = 25°C, I_F = -0.96A
Q_{rr}	Reverse Recovery Charge	——	7.7	12	nC	di/dt = -100A/µs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ Surface mounted on FR-4 board, t ≤ 5sec.

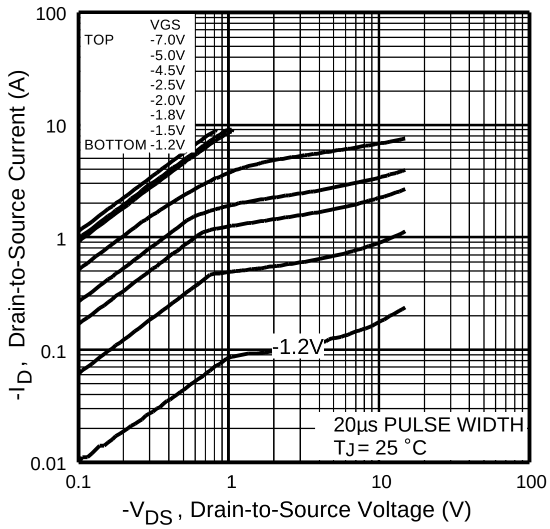


Fig 1. Typical Output Characteristics

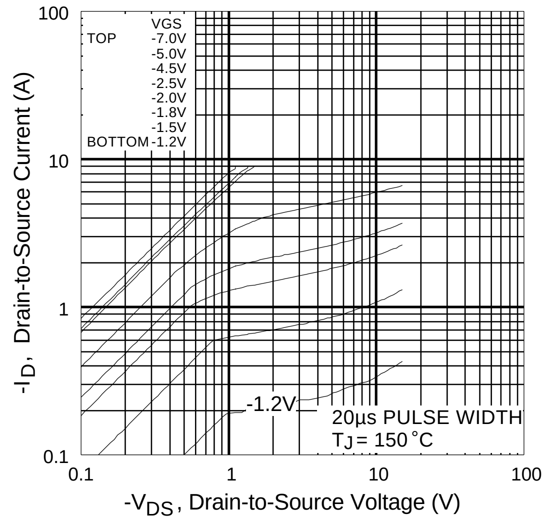


Fig 2. Typical Output Characteristics

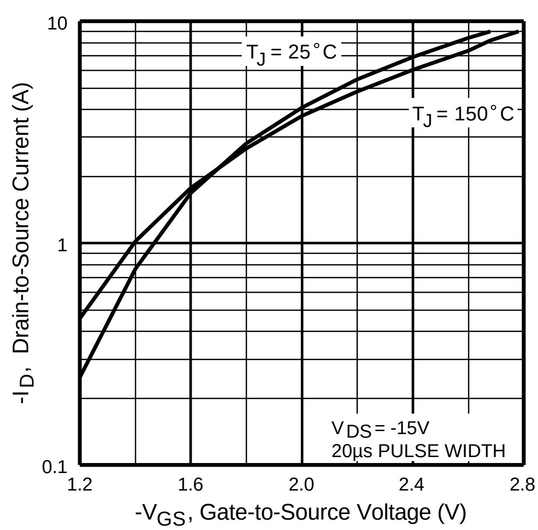


Fig 3. Typical Transfer Characteristics

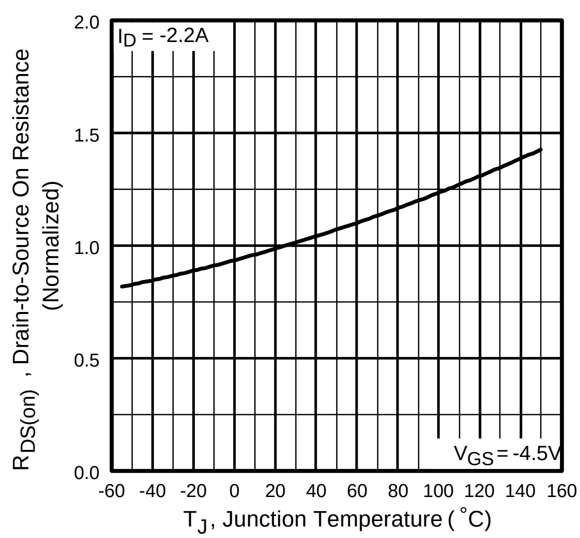


Fig 4. Normalized On-Resistance
Vs. Temperature

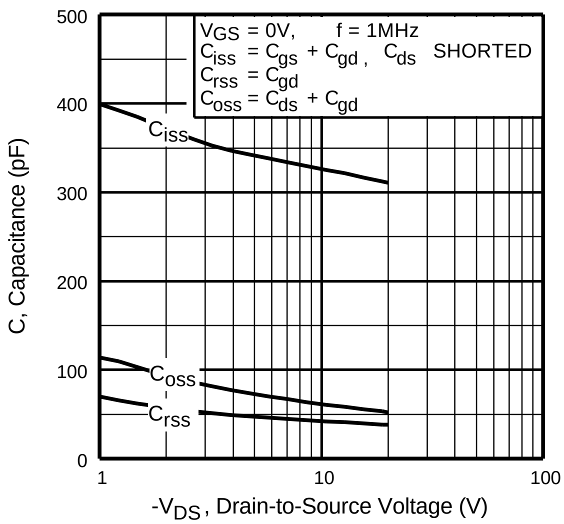


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

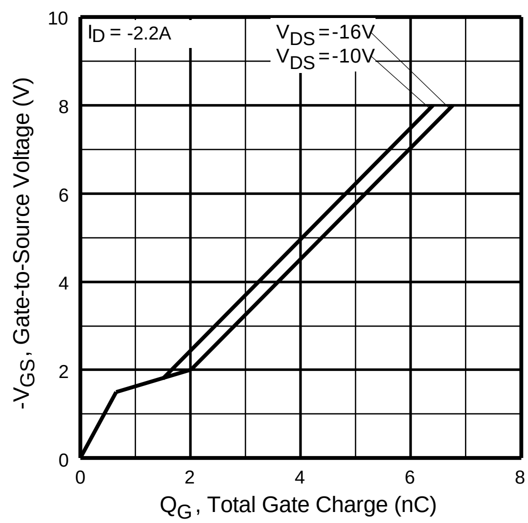


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

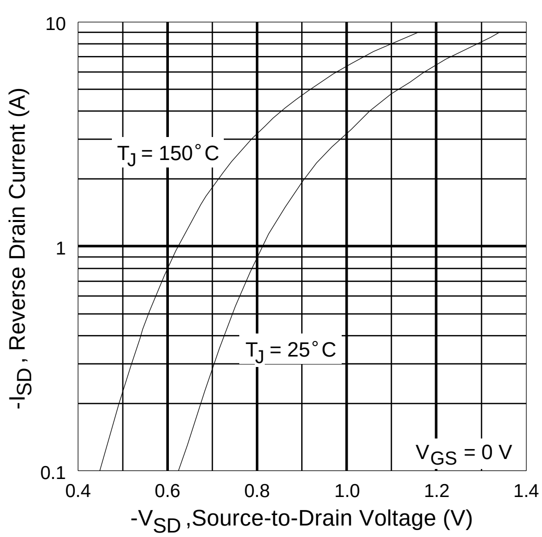


Fig 7. Typical Source-Drain Diode Forward Voltage

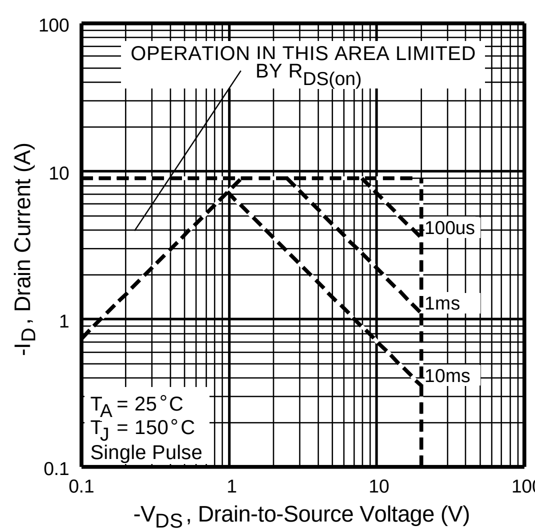


Fig 8. Maximum Safe Operating Area

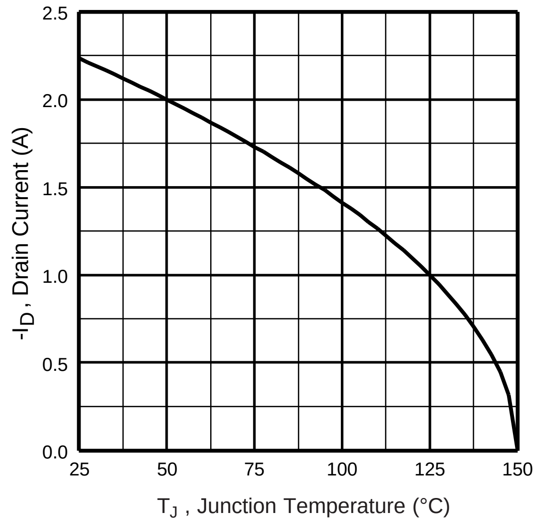


Fig 9. Maximum Drain Current Vs. Junction Temperature

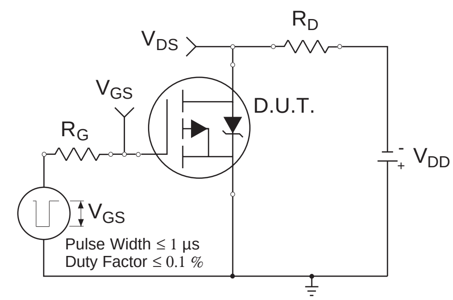


Fig 10a. Switching Time Test Circuit

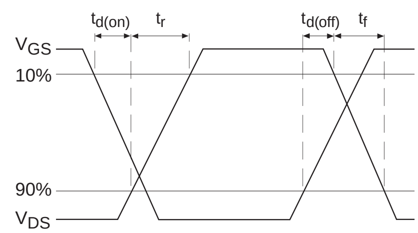


Fig 10b. Switching Time Waveforms

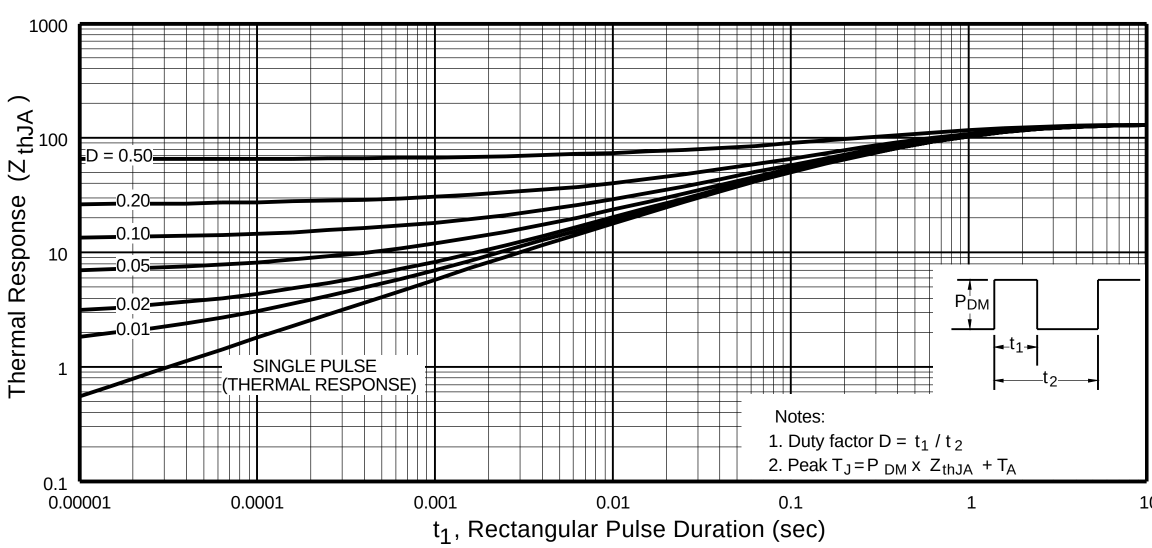


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

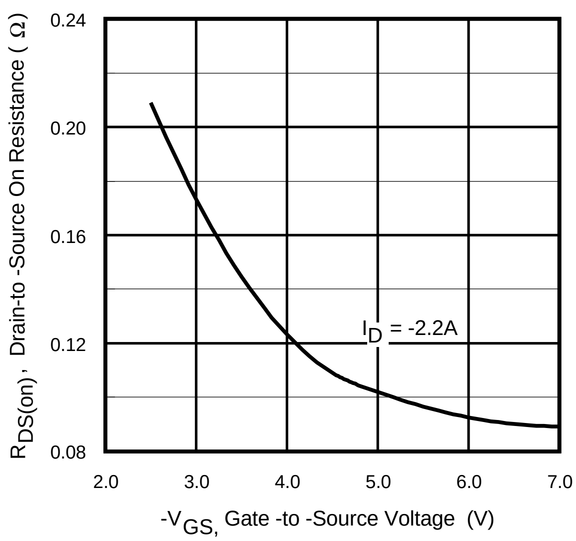


Fig 11. Typical On-Resistance Vs. Gate Voltage

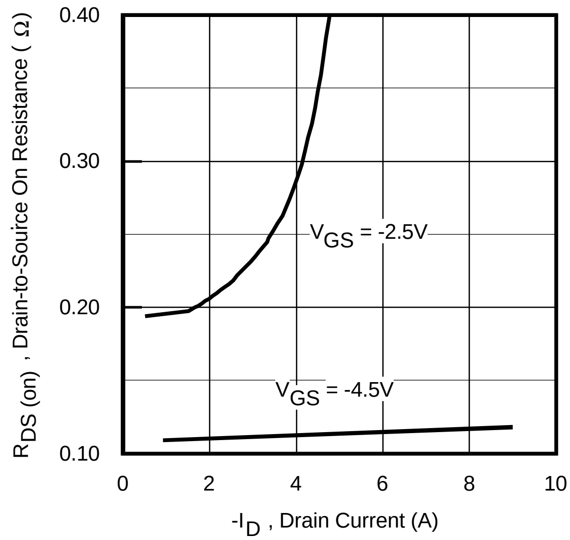


Fig 12. Typical On-Resistance Vs. Drain Current

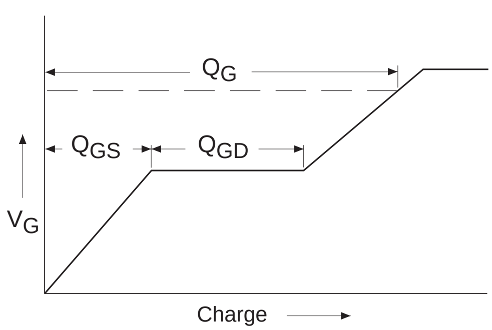


Fig 13a. Basic Gate Charge Waveform

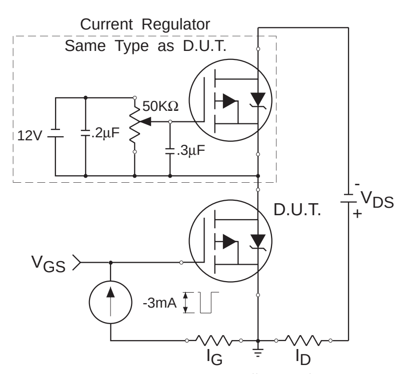


Fig 13b. Gate Charge Test Circuit

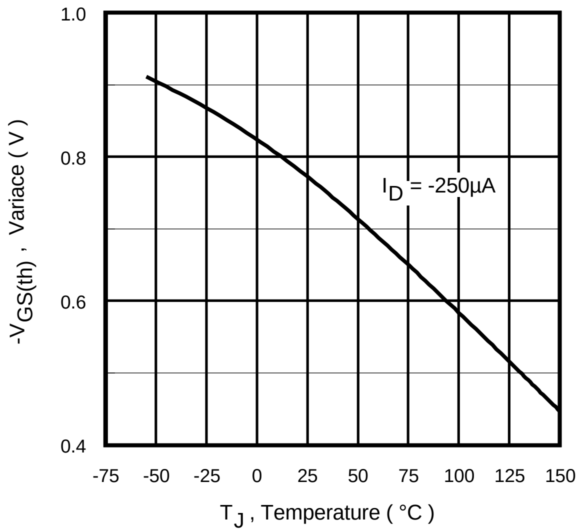


Fig 14. Threshold Voltage Vs. Temperature

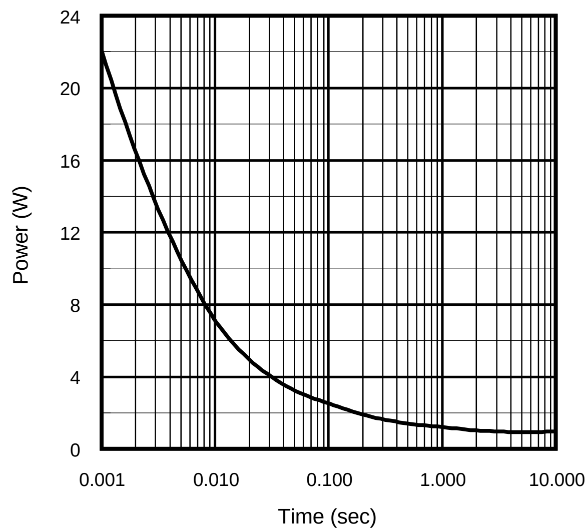
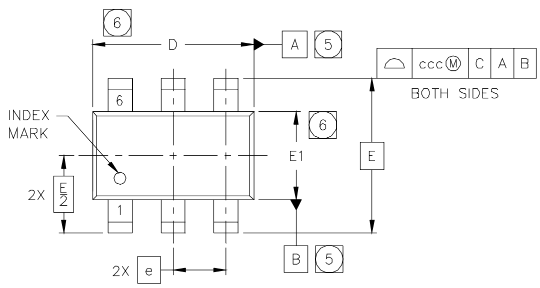
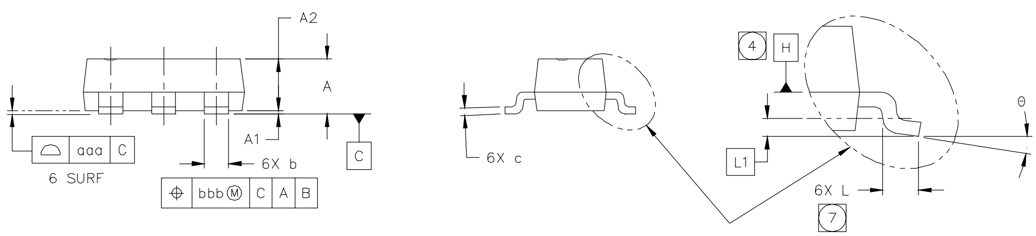


Fig 15. Typical Power Vs. Time

TSOP-6 Package Outline

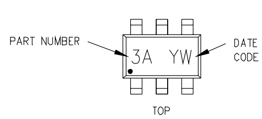


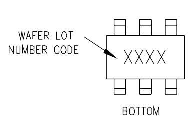
SYMBOL	MO-193AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	.0433
A1	0.01	---	0.10	.0004	---	.0039
A2	0.80	0.90	1.00	.0315	.0354	.0393
b	0.25	---	0.50	.0099	---	.0196
c	0.10	---	0.26	.004	---	.010
D	2.90	3.00	3.10	.115	.118	.122
E	2.75 BSC			.108 BSC		
E1	1.30	1.50	1.70	.052	.059	.066
e	1.00 BSC			.039 BSC		
L	0.20	0.40	0.60	.0079	.0157	.0236
L1	0.30 BSC			.0118 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.004		
bbb	0.15			.006		
ccc	0.25			.010		



TSOP-6 Part Marking Information

EXAMPLE: THIS IS AN SI3443DV





WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

WW = (27-52) IF PRECEDED BY A LETTER

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

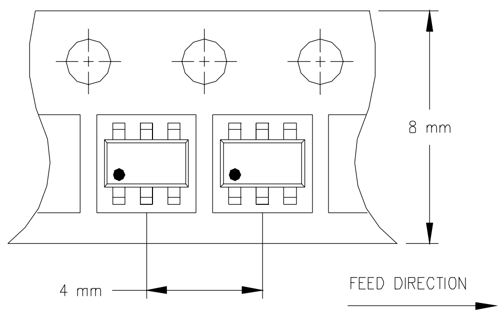
PART NUMBER CODE REFERENCE:

3A = SI3443DV
3B = IRF5800
3C = IRF5850

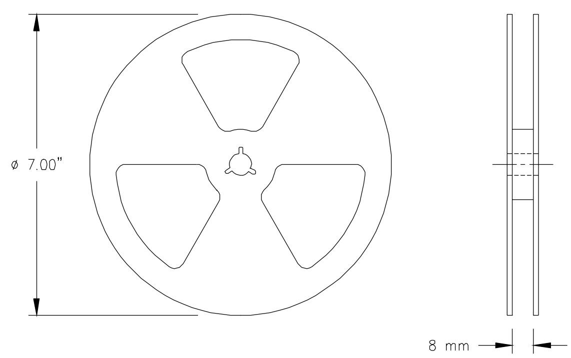
DATE CODE EXAMPLES:

YWW = 9603 = 6C
YWW = 9632 = FF

TSOP-6 Tape & Reel Information



NOTES:
1. OUTLINE CONFORMS TO EIA−481 & EIA−541.



NOTES:
1. OUTLINE CONFORMS TO EIA−481 & EIA−541.

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