Section I. Stratix II Device Family Data Sheet

This section provides designers with the data sheet specifications for Stratix® II devices. They contain feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II devices.

This section contains the following chapters:

- Chapter 1. Introduction
- Chapter 2. Stratix II Architecture
- Chapter 3. Configuration & Testing
- Chapter 4. Hot Socketing, ESD & Power-On Reset
- Chapter 5. DC & Switching Characteristics
- Chapter 6. Reference & Ordering Information

Revision History

The table below shows the revision history for Chapters 1 through 6.

Chapter	Date / Version	Changes Made
1	March 2005, 2.1	Updated "Introduction" and "Features" sections.
	January 2005, v2.0	Added note to Table 1–2.
	October 2004, v1.2	Updated Tables 1–2, 1–3, and 1–4.
	July 2004, v1.1	• Updated Tables 1–1 and 1–2. • Updated "Features" section.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.

Chapter	Date / Version	Changes Made
2	March 2005, 2.1	• Updated "Functional Description" section. • Updated Table 2–3.
	January 2005, v2.0	• Updated the "MultiVolt I/O Interface" and "TriMatrix Memory" sections. • Updated Tables 2–3, 2–17, and 2–19.
	October 2004, v1.2	• Updated Tables 2–9, 2–16, 2–26, and 2–27.
	July 2004, v1.1	• Updated note to Tables 2–9 and 2–16. • Updated Tables 2–16, 2–17, 2–18, 2–19, and 2–20. • Updated Figures 2–41, 2–42, and 2–57. • Removed 3 from list of SERDES factor *J*. • Updated "High-Speed Differential I/O with DPA Support" section. • In "Dedicated Circuitry with DPA Support" section, removed XSBI and changed RapidIO to Parallel RapidIO.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.
3	January 2005, v2.1	Updated JTAG chain device limits.
	January 2005, v2.0	Updated Table 3–3.
	July 2004, v1.1	• Added "Automated Single Event Upset (SEU) Detection" section. • Updated "Device Security Using Configuration Bitstream Encryption" section. • Updated Figure 3–2.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.
4	January 2005, v2.1	Updated input rise and fall time.
	January 2005, v2.0	Updated the "Hot Socketing Feature Implementation in Stratix II Devices", "ESD Protection", and "Power-On Reset Circuitry" sections.
	July 2004, v1.1	• Updated all tables. • Added tables.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.

Chapter	Date / Version	Changes Made
5	March 2005, v2.2	Updated tables in "Internal Timing Parameters" section.
	January 2005, v2.1	Updated input rise and fall time.
	January 2005, v2.0	• Updated the "Power Consumption" section. • Added the "High-Speed I/O Specifications" and "On-Chip Termination Specifications" sections. • Removed the ESD Protection Specifications section. • Updated Tables 5–3 through 5–12, 5–15 through 5–17, 5–20, 5–33, 5–37, and 5–38. • Updated tables in "Timing Model" section. • Added Tables 5–28 and 5–29.
	October 2004, v1.2	• Updated Table 5–3. • Updated introduction text in the "PLL Timing Specifications" section.
	July 2004, v1.1	• Re-organized chapter. • Added typical values and C_{OUTFB} to Table 5–30. • Added undershoot specification to *Note (4)* for Tables 5–1 through 5–9. • Added *Note (1)* to Tables 5–5 and 5–6. • Added V_{ID} and V_{ICM} to Table 5–10. • Added "I/O Timing Measurement Methodology" section. • Added Table 5–69. • Updated Tables 5–1 through 5–2 and Tables 5–22 through 5–27.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.
6	January 2005, v2.0	Contact information was removed.
	October 2004, v1.1	Updated Figure 6–1.
	February 2004, v1.0	Added document to the Stratix II Device Handbook.

1. Introduction

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Introduction

The Stratix® II FPGA family is based on a 1.2-V, 90-nm, all-layer copper SRAM process and features a new logic structure that maximizes performance, and enables device densities approaching 180,000 equivalent logic elements (LEs). Stratix II devices offer up to 9 Mbits of on-chip, TriMatrix™ memory for demanding, memory intensive applications and has up to 96 DSP blocks with up to 384 (18-bit × 18-bit) multipliers for efficient implementation of high performance filters and other DSP functions. Various high-speed external memory interfaces are supported, including double data rate (DDR) SDRAM and DDR2 SDRAM, RLDRAM II, quad data rate (QDR) II SRAM, and single data rate (SDR) SDRAM. Stratix II devices support various I/O standards along with support for 1-gigabit per second (Gbps) source synchronous signaling with DPA circuitry. Stratix II devices offer a complete clock management solution with internal clock frequency of up to 550 MHz and up to 12 phase-locked loops (PLLs). Stratix II devices are also the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm to protect designs.

Features

The Stratix II family offers the following features:

- 15,600 to 179,400 equivalent LEs; see Table 1–1
- New and innovative adaptive logic module (ALM), the basic building block of the Stratix II architecture, maximizes performance and resource usage efficiency
- Up to 9,383,040 RAM bits (1,172,880 bytes) available without reducing logic resources
- TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 24 clocking resources per device region
- Clock control block supports dynamic clock network enable/disable, which allows clock networks to power down to reduce power consumption in user mode
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting

- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 156 channels with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

Table 1–1. Stratix II FPGA Family Features

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) *(1)*	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs *(2)*	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
M4K RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers *(3)*	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

Notes to Table 1–1:
(1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus II software for logic synthesis.
(2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).
(3) These multipliers are implemented using the DSP blocks.

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3). All Stratix II devices support vertical migration within the same package (for example, the designer can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308 *(4)*		534 *(4)*	758	902
EP2S130 *(3)*				534 *(4)*	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as a general-purpose I/O pin. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

(4) The I/O count for this package is preliminary and is subject to change.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1–4 shows Stratix II device speed-grade offerings.

Table 1–4. Stratix II Device Speed Grades

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	-3, -4, -5		-3, -4, -5			
EP2S30	-3, -4, -5		-3, -4, -5			
EP2S60	-3, -4, -5		-3, -4, -5		-3, -4, -5	
EP2S90		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
EP2S130				-4, -5	-4, -5	-4, -5
EP2S180					-4, -5	-4, -5

2. Stratix II Architecture

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Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 400 MHz. Several M-RAM blocks are located individually in the device's logic array.

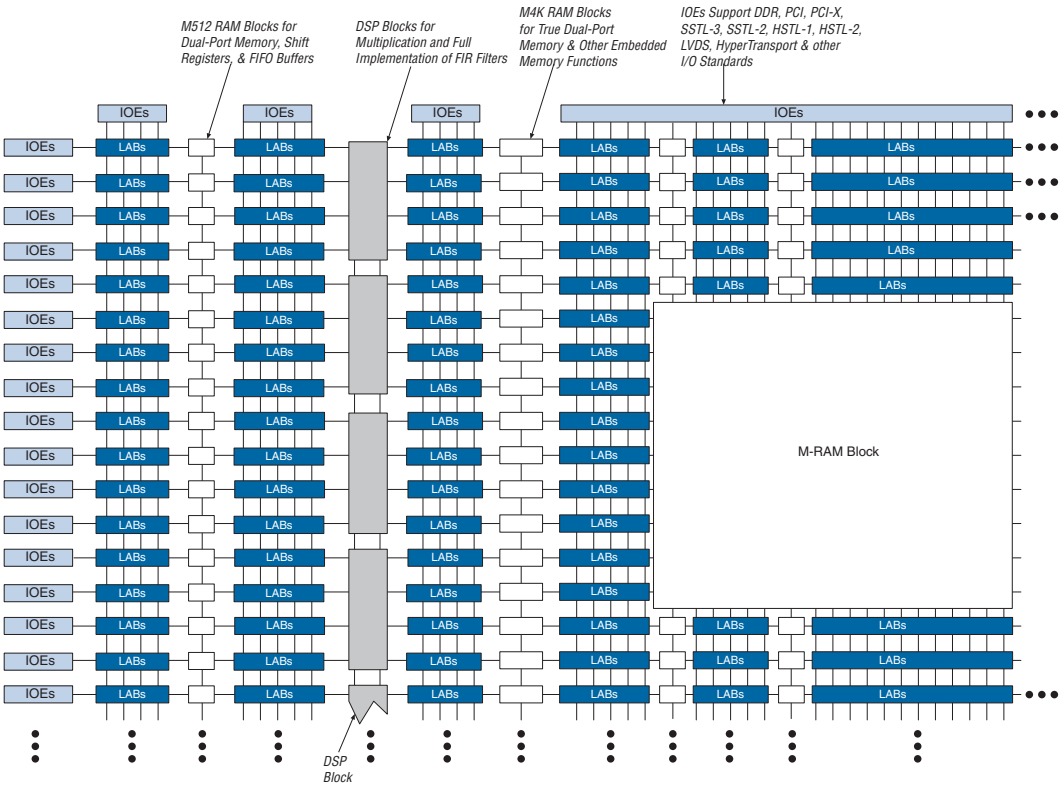
DSP blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device.

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards.

Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2–1 shows an overview of the Stratix II device.

Figure 2–1. Stratix II Block Diagram



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix II devices.

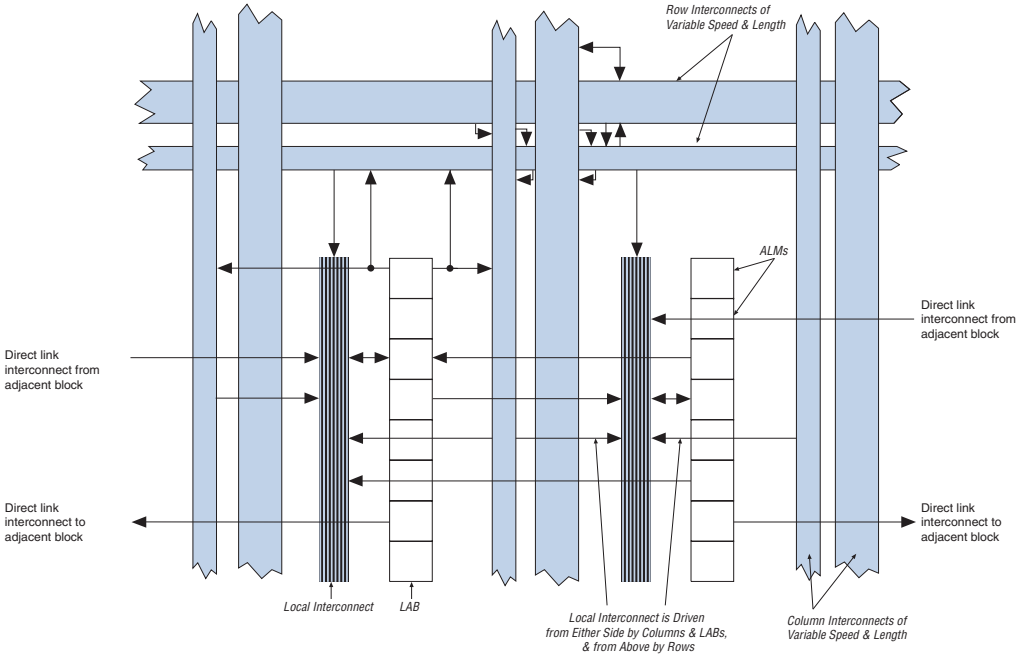
Table 2–1. Stratix II Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2S15	4 / 104	3 / 78	0	2 / 12	30	26
EP2S30	6 / 202	4 / 144	1	2 / 16	49	36
EP2S60	7 / 329	5 / 255	2	3 / 36	62	51
EP2S90	8 / 488	6 / 408	4	3 / 48	71	68
EP2S130	9 / 699	7 / 609	6	3 / 63	81	87
EP2S180	11 / 930	8 / 768	9	4 / 96	100	96

Logic Array Blocks

Each LAB consists of eight ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix II LAB structure.

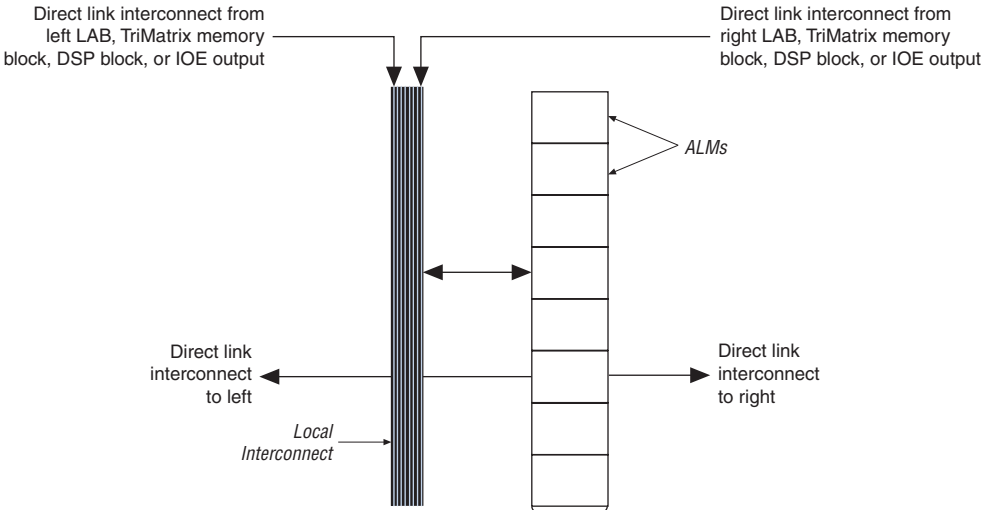
Figure 2–2. Stratix II LAB Structure



LAB Interconnects

The LAB local interconnect can drive ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



LAB Control Signals

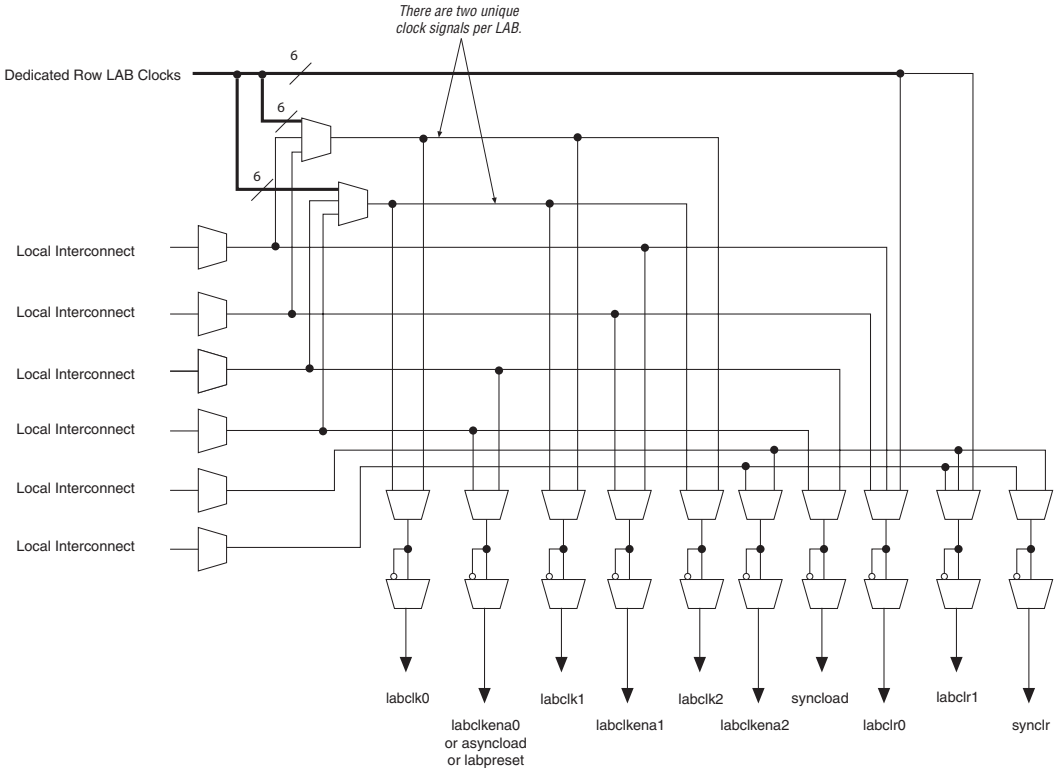
Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals. This gives a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–4. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal will turn off the corresponding LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Stratix II architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–5 shows a high-level block diagram of the Stratix II ALM while Figure 2–6 shows a detailed view of all the connections in the ALM.

Figure 2–5. High-Level Block Diagram of the Stratix II ALM

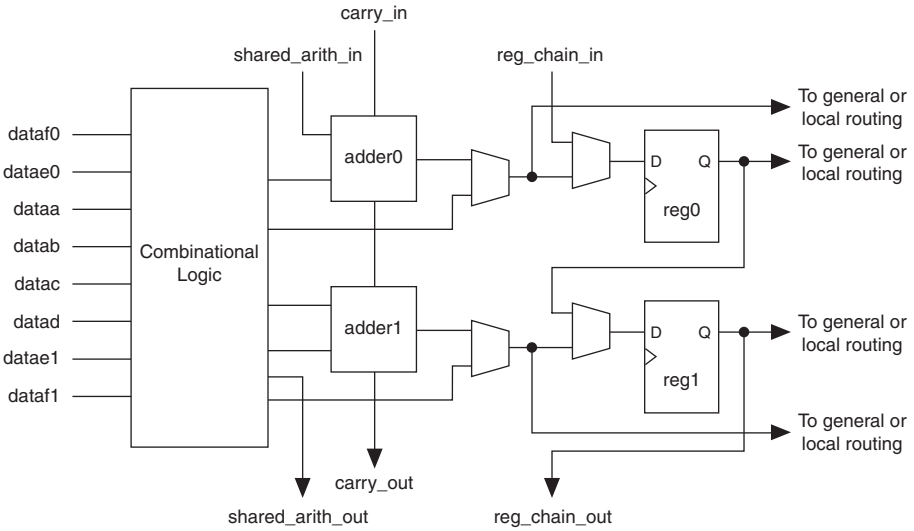
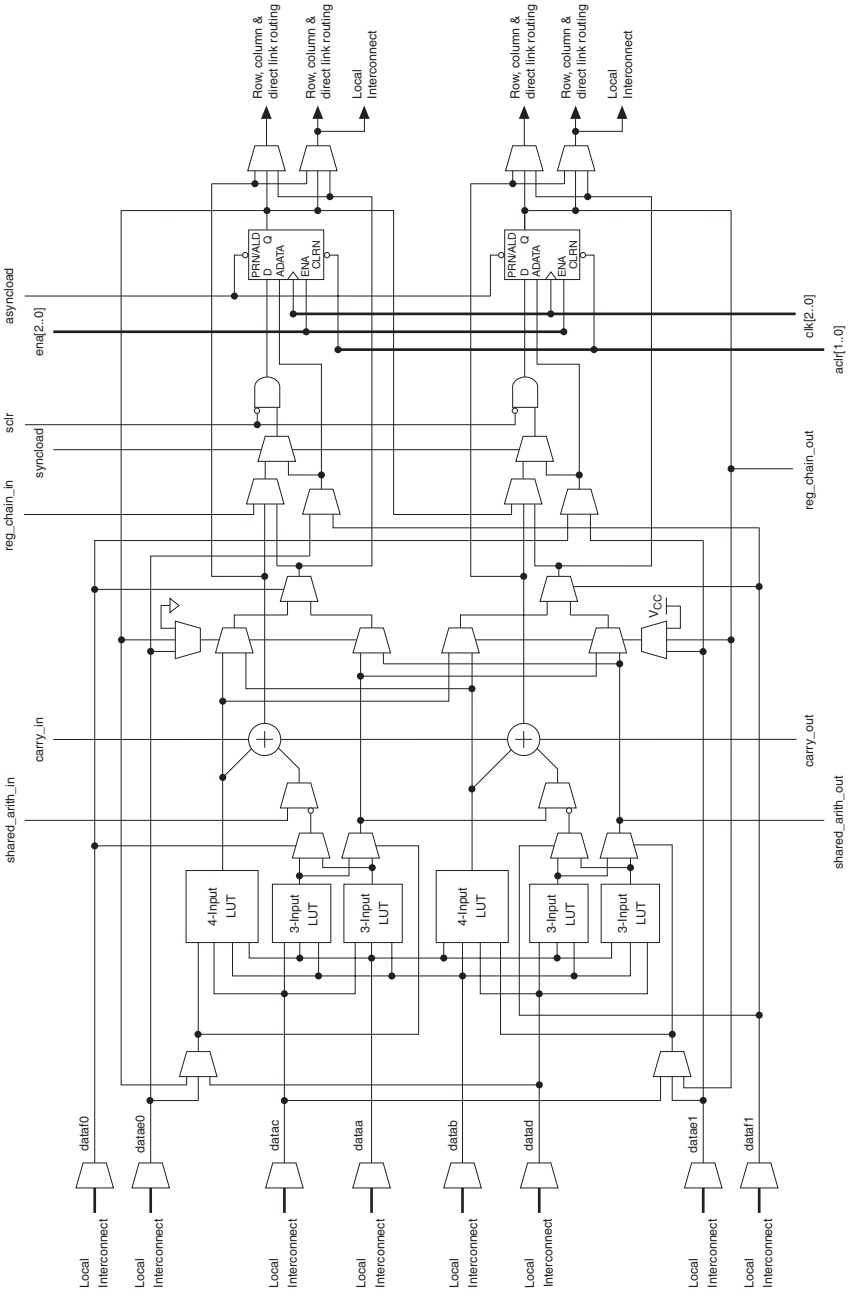


Figure 2–6. Stratix II ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM--the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection--are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

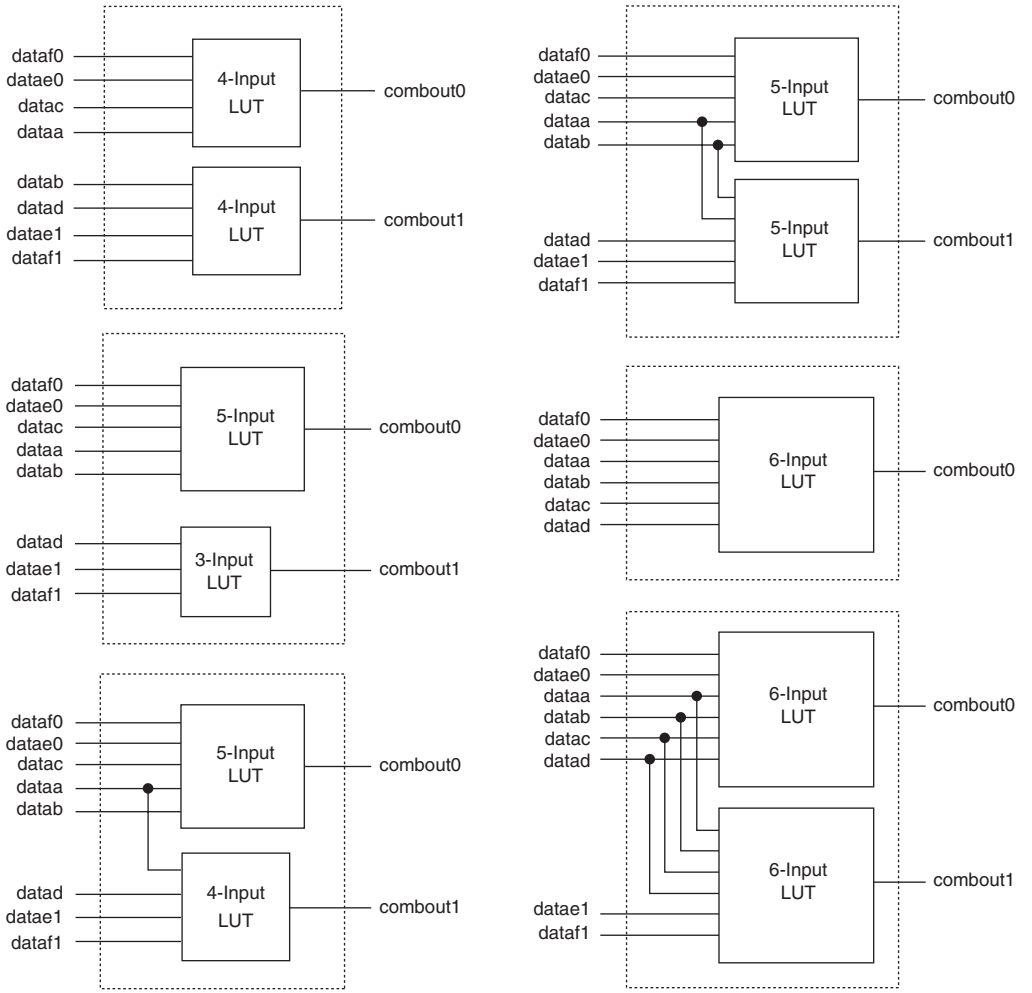
synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. See the "LAB Control Signals" section for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, the designer can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

Figure 2–7. ALM in Normal Mode *Note (1)*



Note to Figure 2–7:

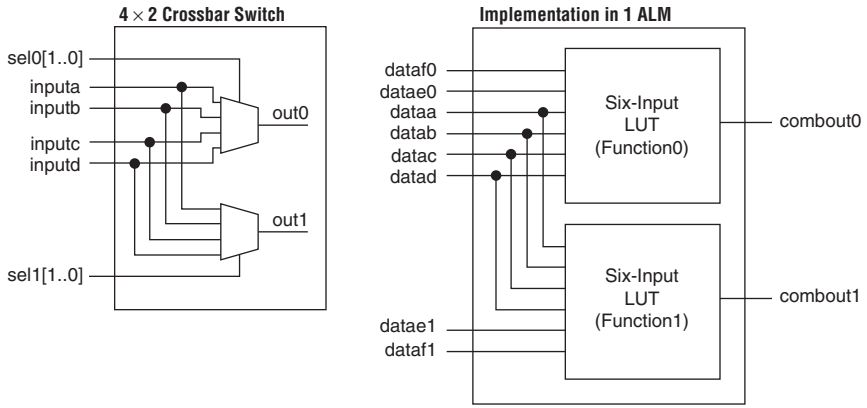
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–8. 4 × 2 Crossbar Switch Example

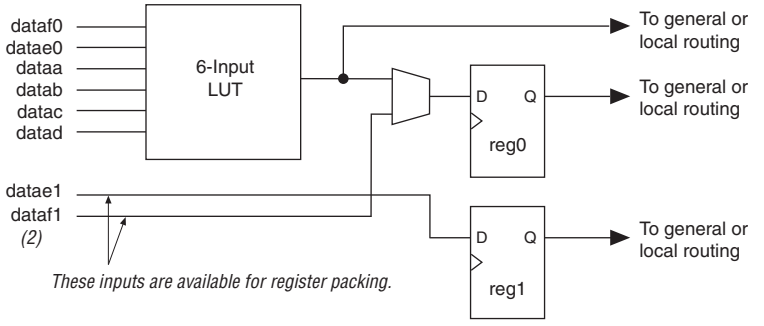


In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler will spread a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software will automatically utilize the full potential of the Stratix II ALM. The Quartus II Compiler will automatically search for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, the designer can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output will be driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If

datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–9. 6-Input Function in Normal Mode *Notes (1), (2)*



Notes to Figure 2–9:

(1) If datae1 and dataf1 are used as inputs to the six-input function, then datae0 and dataf0 are available for register packing.

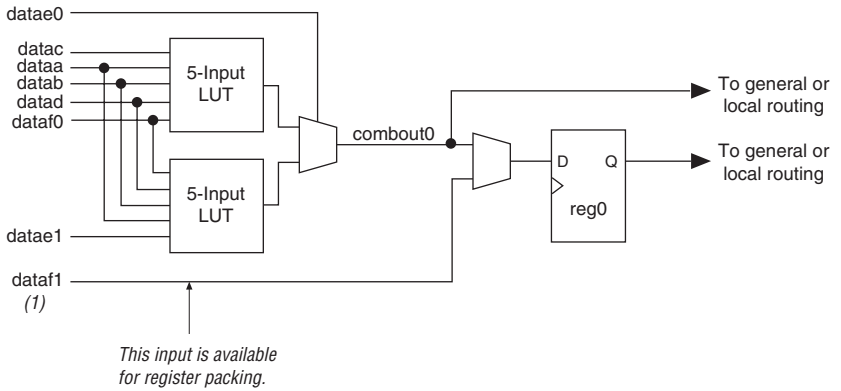
(2) The dataf1 input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–10 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing.

Functions that fit into the template shown in Figure 2–10 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode



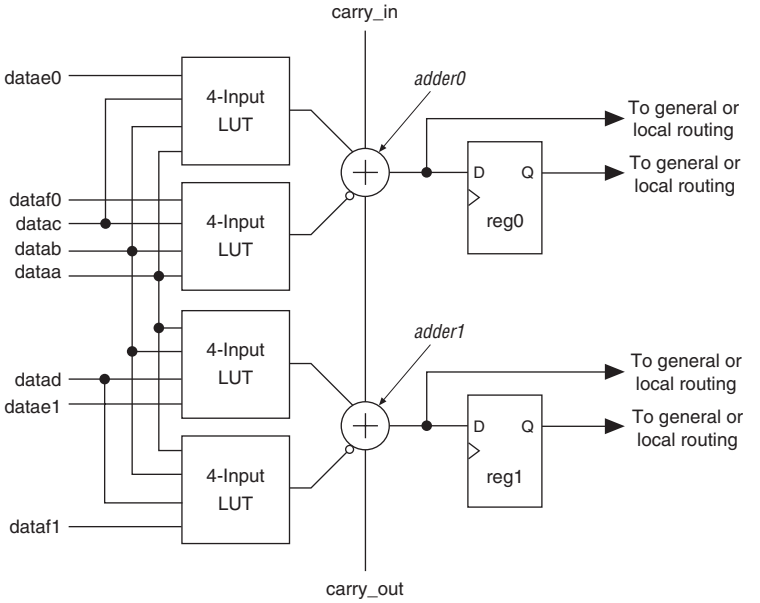
Note to Figure 2–10:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–11. ALM in Arithmetic Mode

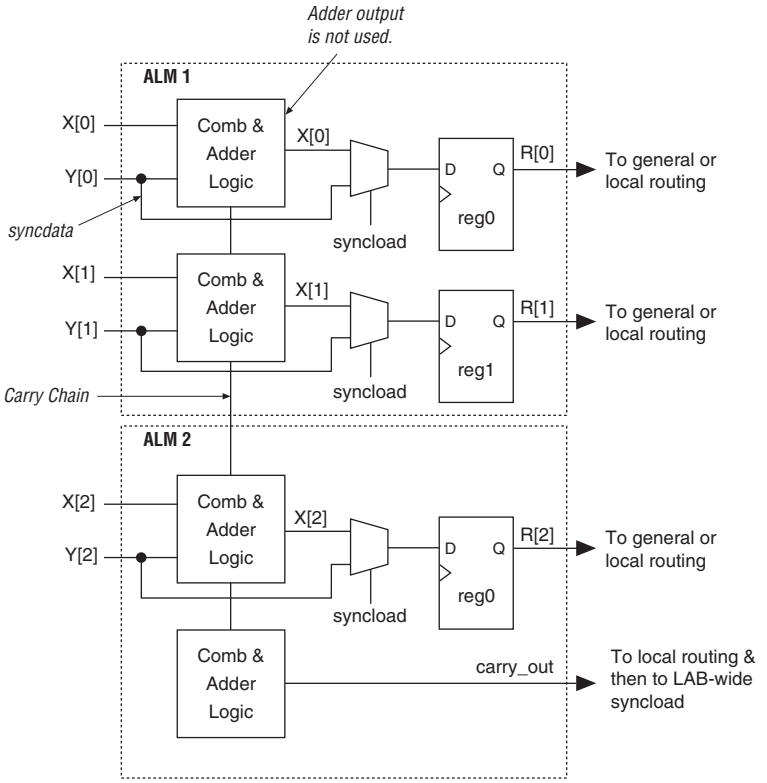


While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–12. The equation for this example is:

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X.' If 'X' is less than 'Y,' the `carry_out` signal will be '1.' The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y,' the `syncload` signal is de-asserted and 'X' drives the data port of the registers.

Figure 2–12. Conditional Operation Example



The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or the designer can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

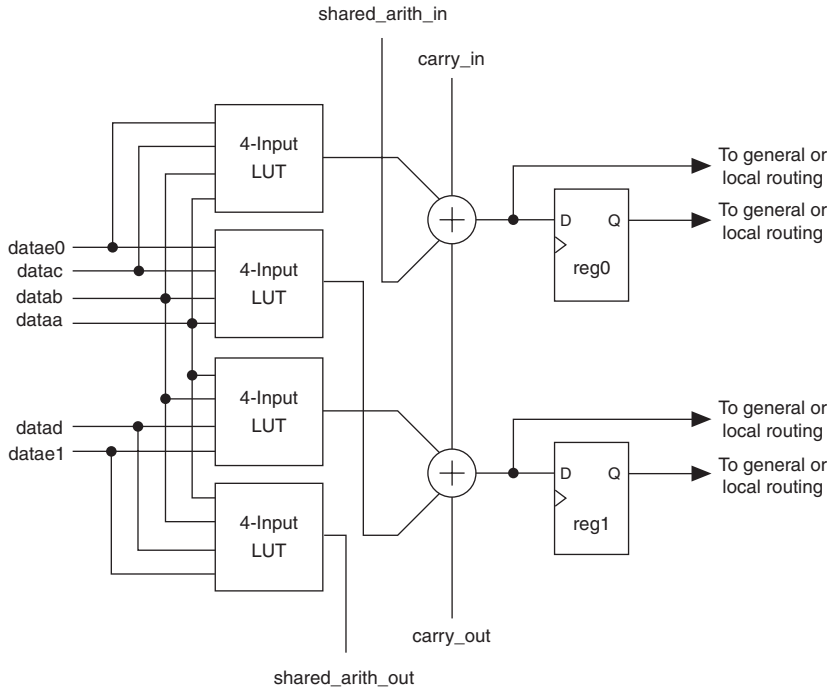
To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB will carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB will carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" section for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM in shared arithmetic mode.

Figure 2–13. ALM in Shared Arithmetic Mode

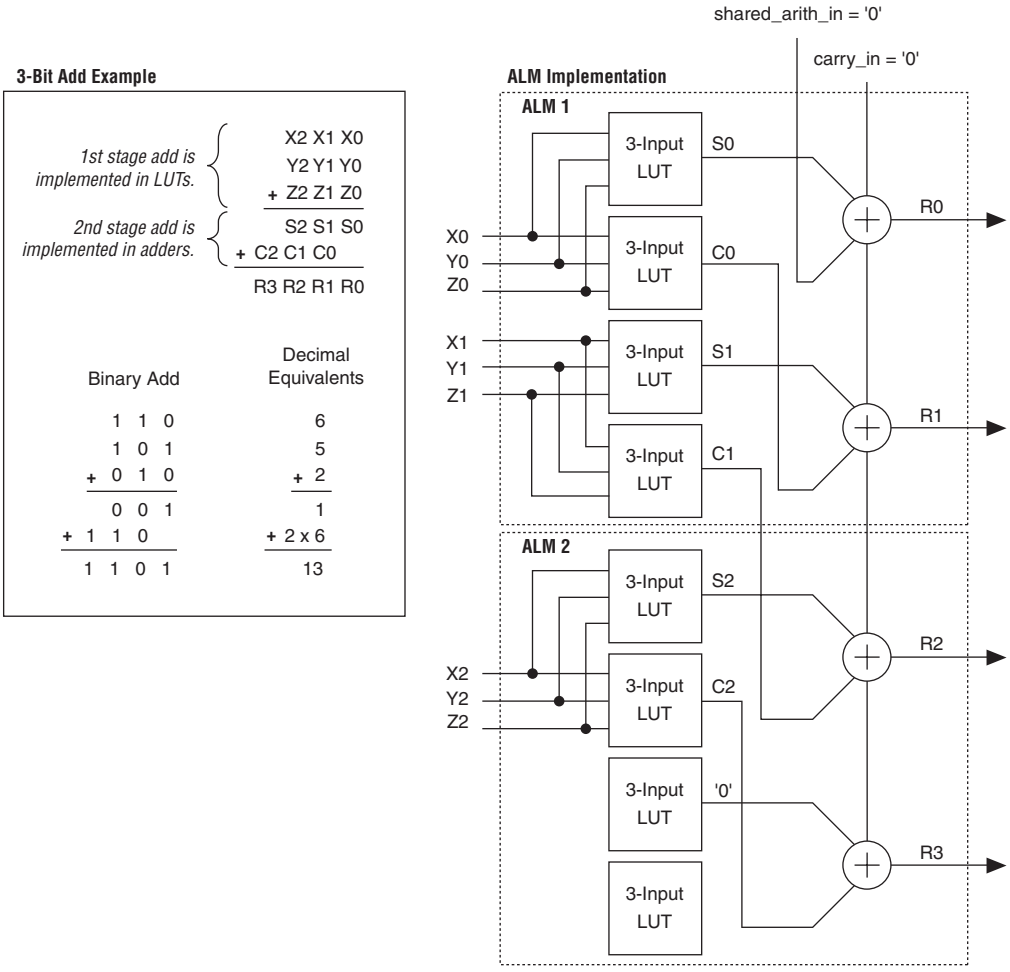


Note to Figure 2–13:
(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees can be found in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology.

An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–14. The partial sum `(S[2..0])` and the partial carry `(C[2..0])` is obtained using the LUTs, while the result `(R[2..0])` is computed using the dedicated adders.

Figure 2–14. Example of a 3-bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

In addition to the dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add. This significantly reduces the resources necessary to implement large adder trees or correlator functions.

The shared arithmetic chains can begin in either the first or fifth ALM in an LAB. The Quartus II Compiler creates shared arithmetic chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long shared

arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column.

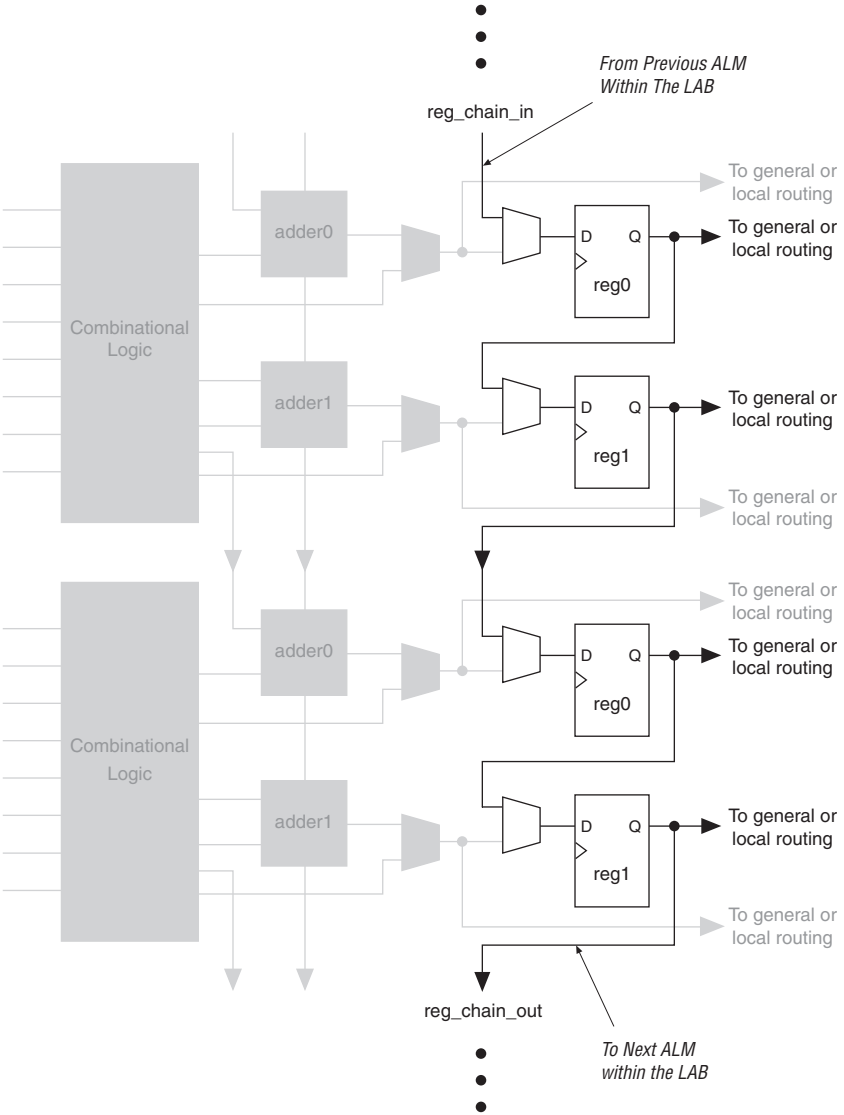
Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" section for more information on shared arithmetic chain interconnect.

Register Chain

In addition to the general routing outputs, the ALMs in an LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see Figure 2–15). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance.

Figure 2–15. Register Chain within an LAB *Note (1)*



Note to Figure 2–15:
(1) The combinational or adder logic can be utilized to implement an unrelated, un-registered function.

See the "MultiTrack Interconnect" section for more information on register chain interconnect.

Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix II devices support simultaneous asynchronous load/preset, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix II architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

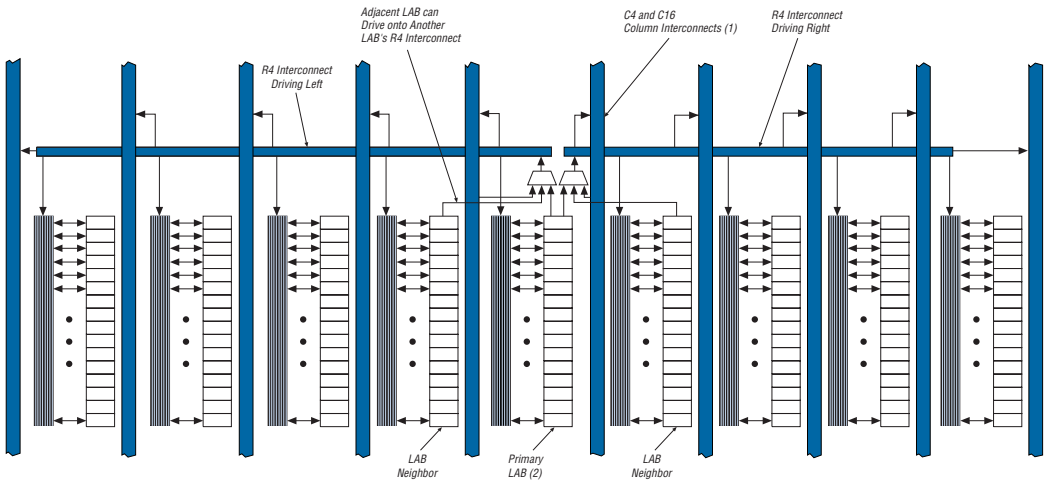
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–16 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–16. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–16:

(1) C4 and C16 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The LABs in Figure 2–16 show the 16 possible logical outputs per LAB.

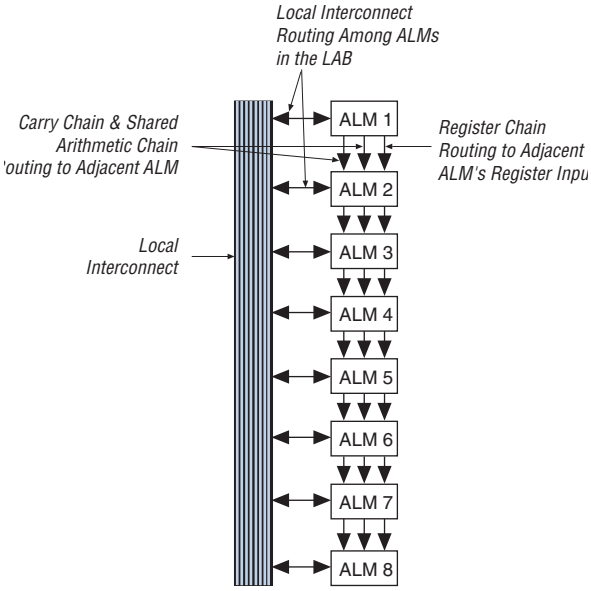
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Shared arithmetic chain interconnects in an LAB
- Carry chain interconnects in an LAB and from LAB to LAB
- Register chain interconnects in an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

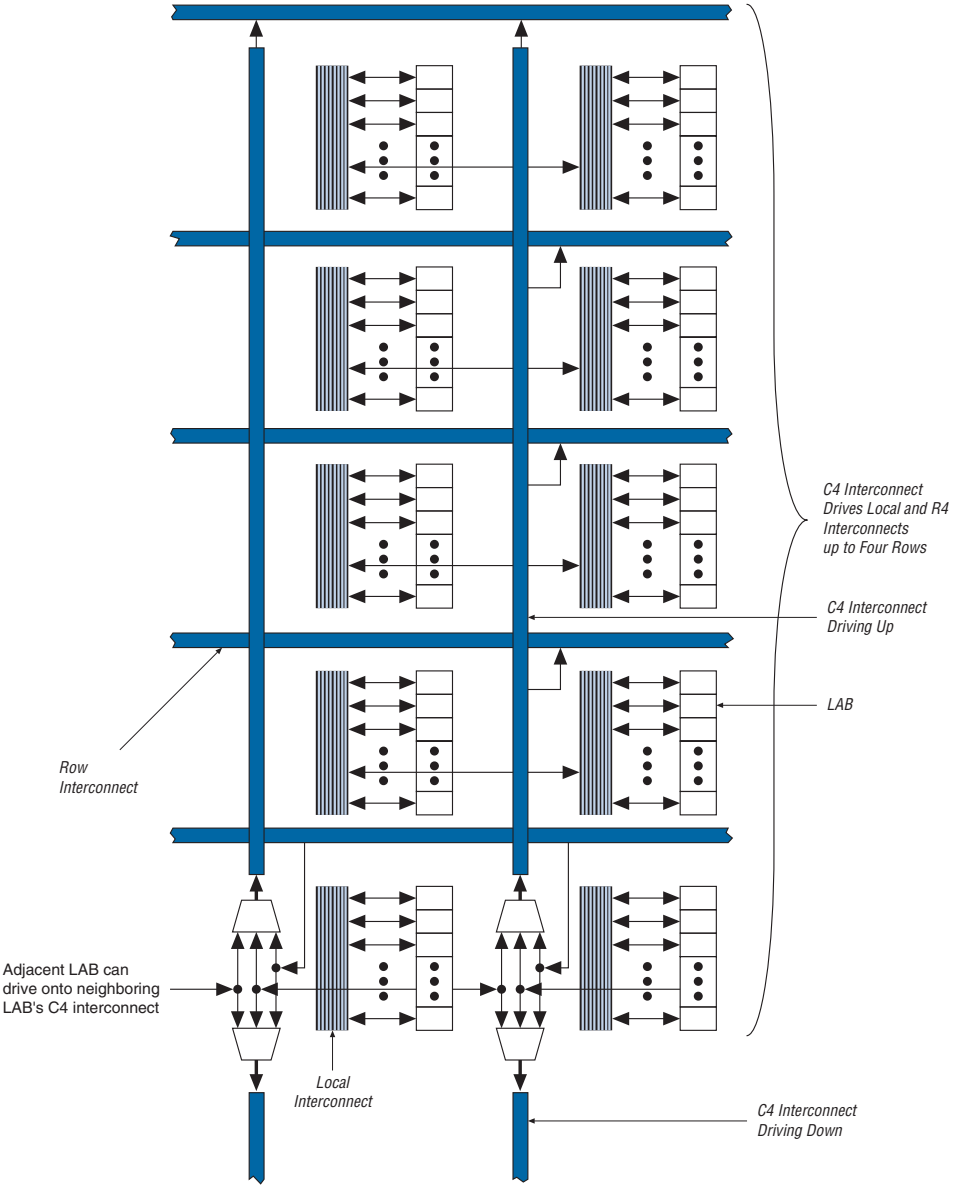
Stratix II devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM to ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–17 shows the shared arithmetic chain, carry chain and register chain interconnects.

Figure 2–17. Shared Arithmetic Chain, Carry Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–18 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–18. C4 Interconnect Connections *Note (1)*



Note to Figure 2–18:
(1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–2 shows the Stratix II device's routing scheme.

Table 2–2. Stratix II Device Routing Scheme (Part 1 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain										✓						
Carry chain										✓						
Register chain										✓						
Local interconnect										✓	✓	✓	✓	✓	✓	✓
Direct link interconnect				✓												
R4 interconnect				✓		✓	✓	✓	✓							
R24 interconnect						✓	✓	✓	✓							
C4 interconnect				✓		✓		✓								
C16 interconnect						✓	✓	✓	✓							
ALM	✓	✓	✓	✓	✓	✓		✓								
M512 RAM block				✓	✓	✓		✓								
M4K RAM block				✓	✓	✓		✓								
M-RAM block					✓	✓	✓	✓								
DSP blocks					✓	✓		✓								

Table 2–2. Stratix II Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–3 shows the size and features of the different RAM blocks.

Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. The designer can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

Table 2–3. TriMatrix Memory Features

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	400 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The six `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–19 shows the M512 RAM block control signal generation logic.

The RAM blocks in Stratix II devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–20 shows the M512 RAM block to logic array interface.

Figure 2–19. M512 RAM Block Control Signals

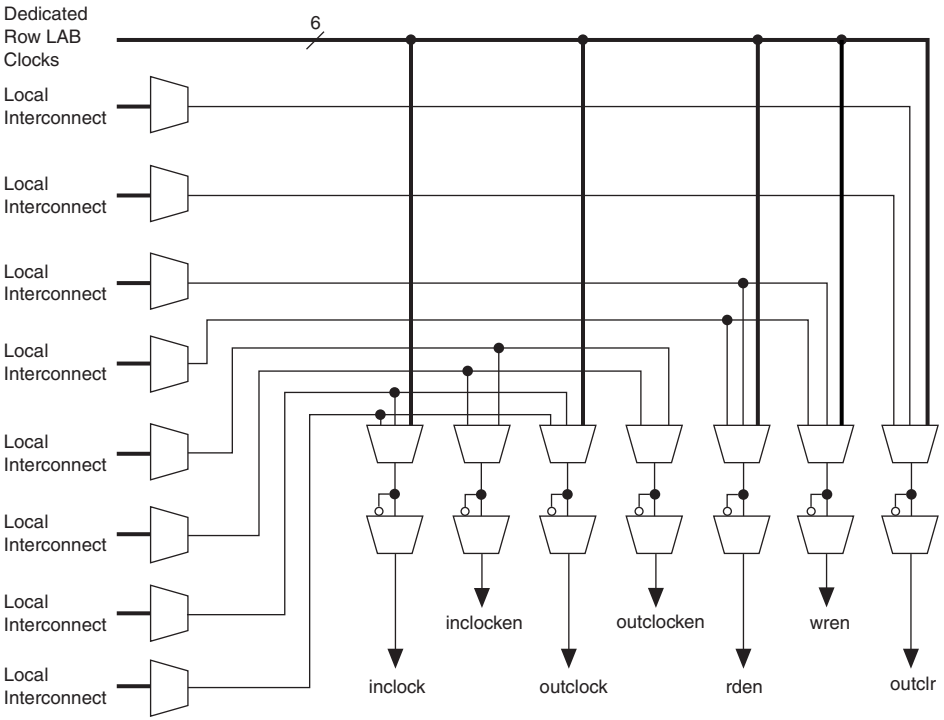
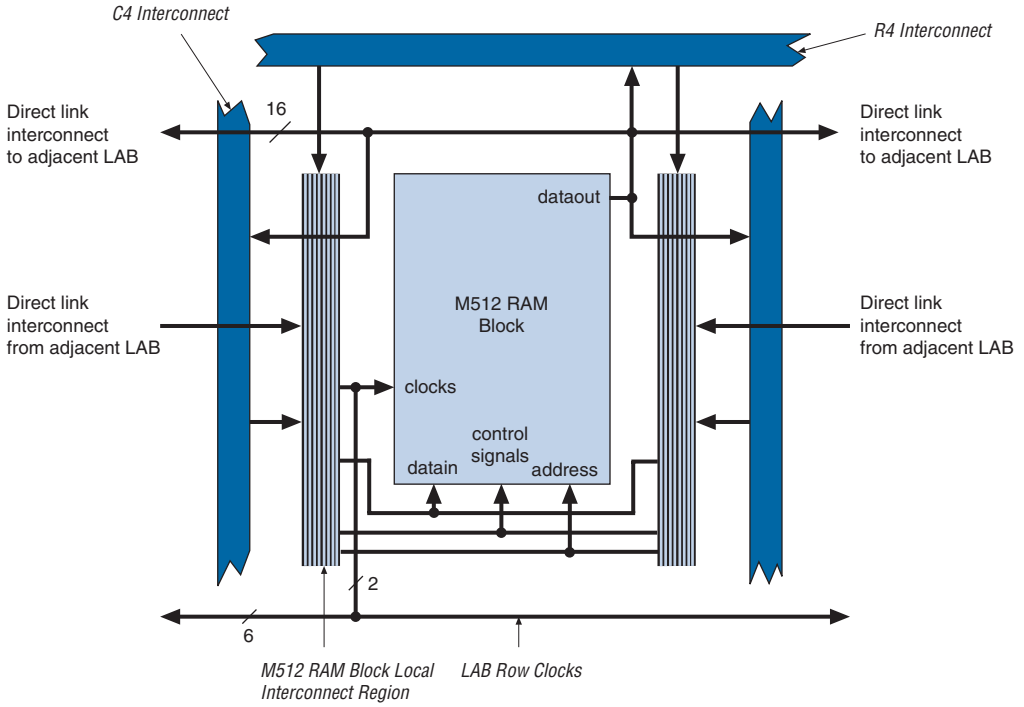


Figure 2–20. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–21.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–22 shows the M4K RAM block to logic array interface.

Figure 2–21. M4K RAM Block Control Signals

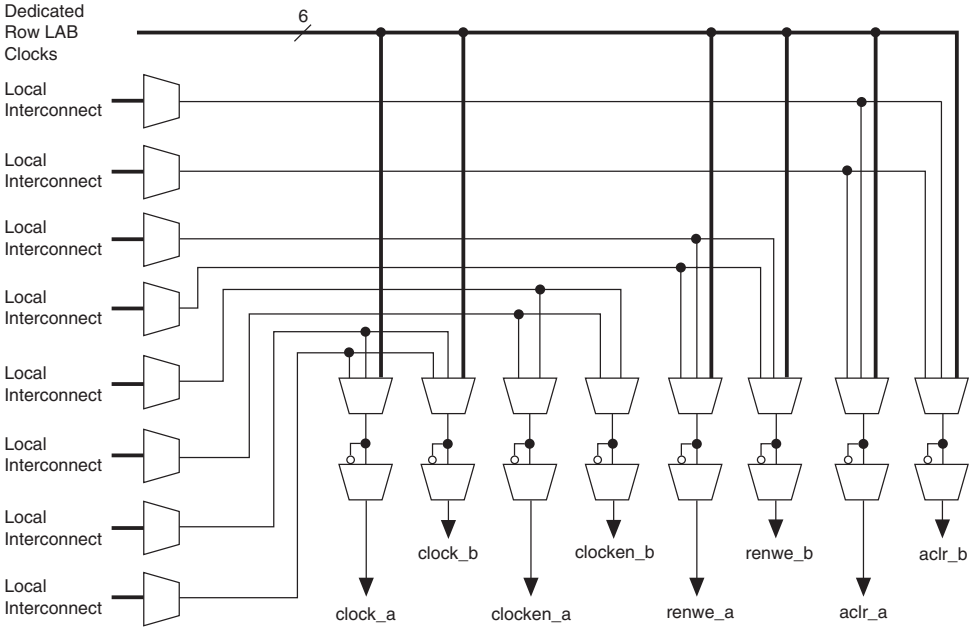
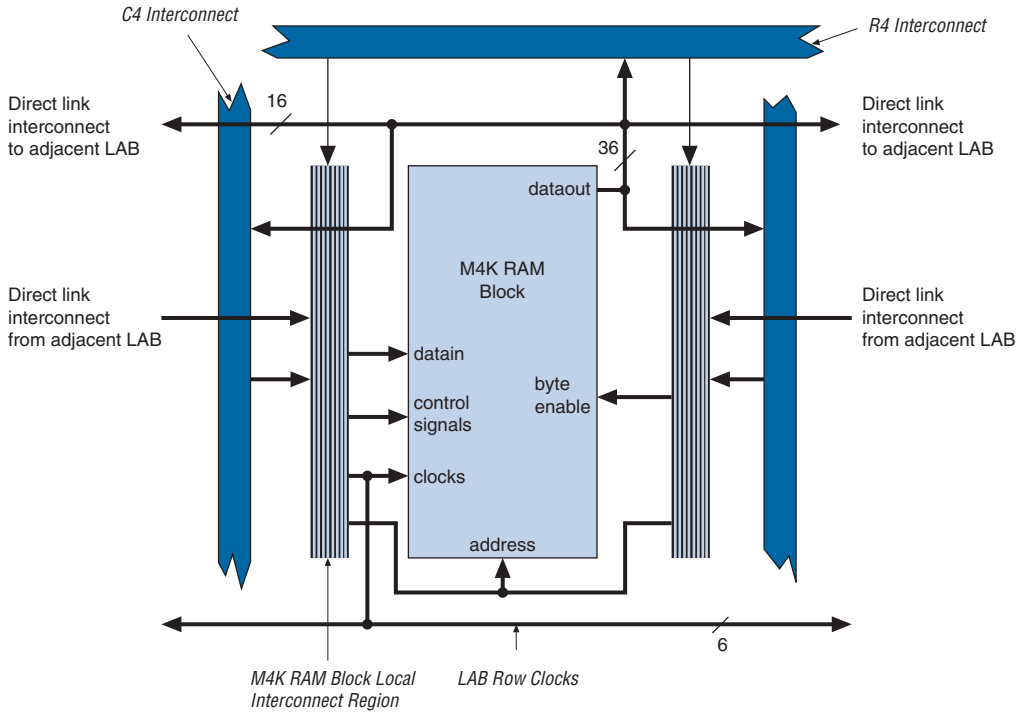


Figure 2–22. M4K RAM Block LAB Row Interface



M-RAM Block

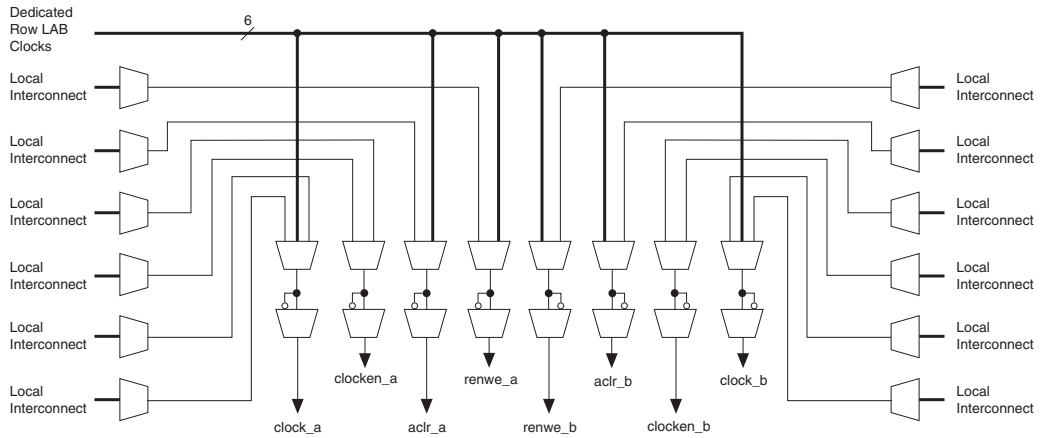
The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

The designer cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

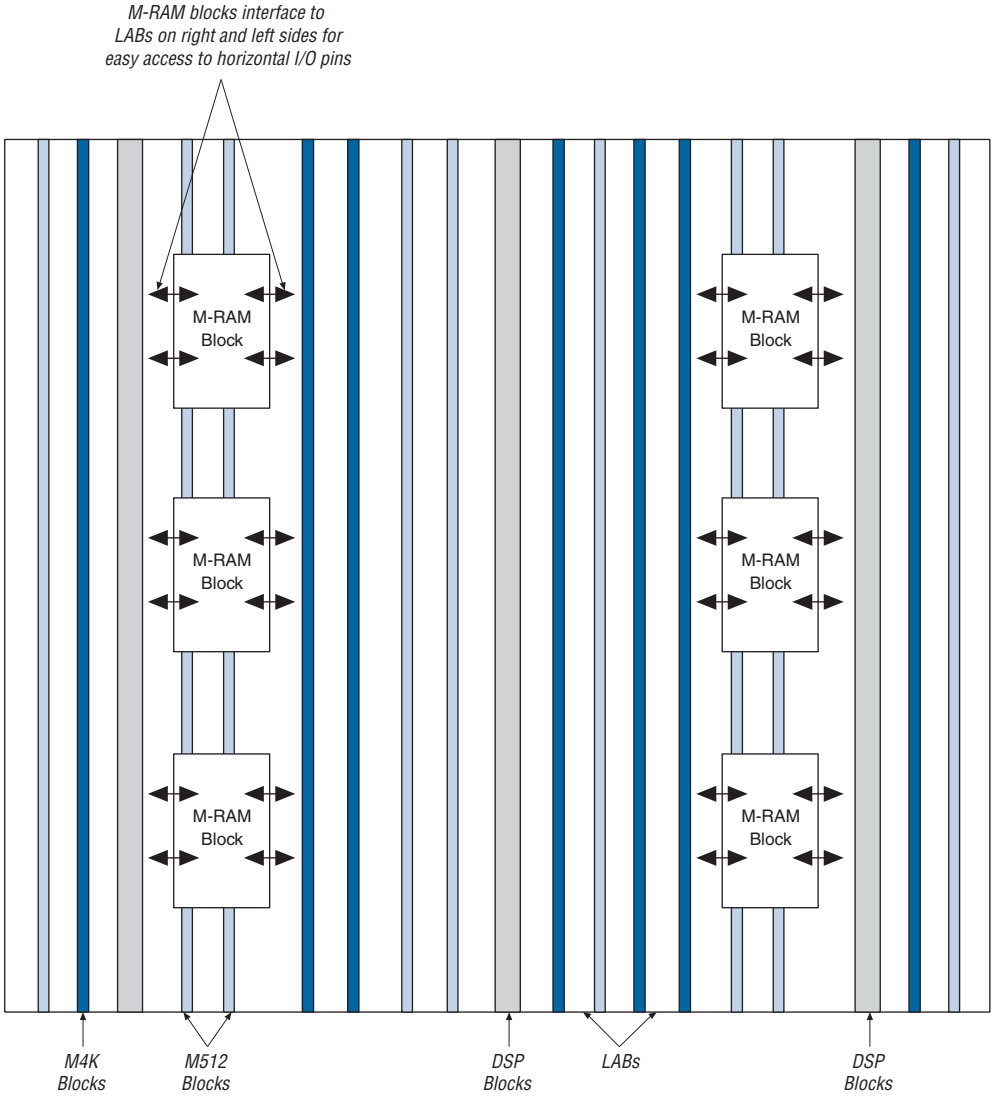
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (renwe, address, byte enable, datain, and output registers). The output register can be bypassed. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals as shown in Figure 2–23.

Figure 2–23. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–24 shows an example floorplan for the EP2S130 device and the location of the M-RAM interfaces. Figures 2–25 and 2–26 show the interface between the M-RAM block and the logic array.

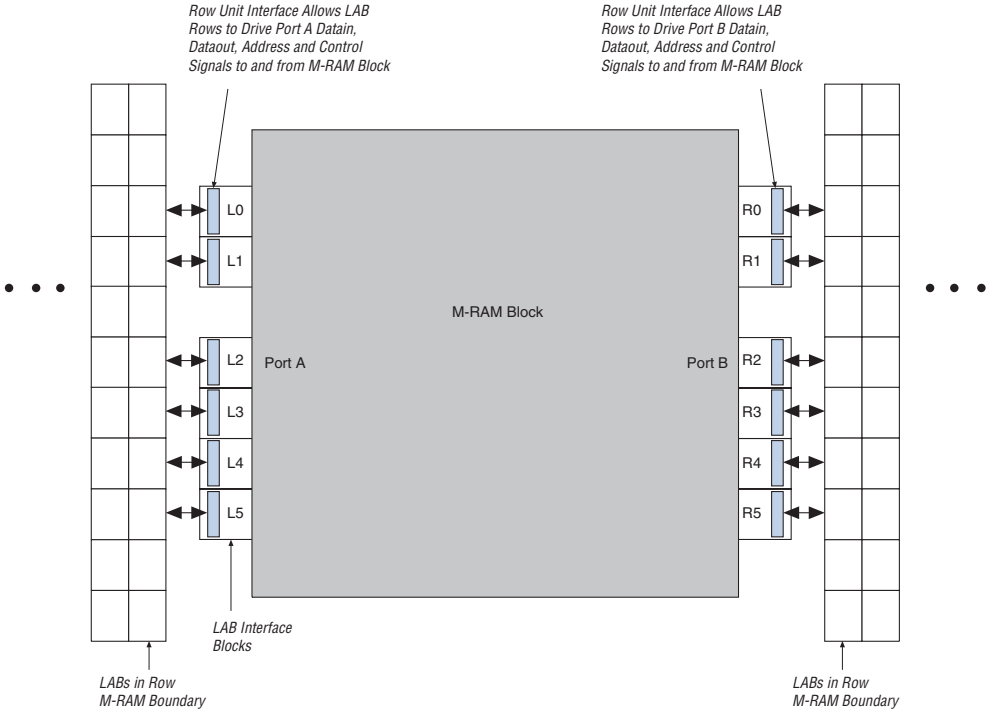
Figure 2–24. EP2S130 Device with M-RAM Interface Locations *Note (1)*



Note to Figure 2–24:

(1) The device shown is an EP2S130 device. The number and position of M-RAM blocks varies in other devices.

Figure 2–25. M-RAM Block LAB Row Interface *Note (1)*



Note to Figure 2–25:
(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Figure 2–26. M-RAM Row Unit Interface to Interconnect

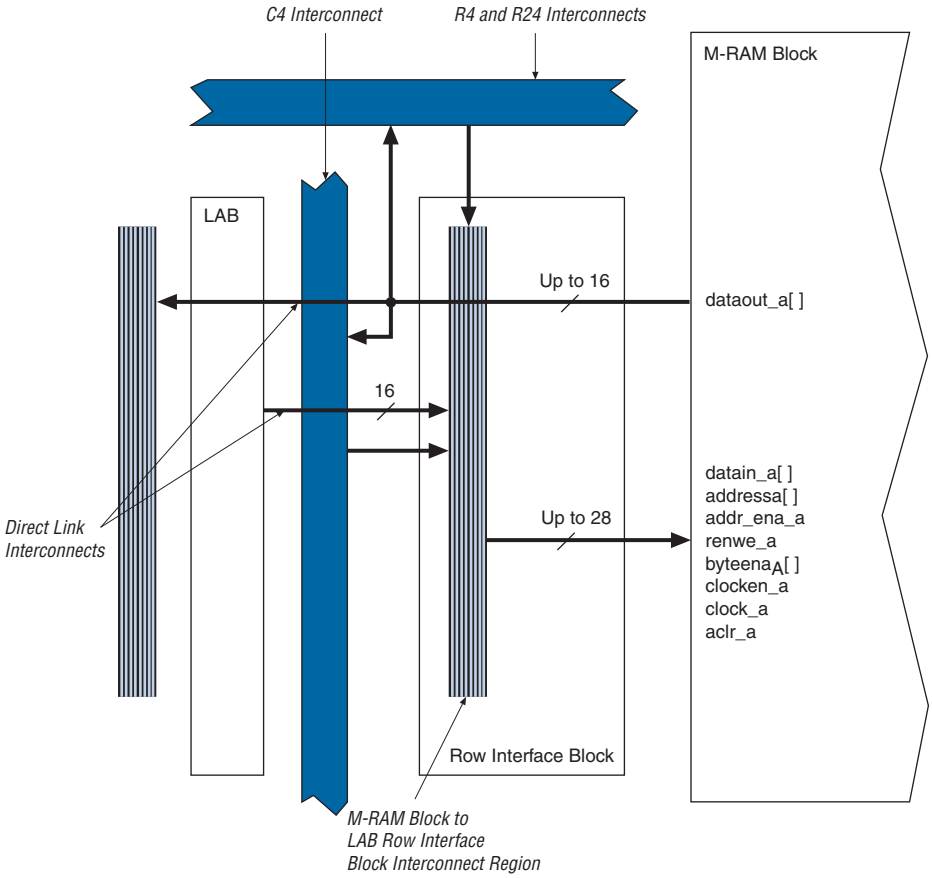


Table 2–4 shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

See the *TriMatrix Embedded Memory Blocks in Stratix II Devices* chapter in the *Stratix II Device Handbook, Volume 2* for more information on TriMatrix memory.

Table 2–4. M-RAM Row Interface Unit Signals

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

Digital Signal Processing Block

The most commonly used DSP functions are FIR filters, complex FIR filters, IIR filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II device has from two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II devices have up to 24 DSP blocks per column (see Table 2–5). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix II DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any combination of signed, unsigned, or mixed sign multiplications.

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–27 shows one of the columns with surrounding LAB rows.

Figure 2–27. DSP Blocks Arranged in Columns

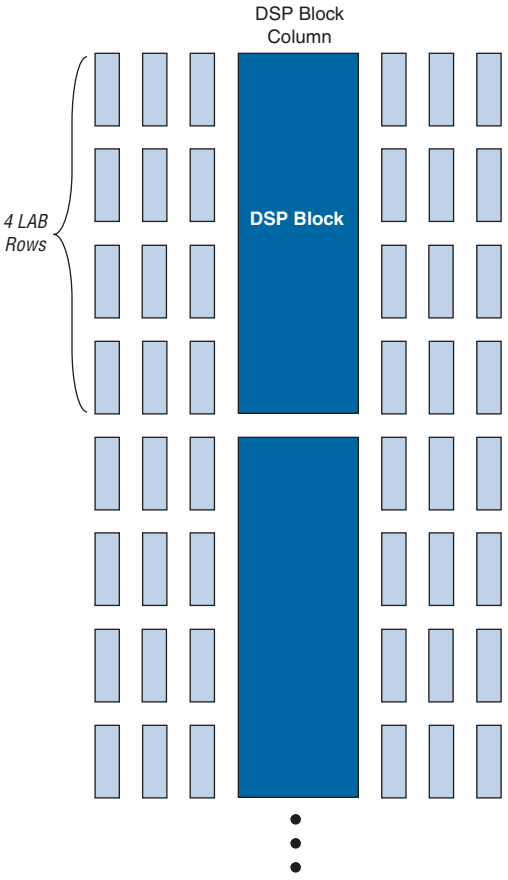


Table 2–5 shows the number of DSP blocks in each Stratix II device.

Table 2–5. DSP Blocks in Stratix II Devices *Note (1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP2S15	12	96	48	12
EP2S30	16	128	64	16
EP2S60	36	288	144	36
EP2S90	48	384	192	48
EP2S130	63	504	252	63
EP2S180	96	768	384	96

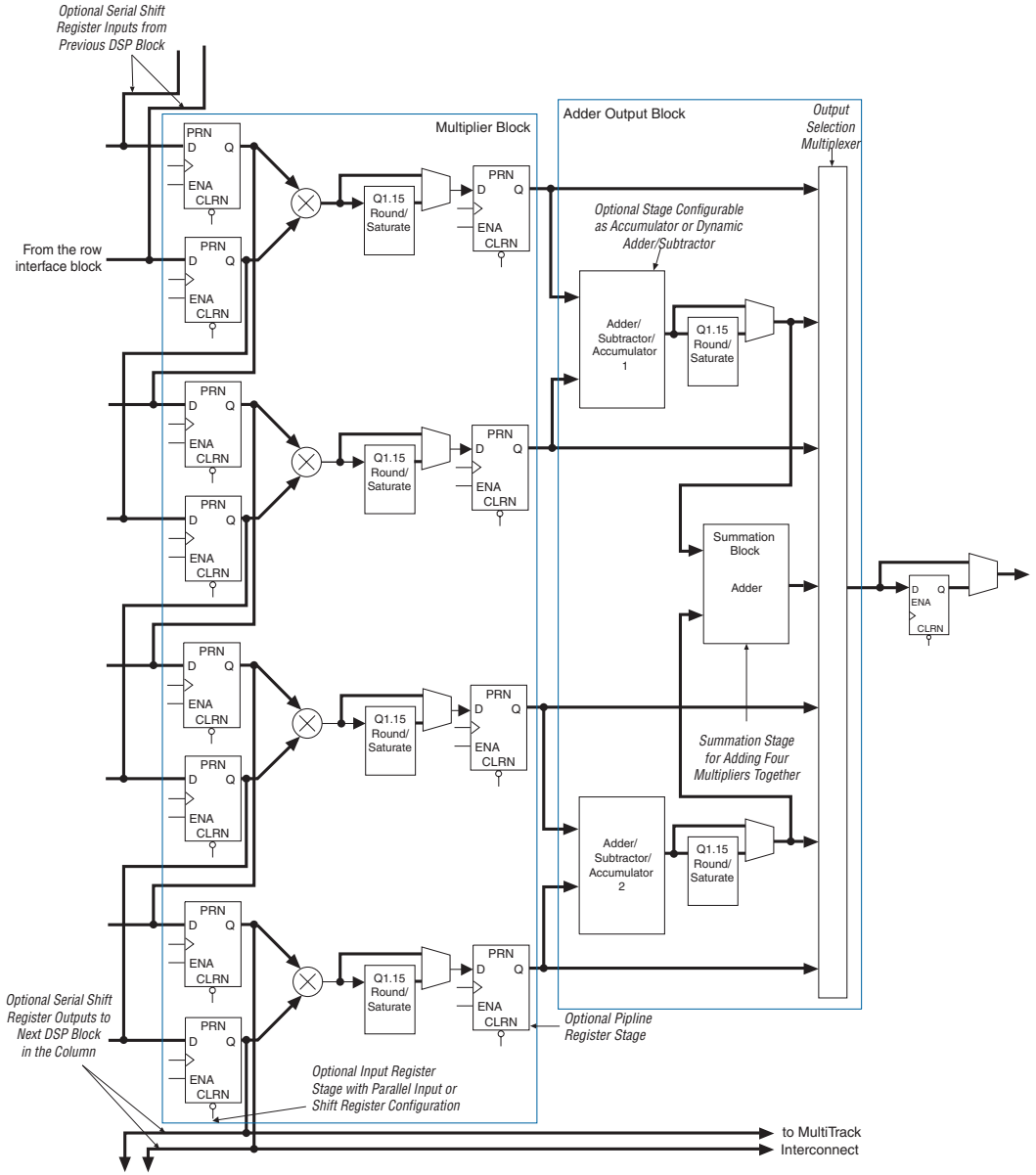
Note to Table 2–5:

(1) Each device has either the numbers of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on the configuration. This makes routing to ALMs easier, saves ALM routing resources, and increases performance, because all connections and blocks are in the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications, and DSP blocks support Q1.15 format rounding and saturation.

Figure 2–28 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration



Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–6. Multiplier Size & Configurations per DSP Block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. The designer can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2–29 and 2–30 show the DSP block interfaces to LAB rows.

Figure 2–29. DSP Block Interconnect Interface

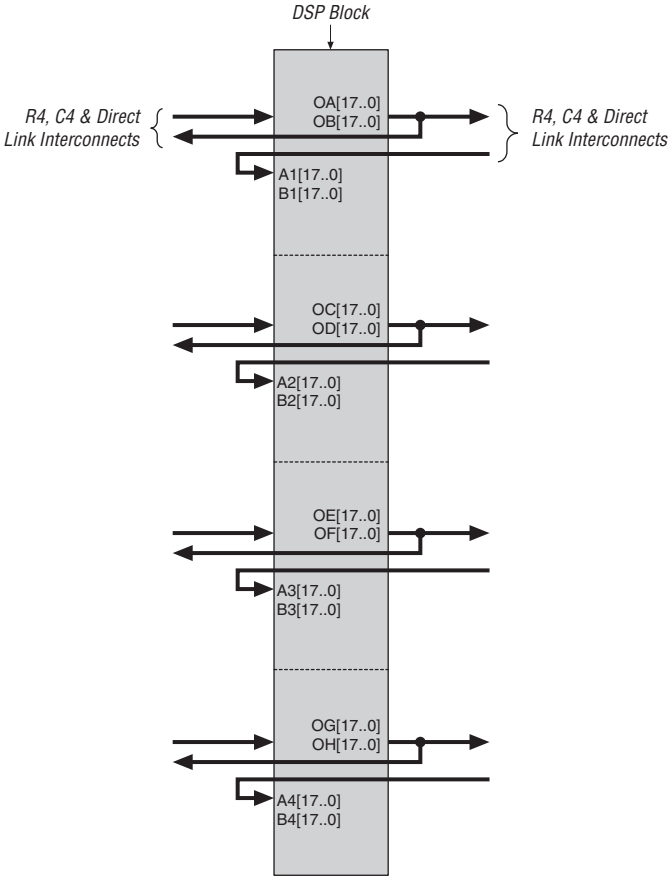
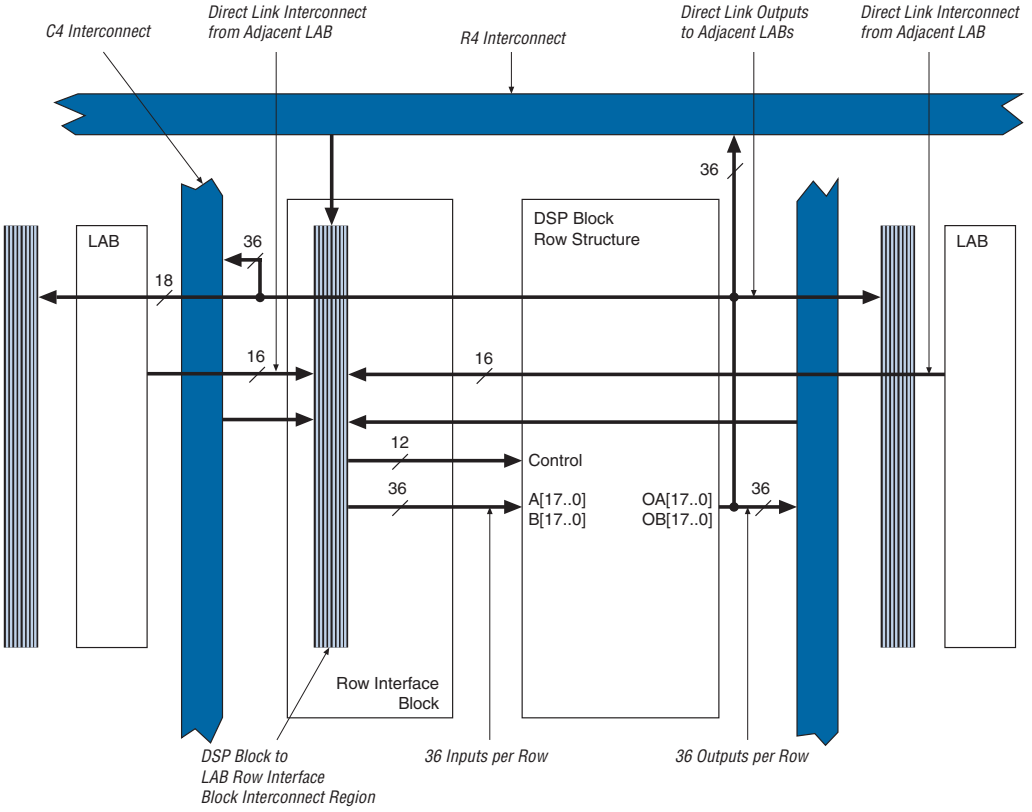


Figure 2–30. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed/unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock

signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–7.

Table 2–7. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

See the DSP Blocks in Stratix II Devices chapter in the *Stratix II Device Handbook, Volume 2* for more information on DSP blocks.

PLLs & Clock Networks

Stratix II devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

Stratix II devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II devices.

There are 16 dedicated clock pins (CLK[15..0]) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–31 and 2–32. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables/disables the clock to reduce power consumption. Table 2–8 shows global and regional clock features.

Table 2–8. Global & Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	CLK pins, PLL outputs, or internal logic	CLK pins, PLL outputs, or internal logic
Dynamic clock source selection	✓ (1)	
Dynamic enable/disable	✓	✓

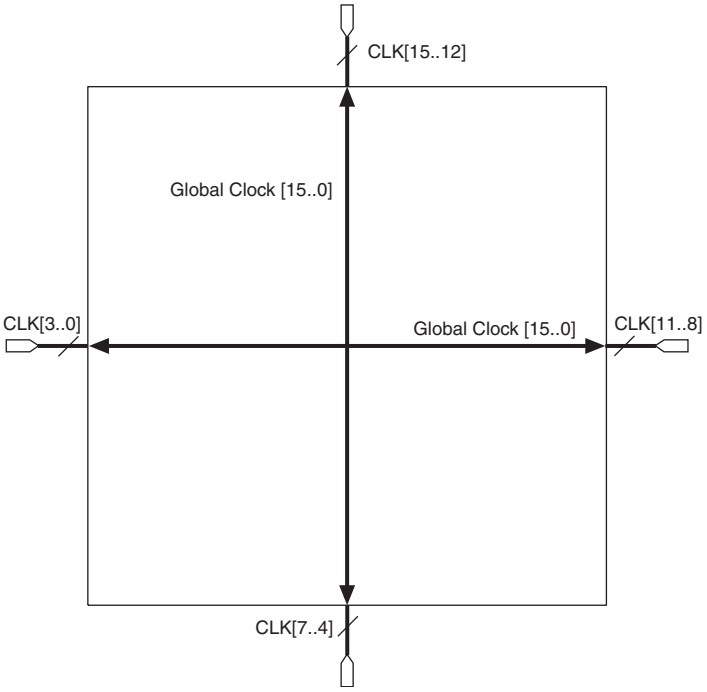
Note to Table 2–8:
(1) Dynamic source clock selection is supported for selecting between CLKp pins and PLL outputs only.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device-IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The

global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

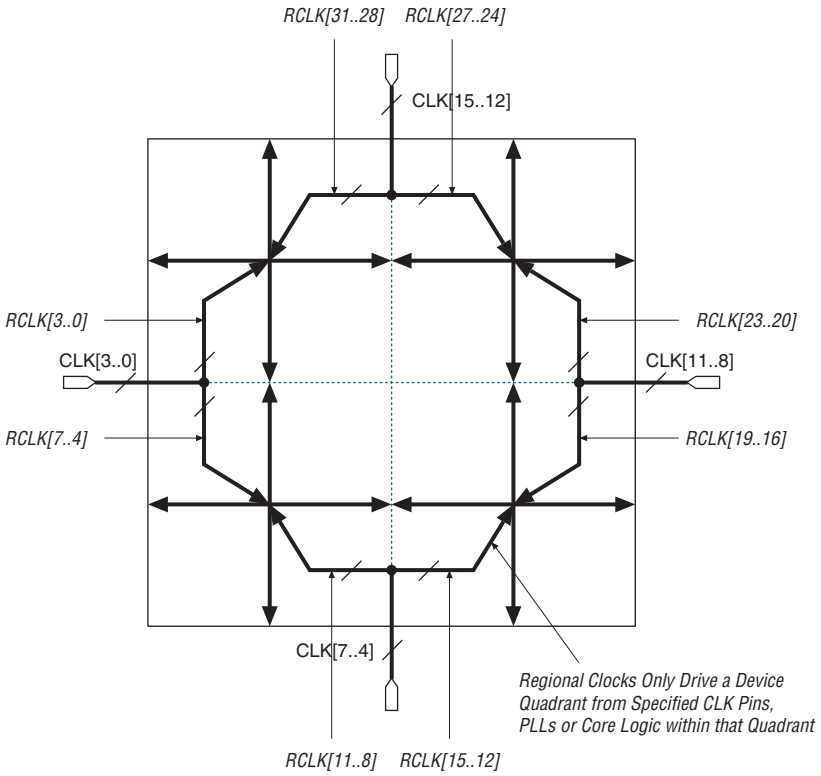
Figure 2–31. Global Clocking



Regional Clock Network

There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

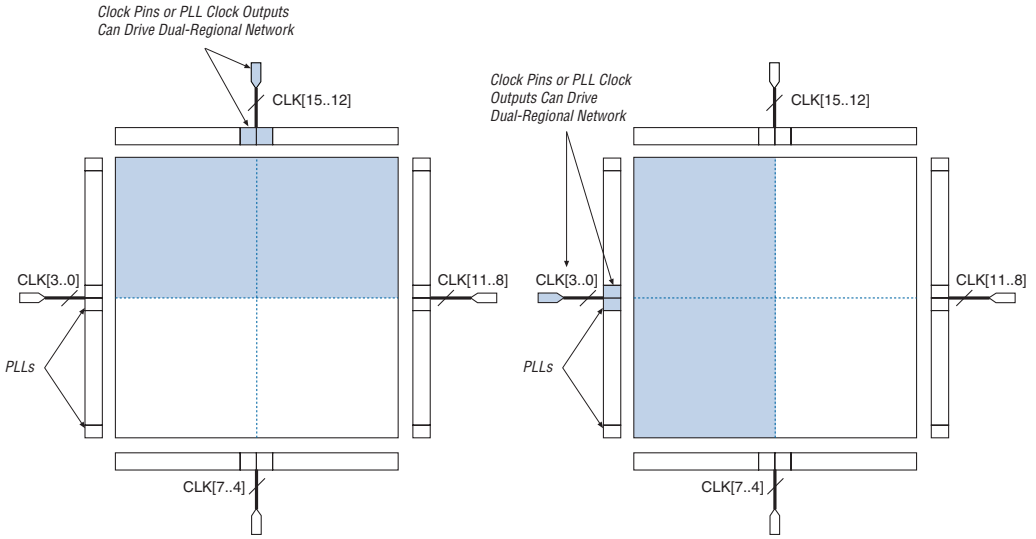
Figure 2–32. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–33. Corner PLLs cannot drive dual-regional clocks.

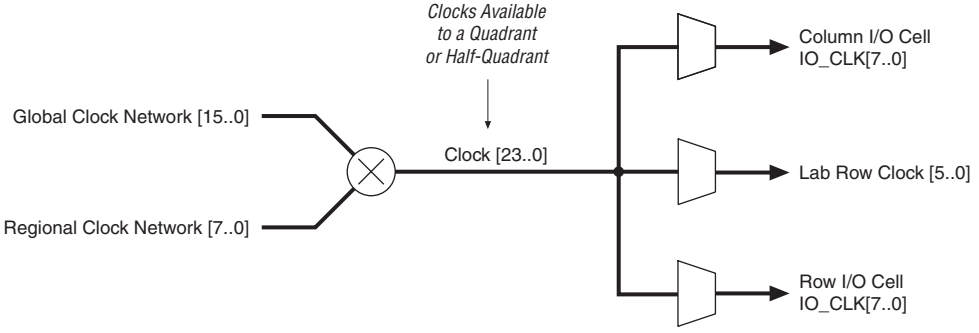
Figure 2–33. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (see Figure 2–34).

Figure 2–34. Hierarchical Clock Networks Per Quadrant



IOE clocks have row and column block regions that are clocked by eight I/O clock signals chosen from the 24 quadrant clock resources. Figures 2–35 and 2–36 show the quadrant relationship to the I/O clock regions.

Figure 2–35. EP2S15 & EP2S30 Device I/O Clock Groups

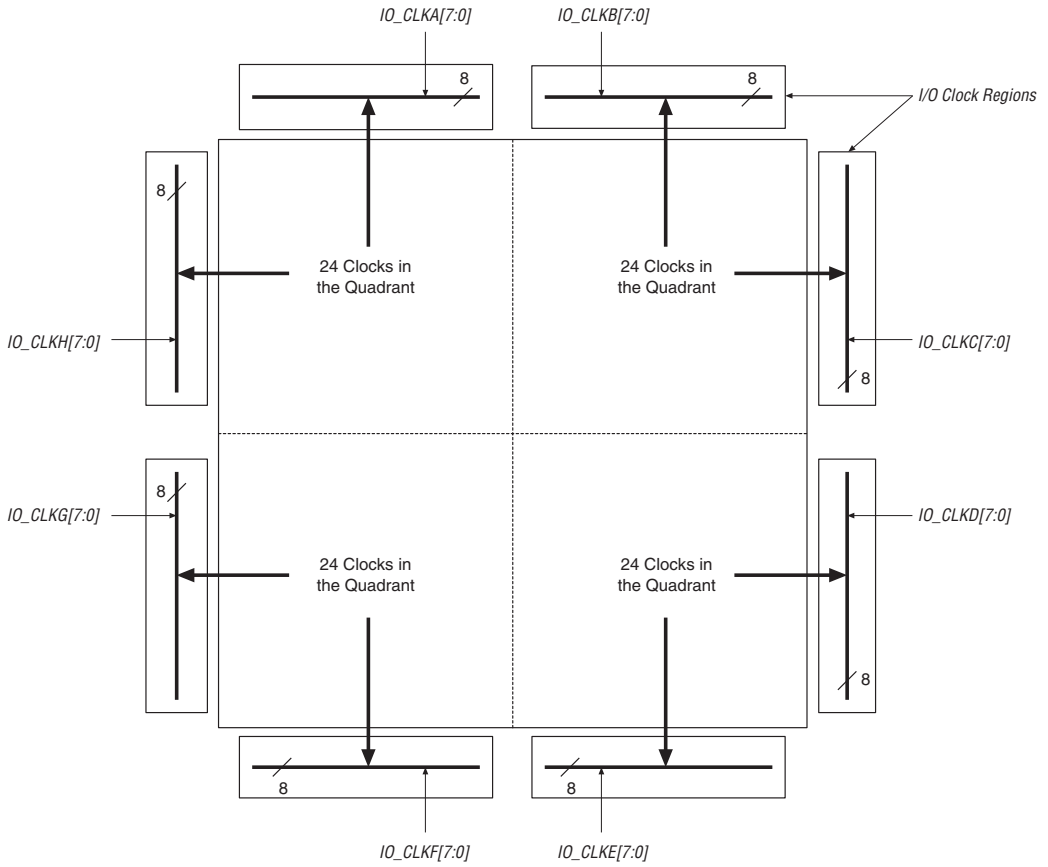
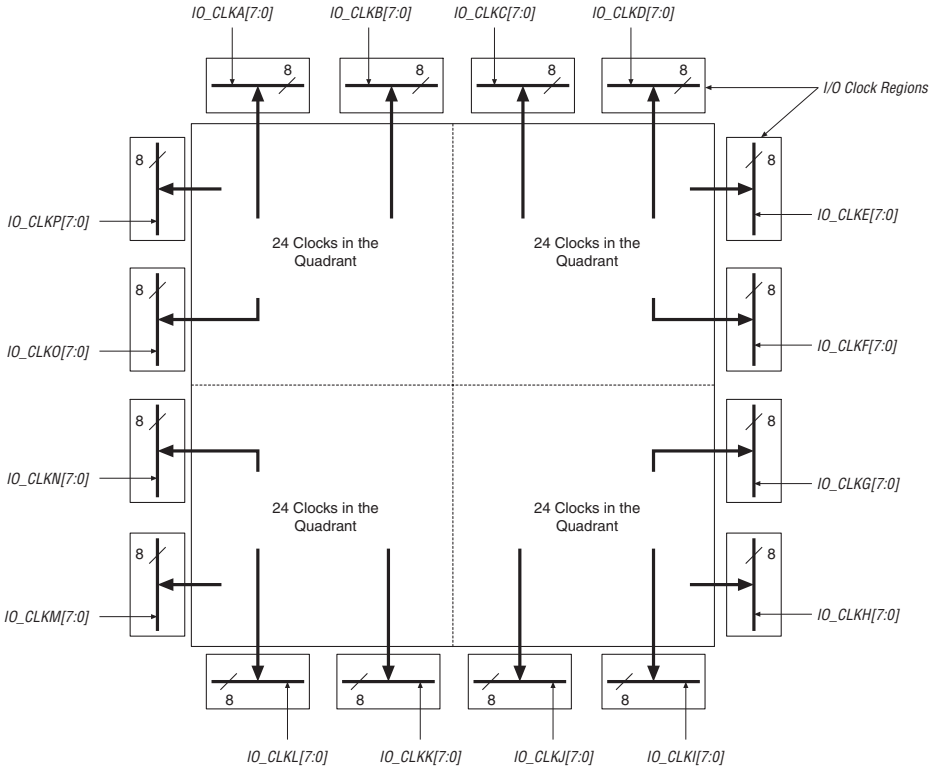


Figure 2–36. EP2S60, EP2S90, EP2S130 & EP2S180 Device I/O Clock Groups



Designers can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

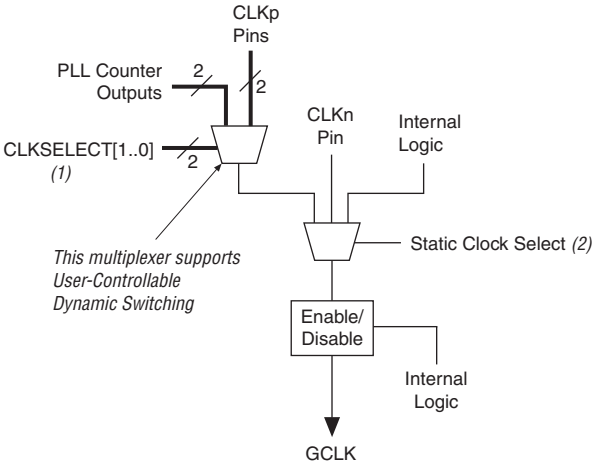
Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable/disable)

Figures 2–37 through 2–39 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–37. Global Clock Control Blocks

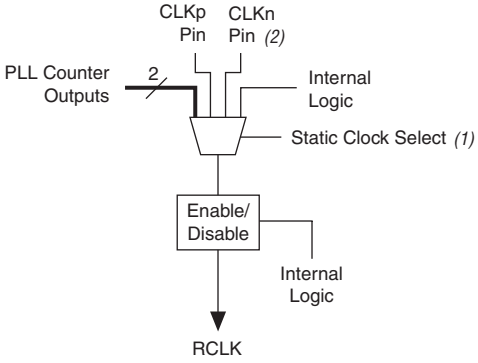


Notes to Figure 2–37:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

Figure 2–38. Regional Clock Control Blocks

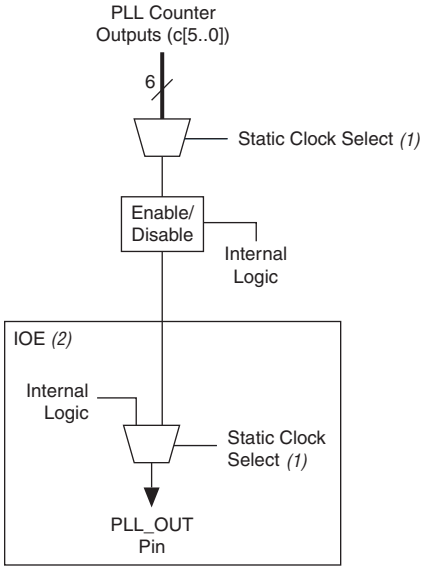


Notes to Figure 2–38:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the CLKn pins on the top and bottom of the device feed to regional clock select blocks.

Figure 2–39. External PLL Output Clock Control Blocks



Notes to Figure 2–39:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. The user has the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or the user can control the selection dynamically by using internal logic to drive the multiplexor select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexor. When selecting the clock source dynamically, the user can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 c1ock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexor can be set as the clock source.

The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on `GCLK` and `RCLK` nets and `PLL_OUT` pins. This function is independent of the PLL and is applied directly on the clock network or `PLL_OUT` pin, as shown in Figures 2–37 through 2–39.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide designers with complete control of their clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–9 shows the PLLs available for each Stratix II device and their type.

Table 2–9. Stratix II Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5	6	11	12
EP2S15	✓	✓	✓	✓					✓	✓		
EP2S30	✓	✓	✓	✓					✓	✓		
EP2S60 *(1)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S90 *(2)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S130 *(3)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–9:

(1) EP2S60 devices in the 1020-pin package contain 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

(2) EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLS 1–4 and enhanced PLLs 5 and 6.

(3) EP2S130 devices in the 1020-pin and 1508-pin packages contain 12PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

Table 2–10 shows the enhanced PLL and fast PLL features in Stratix II devices.

Table 2–10. Stratix II PLL Features

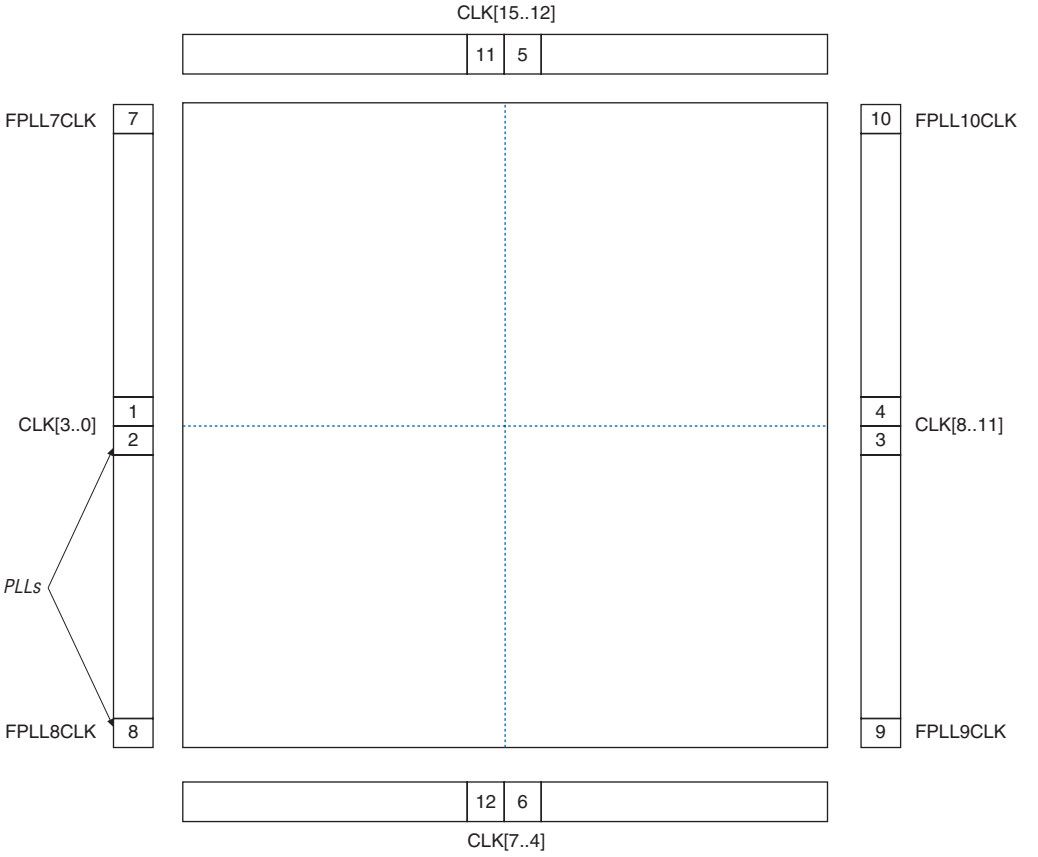
Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	

Notes to Table 2–10:

(1) For enhanced PLLs, m, n, range from 1 to 512 and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate txclkout.
(7) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.
(8) Every Stratix II device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

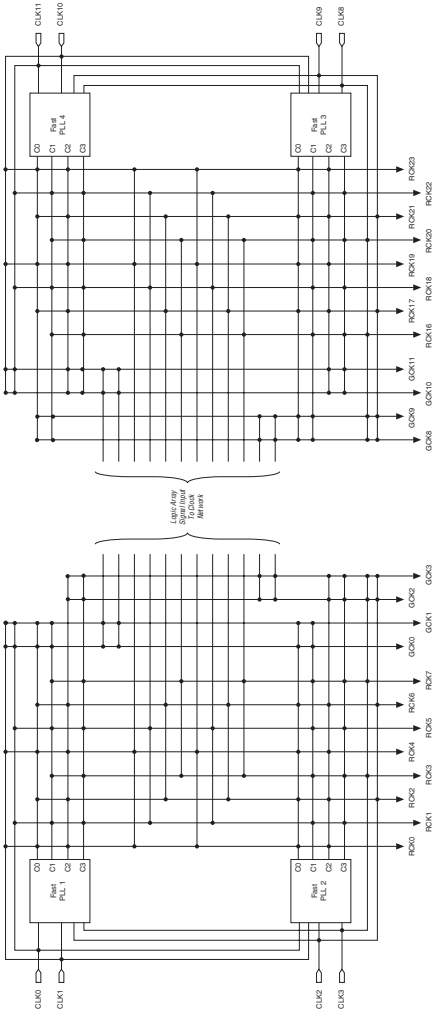
Figure 2–40 shows a top-level diagram of the Stratix II device and PLL floorplan.

Figure 2–40. PLL Locations



Figures 2–41 and 2–42 shows the global and regional clocking from the fast PLL outputs and the side clock pins. The connections to the global and regional clocks from the fast PLL outputs, internal drivers, and the CLK pins on the left and right sides of the device are shown in table format in Tables 2–11 and 2–12, respectively.

Figure 2–41. Global & Regional Clock Connections from Center Clock Pins & Fast PLL Outputs *Note (1)*

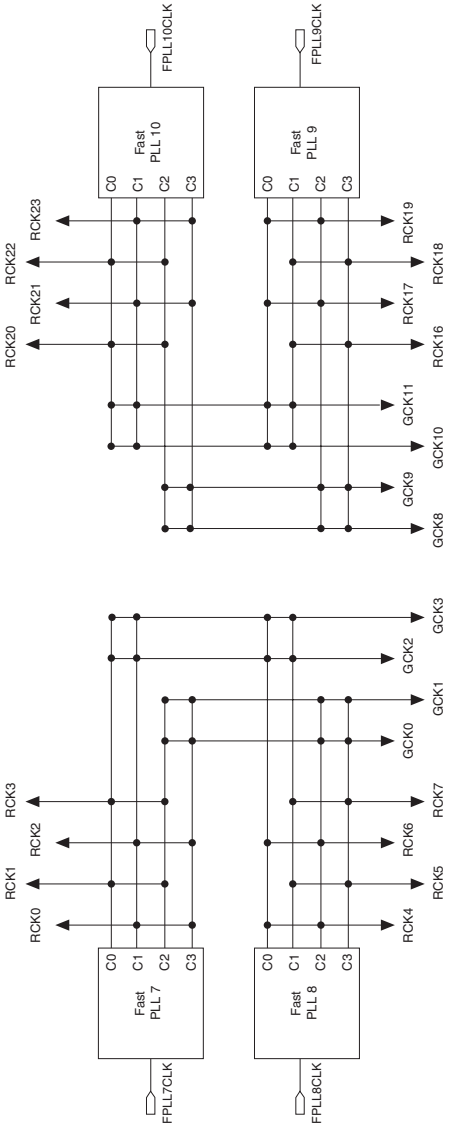


Notes to Figure 2–41:

(1) EP2S15 and EP2S30 devices only have four fast PLLs (1, 2, 3, and 4), but the connectivity from these four PLLs to the global and regional clock networks remains the same as shown.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Figure 2–42. Global & Regional Clock Connections from Corner Clock Pins & Fast PLL Outputs *Note (1)*



Note to Figure 2–42:

(1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input to the fast PLL can be driven from another PLL, a pin-driven global or regional clock, or internally generated global signals.

Table 2–11. Global & Regional Clock Connections from Left Side Clock Pins & Fast PLL Outputs (Part 1 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Clock pins												
CLK0p	✓	✓			✓				✓			
CLK1p	✓	✓				✓				✓		
CLK2p			✓	✓			✓				✓	
CLK3p			✓	✓				✓				✓
Drivers from internal logic												
GCLKDRV0	✓	✓										
GCLKDRV1	✓	✓										
GCLKDRV2			✓	✓								
GCLKDRV3			✓	✓								
RCLKDRV0					✓				✓			
RCLKDRV1						✓				✓		
RCLKDRV2							✓				✓	
RCLKDRV3								✓				✓
RCLKDRV4					✓				✓			
RCLKDRV5						✓				✓		
RCLKDRV6							✓				✓	
RCLKDRV7								✓				✓
PLL 1 outputs												
c0	✓	✓			✓		✓		✓		✓	
c1	✓	✓				✓		✓		✓		✓
c2			✓	✓	✓		✓		✓		✓	
c3			✓	✓		✓		✓		✓		✓
PLL 2 outputs												
c0	✓	✓				✓		✓		✓		✓
c1	✓	✓			✓		✓		✓		✓	
c2			✓	✓		✓		✓		✓		✓
c3			✓	✓	✓		✓		✓		✓	

Table 2–11. Global & Regional Clock Connections from Left Side Clock Pins & Fast PLL Outputs (Part 2 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
PLL 7 outputs												
c0			✓	✓		✓		✓				
c1			✓	✓	✓		✓					
c2	✓	✓				✓		✓				
c3	✓	✓			✓		✓					
PLL 8 outputs												
c0			✓	✓					✓		✓	
c1			✓	✓						✓		✓
c2	✓	✓							✓		✓	
c3	✓	✓								✓		✓

Table 2–12. Global & Regional Clock Connections from Right Side Clock Pins & Fast PLL Outputs (Part 1 of 2)

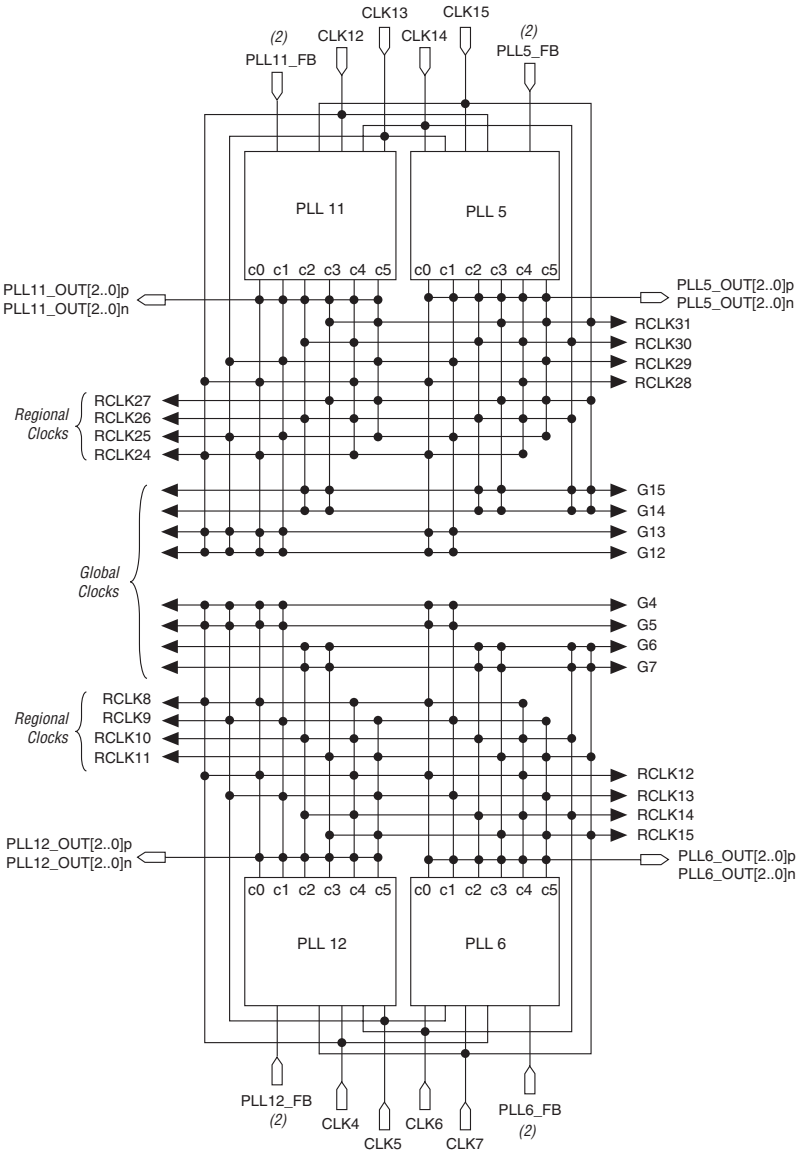
Right Side Global & Regional Clock Network Connectivity	CLK8	CLK9	CLK10	CLK11	RCLK16	RCLK17	RCLK18	RCLK19	RCLK20	RCLK21	RCLK22	RCLK23
Clock pins												
CLK8p	✓	✓			✓				✓			
CLK9p	✓	✓				✓				✓		
CLK10p			✓	✓			✓				✓	
CLK11p			✓	✓				✓				✓
Drivers from internal logic												
GCLKDRV0	✓	✓										
GCLKDRV1	✓	✓										
GCLKDRV2			✓	✓								
GCLKDRV3			✓	✓								
RCLKDRV0					✓				✓			
RCLKDRV1						✓				✓		
RCLKDRV2							✓				✓	
RCLKDRV3								✓				✓

Table 2–12. Global & Regional Clock Connections from Right Side Clock Pins & Fast PLL Outputs (Part 2 of 2)

Right Side Global & Regional Clock Network Connectivity	CLK8	CLK9	CLK10	CLK11	RCLK16	RCLK17	RCLK18	RCLK19	RCLK20	RCLK21	RCLK22	RCLK23
RCLKDRV4					✓				✓			
RCLKDRV5						✓				✓		
RCLKDRV6							✓				✓	
RCLKDRV7								✓				✓
PLL 3 outputs												
c0	✓	✓			✓		✓		✓		✓	
c1	✓	✓				✓		✓		✓		✓
c2			✓	✓	✓		✓		✓		✓	
c3			✓	✓		✓		✓		✓		✓
PLL 4 outputs												
c0	✓	✓				✓		✓		✓		✓
c1	✓	✓			✓		✓		✓		✓	
c2			✓	✓		✓		✓		✓		✓
c3			✓	✓	✓		✓		✓		✓	
PLL 9 outputs												
c0			✓	✓		✓		✓				
c1			✓	✓	✓		✓					
c2	✓	✓				✓		✓				
c3	✓	✓			✓		✓					
PLL 10 outputs												
c0			✓	✓					✓		✓	
c1			✓	✓						✓		✓
c2	✓	✓							✓		✓	
c3	✓	✓								✓		✓

Figure 2–43 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins. The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs is shown in Table 2–13. The connections to the clocks from the bottom clock pins is shown in Table 2–14.

Figure 2–43. Global & Regional Clock Connections from Top & Bottom Clock Pins & Enhanced PLL Outputs Note (1)



Notes to Figure 2–43:

(1) EP2S15 and EP2S30 devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.

(2) If the design uses the feedback input, you will lose one (or two, if FBIN is differential) external clock output pin.

Table 2–13. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓			✓				✓			
CLK13p	✓	✓	✓				✓				✓		
CLK14p	✓			✓	✓			✓				✓	
CLK15p	✓			✓	✓				✓				✓
CLK12n		✓				✓				✓			
CLK13n			✓				✓				✓		
CLK14n				✓				✓				✓	
CLK15n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL5 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓

Table 2–13. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–14. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			

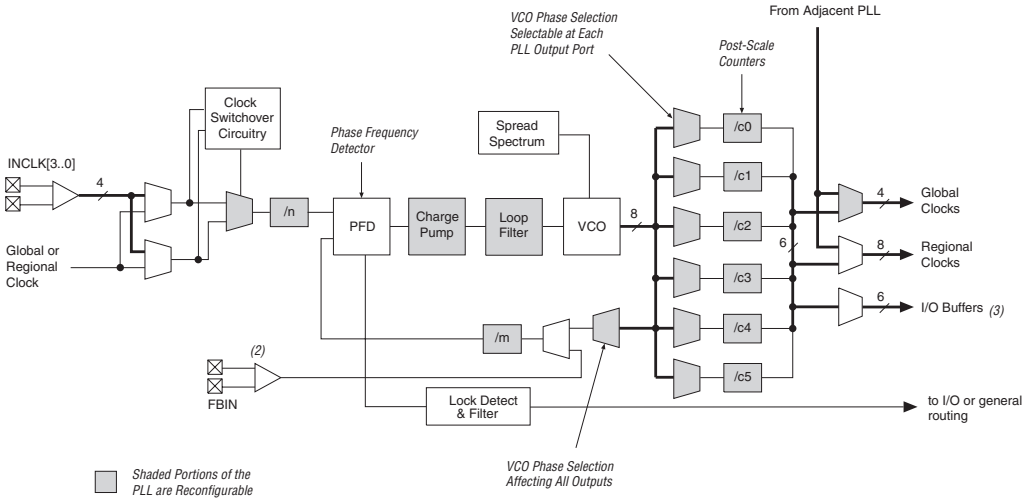
Table 2–14. Global & Regional Clock Connections from Bottom Clock Pins & Enhanced PLL Outputs (Part 2 of 2)

Bottom Side Global & Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 12 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Enhanced PLLs

Stratix II devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–44 shows a diagram of the enhanced PLL.

Figure 2–44. Stratix II Enhanced PLL *Note (1)*



Notes to Figure 2–44:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

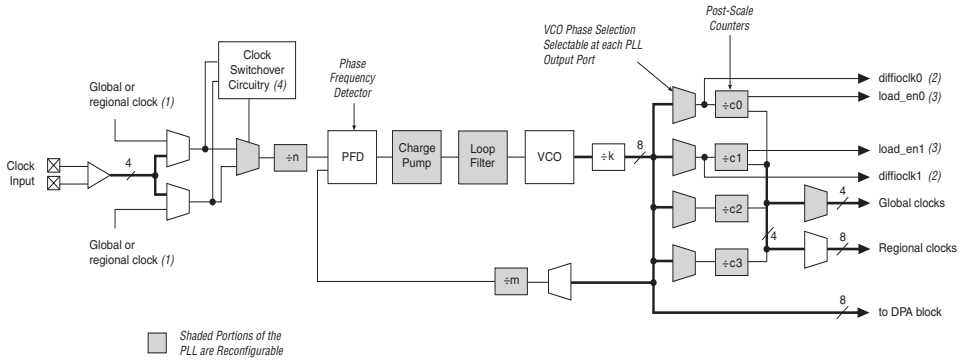
(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.

(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

Fast PLLs

Stratix II devices contain up to eight fast PLLs with high-speed serial interfacing ability. Figure 2–45 shows a diagram of the fast PLL.

Figure 2–45. Stratix II Device Fast PLL *Notes (1), (2), (3)*



Notes to Figure 2–45:

(1) The global or regional clock input can be driven by an output from another PLL or a pin-driven global or regional clock. It cannot be driven by internally-generated global signals.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES circuitry. Stratix II devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a differential I/O SERDES control signal.

(4) Stratix II fast PLLs only support manual clock switchover.

See the *PLLs in Stratix II Devices* chapter in the *Stratix II Device Handbook, Volume 2* for more information on enhanced and fast PLLs. See "High-Speed Differential I/O with DPA Support" for more information on high-speed differential I/O support.

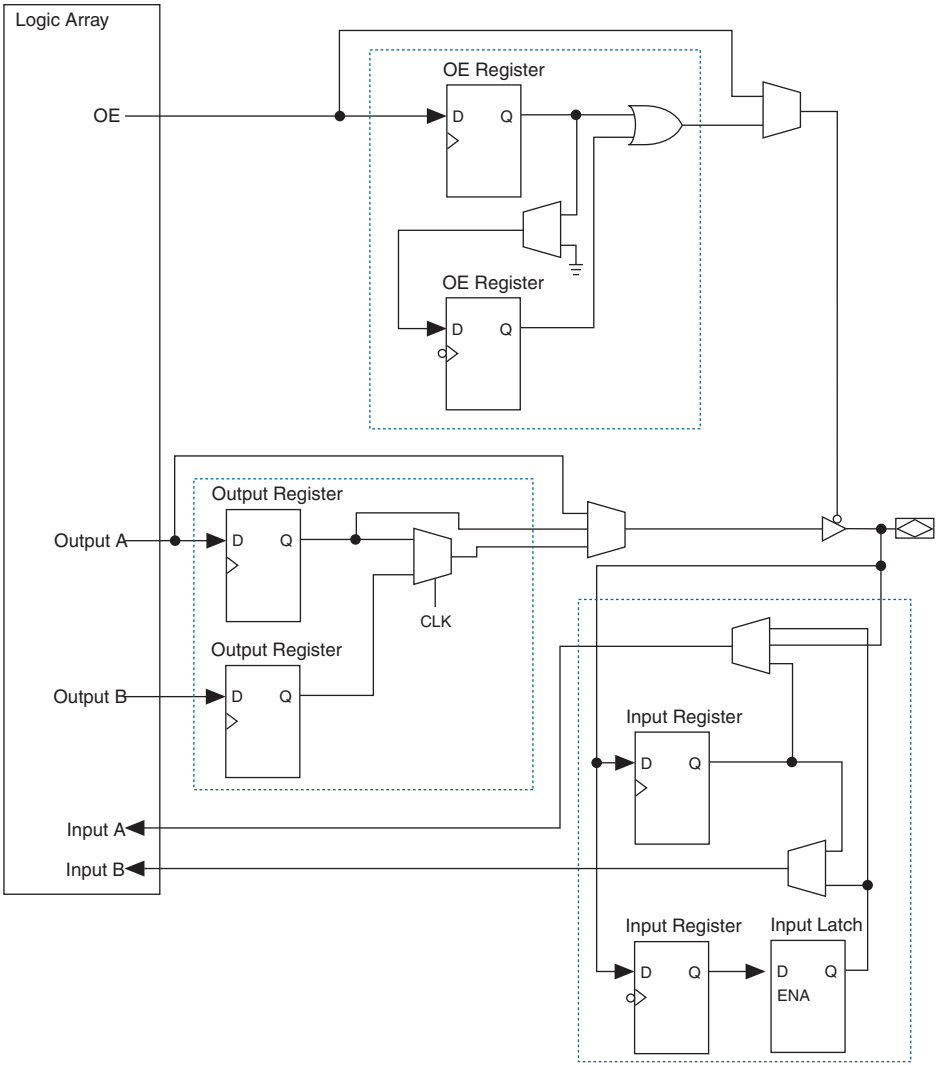
I/O Structure

The Stratix II IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- On-chip driver series termination
- On-chip termination for differential standards
- Programmable pull-up during configuration
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

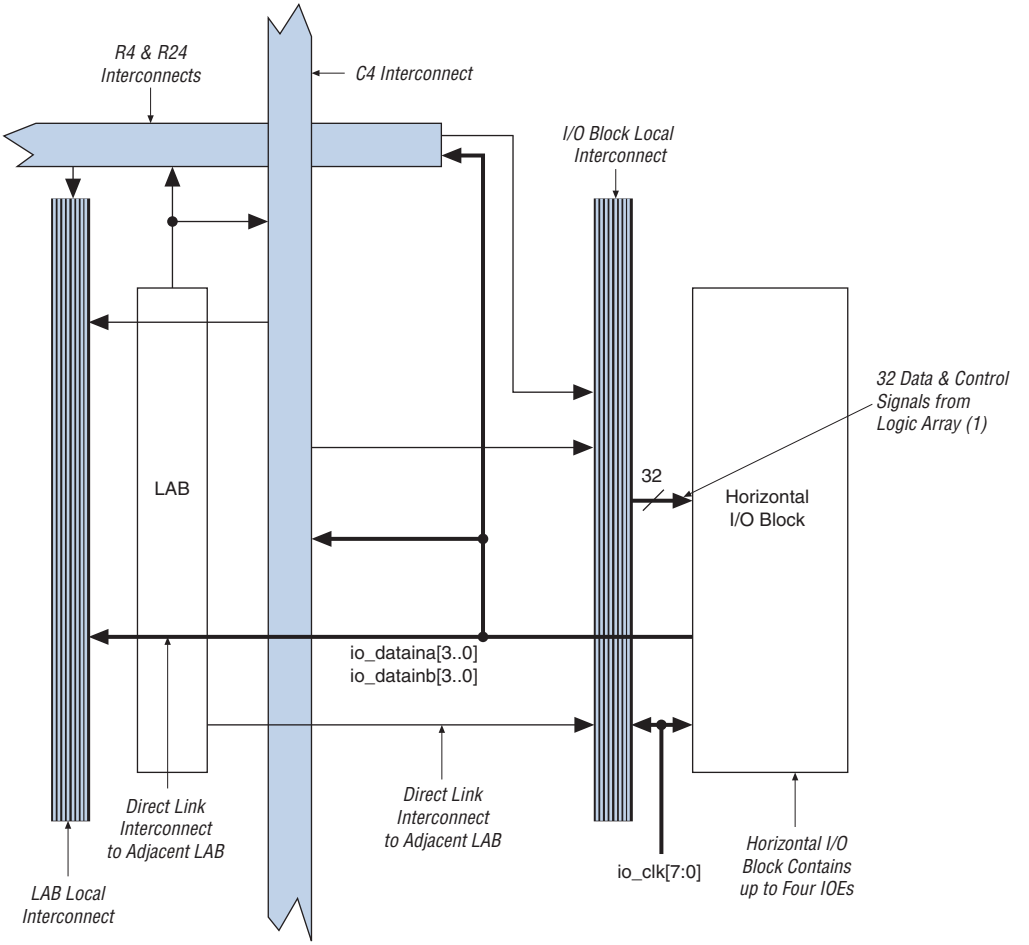
The IOE in Stratix II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–46 shows the Stratix II IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–46. Stratix II IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–47 shows how a row I/O block connects to the logic array. Figure 2–48 shows how a column I/O block connects to the logic array.

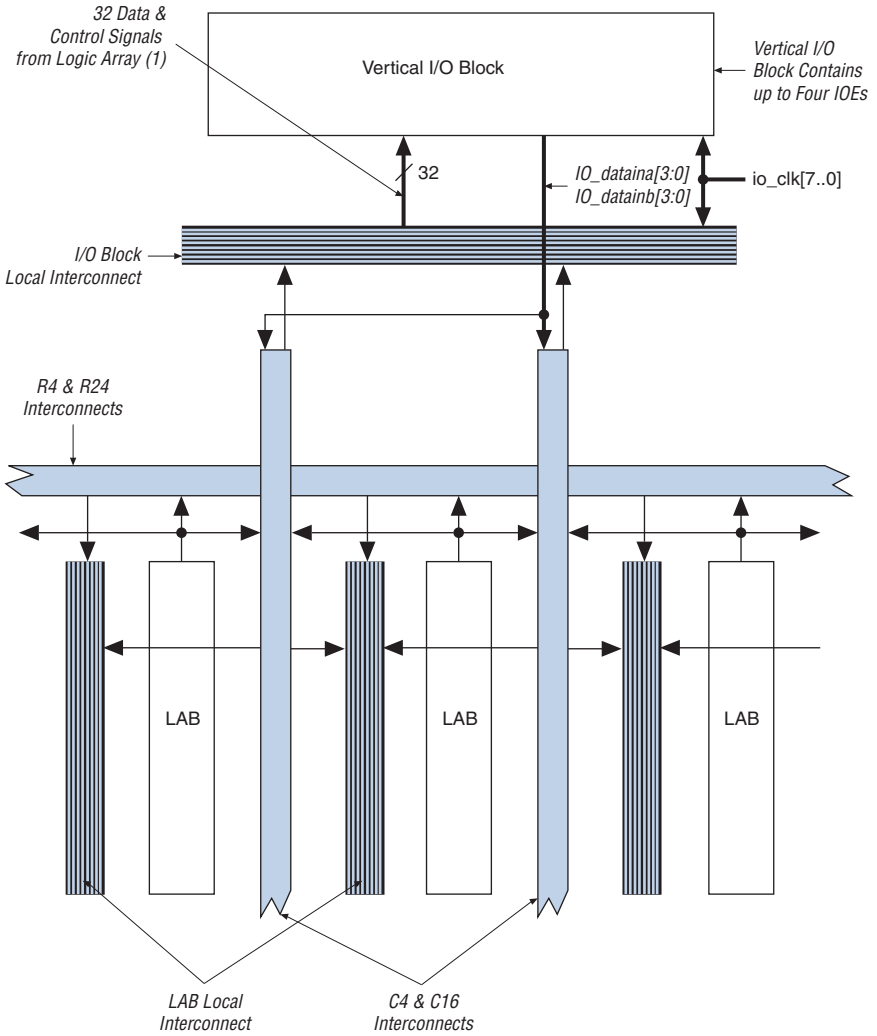
Figure 2–47. Row I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–47:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–48. Column I/O Block Connection to the Interconnect *Note (1)*

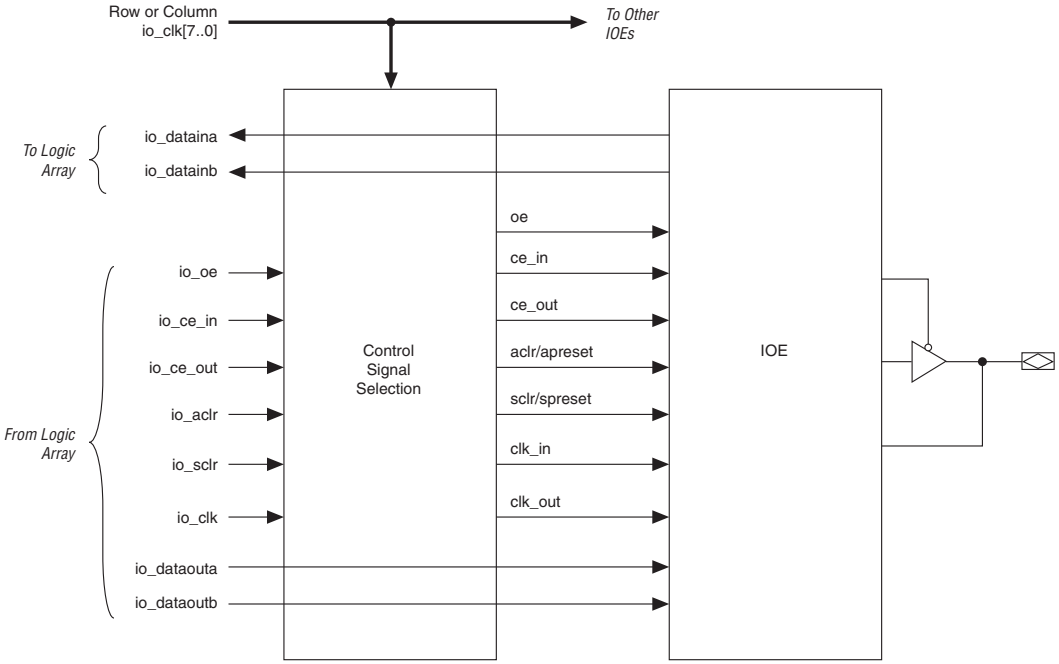


Note to Figure 2–48:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

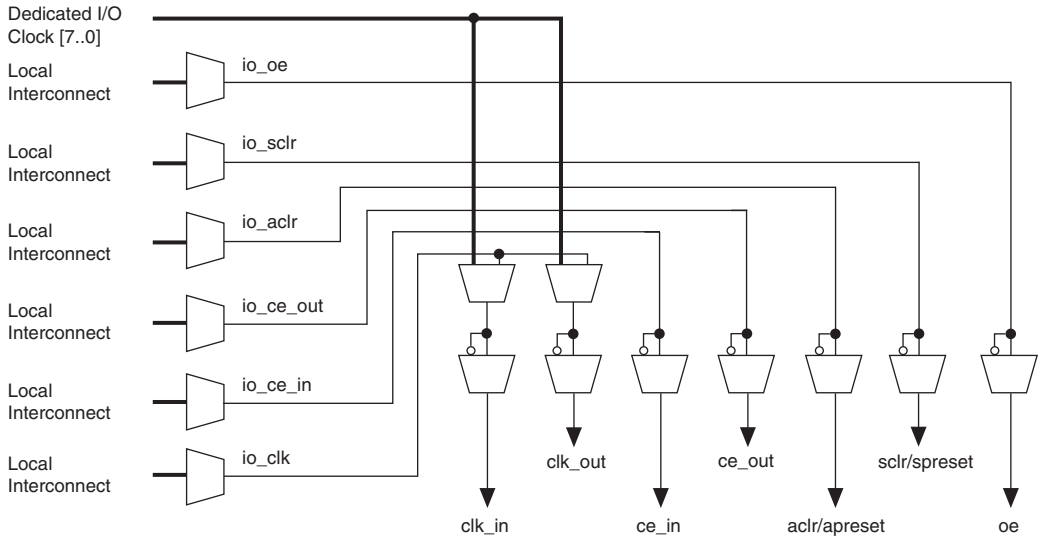
There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

Figure 2–50. Control Signal Selection per IOE

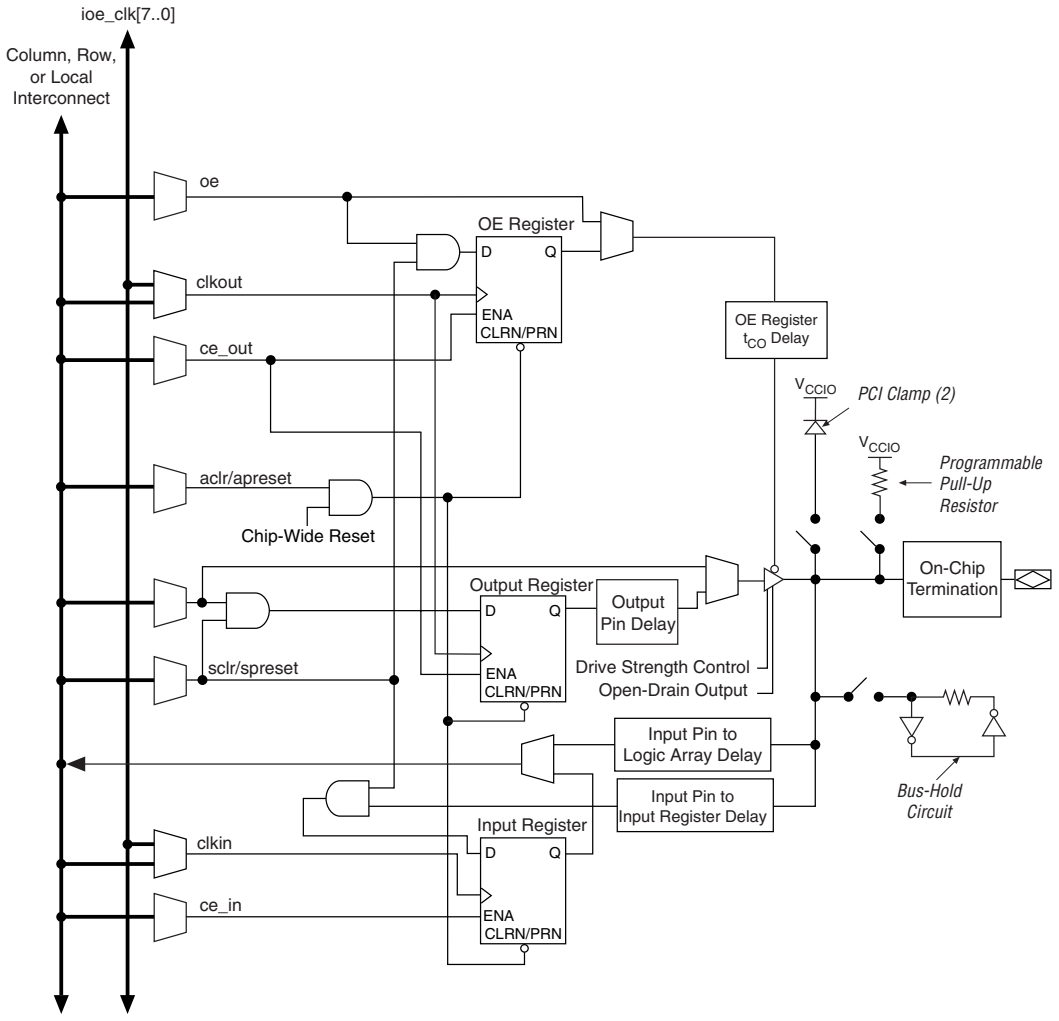


Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–51 shows the IOE in bidirectional configuration.

Figure 2–51. Stratix II IOE in Bidirectional I/O Configuration *Note (1)*



Notes to Figure 2–51:
(1) All input signals to the IOE can be inverted at the IOE.
(2) The optional PCI clamp is only available on column I/O pins.

The Stratix II device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. Table 2–15 shows the programmable delays for Stratix II devices.

Table 2–15. Stratix II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

The IOE registers in Stratix II devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

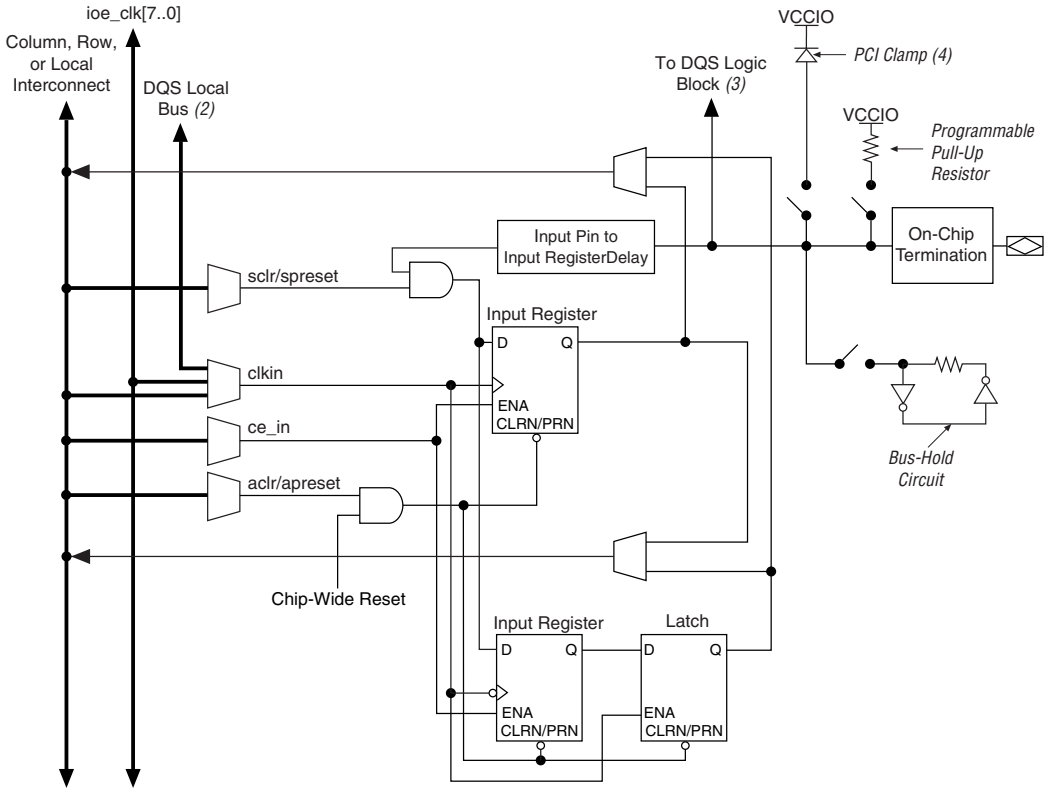
Double Data Rate I/O Pins

Stratix II devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with

the same clock edge (either rising or falling). Figure 2–52 shows an IOE configured for DDR input. Figure 2–53 shows the DDR input timing diagram.

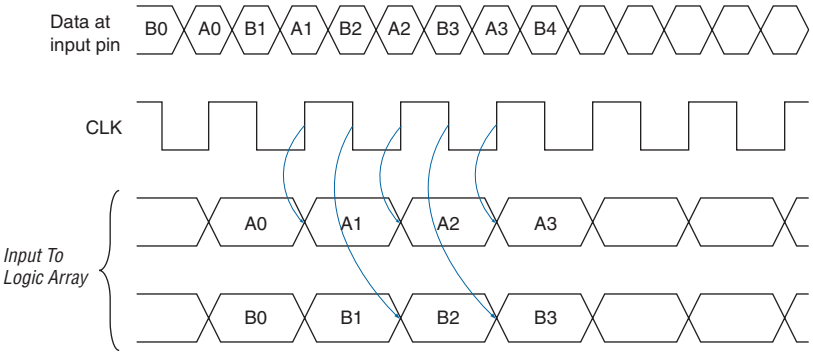
Figure 2–52. Stratix II IOE in DDR Input I/O Configuration *Notes (1), (2), (3)*



Notes to Figure 2–52:

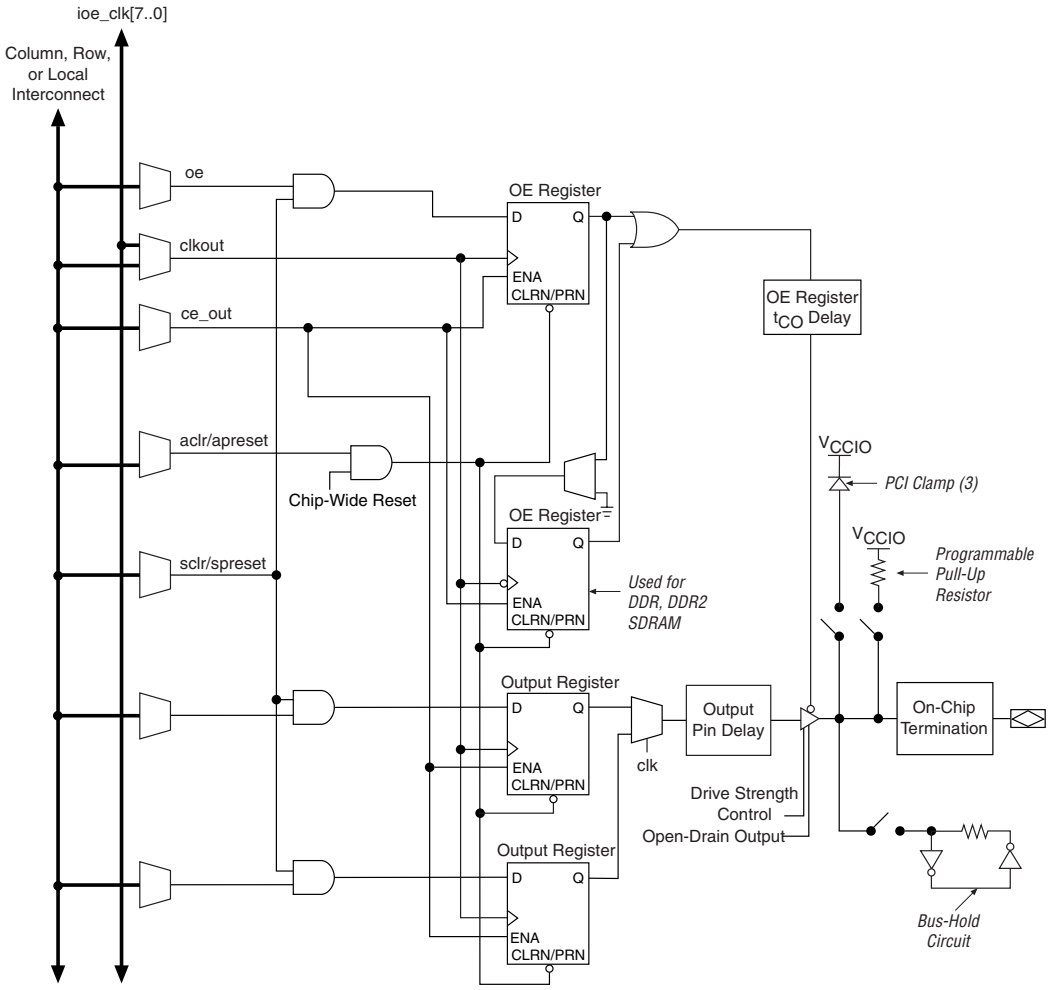
(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Figure 2–53. Input Timing Diagram in DDR Mode



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–54 shows the IOE configured for DDR output. Figure 2–55 shows the DDR output timing diagram.

Figure 2–54. Stratix II IOE in DDR Output I/O Configuration *Notes (1), (2)*



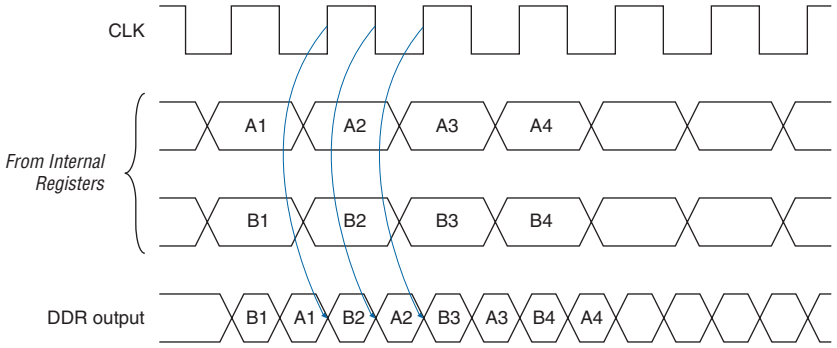
Notes to Figure 2–54:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port.

(3) The optional PCI clamp is only available on column I/O pins.

Figure 2–55. Output TIming Diagram in DDR Mode



The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–16 shows the number of DQ and DQS buses that are supported per device.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Table 2–16. DQS & DQ Bus Mode Support *Notes (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA *(2)*	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA *(2)*	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA *(2)*	18	8	4	0
	1,020-pin FineLine BGA *(3)*	36	18	8	4
EP2S90	484-pin Hybrid FineLine BGA	*(4)*	*(4)*	*(4)*	*(4)*
	780-pin FineLine BGA	*(4)*	*(4)*	*(4)*	*(4)*
	1,020-pin FineLine BGA *(3)*	36	18	8	4
	1,508-pin FineLine BGA *(3)*	36	18	8	4
EP2S130	780-pin FineLine BGA	*(4)*	*(4)*	*(4)*	*(4)*
	1,020-pin FineLine BGA *(3)*	36	18	8	4
	1,508-pin FineLine BGA *(3)*	36	18	8	4
EP2S180	1,020-pin FineLine BGA *(3)*	36	18	8	4
	1,508-pin FineLine BGA *(3)*	36	18	8	4

Notes to Table 2–16:

(1) Numbers are preliminary until devices are available.

(2) These device and package combinations can support one 72-bit DIMM in ×4 mode or one 64-bit DIMM in ×8/×9 mode.

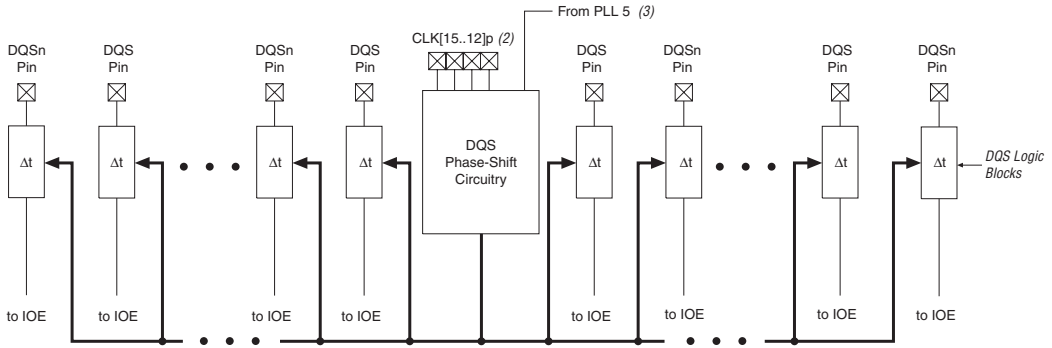
(3) These device and package combinations can support two 64- or 72-bit DIMMs in ×4 and ×8/×9 modes.

(4) The number of DQ and DQS buses will be updated in the next version of the *Stratix II Device Handbook*.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits.

Figure 2–56 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–56. DQS Phase-Shift Circuitry *Notes (1), (2), (3), (4)*



Notes to Figure 2–56:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The Δt module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook.*

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–17 shows the possible settings for the I/O standards with drive strength control.

Table 2–17. Programmable Drive Strength *Note (1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 class I	12, 8	12, 8
SSTL-2 class II	24, 20, 16	16
SSTL-18 class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 class II	20, 18, 16, 8	-
HSTL-18 class I	12, 10, 8, 6, 4	-
HSTL-18 class II	20, 18, 16	-
HSTL-15 class I	12, 10, 8, 6, 4	-
HSTL-15 class II	20, 18, 16	-

Note to Table 2–17:

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Stratix II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Bus Hold

Each Stratix II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. See the *DC & Switching Characteristics* chapter in the *Stratix II Device Handbook, Volume 1*, for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix II device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the output pin's bank.

Advanced I/O Standard Support

Stratix II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- HyperTransport technology
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II
- Differential SSTL-2 class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–18 describes the I/O standards supported by Stratix II devices.

Table 2–18. Stratix II Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5-V LVCMOS	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X mode 1	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	2.5 *(3)*	N/A
LVPECL *(1)*	Differential	N/A	3.3	N/A
HyperTransport technology	Differential	N/A	2.5 *(3)*	N/A
Differential 1.5-V HSTL class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II *(2)*	Differential	1.25	2.5	1.25
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–18:

(1) This I/O standard is only available on input and output column clock pins.

(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.

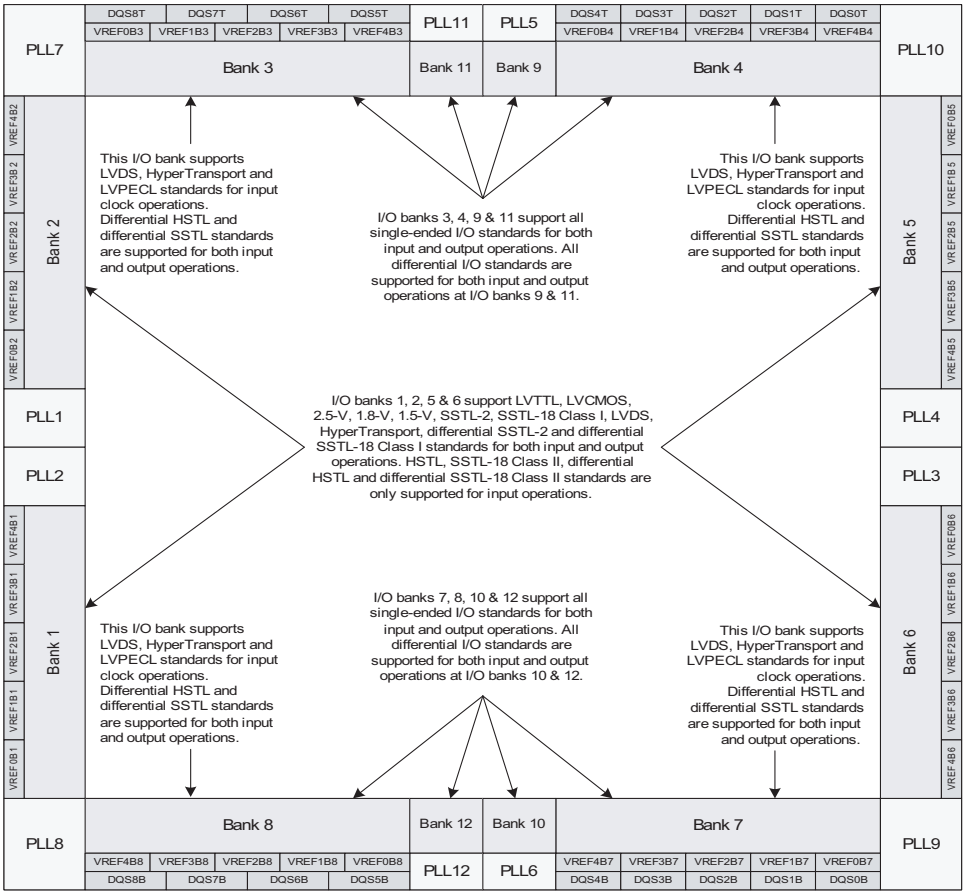
(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 3, 4, 7, 8, 9, 10, 11, and 12).

For more information on I/O standards supported by Stratix II I/O banks, refer to the *Selectable I/O Standards in Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook*.

Stratix II devices contain eight I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–57. The four I/O banks on the right and left of the device contain circuitry to support high-speed

differential I/O for LVDS and HyperTransport inputs and outputs. These banks support all Stratix II I/O standards except PCI or PCI-X I/O pins, and SSTL-18 class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Figure 2–57. Stratix II I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 2–57:

(1) Figure 2–57 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. See the *High Speed Differential I/O Interfaces in Stratix II Devices* chapter in the *Stratix II Device Handbook, Volume 2* for more information on differential I/O standards.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Stratix II devices provide differential (for the LVDS or HyperTransport technology I/O standard) and series on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II devices provide three types of termination:

- Differential termination (R_D)
- Series termination (R_S) without calibration
- Series termination (R_S) with calibration

Table 2–19 shows the Stratix II on-chip termination support per I/O bank.

Table 2–19. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)
Series termination without calibration	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	
	1.5-V LVCMOS	✓	
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I and II	✓	✓ *(1)*
	1.8-V HSTL class I	✓	
	1.8-V HSTL class II	✓	
	1.5-V HSTL class I	✓	

Table 2–19. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)
Series termination with calibration	3.3-V LVTTL	✓	
	3.3-V LVCMOS	✓	
	2.5-V LVTTL	✓	
	2.5-V LVCMOS	✓	
	1.8-V LVTTL	✓	
	1.8-V LVCMOS	✓	
	1.5-V LVTTL *(2)*	✓	
	1.5-V LVCMOS *(2)*	✓	
	SSTL-2 class I and II	✓	
	SSTL-18 class I and II	✓	
	1.8-V HSTL class I	✓	
	1.8-V HSTL class II	✓	
	1.5-V HSTL class I	✓	
Differential termination *(2)*	LVDS	✓	
	HyperTransport technology	✓	

Notes to Table 2–19:

(1) Clock pins `CLK1`, `CLK3`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential on-chip termination. Clock pins `CLK0`, `CLK2`, `CLK8`, and `CLK10` do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

(2) The I/O pins in the left and right banks do not support the SSTL-18 class II output standard.

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter in Volume 1 of the *Stratix II Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II Devices* in Volume 2 of the *Stratix II Device Handbook*.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in Volume 1 of the *Stratix II Device Handbook.*

On-Chip Series Termination without Calibration

Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25Ω and 50Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–19 shows the list of output standards that support on-chip series termination without calibration.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook*.

For more information on tolerance specifications for on-chip termination without calibration, refer to the *DC & Switching Characteristics* chapter in Volume 1 of the *Stratix II Device Handbook.*

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/Os in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25-Ω or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook*.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in Volume 1 of the *Stratix II Device Handbook*.

MultiVolt I/O Interface

The Stratix II architecture supports the MultiVolt I/O interface feature that allows Stratix II devices in all packages to interface with systems of different supply voltages.

The Stratix II VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix II VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–20 summarizes Stratix II MultiVolt I/O support.

Table 2–20. Stratix II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)				
	1.5	1.8	2.5	3.3	1.5	1.8	2.5	3.3	5.0
1.5	✓	✓	✓ (2)	✓ (2)	✓				
1.8	✓ (2)	✓	✓ (2)	✓ (2)	✓ (3)	✓			
2.5			✓	✓	✓ (3)	✓ (3)	✓		
3.3			✓ (2)	✓	✓ (3)	✓ (3)	✓ (3)	✓	✓

Notes to Table 2–20:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix II device to drive out, a receiving device powered at a different level can still interface with the Stratix II device if it has inputs that tolerate the V_{CCIO} value.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside in. TDO is in I/O bank 4 and nCEO is in I/O bank 7.

Ideally, the VCC supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by VCCSEL on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out TDO or nCEO to a slave device.

For multi-device passive configuration schemes, the nCEO pin of the master device will be driving the nCE pin of the slave device. The VCCSEL pin on the slave device selects which input buffer is used for nCE. When VCCSEL is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When VCCSEL is logic low it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the VCCSEL settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application. Table 2–21 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

Table 2–21. Board Design Recommendations for nCEO

nCE Input Buffer Power	Stratix II nCEO VCCIO Voltage Level in I/O Bank 7			
	V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V
VCCSEL high (V_{CCIO} = 1.5 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓ *(5)*	✓
VCCSEL high (V_{CCIO} = 1.8 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓	✓
VCCSEL low (V_{CCPD} = 3.3 V)	✓	✓ *(4)*	✓ *(6)*	Level shifter required

Notes to Table 2–21:
(1) Input buffer is 3.3-V tolerant.
(2) The nCEO output buffer meets V_{OH} (MIN) = 2.4 V.
(3) Input buffer is 2.5-V tolerant.
(4) The nCEO output buffer meets V_{OH} (MIN) = 2.0 V.
(5) Input buffer is 1.8-V tolerant.
(6) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

For JTAG chains, the TDO pin of the first device will be driving the TDI pin of the second device in the chain. The V_{CCSEL} input on JTAG input I/O cells (TCK, TMS, TDI, and TRST) is internally hardwired to GND selecting the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the TDO bank from the first device to match the V_{CCSEL} settings for TDI on the second device, but that may not be possible depending on the application. Table 2–22 contains board design recommendations to ensure proper JTAG chain operation.

Table 2–22. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Stratix II TDO V_{CCIO} Voltage Level in I/O Bank 4			
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V
Stratix II	Always V_{CCPD} (3.3V)	✓ (1)	✓ (2)	✓ (3)	Level shifter required
Non-Stratix II	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓

Notes to Table 2–22:
(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS and HyperTransport differential I/O standards are supported in the Stratix II device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO
- HyperTransport technology

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–23 through 2–28 show the number of channels that each fast PLL can clock in each of the Stratix II devices. In Tables 2–23 through 2–28 the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum

channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP2S15 device, PLL 1 can drive a maximum of 10 transmitter channels in I/O bank 1 or a maximum of 19 transmitter channels in I/O banks 1 and 2. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–23. EP2S15 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21

Table 2–24. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

Table 2–25. EP2S60 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	10	9	9	10
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	11	10	10	11
		(3)	21	21	21	21	-	-	-	-
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16	16	13	13	16
		(3)	29	29	29	29	-	-	-	-
	Receiver	62 *(2)*	17	14	14	17	17	14	14	17
		(3)	31	31	31	31	-	-	-	-
1,020-pin FineLine BGA	Transmitter	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-
	Receiver	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-

Table 2–26. EP2S90 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin Hybrid FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	-	-	-	-
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	-	-	-	-
		(3)	21	21	21	21	-	-	-	-
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	90 *(2)*	23	22	22	23	23	22	22	23
		(3)	45	45	45	45	-	-	-	-
	Receiver	94 *(2)*	23	24	24	23	23	24	24	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-
	Receiver	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-

Table 2–27. EP2S130 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Table 2–28. EP2S180 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Notes to Tables 2–23 to 2–28:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

(2) This is the maximum number of channels the PLLs can directly drive.

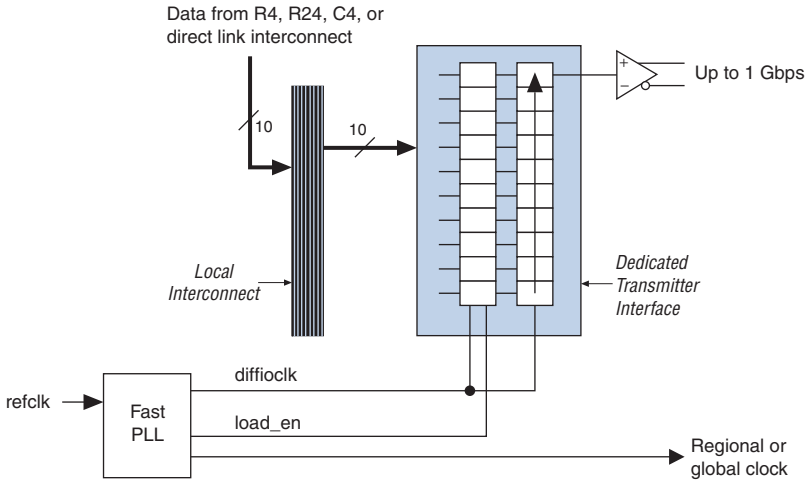
(3) This is the maximum number of channels if the device uses cross bank channels from the adjacent center PLL.

(4) The channels accessible by the center fast PLL overlap with the channels accessible by the corner fast PLL. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10.

Dedicated Circuitry with DPA Support

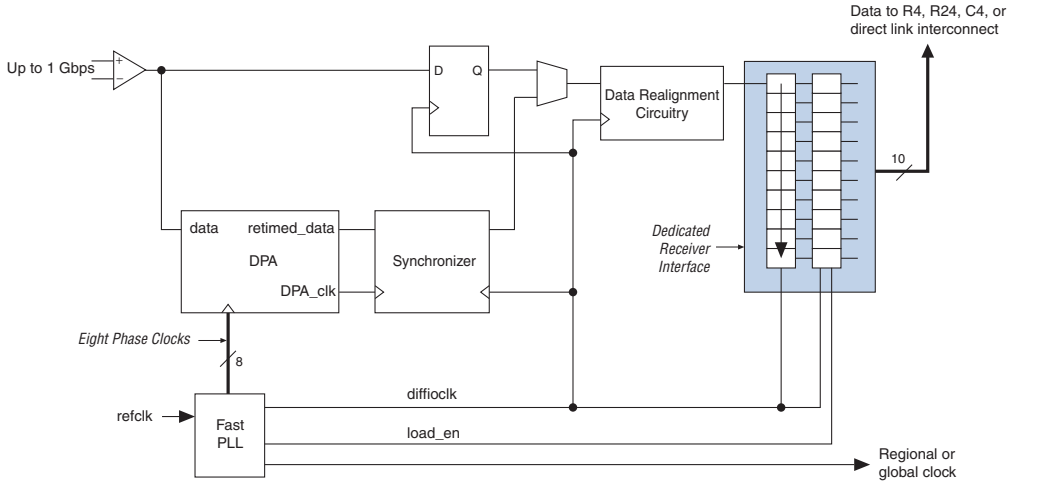
Stratix II devices support source-synchronous interfacing with LVDS or HyperTransport signaling at up to 1 Gbps. Stratix II devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. For example, a HyperTransport technology application where the data rate is 1,000 Mbps and the clock rate is 500 MHz would require that W be set to 2. The SERDES factor *J* determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor *J* can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these *J* factor values. For a *J* factor of 1, the Stratix II device bypasses the SERDES block. For a *J* factor of 2, the Stratix II device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–58 shows the block diagram of the Stratix II transmitter channel.

Figure 2–58. Stratix II Transmitter Channel



Each Stratix II receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array. Figure 2–59 shows the block diagram of the Stratix II receiver channel.

Figure 2–59. Stratix II Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry. For more information on the fast PLL, see the *PLLs in Stratix II Devices* chapter in the *Stratix II Handbook, Volume 2*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

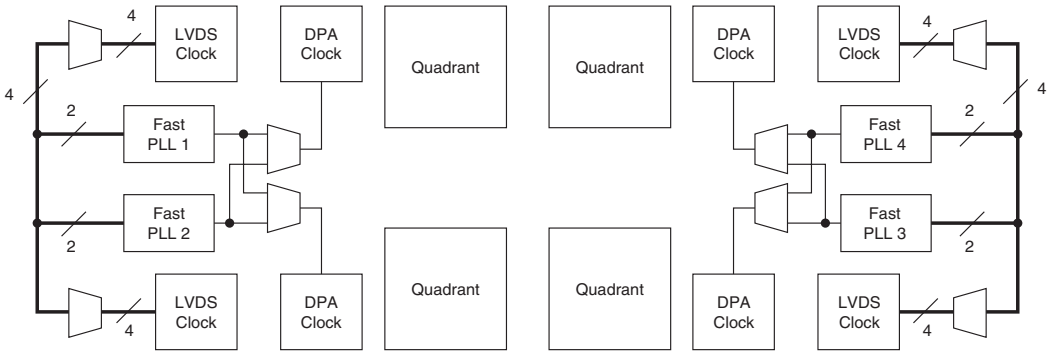
For high-speed source synchronous interfaces such as POS-PHY 4, Parallel RapidIO, and HyperTransport, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II device's high-speed differential I/O

circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. The designer can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL & Channel Layout

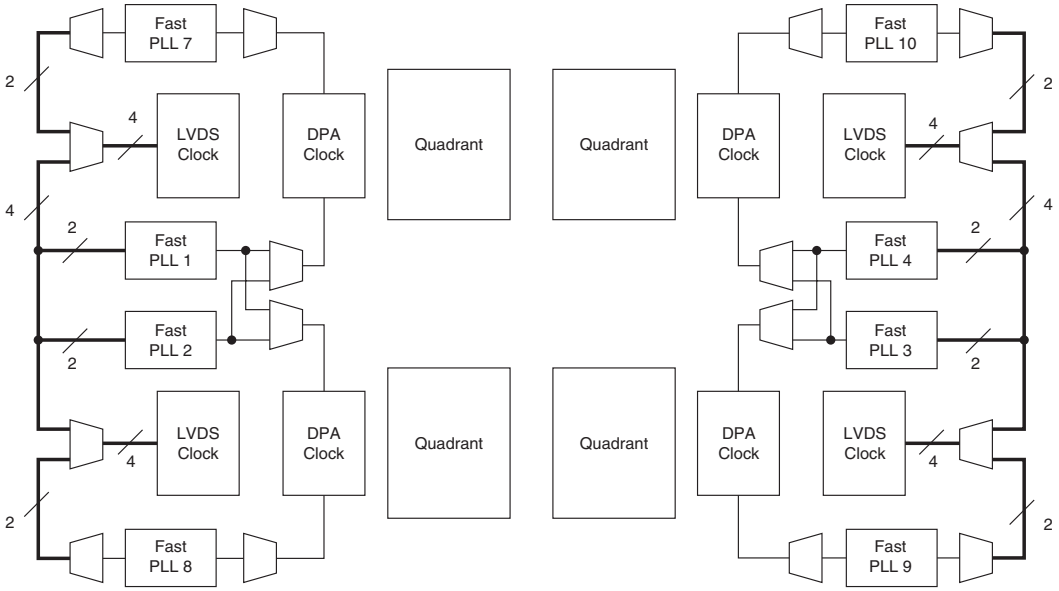
The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–60 shows the fast PLL and channel layout in the EP2S15 and EP2S30 devices. Figure 2–61 shows the fast PLL and channel layout in the EP2S60 to EP2S180 devices.

Figure 2–60. Fast PLL & Channel Layout in the EP2S15 & EP2S30 Devices *Note (1)*



Note to Figure 2–60:
(1) See Table 2–23 for the number of channels each device supports.

Figure 2–61. Fast PLL & Channel Layout in the EP2S60 to EP2S180 Devices *Note (1)*



Note to Figure 2–61:

(1) See Tables 2–24 through 2–28 for the number of channels each device supports.

3. Configuration & Testing

SII51003-2.1

IEEE Std. 1149.1 JTAG Boundary-Scan Support

All Stratix® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix II devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. Designers can use this capability for JTAG testing before configuration when some of the Stratix II pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix II device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows designers to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, `TDI`,`TDO`, `TMS`, and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, while the `TDI`,`TMS` and `TRST` pins have weak internal pull-ups. The JTAG input pins are powered by the 3.3-V `VCCPD` pins. The TDO output pin is powered by the V_{CCIO} power supply of bank 4.

Stratix II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II devices support the JTAG instructions shown in Table 3–1.

Stratix II, Stratix, Cyclone II, and Cyclone devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II, or Cyclone devices are in the 18th of further position, they will fail configuration. This does not affect SignalTap II.

Table 3–1. Stratix II JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction will hold nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

The Stratix II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix II devices.

Table 3–2. Stratix II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2S15	1,140
EP2S30	1,692
EP2S60	2,196
EP2S90	2,748
EP2S130	3,420
EP2S180	3,948

Table 3–3. 32-Bit Stratix II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2S15	0000	0010 0000 1001 0001	000 0110 1110	1
EP2S30	0000	0010 0000 1001 0010	000 0110 1110	1
EP2S60	0001	0010 0000 1001 0011	000 0110 1110	1
EP2S90	0000	0010 0000 1001 0100	000 0110 1110	1
EP2S130	0000	0010 0000 1001 0101	000 0110 1110	1
EP2S180	0000	0010 0000 1001 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Stratix, Stratix II, Cyclone, and Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Stratix II, Cyclone, and Cyclone II devices are in the 18th or after they will fail configuration. This does not affect SignalTap II.

For more information on JTAG, see the following documents:

- Chapter 9, IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Stratix II Devices in the *Stratix II Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera FPGA devices are reconfigurable and every device is tested with a high coverage production test program so the designer does not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see the "Configuration Schemes" section.

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up,

and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_PULLUP, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

The configuration input pins (nCONFIG, DCLK (when used as an input), nIO_PULLUP, RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}.

VCCSEL is sampled during power-up. Therefore, the VCCSEL setting cannot change on the fly or during a reconfiguration. The VCCSEL input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high VCCSEL connection selects the 1.8-V/1.5-V input buffer, and

a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX® II/microprocessor.

If you need to support configuration input voltages of 3.3 V/2.5 V, you should set the VCCSEL to a logic low; you can set the V_{CCIO} of the I/O bank that contains the configuration inputs to any supported voltage. If you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the "MultiVolt I/O Interface" section in the *Stratix II Architecture* chapter in Volume 1 of the *Stratix II Handbook*.

Configuration Schemes

Designers can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–4), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

Multiple Stratix II devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–4 summarizes which configuration features can be used in each configuration scheme.

See the Configuring Stratix II Devices chapter in the *Stratix II Device Handbook, Volume 2* for more information about configuration schemes in Stratix II devices.

Table 3–4. Stratix II Configuration Features

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ (1)	✓ (1)	✓
	Enhanced configuration device		✓ (2)	✓
AS	Serial configuration device	✓	✓	✓ (3)
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	
PPA	MAX II device or microprocessor and flash device			✓
JTAG	Download cable (4)			
	MAX II device or microprocessor and flash device			

Notes for Table 3–4:

(1) In these modes, the host system must send a DCLK that is 4× the data rate.

(2) The enhanced configuration device decompression feature is available, while the Stratix II decompression feature is not available.

(3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.

(4) The supported download cables include the Altera USB Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

Device Security Using Configuration Bitstream Encryption

Stratix II FPGAs are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II FPGA. To successfully configure a Stratix II FPGA that has the design security feature enabled, it must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II device. This non-volatile memory does not require any external devices, such as a battery back-up, for storage.

An encryption configuration file is the same size as a non-encryption configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme us used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security, nor decompression feature enabled. For more information about this feature, contact your local Altera sales representative.

Device Configuration Data Decompression

Stratix II FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory, and transmit this compressed bit stream to Stratix II FPGAs. During configuration, the Stratix II FPGA decompresses the bit stream in real time and programs its SRAM cells.

Stratix II FPGAs support decompression in the FPP (when using a MAX II device/microprocessor and flash memory), AS and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by modern system designers. Stratix II devices can help effectively deal with these challenges with their inherent re-programmability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reduce time to market, and extend product life.

Stratix II FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios processor or user logic) implemented in the Stratix II device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

RSC is supported in the following Stratix II configuration schemes: FPP, AS, PS, and PPA. RSC can also be implemented in conjunction with advanced Stratix II features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

See the Remote System Upgrades with Stratix II Devices chapter in the *Stratix II Device Handbook, Volume 2* for more information about remote configuration in Stratix II devices.

Configuring Stratix II FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix II FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File **(.rbf)** format. JRunner also requires a Chain Description File **(.cdf)** generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, see the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and the source files on the Altera web site **(www.altera.com)**.

Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit in different embedded systems. SRunner is able to read a **.rpd** file (Raw Programming Data) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming* White Paper and the source code on the Altera web site at **www.altera.com**.

For more information on programming serial configuration devices, see the Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet in the *Configuration Handbook.*

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site (**www.altera.com**).

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. Designers can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

See the Stratix II PLLs and Clocking Structures chapter in the *Stratix II Device Handbook, Volume 2* for more information on Stratix II PLLs.

Temperature Sensing Diode

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

Figure 3–1. External Temperature-Sensing Diode

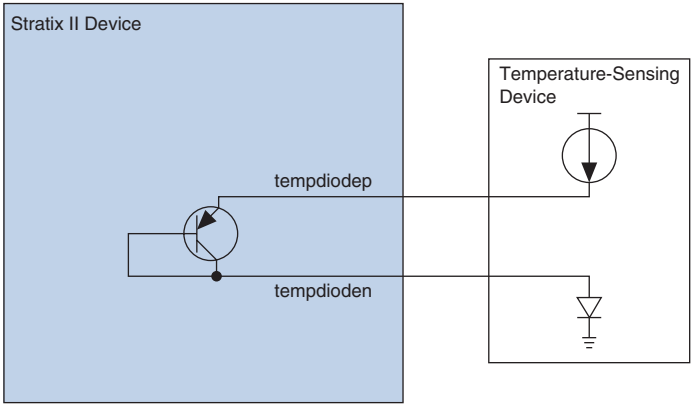


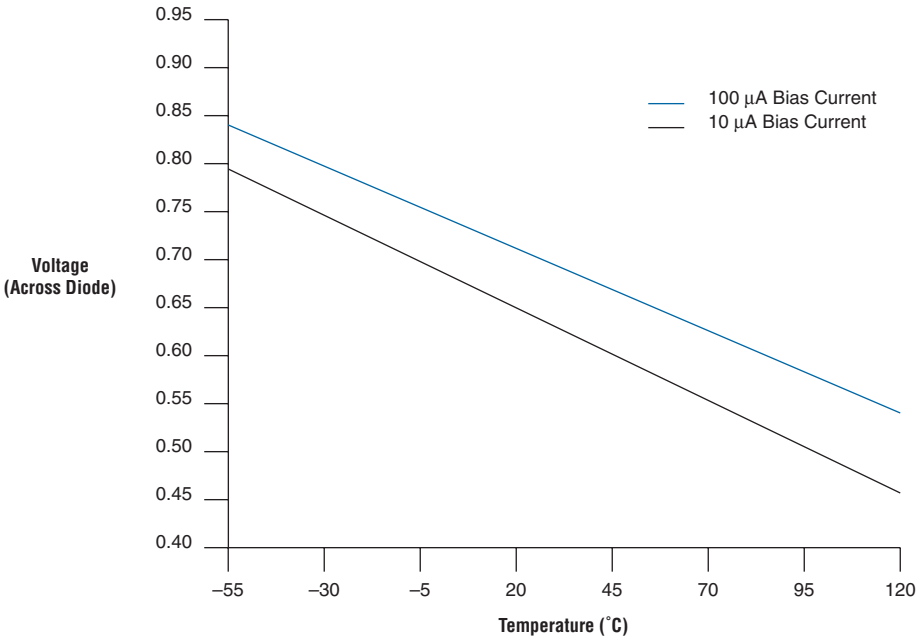
Table 3–5 shows the specifications for bias voltage and current of the Stratix II temperature sensing diode.

Table 3–5. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3–2.

Figure 3–2. Temperature vs. Temperature-Sensing Diode Voltage



Automated Single Event Upset (SEU) Detection

Stratix II devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the Device & Pin Options dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

Designers can implement the error detection CRC feature with existing circuitry in Stratix II devices, eliminating the need for external logic. For Stratix II, CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built in the Stratix II devices to perform error detection automatically. This error detection circuitry in Stratix II devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. Designers can monitor one external pin for the error and use it to trigger a re-configuration cycle. The designer can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, designers can turn on the automated error detection CRC feature in the Device & Pin Options dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to AN 357: Error Detection Using CRC in Altera FPGA Devices.

4. Hot Socketing, ESD & Power-On Reset

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Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. Designers can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when designers use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, designers no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the electro-static discharge (ESD) protection and the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

Devices Can Be Driven before Power-Up

You can drive signals into the I/O pins, dedicated input pins and dedicated clock pins of Stratix II devices before or during power-up or power-down without damaging the device. Stratix II devices support any power-up or power-down sequence (V_{CCIO}, V_{CCINT}, and V_{CCPD}) in order to simplify system level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, Stratix II device's output buffers are turned off during system power-up or power-down. Stratix II device also does not drive out until the device is configured and has attained proper operating conditions.

Signal Pins Do Not Drive the V_{CCIO}, V_{CCINT} or V_{CCPD} Power Supplies

Devices that do not support hot-socketing can short power supplies together when powered-up through the device signal pins. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

Stratix II devices do not have a current path from I/O pins, dedicated input pins, or dedicated clock pins to the V_{CCIO}, V_{CCINT}, or V_{CCPD} pins before or during power-up. A Stratix II device may be inserted into (or removed from) a powered-up system board without damaging or interfering with system-board operation. When hot-socketing, Stratix II devices may have a minimal effect on the signal integrity of the backplane.

You can power up or power down the V_{CCIO}, V_{CCINT}, and V_{CCPD} pins in any sequence. The power supply ramp rates can range from 100 µs to 100 ms. All V_{CC} supplies must power down within 100 ms of each other. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Stratix II devices meet the following hot socketing specification.

- The hot socketing DC specification is: $| I_{IOPIN} | < 300$ µA
- The hot socketing AC specification is: $| I_{IOPIN} | < 8$ mA or $| I_{IOPIN} | > 8$ mA for 10 ns or less

I_{IOPIN} is the current at any user I/O pin on the device. The AC specification has two requirements. The peak current during power-up or power-down is < 8 mA. The peak current is allowed to exceed 8 mA for 10 ns or less.

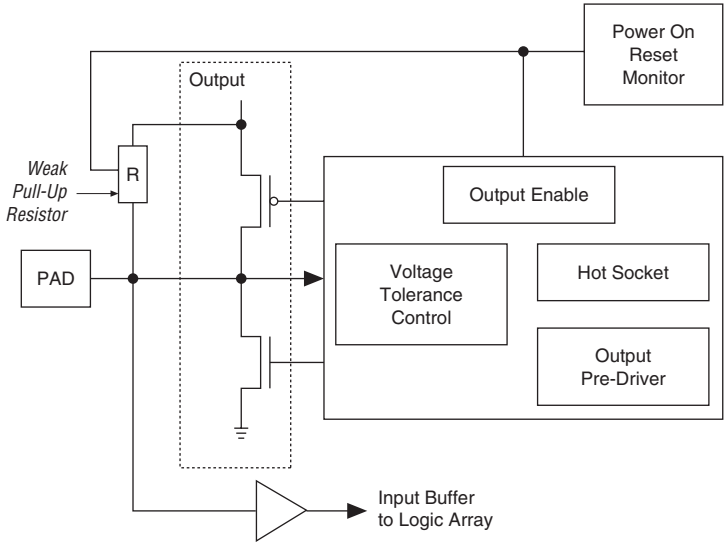
A possible concern regarding hot-socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage. Nevertheless, Stratix II devices are immune to latch-up when hot-socketing.

Hot Socketing Feature Implementation in Stratix II Devices

The hot socketing feature turns off the output buffer during the power-up event (either V_{CCINT}, V_{CCIO}, or V_{CCPD} supplies) or power down. The hot-socket circuit will generate an internal HOTSCKT signal when either V_{CCINT}, V_{CCIO}, or V_{CCPD} is below threshold voltage. The HOTSCKT signal will cut off the output buffer to make sure that no DC current (except for weak pull up leaking) leaks through the pin. When V_{CC} ramps up very slowly, V_{CC} is still relatively low even after the POR signal is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer can not flip from the state set by the hot socketing circuit at this low V_{CC} voltage. Therefore, the hot socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. It is expected behavior for these pins to drive out during power-up and power-down sequences.

Each I/O pin has the following circuitry shown in Figure 4–1.

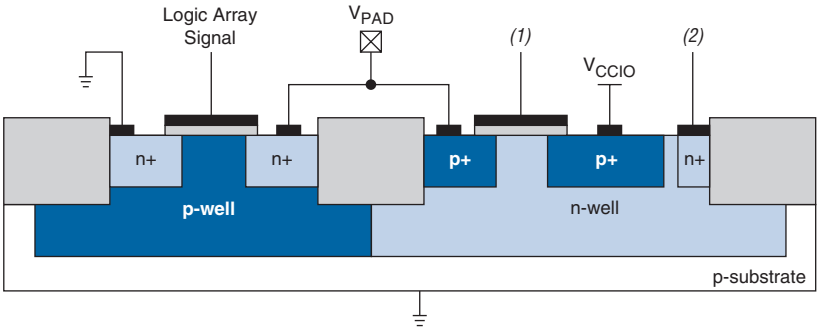
Figure 4–1. Hot Socketing Circuit Block Diagram for Stratix II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is present to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} and/or V_{CCPD} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO}, V_{CCINT}, and V_{CCPD} when driven by external signals before the device is powered.

Figure 4–2 shows a transistor level cross section of the Stratix II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} or V_{CCPD} during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



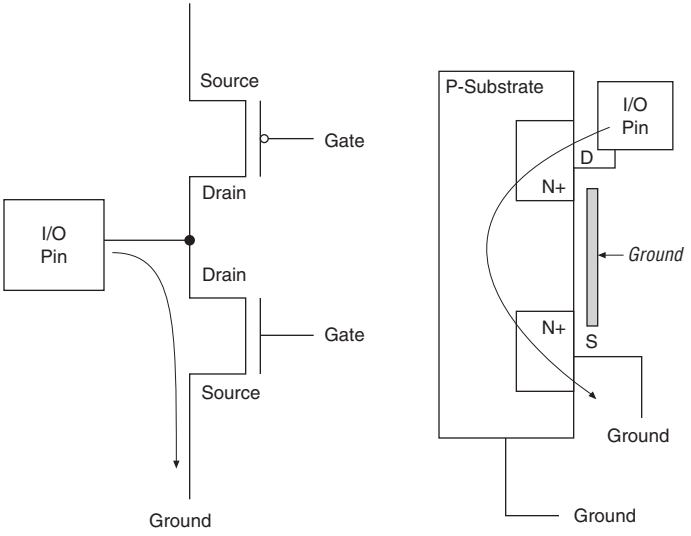
Notes to Figure 4–2:
(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

ESD Protection

The CMOS output drivers in the I/O pins intrinsically provide ESD protection. ESD voltage strikes can cause a positive voltage zap or a negative voltage zap.

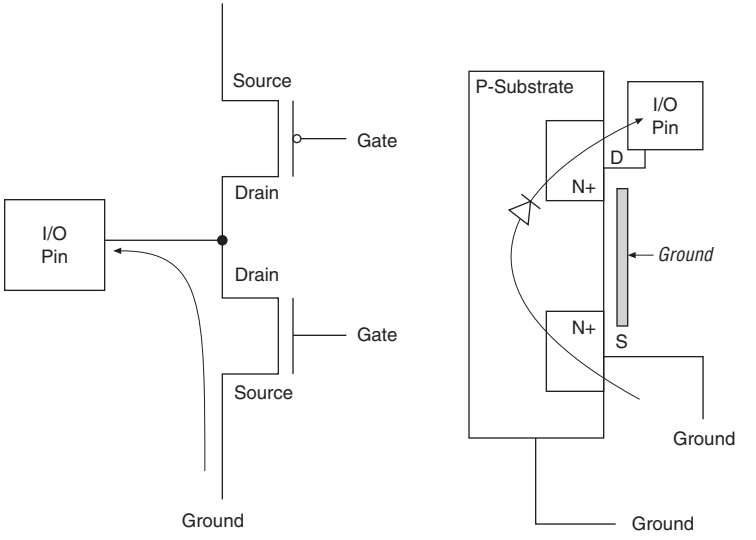
A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turns on to discharge ESD current from I/O pin to GND. The arrows in Figure 4–3 show the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap



When the I/O pin receives a negative ESD zap at the pin that is less than –0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Hence, the discharge ESD current path is from GND to the I/O pin as shown in Figure 4–4.

Figure 4–4. ESD Protection During Negative Voltage Zap



For the maximum specification of ESD protection, see the *DC & Switching Characteristics* chapter in Volume 1 of the *Stratix II Device Handbook*.

The maximum specification of ESD protection will be published in a future version of the Reliability Report, available on the Altera web site at **www.altera.com**.

Power-On Reset Circuitry

Stratix II devices have a POR circuit to keep the whole device system in reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCPD} voltage levels and tri-states all the user I/O pins while V_{CC} is ramping up until normal user levels are reached. The POR circuitry also ensures that all eight I/O bank V_{CCIO} voltages, V_{CCPD} voltage, as well as the logic array V_{CCINT} voltage, reach an acceptable level before configuration is triggered. After the Stratix II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If there is a V_{CCINT} voltage sag below the Stratix II operational level during user mode, the POR circuit resets the device.

When power is applied to a Stratix II device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). The maximum V_{CC} rise time for Stratix II device is 100 ms. Stratix II devices provide a dedicated input pin (PORSEL) to select POR delay times of 12 or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

5. DC & Switching Characteristics

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Operating Conditions

Stratix® II devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 and -5 speed grades and commercial devices are offered in -3 (fastest), -4, -5 speed grades.

Tables 5–1 through 5–30 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II devices.

Absolute Maximum Ratings

Table 5–1 contains the absolute maximum ratings for the Stratix II device family.

Table 5–1. Stratix II Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	3.0	3.6	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	–55	125	°C

Notes to Tables 5–1

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–2. Maximum Duty Cycles in Voltage Transitions	
V_{IN} (Volts)	Maximum Duty Cycles
4.0	100%
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	Maximum risetime = 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	Maximum risetime = 100 ms *(3)*	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	Maximum risetime = 100 ms *(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	Maximum risetime = 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	Maximum risetime = 100 ms *(3)*	1.425	1.575	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≥ risetime ≥ 100 ms *(4)*	3.135	3.465	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C

Notes to Table 5–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(2) During transitions, the inputs may overshoot to the voltage shown in Table 5–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If VCCPD is not ramped up within this specified time, your Stratix II device will not configure successfully. If your system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, you must hold `nCONFIG` low until all power supplies are reliable.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.

DC Electrical Characteristics

Table 5–4 shows the Stratix II device family DC electrical characteristics.

Table 5–4. Stratix II Device DC Operating Conditions *Note (1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (all memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs		*(3)*		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(4)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(4)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(4)*	60		150	kΩ

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) This specification is pending device characterization.

(4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–30 show the Stratix II device family I/O standard specifications.

Table 5–5. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*		0.45	V

Notes to Tables 5–5:
(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–6. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*		0.2	V

Notes to Table 5–6:
(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
(2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1mA *(2)*	2.0		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*		0.4	V

Notes to Table 5–7:
(1) Stratix II devices V_{CCIO} voltage level support of 2.5 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Notes to Table 5–8:
(1) The Stratix II device family's V_{CCIO} voltage level support of 1.8 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–9. 1.5-V I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 × V_{CCIO}		V

Table 5–9. 1.5-V I/O Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.25 × V_{CCIO}	V

Notes to Table 5–7:

(1) The Stratix II device family's V_{CCIO} voltage level support of 1.5 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Figures 5–1 and 5–2 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, LVPECL, and HyperTransport technology).

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards

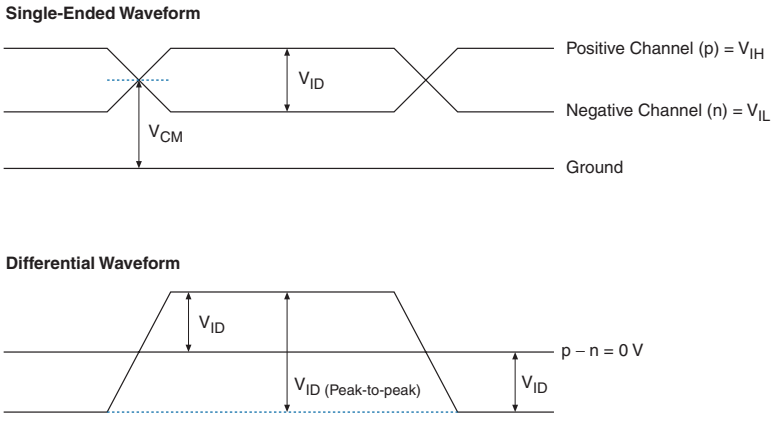


Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards

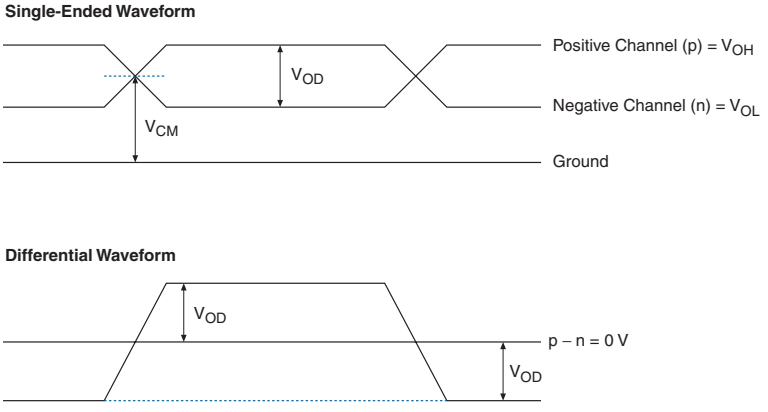


Table 5–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.5	2.625	V
	Output/feedback pins in PLL banks 9, 10, 11, and 12 *(1)*		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		200		1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	375	550	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω			50	mV
R_L	Receiver differential input discrete resistor (external to Stratix devices)		90	100	110	Ω

Notes to Tables 5–10:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, VCC_PLL_OUT should be connected to 3.3 V.

Table 5–11. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		1.0		2.0	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	700	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	525	700	970	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Notes to Table 5–11:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, VCC_PLL_OUT should be connected to 3.3 V.

(2) This specification is pending device characterization.

Table 5–12. HyperTransport Technology Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.5	2.625	V
	Output/feedback pins in PLL banks 9, 10, 11, and 12 *(1)*		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)	R_L = 100 Ω	300	600	900	mV
V_{ICM}	Input common mode voltage	R_L = 100 Ω	385	600	845	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	400	600	820	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			75	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	600	780	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 5–12:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, VCC_PLL_OUT should be connected to 3.3 V.

Table 5–13. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–14. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.3		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.25			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Notes to Table 5–15:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–16. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.25			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Notes to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–17. SSTL-18 Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
$V_{SWING (DC)}$	DC differential input voltage		0.25			V
$V_{X (AC)}$	AC differential input cross point voltage		(V_{CCIO}/2) – 0.175		(V_{CCIO}/2) + 0.175	V
$V_{SWING (AC)}$	AC differential input voltage		0.5			V
V_{ISO}	Input clock signal offset voltage			0.5 × V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
$V_{OX(AC)}$	AC differential cross point voltage		(V_{CCIO}/2) – 0.125		(V_{CCIO}/2) + 0.125	V

Table 5–18. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.25	1.313	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Notes to Table 5–18:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–19. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.25	1.313	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Notes to Table 5–19:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–20. SSTL-2 Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
$V_{SWING (DC)}$	DC differential input voltage		0.36			V
$V_{X (AC)}$	AC differential input cross point voltage		$(V_{CCIO}/2) – 0.2$		$(V_{CCIO}/2) + 0.2$	V
$V_{SWING (AC)}$	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			$0.5 \times V_{CCIO}$		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
$V_{OX(AC)}$	AC differential output cross point voltage		$(V_{CCIO}/2) – 0.2$		$(V_{CCIO}/2) + 0.2$	V

Table 5–21. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.5	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} – 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} – 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = 8$ mA *(1)*	$V_{CCIO} – 0.4$			V
V_{OL}	Low-level output voltage	$I_{OH} = –8$ mA *(1)*			0.4	V

Notes to Table 5–21:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–22. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.50	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Notes to Table 5–22:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–23. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Table 5–24. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Notes to Table 5–24:
(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–25. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Notes to Table 5–25:
(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in Table 2–17 on page 2–85.

Table 5–26. 1.8-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Bus Hold Specifications

Table 5–27 shows the Stratix II device family bus hold specifications.

Table 5–27. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	*(1)*		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	*(1)*		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		*(1)*		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		*(1)*		–200		–300		–500	µA

Notes to Table 5–27:
(1) This specification is pending device characterization.

On-Chip Termination Specifications

Tables 5–28 and 5–29 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 5–28. Series On-Chip Termination Specification for Top & Bottom I/O Banks (3, 4, 7, and 8)

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	*(1)*	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	*(1)*	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8V	±6	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8V	±30	*(1)*	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±6	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30	*(1)*	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5V	*(1)*	*(1)*	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	*(1)*	%

Note for Table 5–28:
(1) This specification is pending device characterization.

Table 5–29. Series & Differential On-Chip Termination Specification for Left & Right I/O Banks (1, 2, 5, and 6)

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	*(1)*	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8V	±30	*(1)*	%
R_D	Internal differential termination for LVDS or HyperTransport technology		*(1)*	*(1)*	%

Note to Table 5–29:
(1) This specification is pending device characterization.

Pin Capacitance

Table 5–30 shows the Stratix II device family pin capacitance.

Table 5–30. Stratix II Device Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.		5.0	*(1)*	pF
C_{IOLR}	Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins.		6.1	*(1)*	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.		6.0	*(1)*	pF
C_{CLKLR}	Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK8`, `CLK10`.		6.1	*(1)*	pF
C_{CLKLR+}	Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK9`, and `CLK11`.		3.3	*(1)*	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 9, 10, 11, and 12.		6.7	*(1)*	pF

Notes to Table 5–30:
(1) This specification is pending device characterization.

Power Consumption

Altera® offers two ways to calculate power for a design: the Excel-based PowerPlay Early Power Estimator power calculator and the Quartus II PowerPlay Power Analyzer feature.

The interactive Excel-based PowerPlay Early Power Estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The Power Analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Early Power Estimator* and *PowerPlay Power Analyzer* chapters in Volume 3 of the *Quartus II Handbook*.

The PowerPlay Early Power Estimator is available on the Altera web site at **www.altera. com**.

Timing Model

The DirectDrive™ technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 4.2. There are performance numbers shown throughout this handbook that reflect increased performance based on device characterization that will be incorporated in the Quartus II software version 5.0.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 5-30 shows the status of the Stratix II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 5–31. Stratix II Device Timing Model Status

Device	Preliminary	Final
EP2S15	✓	
EP2S30	✓	
EP2S60	✓	
EP2S90	✓	
EP2S130	✓	
EP2S180	✓	

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI which uses 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 5–32. Use the following equations to calculate clock pin to output pin timing for Stratix II devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

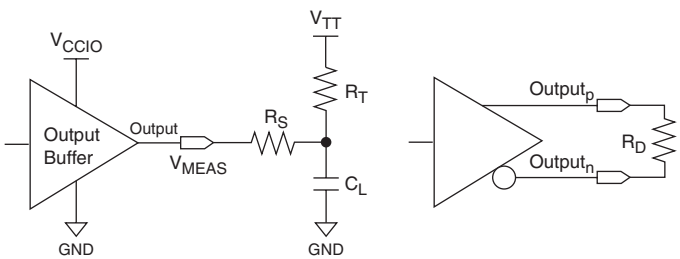
t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by Quartus II and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 5–32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

Quartus II reports the timing with the conditions shown in Table 5–32 using the above equation. Figure 5–3 shows the model of the circuit that is represented by Quartus II output timing.

Figure 5–3. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 5–3:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.
(2) V_{CCPD} is 3.085 V unless otherwise specified.
(3) V_{CCINT} is 1.12 V unless otherwise specified.

Figures 5–4 and 5–5 show the measurement setup for output disable and output enable timing.

Table 5–32. Output Timing Measurement Methodology for Output Pins *Notes (1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*				3.135	3.135	0	1.5675
LVCMOS *(4)*				3.135	3.135	0	1.5675
2.5 V *(4)*				2.375	2.375	0	1.1875
1.8 V *(4)*				1.710	1.710	0	0.855
1.5 V *(4)*				1.425	1.425	0	0.7125
PCI *(5)*				2.970	2.970	10	1.485
PCI-X *(5)*				2.970	2.970	10	1.485
SSTL-2 class I	25		50	2.325	1.123	0	1.1625
SSTL-2 class II	25		25	2.325	1.123	0	1.1625
SSTL-18 class I	25		50	1.660	0.790	0	0.83
SSTL-18 class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL class I			50	1.660	0.790	0	0.83
1.8-V HSTL class II			25	1.660	0.790	0	0.83
1.5-V HSTL class I			50	1.375	0.648	0	0.6875
1.5-V HSTL class II			25	1.375	0.648	0	0.6875
Differential SSTL-2 class I	25		50	2.325	1.123	0	1.1625
Differential SSTL-2 class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 class I	25		50	1.660	0.790	0	0.83
Differential SSTL-18 class II	25		25	1.660	0.790	0	0.83
1.5-V differential HSTL class I			50	1.375	0.648	0	0.6875
1.5-V differential HSTL class II			25	1.375	0.648	0	0.6875
1.8-V differential HSTL class I			50	1.660	0.790	0	0.83
1.8-V differential HSTL class II			25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
HyperTransport		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 5–32:

(1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.

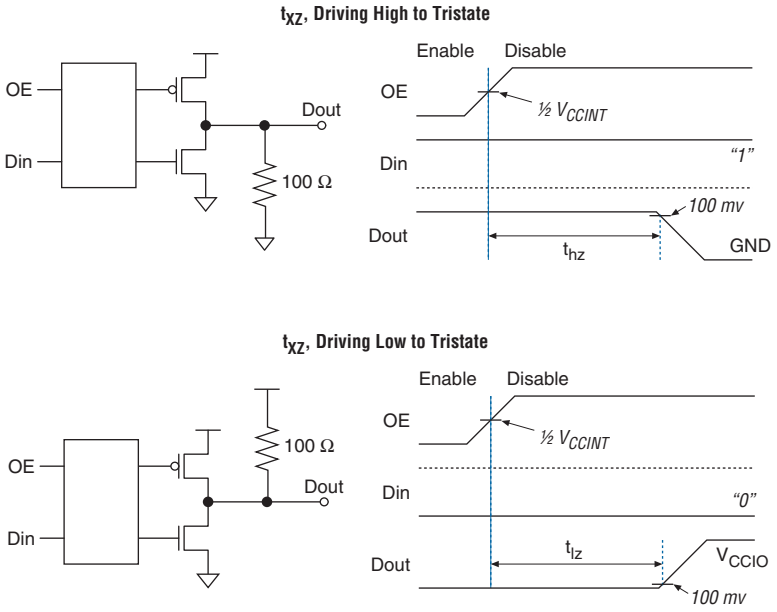
(2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple

(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V

Figure 5–4. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 5–4:
(1) V_{CCINT} is 1.12 V for this measurement.

Figure 5–5. Measurement Setup for t_{zx}

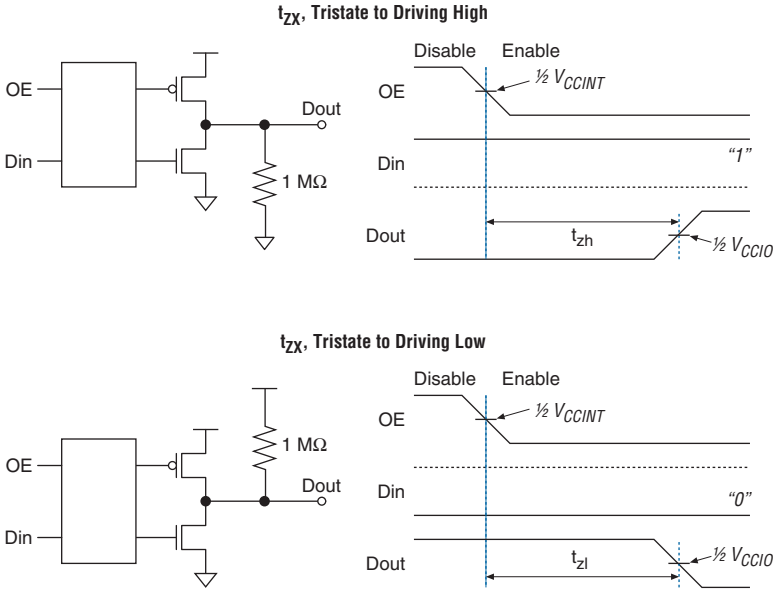


Table 5–33 specifies the input timing measurement setup.

Table 5–33. Timing Measurement Methodology for Input Pins (Part 1 of 2) *Notes (1)–(4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135		3.135	1.5675
LVCMOS *(5)*	3.135		3.135	1.5675
2.5 V *(5)*	2.375		2.375	1.1875
1.8 V *(5)*	1.710		1.710	0.855
1.5 V *(5)*	1.425		1.425	0.7125
PCI *(6)*	2.970		2.970	1.485
PCI-X *(6)*	2.970		2.970	1.485
SSTL-2 class I	2.325	1.163	2.325	1.1625
SSTL-2 class II	2.325	1.163	2.325	1.1625
SSTL-18 class I	1.660	0.830	1.660	0.83
SSTL-18 class II	1.660	0.830	1.660	0.83
1.8-V HSTL class I	1.660	0.830	1.660	0.83

Table 5–33. Timing Measurement Methodology for Input Pins (Part 2 of 2) *Notes (1)–(4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
1.8-V HSTL class II	1.660	0.830	1.660	0.83
1.5-V HSTL class I	1.375	0.688	1.375	0.6875
1.5-V HSTL class II	1.375	0.688	1.375	0.6875
Differential SSTL-2 class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 class I	1.660	0.830	1.660	0.83
Differential SSTL-18 class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL class II	1.660	0.830	1.660	0.83
LVDS	2.325		0.100	1.1625
HyperTransport	2.325		0.400	1.1625
LVPECL	3.135		0.100	1.5675

Notes to Table 5–33:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is $0.5 \times V_{CCIO}$.
(3) Output measuring point is $0.5 \times V_{CC}$ at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V

Performance

Table 5–34 shows Stratix II performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM), or MegaCore® functions for the finite impulse response (FIR) and fast Fourier transform (FFT) designs.

The performance numbers in Table 5–34 are extracted from the Quartus II software version 4.2. There are performance numbers shown throughout this handbook that reflect increased performance based on device characterization that will be incorporated in the Quartus II software version 5.0.

Table 5–34. Stratix II Performance Notes (Part 1 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
LE	16-to-1 multiplexer *(2)*	21	0	0	422.11	422.11	358.8	MHz
	32-to-1 multiplexer *(2)*	38	0	0	422.11	391.23	344.82	MHz
	16-bit counter	16	0	0	422.11	422.11	358.8	MHz
	64-bit counter	64	0	0	239.0	209.42	174.06	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	380.22	345.78	305.99	MHz
	FIFO 32 x 18 bit	22	1	0	380.22	345.78	305.99	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	400.0	347.94	290.02	MHz
	True dual-port RAM 128 × 18 bit	0	1	0	400.0	347.94	290.02	MHz
	FIFO 128 × 36 bit	22	1	0	400.0	347.94	290.02	MHz

Table 5–34. Stratix II Performance Notes (Part 2 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory M-RAM block	Single port RAM 4K × 144 bit	0	1	0	400.0	348.43	289.85	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	400.0	348.43	289.85	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	400.0	348.43	289.85	MHz
	Single port RAM 8K × 72 bit	0	1	0	400.0	348.43	289.85	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	400.0	348.43	289.85	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	400.0	348.43	289.85	MHz
	Single port RAM 16K × 36 bit	0	1	0	400.0	348.43	289.85	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	400.0	348.43	289.85	MHz
	True dual-port RAM 16K × 36 bit	0	1	0	400.0	348.43	289.85	MHz
	Single port RAM 32K × 18 bit	0	1	0	400.0	348.43	289.85	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	400.0	348.43	289.85	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	400.0	348.43	289.85	MHz
	Single port RAM 64K × 9 bit	0	1	0	400.0	348.43	289.85	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	400.0	348.43	289.85	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	400.0	348.43	289.85	MHz

Table 5–34. Stratix II Performance Notes (Part 3 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
DSP block	9 × 9-bit multiplier *(3)*	0	0	1	420.16	365.49	304.5	MHz
	18 × 18-bit multiplier *(3)*	0	0	1	420.16	365.49	304.5	MHz
	36 × 36-bit multiplier *(3)*	0	0	1	250.0	217.48	181.19	MHz
	36 × 36-bit multiplier *(4)*	0	0	1	420.16	365.49	304.5	MHz
	18-bit, four tap FIR filter	0	0	1	420.16	365.49	304.5	MHz
Larger Designs	8-bit,16 tap parallel FIR filter	58	0	4	254.77	222.41	175.65	MHz
	8-bit, 1024-point, streaming, three multipliers and five adders FFT function	2976	19	9	308.83	270.27	219.15	MHz
	8-bit, 1024-point, streaming, four multipliers and two adders FFT function	2781	19	12	377.78	338.18	279.56	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, three multipliers and five adders FFT function	984	5	3	400.0	343.17	235.96	MHz
	8-bit, 1024-point, single output, one parallel FFT engine, burst, four multipliers and two adders FFT function	919	5	4	400.0	347.94	290.02	MHz

Table 5–34. Stratix II Performance Notes (Part 4 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
Larger Designs	8-bit, 1024-point, single output, two parallel FFT engines, burst, three multiplier and five adders FFT function	1725	7	6	320.51	279.95	269.39	MHz
	8-bit, 1024-point, single output, two parallel FFT engines, burst, four multipliers and two adders FFT function	1594	7	8	389.25	338.52	277.93	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, burst, three multipliers and five adders FFT function	2361	7	9	356.25	278.78	259.67	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, burst, four multipliers and two adders FFT function	2165	7	12	276.16	330.68	283.76	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, burst, three multipliers and five adders FFT function	3996	11	18	293.59	304.87	193.38	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, burst, four multipliers and two adders FFT function	3604	11	24	360.75	335.12	279.17	MHz

Table 5–34. Stratix II Performance Notes (Part 5 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
Larger Designs	8-bit, 1024-point, quadrant output, four parallel FFT engines, burst, three multipliers and five adders FFT function	6850	22	36	277.08	268.88	227.32	MHz
	8-bit, 1024-point, quadrant output, four parallel FFT engines, burst, four multipliers two adders FFT function	6067	22	48	334.44	308.54	253.67	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, buffered burst, three multipliers and adders FFT function	2730	15	9	323.2	311.33	269.61	MHz
	8-bit, 1024-point, quadrant output, one parallel FFT engine, buffered burst, four multipliers and two adders FFT function	2534	15	12	400.0	322.26	278.08	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, buffered burst, three multipliers five adders FFT function	4358	19	18	329.92	272.25	227.01	MHz
	8-bit, 1024-point, quadrant output, two parallel FFT engines, buffered burst four multipliers and two adders FFT function	3966	19	24	373.97	320.1	209.59	MHz

Table 5–34. Stratix II Performance Notes (Part 6 of 6) *Notes (1)*

Applications		Resources Used			Performance			
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
Larger Designs	8-bit, 1024-point, quadrant output, four parallel FFT engines, buffered burst, three multipliers five adders FFT function	7385	38	36	284.25	249.62	189.1	MHz
	8-bit, 1024-point, quadrant output, four parallel FFT engines, buffered burst, four multipliers and two adders FFT function	6601	38	48	344.82	279.32	212.63	MHz

Notes for Table 5–34:
(1) These design performance numbers were obtained using the Quartus II software version 4.2.
(2) This application uses registered inputs and outputs.
(3) This application uses registered multiplier input and output stages within the DSP block.
(4) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Internal Timing Parameters

See Tables 5–35 through 5–40 for internal timing parameters.

Table 5–35. LE_FF Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{SU}	LE register setup time before clock	91		105		126		ps
t_{H}	LE register hold time after clock	149		171		206		ps
t_{CO}	LE register clock-to-output delay		95		110		132	ps
t_{CLR}	Minimum clear pulse width	206		236		284		ps
t_{PRE}	Minimum preset pulse width	206		236		284		ps
t_{CLKL}	Minimum clock low time	618		710		852		ps
t_{CLKH}	Minimum clock high time	618		710		852		ps

Table 5–36. IOE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{SU}	IOE input and output register setup time before clock	72		82		99		ps
t_{H}	IOE input and output register hold time after clock	72		82		99		ps
t_{CO}	IOE input and output register clock-to-output delay		169		194		233	ps
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output		529		608		730	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output		748		860		1,032	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin		1,678		1,929		2,314	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin		1,675		1,925		2,311	ps
t_{CLR}	Minimum clear pulse width	200			229		276	ps
t_{PRE}	Minimum preset pulse width	200		229		276		ps
t_{CLKL}	Minimum clock low time	600		690		827		ps
t_{CLKH}	Minimum clock high time	600		690		827		ps

Table 5–37. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		57		69		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		206		248		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay		0		0		0	ps
$t_{INREG2PIPE9}$	Input Register to DSP Block pipeline register in 9 × 9-bit mode		2,030		2,334		2,801	ps
$t_{INREG2PIPE18}$	Input Register to DSP Block pipeline register in 18 × 18-bit mode		2,010		2,311		2,773	ps

Table 5–37. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE36}$	Input Register to DSP Block pipeline register in 36 × 36-bit mode		2,010		2,311		2,773	ps
$t_{PIPE2OUTREG2ADD}$	DSP Block Pipeline Register to output register delay in Two-Multipliers Adder mode		1,450		1,667		2,000	ps
$t_{PIPE2OUTREG4ADD}$	DSP Block Pipeline Register to output register delay in Four-Multipliers Adder mode		1,850		2,127		2,553	ps
t_{PD9}	Combinational input to output delay for 9 × 9		2,880		3,312		3,973	ps
t_{PD18}	Combinational input to output delay for 18 × 18		2,990		3,438		4,125	ps
t_{PD36}	Combinational input to output delay for 36 × 36		4,450		5,117		6,140	ps
t_{CLR}	Minimum clear pulse width	2,212		2,543		3,052		ps
t_{CLKL}	Minimum clock low time	1,190		1,368		1,642		ps
t_{CLKH}	Minimum clock high time	1,190		1,368		1,642		ps

Table 5–38. M512 Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{M512RC}	Synchronous read cycle time		2,829		3,134		3,579	ps
$t_{M512WERESU}$	Write or read enable setup time before clock	22		24		27		ps
$t_{M512WEREH}$	Write or read enable hold time after clock	203		223		252		ps
$t_{M512DATASU}$	Data setup time before clock	22		24		27		ps
$t_{M512DATAH}$	Data hold time after clock	203		223		252		ps
$t_{M512WADDRSU}$	Write address setup time before clock	22		24		27		ps
$t_{M512WADDRH}$	Write address hold time after clock	203		223		252		ps
$t_{M512RADDRSU}$	Read address setup time before clock	22		24		27		ps

Table 5–38. M512 Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
$t_{M512RADDRH}$	Read address hold time after clock	203		223		252		ps
$t_{M512DATACO1}$	Clock-to-output delay when using output registers		478		545		649	ps
$t_{M512DATACO2}$	Clock-to-output delay without output registers		2,865		3,171		3,617	ps
$t_{M512CLKL}$	Minimum clock low time	1,315		1,446		1,634		ps
$t_{M512CLKH}$	Minimum clock high time	1,315		1,446		1,634		ps
$t_{M512CLR}$	Minimum clear pulse width	144		158		178		ps

Note to Table 5–38:
(1) F_{MAX} of M512 Block obtained using the Quartus II software does not necessarily equal to 1/TM512RC.

Table 5–39. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{M4KRC}	Synchronous read cycle time		2,240		2,575		3,089	ps
$t_{M4KWERESU}$	Write or read enable setup time before clock	22		25		30		ps
$t_{M4KWEREH}$	Write or read enable hold time after clock	203		233		280		ps
$t_{M4KBESU}$	Byte enable setup time before clock	22		25		30		ps
t_{M4KBEH}	Byte enable hold time after clock	203		233		280		ps
$t_{M4KDATAASU}$	A port data setup time before clock	22		25		30		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		233		280		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		25		30		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		233		280		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		25		30		ps
$t_{M4KDATABH}$	B port data hold time after clock	203		233		280		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		25		30		ps

Table 5–39. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
$t_{M4KRADDRBH}$	B port address hold time after clock	203		233		280		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers		526		604		725	ps
$t_{M4KDATACO2}$	Clock-to-output delay without output registers		2,460		2,828		3,393	ps
$t_{M4KCLKH}$	Minimum clock high time	1,250		1,437		1,724		ps
$t_{M4KCLKL}$	Minimum clock low time	1,250		1,437		1,724		ps
t_{M4KCLR}	Minimum clear pulse width	144		165		198		ps

Note to Table 5–39:

(1) F_{MAX} of M4K Block obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.

Table 5–40. M-RAM Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
t_{MEGARC}	Synchronous read cycle time		2,688		3,090		3,708	ps
$t_{MEGAWERESU}$	Write or read enable setup time before clock	22		25		30		ps
$t_{MEGAWEREH}$	Write or read enable hold time after clock	203		233		280		ps
$t_{MEGABESU}$	Byte enable setup time before clock	22		25		30		ps
$t_{MEGABEH}$	Byte enable hold time after clock	203		233		280		ps
$t_{MEGADATAASU}$	A port data setup time before clock	22		25		30		ps
$t_{MEGADATAAH}$	A port data hold time after clock	203		233		280		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	22		25		30		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	203		233		280		ps
$t_{MEGADATABSU}$	B port setup time before clock	22		25		30		ps
$t_{MEGADATABH}$	B port hold time after clock	203		233		280		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	22		25		30		ps

Table 5–40. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
$t_{MEGAADDRBH}$	B port address hold time after clock	203		233		280		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers		715		821		986	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers		2,803		3,222		3,866	ps
$t_{MEGACLKL}$	Minimum clock low time	1,250		1,437		1,724		ps
$t_{MEGACLKH}$	Minimum clock high time	1,250		1,437		1,724		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		165		198		ps

Note to Table 5–40:
(1) F_{MAX} of M-RAM Block obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.

Stratix II Clock Timing Parameters

See Tables 5–41 through 5–65 for Stratix II clock timing parameters.

Table 5–41. Stratix II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2S15 Clock Timing Parameters

Tables 5–42 though 5–45 show the maximum clock timing parameters for EP2S15 devices.

Table 5–42. EP2S15 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.205	2.689	3.213	ns
t_{COUT}	1.950	2.396	2.861	ns
t_{PLLCIN}	0.418	0.467	0.546	ns
$t_{PLLCOUT}$	0.163	0.174	0.194	ns

Table 5–43. EP2S15 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.341	2.680	3.202	ns
t_{COUT}	2.086	2.387	2.850	ns
t_{PLLCIN}	0.445	0.499	0.587	ns
$t_{PLLCOUT}$	0.190	0.206	0.235	ns

Table 5–44. EP2S15 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	1.941	2.403	2.869	ns
t_{COUT}	1.940	2.402	2.868	ns
t_{PLLCIN}	0.158	0.169	0.190	ns
$t_{PLLCOUT}$	0.157	0.168	0.189	ns

Table 5–45. EP2S15 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.103	2.406	2.873	ns
t_{COUT}	2.102	2.405	2.872	ns
t_{PLLCIN}	0.205	0.223	0.256	ns
$t_{PLLCOUT}$	0.204	0.222	0.255	ns

EP2S30 Clock Timing Parameters

Tables 5–46 through 5–49 show the maximum clock timing parameters for EP2S30 devices.

Table 5–46. EP2S30 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.334	2.672	3.196	ns
t_{COUT}	2.079	2.379	2.844	ns
t_{PLLCIN}	0.368	0.407	0.477	ns
$t_{PLLCOUT}$	0.113	0.114	0.125	ns

Table 5–47. EP2S30 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.510	2.873	3.435	ns
t_{COUT}	2.255	2.580	3.083	ns
t_{PLLCIN}	0.442	0.494	0.581	ns
$t_{PLLCOUT}$	0.187	0.201	0.229	ns

Table 5–48. EP2S30 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.026	2.316	2.767	ns
t_{COUT}	2.025	2.315	2.766	ns
t_{PLLCIN}	0.080	0.077	0.080	ns
$t_{PLLCOUT}$	0.079	0.076	0.079	ns

Table 5–49. EP2S30 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.234	2.554	3.054	ns
t_{COUT}	2.233	2.553	3.053	ns
t_{PLLCIN}	0.170	0.183	0.208	ns
$t_{PLLCOUT}$	0.169	0.182	0.207	ns

EP2S60 Clock Timing Parameters

Tables 5–50 through 5–53 show the maximum clock timing parameters for EP2S60 devices.

Table 5–50. EP2S60 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.590	2.965	3.545	ns
t_{COUT}	2.335	2.672	3.193	ns
t_{PLLCIN}	0.486	0.545	0.643	ns
$t_{PLLCOUT}$	0.231	0.252	0.291	ns

Table 5–51. EP2S60 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.779	3.184	3.807	ns
t_{COUT}	2.524	2.891	3.455	ns
t_{PLLCIN}	0.491	0.551	0.648	ns
$t_{PLLCOUT}$	0.236	0.258	0.296	ns

Table 5–52. EP2S60 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.312	2.646	3.163	ns
t_{COUT}	2.311	2.645	3.162	ns
t_{PLLCIN}	0.217	0.235	0.271	ns
$t_{PLLCOUT}$	0.216	0.234	0.270	ns

Table 5–53. EP2S60 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.533	2.900	3.467	ns
t_{COUT}	2.532	2.899	3.466	ns
t_{PLLCIN}	0.247	0.270	0.312	ns
$t_{PLLCOUT}$	0.246	0.269	0.311	ns

EP2S90 Clock Timing Parameters

Tables 5–54 through 5–57 show the maximum clock timing parameters for EP2S90 devices.

Table 5–54. EP2S90 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.686	3.075	3.678	ns
t_{COUT}	2.431	2.782	3.326	ns
t_{PLLCIN}	0.355	0.372	0.434	ns
$t_{PLLCOUT}$	0.080	0.079	0.082	ns

Table 5–55. EP2S90 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.967	3.398	4.068	ns
t_{COUT}	2.712	3.105	3.716	ns
t_{PLLCIN}	0.316	0.350	0.411	ns
$t_{PLLCOUT}$	0.061	0.057	0.059	ns

Table 5–56. EP2S90 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.390	2.737	3.271	ns
t_{COUT}	2.389	2.736	3.270	ns
t_{PLLCIN}	0.055	0.048	0.048	ns
$t_{PLLCOUT}$	0.054	0.047	0.047	ns

Table 5–57. EP2S90 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.701	3.093	3.699	ns
t_{COUT}	2.700	3.092	3.698	ns
t_{PLLCIN}	0.059	0.053	0.053	ns
$t_{PLLCOUT}$	0.058	0.052	0.052	ns

EP2S130 Clock Timing Parameters

Tables 5–58 through 5–61 show the maximum clock timing parameters for EP2S130 devices.

Table 5–58. EP2S130 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.881	3.301	3.948	ns
t_{COUT}	2.626	3.008	3.596	ns
t_{PLLCIN}	0.496	0.557	0.656	ns
$t_{PLLCOUT}$	0.241	0.264	0.304	ns

Table 5–59. EP2S130 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	3.207	3.675	4.397	ns
t_{COUT}	2.952	3.382	4.045	ns
t_{PLLCIN}	0.558	0.628	0.743	ns
$t_{PLLCOUT}$	0.303	0.335	0.391	ns

Table 5–60. EP2S130 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.628	3.008	3.596	ns
t_{COUT}	2.627	3.007	3.595	ns
t_{PLLCIN}	0.252	0.277	0.321	ns
$t_{PLLCOUT}$	0.251	0.276	0.320	ns

Table 5–61. EP2S130 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.941	3.368	4.028	ns
t_{COUT}	2.940	3.367	4.027	ns
t_{PLLCIN}	0.297	0.326	0.379	ns
$t_{PLLCOUT}$	0.296	0.325	0.378	ns

EP2S180 Clock Timing Parameters

Tables 5–62 through 5–65 show the maximum clock timing parameters for EP2S180 devices.

Table 5–62. EP2S180 Column Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	3.048	3.493	4.178	ns
t_{COUT}	2.793	3.200	3.826	ns
t_{PLLCIN}	0.316	0.347	0.407	ns
$t_{PLLCOUT}$	0.061	0.054	0.055	ns

Table 5–63. EP2S180 Column Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	3.386	3.882	4.646	ns
t_{COUT}	3.131	3.589	4.294	ns
t_{PLLCIN}	0.279	0.307	0.359	ns
$t_{PLLCOUT}$	0.024	0.014	0.007	ns

Table 5–64. EP2S180 Row Pins Regional Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	2.737	3.134	3.746	ns
t_{COUT}	2.736	3.133	3.745	ns
t_{PLLCIN}	0.032	0.022	0.015	ns
$t_{PLLCOUT}$	0.031	0.021	0.014	ns

Table 5–65. EP2S180 Row Pins Global Clock Timing Parameters

Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
t_{CIN}	3.109	3.561	4.262	ns
t_{COUT}	3.108	3.560	4.261	ns
t_{PLLCIN}	0.017	0.005	-0.005	ns
$t_{PLLCOUT}$	0.016	0.004	-0.006	ns

IOE Programmable Delay

See Tables 5–66 and 5–67 for IOE programmable delay.

Table 5–66. Stratix II IOE Programmable Delay on Column Pins *Note (1)*

Parameter	Paths Affected	Number of Settings	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0	2,883	0	3,315	0	3,978	ps
Input delay from pin to input register	Pad to I/O input register	64	0	3,277	0	3,768	0	4,521	ps
Delay from output register to output pin	I/O output register to pad	2	0	500	0	575	0	690	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	483	0	556	0	667	ps

Notes to Table 5–66:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

Table 5–67. Stratix II IOE Programmable Delay on Row Pins *Note (1)*

Parameter	Paths Affected	Number of Settings	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0	2,883	0	3,315	0	3,978	ps
Input delay from pin to input register	Pad to I/O input register	64	0	3,277	0	3,768	0	4,521	ps
Delay from output register to output pin	I/O output register to pad	2	0	500	0	575	0	690	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	483	0	556	0	667	ps

Note to Table 5–67:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 5–68 for default capacitive loading of different I/O standards.

Table 5–68. Default Loading of Different I/O Standards for Stratix II

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 class I	0	pF
SSTL-2 class II	0	pF
SSTL-18 class I	0	pF
SSTL-18 class II	0	pF
1.5-V HSTL class I	0	pF
1.5-V HSTL class II	0	pF
1.8-V HSTL class I	0	pF
1.8-V HSTL class II	0	pF
Differential SSTL-2 class I	0	pF
Differential SSTL-2 class II	0	pF
Differential SSTL-18 class I	0	pF
Differential SSTL-18 class II	0	pF
1.5-V differential HSTL class I	0	pF
1.5-V differential HSTL class II	0	pF
1.8-V differential HSTL class I	0	pF
1.8-V differential HSTL class II	0	pF
LVDS	0	pF
HyperTransport	0	pF
LVPECL	0	pF

I/O Delays

See Tables 5–69 through 5–73 for I/O delays.

Table 5–69. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–70. Stratix II I/O Input Delay for Column Pins (Part 1 of 2)

I/O Standard	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	t_{PI}	870	999	1199	ps
	t_{PCOUT}	757	870	1044	ps
2.5 V	t_{PI}	857	984	1181	ps
	t_{PCOUT}	744	855	1026	ps
1.8 V	t_{PI}	1013	1164	1397	ps
	t_{PCOUT}	900	1035	1242	ps
1.5 V	t_{PI}	1083	1244	1493	ps
	t_{PCOUT}	970	1115	1338	ps
LVCMOS	t_{PI}	870	999	1199	ps
	t_{PCOUT}	757	870	1044	ps
SSTL-2 class I	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
SSTL-2 class II	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
SSTL-18 class I	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
SSTL-18 class II	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
1.5-V HSTL class I	t_{PI}	640	735	882	ps
	t_{PCOUT}	527	606	727	ps

Table 5–70. Stratix II I/O Input Delay for Column Pins (Part 2 of 2)

I/O Standard	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.5-V HSTL class II	t_{PI}	640	735	882	ps
	t_{PCOUT}	527	606	727	ps
1.8-V HSTL class I	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
1.8-V HSTL class II	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
PCI	t_{PI}	861	989	1187	ps
	t_{PCOUT}	748	860	1032	ps
PCI-X	t_{PI}	861	989	1187	ps
	t_{PCOUT}	748	860	1032	ps
Differential SSTL-2 class I	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
Differential SSTL-2 class II	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
Differential SSTL-18 class I	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
Differential SSTL-18 class II	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
1.8-V differential HSTL class I	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
1.8-V differential HSTL class II	t_{PI}	545	625	751	ps
	t_{PCOUT}	432	496	596	ps
1.5-V differential HSTL class I	t_{PI}	640	735	882	ps
	t_{PCOUT}	527	606	727	ps
1.5-V differential HSTL class II	t_{PI}	640	735	882	ps
	t_{PCOUT}	527	606	727	ps

Table 5–71. Stratix II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	t_{PI}	873	1002	1203	ps
	t_{PCOUT}	760	873	1048	ps
2.5 V	t_{PI}	859	986	1184	ps
	t_{PCOUT}	746	857	1029	ps
1.8 V	t_{PI}	1013	1164	1397	ps
	t_{PCOUT}	900	1035	1242	ps
1.5 V	t_{PI}	1084	1245	1494	ps
	t_{PCOUT}	971	1116	1339	ps
LVCMOS	t_{PI}	873	1002	1203	ps
	t_{PCOUT}	760	873	1048	ps
SSTL-2 class I	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
SSTL-2 class II	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
SSTL-18 class I	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
SSTL-18 class II	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
1.5-V HSTL class I	t_{PI}	642	737	885	ps
	t_{PCOUT}	529	608	730	ps
1.5-V HSTL class II	t_{PI}	642	737	885	ps
	t_{PCOUT}	529	608	730	ps
1.8-V HSTL class I	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
1.8-V HSTL class II	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
Differential SSTL-2 class I	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
Differential SSTL-2 class II	t_{PI}	465	533	640	ps
	t_{PCOUT}	352	404	485	ps
Differential SSTL-18 class I	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps

Table 5–71. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 class II	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
1.8-V differential HSTL class I	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
1.8-V differential HSTL class II	t_{PI}	546	626	752	ps
	t_{PCOUT}	433	497	597	ps
1.5-V differential HSTL class I	t_{PI}	642	737	885	ps
	t_{PCOUT}	529	608	730	ps
1.5-V differential HSTL class II	t_{PI}	642	737	885	ps
	t_{PCOUT}	529	608	730	ps
LVDS	t_{PI}	534	613	735	ps
	t_{PCOUT}	421	484	580	ps
HyperTransport	t_{PI}	534	613	735	ps
	t_{PCOUT}	421	484	580	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 1 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	t_{OP}	1900	2184	2621	ps
		t_{DIP}	1920	2207	2649	ps
	8 mA	t_{OP}	1774	2039	2447	ps
		t_{DIP}	1794	2062	2475	ps
	12 mA	t_{OP}	1775	2040	2449	ps
		t_{DIP}	1795	2063	2477	ps
	16 mA	t_{OP}	1691	1943	2333	ps
		t_{DIP}	1711	1966	2361	ps
	20 mA	t_{OP}	1655	1902	2283	ps
		t_{DIP}	1675	1925	2311	ps
	24 mA *(1)*	t_{OP}	1655	1902	2283	ps
		t_{DIP}	1675	1925	2311	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 2 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVCMOS	4 mA	t_{OP}	1774	2039	2447	ps
		t_{DIP}	1794	2062	2475	ps
	8 mA	t_{OP}	1654	1901	2282	ps
		t_{DIP}	1674	1924	2310	ps
	12 mA	t_{OP}	1624	1866	2240	ps
		t_{DIP}	1644	1889	2268	ps
	16 mA	t_{OP}	1607	1847	2217	ps
		t_{DIP}	1627	1870	2245	ps
	20 mA	t_{OP}	1596	1834	2201	ps
		t_{DIP}	1616	1857	2229	ps
	24 mA *(1)*	t_{OP}	1581	1817	2181	ps
		t_{DIP}	1601	1840	2209	ps
2.5 V	4 mA	t_{OP}	1785	2051	2462	ps
		t_{DIP}	1805	2074	2490	ps
	8 mA	t_{OP}	1639	1883	2261	ps
		t_{DIP}	1659	1906	2289	ps
	12 mA	t_{OP}	1606	1845	2215	ps
		t_{DIP}	1626	1868	2243	ps
	16 mA *(1)*	t_{OP}	1582	1818	2182	ps
		t_{DIP}	1602	1841	2210	ps
1.8 V	2 mA	t_{OP}	2226	2559	3071	ps
		t_{DIP}	2246	2582	3099	ps
	4 mA	t_{OP}	1895	2178	2614	ps
		t_{DIP}	1915	2201	2642	ps
	6 mA	t_{OP}	1751	2012	2415	ps
		t_{DIP}	1771	2035	2443	ps
	8 mA	t_{OP}	1684	1935	2323	ps
		t_{DIP}	1704	1958	2351	ps
	10 mA	t_{OP}	1625	1867	2242	ps
		t_{DIP}	1645	1890	2270	ps
	12 mA *(1)*	t_{OP}	1625	1867	2242	ps
		t_{DIP}	1645	1890	2270	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 3 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.5 V	2 mA	t_{OP}	2032	2335	2803	ps
		t_{DIP}	2052	2358	2831	ps
	4 mA	t_{OP}	1752	2013	2417	ps
		t_{DIP}	1772	2036	2445	ps
	6 mA	t_{OP}	1668	1917	2301	ps
		t_{DIP}	1688	1940	2329	ps
	8 mA *(1)*	t_{OP}	1640	1885	2262	ps
		t_{DIP}	1660	1908	2290	ps
SSTL-2 class I	8 mA	t_{OP}	1600	1839	2207	ps
		t_{DIP}	1620	1862	2235	ps
	12 mA *(1)*	t_{OP}	1567	1801	2161	ps
		t_{DIP}	1587	1824	2189	ps
SSTL-2 class II	16 mA	t_{OP}	1528	1756	2108	ps
		t_{DIP}	1548	1779	2136	ps
	20 mA	t_{OP}	1522	1749	2099	ps
		t_{DIP}	1542	1772	2127	ps
	24 mA *(1)*	t_{OP}	1520	1747	2097	ps
		t_{DIP}	1540	1770	2125	ps
SSTL-18 class I	4 mA	t_{OP}	1577	1812	2175	ps
		t_{DIP}	1597	1835	2203	ps
	6 mA	t_{OP}	1557	1789	2148	ps
		t_{DIP}	1577	1812	2176	ps
	8 mA	t_{OP}	1545	1775	2131	ps
		t_{DIP}	1565	1798	2159	ps
	10 mA	t_{OP}	1537	1766	2120	ps
		t_{DIP}	1557	1789	2148	ps
	12 mA *(1)*	t_{OP}	1537	1766	2120	ps
		t_{DIP}	1557	1789	2148	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 class II	8 mA	t_{OP}	1519	1745	2095	ps
		t_{DIP}	1539	1768	2123	ps
	16 mA	t_{OP}	1512	1737	2086	ps
		t_{DIP}	1532	1760	2114	ps
	18 mA	t_{OP}	1517	1743	2092	ps
		t_{DIP}	1537	1766	2120	ps
	20 mA *(1)*	t_{OP}	1515	1741	2090	ps
		t_{DIP}	1535	1764	2118	ps
1.8-V HSTL class I	4 mA	t_{OP}	1562	1795	2155	ps
		t_{DIP}	1582	1818	2183	ps
	6 mA	t_{OP}	1545	1775	2131	ps
		t_{DIP}	1565	1798	2159	ps
	8 mA	t_{OP}	1536	1765	2119	ps
		t_{DIP}	1556	1788	2147	ps
	10 mA	t_{OP}	1531	1759	2112	ps
		t_{DIP}	1551	1782	2140	ps
	12 mA *(1)*	t_{OP}	1531	1759	2112	ps
		t_{DIP}	1551	1782	2140	ps
1.8-V HSTL class II	16 mA	t_{OP}	1507	1732	2079	ps
		t_{DIP}	1527	1755	2107	ps
	18 mA	t_{OP}	1509	1734	2081	ps
		t_{DIP}	1529	1757	2109	ps
	20 mA *(1)*	t_{OP}	1507	1732	2079	ps
		t_{DIP}	1527	1755	2107	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 5 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.5-V HSTL class I	4 mA	t_{OP}	1563	1796	2156	ps
		t_{DIP}	1583	1819	2184	ps
	6 mA	t_{OP}	1545	1775	2131	ps
		t_{DIP}	1565	1798	2159	ps
	8 mA	t_{OP}	1540	1770	2124	ps
		t_{DIP}	1560	1793	2152	ps
	10 mA	t_{OP}	1535	1764	2117	ps
		t_{DIP}	1555	1787	2145	ps
	12 mA *(1)*	t_{OP}	1535	1764	2117	ps
		t_{DIP}	1555	1787	2145	ps
1.5-V HSTL class II	16 mA	t_{OP}	1504	1728	2075	ps
		t_{DIP}	1524	1751	2103	ps
	18 mA	t_{OP}	1502	1726	2072	ps
		t_{DIP}	1522	1749	2100	ps
	20 mA	t_{OP}	1510	1735	2083	ps
		t_{DIP}	1530	1758	2111	ps
	24 mA *(1)*	t_{OP}	246	282	339	ps
		t_{DIP}	266	305	367	ps
PCI		t_{OP}	1819	2060	2117	ps
		t_{DIP}	1839	2083	2145	ps
PCI-X		t_{OP}	1819	2060	2117	ps
		t_{DIP}	1839	2083	2145	ps
Differential SSTL-2 class I		t_{OP}	1567	1801	2161	ps
		t_{DIP}	1587	1824	2189	ps
Differential SSTL-2 class II		t_{OP}	1520	1747	2097	ps
		t_{DIP}	1540	1770	2125	ps
Differential SSTL-18 class I		t_{OP}	1537	1766	2120	ps
		t_{DIP}	1557	1789	2148	ps
Differential SSTL-18 class II		t_{OP}	1515	1741	2090	ps
		t_{DIP}	1535	1764	2118	ps
1.8-V differential HSTL class I		t_{OP}	1531	1759	2112	ps
		t_{DIP}	1551	1782	2140	ps

Table 5–72. Stratix II I/O Output Delay for Column Pins (Part 6 of 6)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V differential HSTL class II		t_{OP}	1507	1732	2079	ps
		t_{DIP}	1527	1755	2107	ps
1.5-V differential HSTL class I		t_{OP}	1535	1764	2117	ps
		t_{DIP}	1555	1787	2145	ps
1.5-V differential HSTL class II		t_{OP}	246	282	339	ps
		t_{DIP}	266	305	367	ps

Note to Table 5–72:
(1) This is the default setting in Quartus II software.

Table 5–73. Stratix II I/O Output Delay for Row Pins (Part 1 of 3)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	t_{OP}	1716	1973	2367	ps
		t_{DIP}	1716	1973	2367	ps
	8 mA	t_{OP}	1677	1928	2313	ps
		t_{DIP}	1677	1928	2313	ps
	12 mA	t_{OP}	1678	1929	2314	ps
		t_{DIP}	1678	1929	2314	ps
LVCMOS	4 mA	t_{OP}	1677	1928	2313	ps
		t_{DIP}	1677	1928	2313	ps
	8 mA	t_{OP}	1577	1813	2175	ps
		t_{DIP}	1577	1813	2175	ps
	12 mA	t_{OP}	1553	1785	2142	ps
		t_{DIP}	1553	1785	2142	ps
2.5 V	4 mA	t_{OP}	1662	1911	2292	ps
		t_{DIP}	1662	1911	2292	ps
	8 mA	t_{OP}	1552	1784	2141	ps
		t_{DIP}	1552	1784	2141	ps
	12 mA	t_{OP}	1534	1764	2116	ps
		t_{DIP}	1534	1764	2116	ps

Table 5–73. Stratix II I/O Output Delay for Row Pins (Part 2 of 3)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8 V	2 mA	t_{OP}	1861	2140	2567	ps
		t_{DIP}	1861	2140	2567	ps
	4 mA	t_{OP}	1710	1966	2359	ps
		t_{DIP}	1710	1966	2359	ps
	6 mA	t_{OP}	1625	1868	2241	ps
		t_{DIP}	1625	1868	2241	ps
	8 mA	t_{OP}	1570	1805	2165	ps
		t_{DIP}	1570	1805	2165	ps
1.5 V	2 mA	t_{OP}	1784	2051	2461	ps
		t_{DIP}	1784	2051	2461	ps
	4 mA	t_{OP}	1718	1975	2370	ps
		t_{DIP}	1718	1975	2370	ps
SSTL-2 class I	8 mA	t_{OP}	1550	1782	2138	ps
		t_{DIP}	1550	1782	2138	ps
	12 mA *(1)*	t_{OP}	1524	1752	2102	ps
		t_{DIP}	1524	1752	2102	ps
SSTL-2 class II	16 mA	t_{OP}	1476	1697	2036	ps
		t_{DIP}	1476	1697	2036	ps
	20 mA	t_{OP}	307	353	423	ps
		t_{DIP}	307	353	423	ps
SSTL-18 class I	4 mA	t_{OP}	1525	1753	2103	ps
		t_{DIP}	1525	1753	2103	ps
	6 mA	t_{OP}	1500	1724	2069	ps
		t_{DIP}	1500	1724	2069	ps
	8 mA	t_{OP}	1495	1719	2062	ps
		t_{DIP}	1495	1719	2062	ps
	10 mA	t_{OP}	307	353	423	ps
		t_{DIP}	307	353	423	ps
	12 mA *(1)*	t_{OP}	307	353	423	ps
		t_{DIP}	307	353	423	ps
Differential SSTL-2 class I		t_{OP}	1524	1752	2102	ps
		t_{DIP}	1524	1752	2102	ps

Table 5–73. Stratix II I/O Output Delay for Row Pins (Part 3 of 3)

I/O Standard	Drive Strength	Parameter	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 class II		t_{OP}	307	353	423	ps
		t_{DIP}	307	353	423	ps
Differential SSTL-18 class I		t_{OP}	307	353	423	ps
		t_{DIP}	307	353	423	ps
LVDS		t_{OP}	2787	3205	3845	ps
		t_{DIP}	2787	3205	3845	ps
HyperTransport		t_{OP}	2787	3205	3845	ps
		t_{DIP}	2787	3205	3845	ps

Note to Table 5–73:
(1) This is the default setting in Quartus II software.

Maximum Input & Output Clock Rates

See Tables 5–74 through 5–77 for maximum I/O clock rates.

Table 5–74. Stratix II Maximum Input Clock Rate for Column Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	422	422	358	MHz
2.5 V	422	422	358	MHz
1.8 V	422	422	358	MHz
1.5 V	422	422	358	MHz
LVCMOS	422	422	358	MHz
SSTL-2 class I	400	400	340	MHz
SSTL-2 CLASS II	400	400	340	MHz
SSTL-18 class I	400	400	340	MHz
SSTL-18 class II	400	400	340	MHz
1.5-V HSTL class I	400	400	340	MHz
1.5-V HSTL class II	400	400	340	MHz
1.8-V HSTL class I	400	400	340	MHz
1.8-V HSTL class II	400	400	340	MHz
PCI	420	420	357	MHz
PCI-X	420	420	357	MHz
Differential SSTL-2 class I	400	400	340	MHz

Table 5–74. Stratix II Maximum Input Clock Rate for Column Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 class II	400	400	340	MHz
Differential SSTL-18 class I	400	400	340	MHz
Differential SSTL-18 class II	400	400	340	MHz
1.8-V differential HSTL class I	400	400	340	MHz
1.8-V differential HSTL class II	400	400	340	MHz
1.5-V differential HSTL class I	400	400	340	MHz
1.5 V differential HSTL class II	400	400	340	MHz

Table 5–75. Stratix II Maximum Input Clock Rate for Row Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	422	422	358	MHz
2.5 V	422	422	358	MHz
1.8 V	422	422	358	MHz
1.5 V	422	422	358	MHz
LVCMOS	422	422	358	MHz
SSTL -2 class I	400	400	340	MHz
SSTL-2 class II	400	400	340	MHz
SSTL-18 class I	400	400	340	MHz
SSTL-18 class II	400	400	340	MHz
1.5-V HSTL class I	400	400	340	MHz
1.5-V HSTL class II	400	400	340	MHz
1.8-V HSTL class I	400	400	340	MHz
1.8-V HSTL class II	400	400	340	MHz
PCI	422	422	358	MHz
PCI-X	422	422	358	MHz
Differential SSTL-2 class I	400	400	340	MHz
Differential SSTL-2 class II	400	400	340	MHz
Differential SSTL-18 class I	400	400	340	MHz
Differential SSTL-18 class II	400	400	340	MHz
1.8-V differential HSTL class I	400	400	340	MHz
1.8-V differential HSTL class II	400	400	340	MHz
1.5-V differential HSTL class I	400	400	340	MHz
1.5-V differential HSTL class II	400	400	340	MHz

Table 5–75. Stratix II Maximum Input Clock Rate for Row Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVDS	500	500	425	MHz
HyperTransport	520	520	442	MHz

Table 5–76. Stratix II Maximum Output Clock Rate for Column Pins (Part 1 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
	16 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz
LVCMOS	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
	16 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz
2.5 V	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
	16 mA *(1)*	350	350	297	MHz
1.8 V	2 mA	350	350	297	MHz
	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
1.5 V	2 mA	350	350	297	MHz
	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA *(1)*	350	350	297	MHz
SSTL-2 class I	8 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz

Table 5–76. Stratix II Maximum Output Clock Rate for Column Pins (Part 2 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-2 class II	16 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz
SSTL-18 class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
SSTL-18 class II	8 mA	350	350	297	MHz
	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA *(1)*	350	350	297	MHz
1.8-V HSTL class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
1.8-V HSTL class II	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA *(1)*	350	350	297	MHz
1.5-V HSTL class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
1.5-V HSTL class II	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz
PCI		350	350	297	MHz
PCI-X		350	350	297	MHz
Differential SSTL-2 class I	8 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz

Table 5–76. Stratix II Maximum Output Clock Rate for Column Pins (Part 3 of 3)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 class II	16 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz
Differential SSTL-18 class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
Differential SSTL-18 class II	8 mA	350	350	297	MHz
	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA *(1)*	350	350	297	MHz
1.8-V differential HSTL class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
1.8-V differential HSTL class II	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA *(1)*	350	350	297	MHz
1.5-V differential HSTL class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
1.5-V differential HSTL class II	16 mA	350	350	297	MHz
	18 mA	350	350	297	MHz
	20 mA	350	350	297	MHz
	24 mA *(1)*	350	350	297	MHz

Note to Table 5–76:
(1) This is the1 default setting in Quartus II software.

Table 5–77. Stratix II Maximum Output Clock Rate for Row Pins (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
LVCMOS	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
2.5 V	4 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	12 mA	350	350	297	MHz
1.8 V	2 mA	350	350	297	MHz
	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
1.5 V	2 mA	350	350	297	MHz
	4mA	350	350	297	MHz
SSTL-2 class I	8 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
SSTL-2 class II	1 6mA	350	350	297	MHz
	20 mA	350	350	297	MHz
SSTL-18 class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
Differential SSTL-2 class I	8 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz
Differential SSTL-2 class II	16 mA	350	350	297	MHz
	20 mA *(1)*	350	350	297	MHz
Differential SSTL-18 class I	4 mA	350	350	297	MHz
	6 mA	350	350	297	MHz
	8 mA	350	350	297	MHz
	10 mA	350	350	297	MHz
	12 mA *(1)*	350	350	297	MHz

Table 5–77. Stratix II Maximum Output Clock Rate for Row Pins (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVDS		500	500	425	MHz
HyperTransport		520	520	442	MHz

Note to Table 5–77:
(1) This is the default setting in the Quartus II software.

High-Speed I/O Specifications

Table 5–78 provides high-speed timing specifications definitions.

Table 5–78. High-Speed Timing Specifications & Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter (peak-to-peak)	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 5–79 shows the high-speed I/O timing specifications for -3 speed grade Stratix II devices.

Table 5–79. High-Speed I/O Specifications for -3 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-3 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (Clock Frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	20		520	MHz
	W = 1 (SERDES bypass, LVDS only)	20		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz
f_{HSDR} (Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*		760	Mbps
	J = 1 (LVDS only)	*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
TCCS	All Differential Standards	-		200	ps
SW	All Differential Standards	330		-	ps
Input jitter tolerance (peak-to-peak)				*(5)*	ps
Output jitter tolerance (peak-to-peak)				*(5)*	ps
Output t_{RISE}				*(5)*	ps
Output t_{FALL}				*(5)*	ps
t_{DUTY}				*(5)*	%
t_{LOCK}				*(5)*	us
DPA run length				6,400	UI
DPA jitter tolerance (peak-to-peak)				*(5)*	UI
DPA minimum eye opening (peak-to-peak)				*(5)*	UI
DPA receiver latency				*(5)*	Number of parallel CLK cycles

Table 5–79. High-Speed I/O Specifications for -3 Speed Grade (Part 2 of 2) *Notes (1), (2)*

Symbol	Conditions			-3 Speed Grade			Unit
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Misc	10101010	100%	256			
		01010101		256			

Notes to Table 5–79:

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following FPLL VCO specification: 150 ≤ input clk frequency * W ≤ 1,040.
(4) The minimum specification is dependent on the clock source (FPLL, EPLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.
(5) This specification is pending silicon characterization.

Table 5–80 shows the high-speed I/O timing specifications for -4 speed grade Stratix II devices.

Table 5–80. High-Speed I/O Specifications for -4 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-4 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (Clock Frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	20		520	MHz
	W = 1 (SERDES bypass, LVDS only)	20		500	MHz
	W = 1 (SERDES used, LVDS only)	250		717	MHz
f_{HSDR} (Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*		760	Mbps
	J = 1 (LVDS only)	*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		1,040	Mbps
TCCS	All Differential Standards	-		200	ps
SW	All Differential Standards	330		-	ps

Table 5–80. High-Speed I/O Specifications for -4 Speed Grade (Part 2 of 2) *Notes (1), (2)*

Symbol	Conditions			-4 Speed Grade			Unit
				Min	Typ	Max	
Input jitter tolerance (peak-to-peak)						(5)	ps
Output jitter tolerance (peak-to-peak)						(5)	ps
Output t_{RISE}						(5)	ps
Output t_{FALL}						(5)	ps
t_{DUTY}						(5)	%
t_{LOCK}						(5)	us
DPA run length						6,400	UI
DPA jitter tolerance (peak-to-peak)						(5)	UI
DPA minimum eye opening (peak-to-peak)						(5)	UI
DPA receiver latency						(5)	Number of parallel CLK cycles
DPA lock time	**Standard**	**Training Pattern**	**Transition Density**				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Misc	10101010	100%	256			
		01010101		256			

Notes to Table 5–80:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following FPLL VCO specification: 150 ≤ input clk frequency * W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (FPLL, EPLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) This specification is pending silicon characterization.

Table 5–81 shows the high-speed I/O timing specifications for -5 speed grade Stratix II devices.

Table 5–81. High-Speed I/O Specifications for -5 Speed Grade Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (Clock Frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	20		420	MHz
	W = 1 (SERDES bypass, LVDS only)	20		500	MHz
	W = 1 (SERDES used, LVDS only)	250		640	MHz
f_{HSDR} (Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		840	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*		700	Mbps
	J = 1 (LVDS only)	*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA Data Rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150		840	Mbps
TCCS	All Differential Standards	-		200	ps
SW	All Differential Standards	440		-	ps
Input jitter tolerance (peak-to-peak)				*(5)*	ps
Output jitter tolerance (peak-to-peak)				*(5)*	ps
Output t_{RISE}				*(5)*	ps
Output t_{FALL}				*(5)*	ps
t_{DUTY}				*(5)*	%
t_{LOCK}				*(5)*	us
DPA run length				6,400	UI
DPA jitter tolerance (peak-to-peak)				*(5)*	UI
DPA minimum eye opening (peak-to-peak)				*(5)*	UI
DPA receiver latency				*(5)*	Number of parallel CLK cycles

Table 5–81. High-Speed I/O Specifications for -5 Speed Grade Notes (1), (2)

Symbol	Conditions			-5 Speed Grade			Unit
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density				Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Misc	10101010	100%	256			
		01010101		256			

Notes to Table 5–81:

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following FPLL VCO specification: 150 ≤ input clk frequency * W ≤ 1,040.
(4) The minimum specification is dependent on the clock source (FPLL, EPLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.
(5) This specification is pending silicon characterization.

PLL Timing Specifications

Tables 5–82 and 5–83 describe the Stratix II PLL specifications when operating within the commercial junction temperature range from 0 to 85 °C The industrial junction temperature range specifications will be available upon completion of the PLL characterization across the industrial junction temperature range from -40 to 100 °C.

Table 5–82. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	1.5		450	MHz
f_{INPFD}	Maximum input frequency to the PFD	1.5		300	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			*(1)*	ps (p-p)
$t_{EINIJITTER}$	External feedback input period jitter			*(1)*	ps (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5		500	MHz

Table 5–82. Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Unit
$t_{SCANCLK}$	Scanclk frequency			100	MHz
f_{OUT_EXT}	External PLL output frequency	1.5		450	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled		0.03	10	ms
f_{CLBW}	PLL bandwidth	0.1	1	10	MHz
f_{VCO}	PLL VCO operating range for -3 and -4 speed grade devices	300		1,040	MHz
	PLL VCO operating range for -5 speed grade devices	300		840	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by two identically programmed PLL counters			*(1)*	ps
t_{SPO}	Static phase offset of the PLL itself			*(1)*	ps
f_{SS}	Spread spectrum modulation frequency	100		500	kHz
% spread	Guaranteed value		0.5	500	%
$f_{SWITCH.OVER}$	Frequency range switch-over will function properly	1.5		450	MHz

Note to Table 5–82:
(1) This specification is pending device characterization.

Table 5–83. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input frequency	20		750	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter			300	ps (p-p)
f_{VCO}	Upper VCO frequency range for -3 and -4 speed grades	300		1,040	MHz
	Upper VCO frequency range for -5 speed grades	300		840	MHz
	Lower VCO frequency range for -3 and -4 speed grades	150		520	
	Lower VCO frequency range for -5 speed grades	150		420	
f_{OUT}	PLL output frequency to GCLK or RCLK	9.375		500	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output	45	50	55	%

Table 5–83. Fast PLL Specifications					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{EOUT}	LVTTL external PLL output frequency	1.5		166	MHz
	LVDS external PLL output frequency	1.5		717	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled			1	ms
t_{CLBW}	PLL bandwidth	2	5	30	MHz
$t_{SCANCLK}$	`scanclk` frequency			100	MHz

JTAG Timing Specifications

Figure 5–6 shows the timing requirements for the JTAG signals.

Figure 5–6. Stratix II JTAG Waveforms

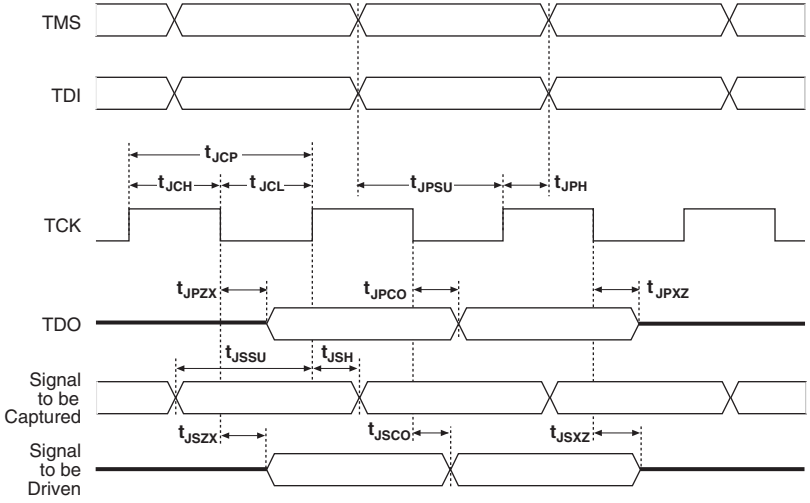


Table 5–84 shows the JTAG timing parameters and values for Stratix II devices.

Table 5–84. Stratix II JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

6. Reference & Ordering Information

SII51006-2.0

Software

Stratix® II devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Stratix II devices are available on the Altera web site at (**www.altera.com**).

Ordering Information

Figure 6–1 describes the ordering codes for Stratix II devices. For more information on a specific package, refer to the *Package Information for Stratix II Devices* chapter in Volume 2 of the *Stratix II Device Handbook*.

Figure 6–1. Stratix II Device Packaging Ordering Information