5 V Upstream Cable Line Driver

AD8328*

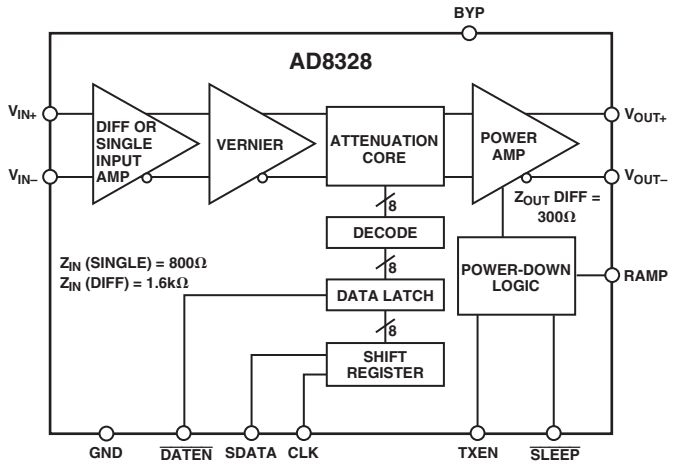
FEATURES

Supports DOCSIS and EuroDOCSIS Standards for Reverse Path Transmission Systems
Gain Programmable in 1 dB Steps over a 59 dB Range
Low Distortion at 60 dBmV Output:
–57.5 dBc SFDR at 21 MHz
–54 dBc SFDR at 65 MHz
Output Noise Level @ Minimum Gain 1.2 nV/√Hz
Maintains 300 Ω Output Impedance TX-Enable and Transmit-Disable Condition
Upper Bandwidth: 107 MHz (Full Gain Range)
5 V Supply Operation
Supports SPI Interfaces

APPLICATIONS

DOCSIS and EuroDOCSIS Cable Modems
CATV Set-Top Boxes
CATV Telephony Modems
Coaxial and Twisted Pair Line Driver

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8328 is a low cost amplifier designed for coaxial line driving. The features and specifications make the AD8328 ideally suited for MCNS-DOCSIS and Euro-DOCSIS applications. The gain of the AD8328 is digitally controlled. An 8-bit serial word determines the desired output gain over a 59 dB range, resulting in gain changes of 1 dB/LSB.

The AD8328 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load through a 2:1 transformer.

Distortion performance of –53 dBc is achieved with an output level up to 60 dBmV at 65 MHz bandwidth over a wide temperature range.

This device has a sleep mode function that reduces the quiescent current to 2.6 mA and a full power-down function that reduces power-down current to 20 μA.

The AD8328 is packaged in a low cost 20-lead LFCSP package and a 20-lead QSOP package. The AD8328 operates from a single 5 V supply and has an operational temperature range of –40°C to +85°C.

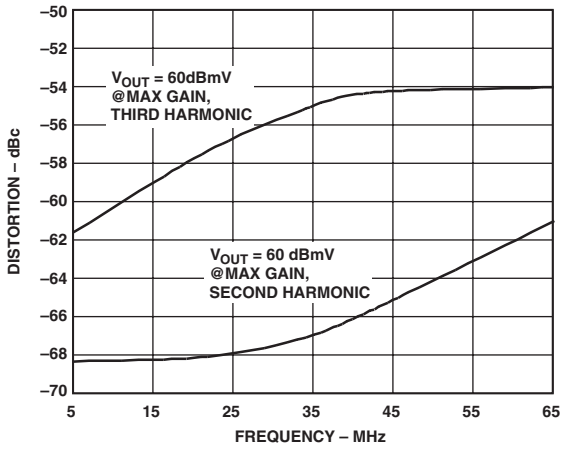


Figure 1. Worst Harmonic Distortion vs. Frequency

*Patent Pending

REV. 0

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AD8328–SPECIFICATIONS

(T_A = 25°C, V_S = 5 V, R_L = R_{IN} = 75 Ω, V_{IN} (Differential) = 29 dBmV. The AD8328 is characterized using a 2:1 transformer[1] at the device output.)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	Output = 60 dBmV, Max Gain		29		dBmV
Input Resistance	Single-Ended Input		800		Ω
	Differential Input		1600		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Voltage Gain Range		58	59.0	60	dB
Max Gain	Gain Code = 60 Dec	30.5	31.5	32.5	dB
Min Gain	Gain Code = 1 Dec	–28.5	–27.5	–26.5	dB
Output Step Size		0.6	1.0	1.4	dB/LSB
Output Step Size Temperature Coefficient	T_A = –40°C to +85°C		± 0.0005		dB/°C
OUTPUT CHARACTERISTICS					
Bandwidth (–3 dB)	All Gain Codes (1–60 Decimal Codes)		107		MHz
Bandwidth Roll-Off	f = 65 MHz		1.2		dB
1 dB Compression Point[2]	Max Gain, f = 10 MHz, Output Referred	17.9	18.4		dBm
	Min Gain, f = 10 MHz, Input Referred	2.2	3.3		dBm
Output Noise[2]					
Max Gain	f = 10 MHz		135	151	nV/$\sqrt{\text{Hz}}$
Min Gain	f = 10 MHz		1.2	1.3	nV/$\sqrt{\text{Hz}}$
Transmit Disable	f = 10 MHz		1.1	1.2	nV/$\sqrt{\text{Hz}}$
Noise Figure[2]					
Max Gain	f = 10 MHz		16.7	17.7	dB
Differential Output Impedance	TX Enable and TX Disable		75 ± 30%[3]		Ω
OVERALL PERFORMANCE					
Second-Order Harmonic Distortion[4, 5]					
	f = 33 MHz, V_{OUT} = 60 dBmV @ Max Gain		–67	–56	dBc
	f = 65 MHz, V_{OUT} = 60 dBmV @ Max Gain		–61	–55	dBc
Third-Order Harmonic Distortion[4, 5]	f = 21 MHz, V_{OUT} = 60 dBmV @ Max Gain		–57.5	–56	dBc
	f = 65 MHz, V_{OUT} = 60 dBmV @ Max Gain		–54	–52.5	dBc
ACPR[2, 6]			–58	–56	dBc
Isolation (Transmit Disable)[2]	Max Gain, f = 65 MHz		–85	–81	dB
POWER CONTROL					
TX Enable Settling Time	Max Gain, V_{IN} = 0		2.5		µs
TX Disable Settling Time	Max Gain, V_{IN} = 0		3.8		µs
Output Switching Transients[2]	Equivalent Output = 31 dBmV		2.5	6	mV p-p
	Equivalent Output = 61 dBmV		16	54	mV p-p
Output Settling					
Due to Gain Change	Min to Max Gain		60		ns
Due to Input Step Change	Max Gain, V_{IN} = 29 dBmV		30		ns
POWER SUPPLY					
Operating Range		4.75	5	5.25	V
Quiescent Current	Max Gain	98	120	140	mA
	Min Gain	18	26	34	mA
	Transmit Disable (TXEN = 0)	1	2.6	3.5	mA
	$\overline{\text{SLEEP}}$ Mode (Power-Down)	1	20	100	µA
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES
[1]TOKO 458PT-1087 used for above specifications. Typical insertion loss of 0.3 dB @ 10 MHz.
[2]Guaranteed by design and characterization to ±4 sigma for T_A = 25°C.
[3]Measured through a 2:1 transformer.
[4]Specification is worst case over all gain codes.
[5]Guaranteed by design and characterization to ±3 sigma for T_A = 25°C.
[6]V_{IN} = 29 dBmV, QPSK modulation, 160 KSPS symbol rate.

LOGIC INPUTS (TTL/CMOS Compatible Logic) ($\overline{DATEN}$, CLK, SDATA, TXEN, $\overline{SLEEP}$, V_{CC} = 5 V. Full Temperature Range.)

Parameter	Min	Typ	Max	Unit
Logic 1 Voltage	2.1		5.0	V
Logic 0 Voltage	0		0.8	V
Logic 1 Current (V_{INH} = 5 V) CLK, SDATA, $\overline{DATEN}$	0		20	nA
Logic 0 Current (V_{INL} = 0 V) CLK, SDATA, $\overline{DATEN}$	–600		–100	nA
Logic 1 Current (V_{INH} = 5 V) TXEN	50		190	µA
Logic 0 Current (V_{INL} = 0 V) TXEN	–250		–30	µA
Logic 1 Current (V_{INH} = 5 V) $\overline{SLEEP}$	50		190	µA
Logic 0 Current (V_{INL} = 0 V) $\overline{SLEEP}$	–250		–30	µA

Specifications subject to change without notice.

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} = 5 V, $t_R = t_F$ = 4 ns, f_{CLK} = 8 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Clock Pulsewidth (t_{WH})	16.0			ns
Clock Period (t_C)	32.0			ns
Setup Time SDATA vs. Clock (t_{DS})	5.0			ns
Setup Time $\overline{DATEN}$ vs. Clock (t_{ES})	15.0			ns
Hold Time SDATA vs. Clock (t_{DH})	5.0			ns
Hold Time $\overline{DATEN}$ vs. Clock (t_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{DATEN}$, Clock (t_R, t_F)			10	ns

Specifications subject to change without notice.

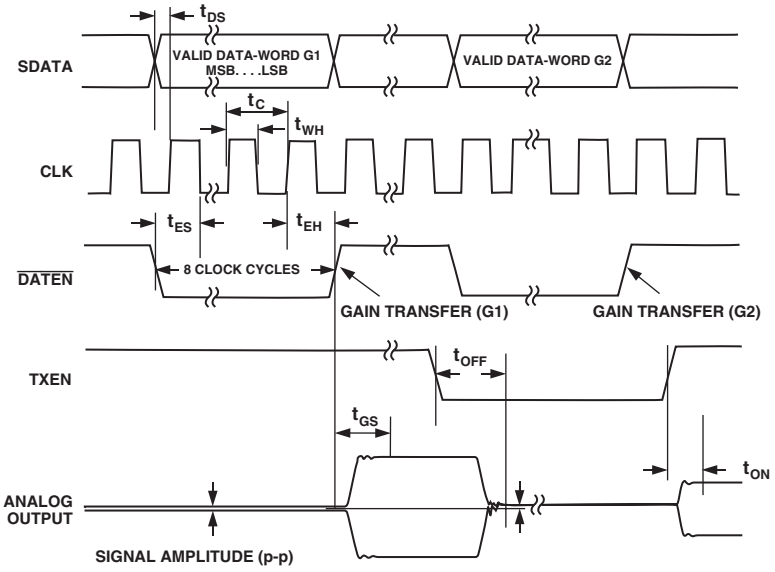


Figure 2. Serial Interface Timing

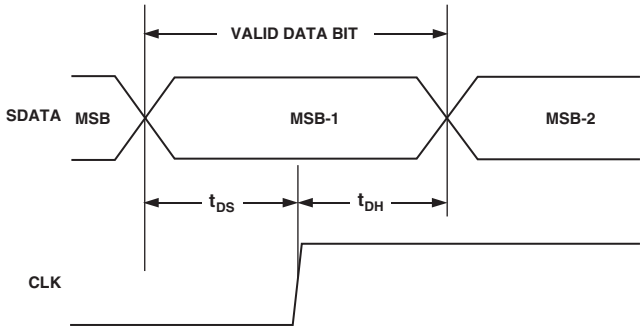


Figure 3. SDATA Timing

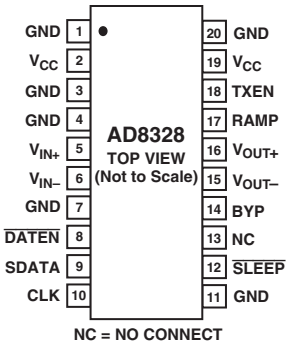
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_{CC} . . . . . 6 V
Input Voltage
VIN+, VIN– . . . . . 1.5 V p-p
$\overline{\text{DATEN}}$, SDATA, CLK,
$\overline{\text{SLEEP}}$, TXEN . . . . . –0.8 V to +5.5 V
Internal Power Dissipation
QSOP, LFCSP . . . . . 700 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering 60 seconds . . . . . 300°C

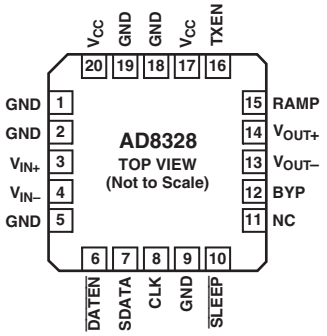
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

20-Lead QSOP



20-Lead LFCSP



PIN FUNCTION DESCRIPTIONS

Pin No. 20-Lead LFCSP	Pin No. 20-Lead QSOP	Mnemonic	Description
1 ,2, 5, 9, 18, 19	1, 3, 4, 7, 11, 20	GND	Common External Ground Reference
17, 20	2, 19	V_{CC}	Common Positive External Supply Voltage. A 0.1 µF capacitor must decouple each pin.
3	5	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
4	6	V_{IN-}	Inverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
6	8	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
7	9	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
8	10	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data-word to be valid at or before this clock transition.
10	12	$\overline{\text{SLEEP}}$	Low Power Sleep Mode. In the Sleep mode, the AD8328's supply current is reduced to 20 µA. A Logic 0 powers down the part (High Z_{OUT} State), and a Logic 1 powers up the part.
12	14	BYP	Internal Bypass. This pin must be externally ac-coupled (0.1 µF capacitor).
13	15	V_{OUT-}	Negative Output Signal
14	16	V_{OUT+}	Positive Output Signal
15	17	RAMP	External RAMP Capacitor (optional)
16	18	TXEN	Logic 0 disables forward transmission. Logic 1 enables forward transmission.

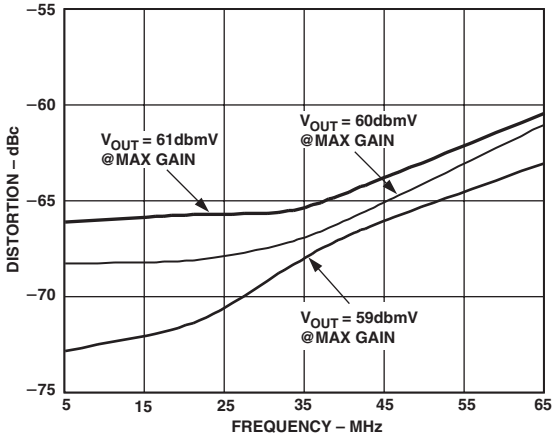
ORDERING GUIDE

Model	Temperature Range	Package Description	θ_{JA}	Package Option
AD8328ARQ	–40°C to +85°C	20-Lead QSOP	83.2°C/W[1]	RQ-20
AD8328ARQ-REEL	–40°C to +85°C	20-Lead QSOP	83.2°C/W[1]	RQ-20
AD8328ARQ-EVAL		Evaluation Board		
AD8328ACP	–40°C to +85°C	20-Lead LFCSP	30.4°C/W[2]	CP-20
AD8328ACP-REEL	–40°C to +85°C	20-Lead LFCSP	30.4°C/W[2]	CP-20
AD8328ACP-EVAL		Evaluation Board		

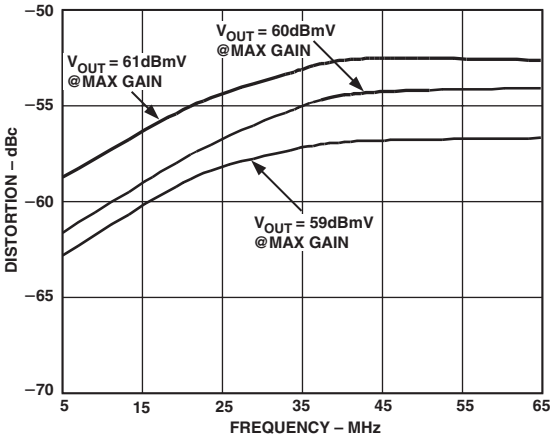
[1]Thermal Resistance measured on SEMI standard 4-layer board.
[2]Thermal Resistance measured on SEMI standard 4-layer board, paddle soldered to board.

CAUTION

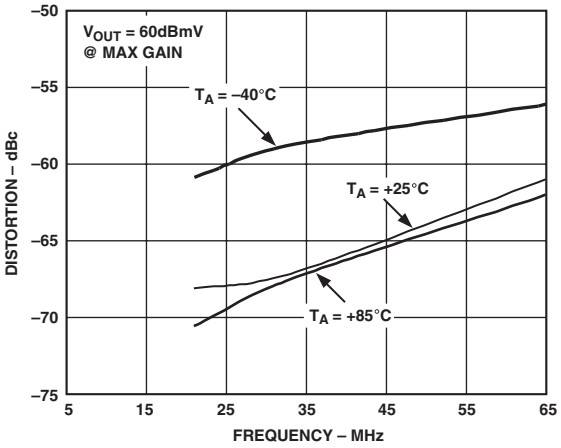
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8328 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



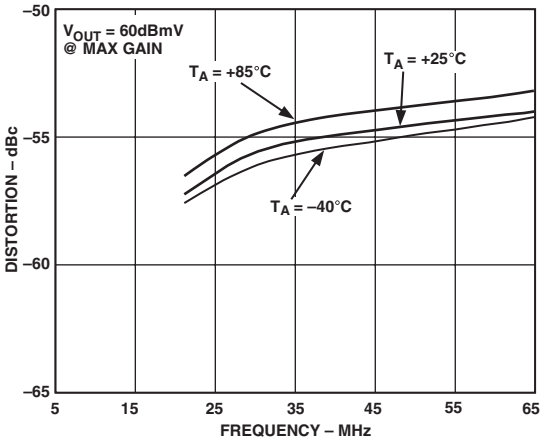
TPC 1. Second-Order Harmonic Distortion vs. Frequency for Various Output Powers



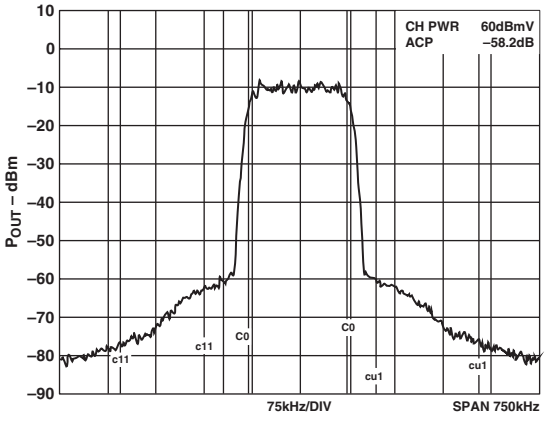
TPC 4. Third-Order Harmonic Distortion vs. Frequency for Various Output Powers



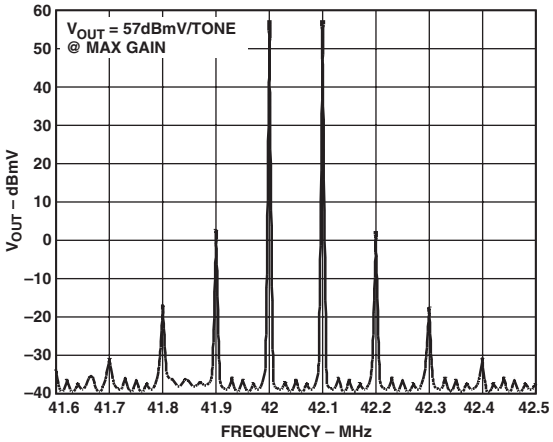
TPC 2. Second-Order Harmonic Distortion vs. Frequency vs. Temperature



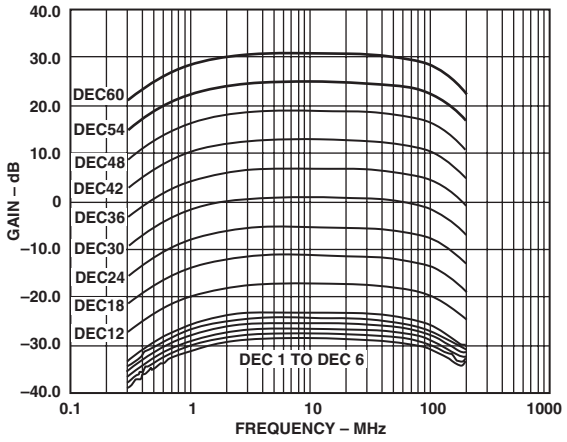
TPC 5. Third-Order Harmonic Distortion vs. Frequency vs. Temperature



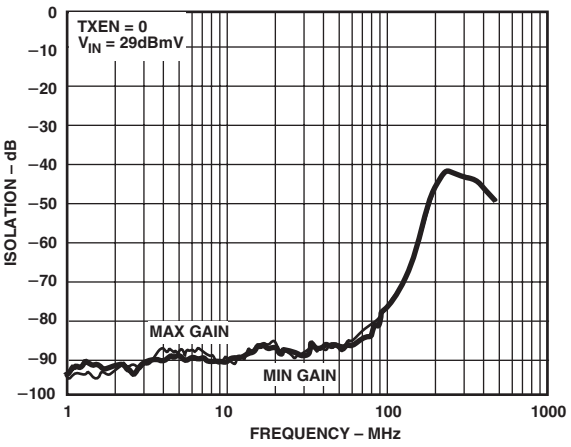
TPC 3. Adjacent Channel Power



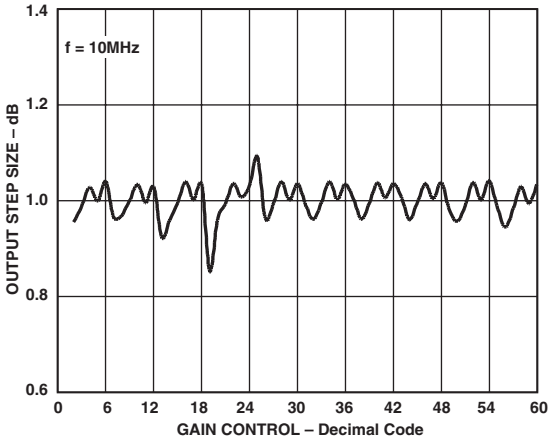
TPC 6. Two-Tone Intermodulation Distortion



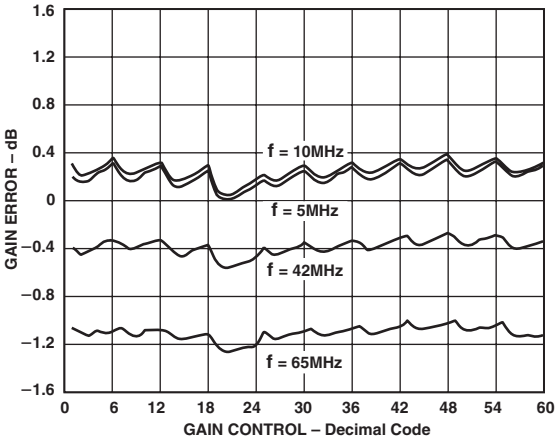
TPC 7. AC Response



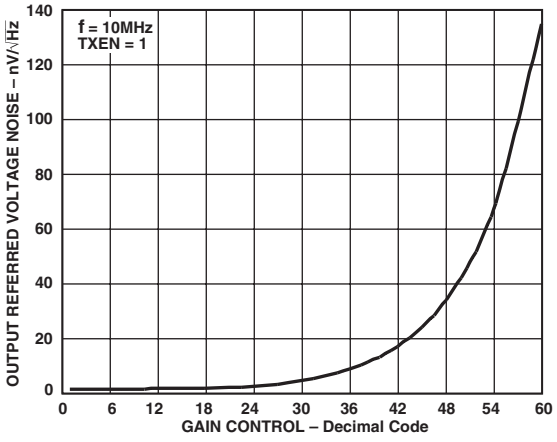
TPC 10. Isolation in Transmit Disable Mode vs. Frequency



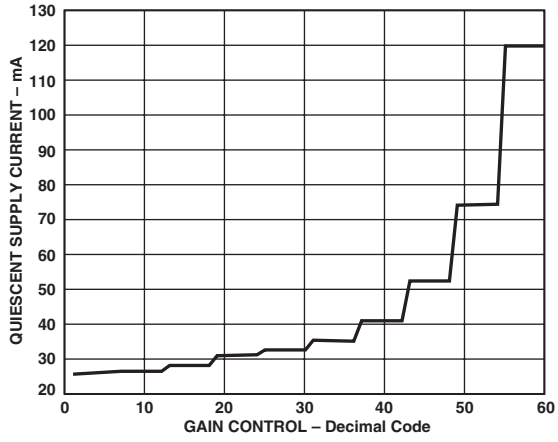
TPC 8. Output Step Size vs. Gain Control



TPC 11. Gain Error vs. Gain Control



TPC 9. Output Referred Voltage Noise vs. Gain Control



TPC 12. Supply Current vs. Gain Control

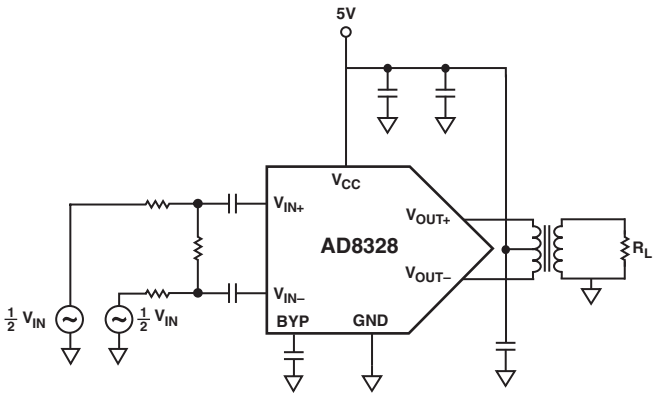


Figure 4. Characterization Circuit

APPLICATIONS

General Applications

The AD8328 is primarily intended for use as the power amplifier (PA) in DOCSIS (Data Over Cable Service Interface Specification) certified cable modems and CATV set-top boxes. The upstream signal is either a QPSK or QAM signal generated by a DSP, a dedicated QPSK/QAM modulator, or a DAC. In all cases, the signal must be low-pass filtered before being applied to the PA in order to filter out-of-band noise and higher order harmonics from the amplified signal.

Due to the varying distances between the cable modem and the head-end, the upstream PA must be capable of varying the output power by applying gain or attenuation. The ability to vary the output power of the AD8328 ensures that the signal from the cable modem will have the proper level once it arrives at the head-end. The upstream signal path commonly includes a diplexer and cable splitters. The AD8328 has been designed to overcome losses associated with these passive components in the upstream cable path.

Circuit Description

The AD8328 is composed of three analog functions in the power-up or forward mode. The input amplifier (preamp) can be used single-ended or differentially. If the input is used in the differential configuration, it is imperative that the input signals be 180 degrees out of phase and of equal amplitude. A vernier is used in the input stage for controlling the fine 1 dB gain steps. This stage then drives a DAC, which provides the bulk of the AD8328's attenuation. The signals in the preamp and DAC gain blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC into the output stage. The output stage maintains 300 Ω differential output impedance, which maintains proper match to 75 Ω when used with a 2:1 balun transformer.

SPI Programming and Gain Adjustment

The AD8328 is controlled through a serial peripheral interface (SPI) of three digital data lines: CLK, $\overline{\text{DATEN}}$, and SDATA. Changing the gain requires eight bits of data to be streamed into the SDATA port. The sequence of loading the SDATA register begins on the falling edge of the $\overline{\text{DATEN}}$ pin, which activates the CLK line. With the CLK line activated, data on the SDATA line is clocked into the serial shift register on the rising edge of the CLK pulses, most significant bit (MSB) first. The 8-bit data-word is latched into the attenuator core on the rising edge of the $\overline{\text{DATEN}}$ line. This provides control over the changes in the output signal level. The serial interface timing for the AD8328 is shown in Figures 2 and 3. The programmable gain range of the AD8328 is –28 dB to +31 dB with steps of 1 dB per least significant bit (LSB). This provides a total gain range of 59 dB. The AD8328 was characterized with a differential signal on the input and a TOKO 458PT-1087 2:1 transformer on the output. The AD8328 incorporates supply current scaling with gain code, as seen in TPC 12. This allows reduced power consumption when operating in lower gain codes.

Input Bias, Impedance, and Termination

The V_{IN+} and V_{IN-} inputs have a dc bias level of $V_{CC}/2$; therefore the input signal should be ac-coupled as seen in the typical application circuit (see Figure 5). The differential input impedance of the AD8328 is approximately 1.6 kΩ, while the single-ended input is 800 Ω. The high input impedance of the AD8328 allows flexibility in termination and properly matching filter networks. The AD8328 will exhibit optimum performance when driven with a pure differential signal.

Output Bias, Impedance, and Termination

The output stage of the AD8328 requires a bias of +5 V. The +5 V power supply should be connected to the center tap of the output transformer. Also, the V_{CC} that is being applied to the center tap of the transformer should be decoupled as seen in the typical applications circuit (Figure 5).

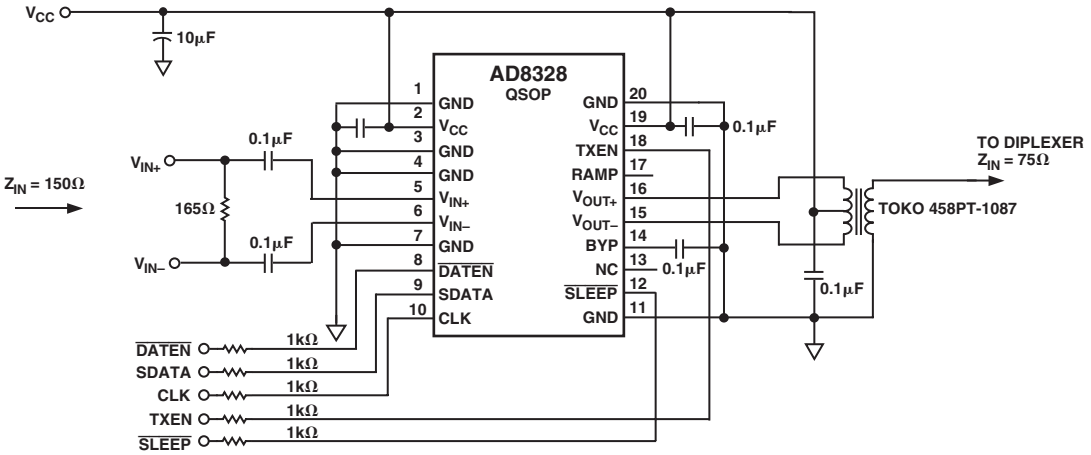


Figure 5. Typical Application Circuit

Table I. Adjacent Channel Power

	Adjacent Channel Symbol Rate (kSym/s)					
Channel Symbol Rate (kSym/s)	**160**	**320**	**640**	**1280**	**2560**	**5120**
160	–58	–60	–63	–66	–66	–64
320	–58	–59	–60	–64	–66	–65
640	–60	–58	–59	–61	–64	–65
1280	–62	–60	–59	–60	–61	–63
2560	–64	–62	–60	–59	–60	–61
5120	–66	–65	–62	–61	–59	–60

The output impedance of the AD8328 is 300 Ω, regardless of whether the amplifier is in transmit enable or transmit disable mode. This, when combined with a 2:1 voltage ratio (4:1 impedance ratio) transformer, eliminates the need for external back termination resistors. If the output signal is being evaluated using standard 50 Ω test equipment, a minimum loss 75 Ω–50 Ω pad must be used to provide the test circuit with the proper impedance match. The AD8328 evaluation board provides a convenient means to implement a matching attenuator. Soldering a 43.3 Ω resistor in the R15 placeholder and an 86.6 Ω resistor in the R16 placeholder will allow testing on a 50 Ω system. When using a matching attenuator, it should be noted that there will be a 5.7 dB of power loss (7.5 dB voltage) through the network.

Power Supply

The 5 V supply should be delivered to each of the V_{CC} pins via a low impedance power bus to ensure that each pin is at the same potential. The power bus should be decoupled to ground using a 10 μF tantalum capacitor located close to the AD8328. In addition to the 10 μF capacitor, each V_{CC} pin should be individually decoupled to ground with ceramic chip capacitors located close to the pins. The bypass pin, labeled BYP, should also be decoupled. The PCB should have a low impedance ground plane covering all unused portions of the board, except in areas of the board where input and output traces are in close proximity to the AD8328 and the output transformer. All AD8328 ground pins must be connected to the ground plane to ensure proper grounding of all internal nodes.

Signal Integrity Layout Considerations

Careful attention to printed circuit board layout details will prevent problems due to board parasitics. Proper RF design techniques are mandatory. The differential input and output traces should be kept as short as possible. Keeping the traces short will minimize parasitic capacitance and inductance. This is most critical between the outputs of the AD8328 and the 2:1 output transformer. It is also critical that all differential signal paths be symmetrical in length and width. In addition, the input and output traces should be adequately spaced to minimize coupling (crosstalk) through the board. Following these guidelines will optimize the overall performance of the AD8328 in all applications.

Initial Power-Up

When the supply voltage is first applied to the AD8328, the gain of the amplifier is initially set to gain code 1. As power is first applied to the amplifier, the TXEN pin should be held low (Logic 0) to prevent forward signal transmission. After power has been applied to the amplifier, the gain can be set to the desired level by following the procedure provided in the SPI Programming and Gain Adjustment section. The TXEN pin can then be brought from Logic 0 to Logic 1, enabling forward signal transmission at the desired gain level.

RAMP Pin and BYP Pin Features

The RAMP pin (Pin 15) is used to control the length of the burst on and off transients. By default, leaving the RAMP pin unconnected will result in a transient that is fully compliant with DOCSIS 2.0 Section 6.2.21.2, *Spurious Emissions During Burst On/Off Transients.* DOCSIS requires that all between burst transients must be dissipated no faster than 2 μs. Adding capacitance to the RAMP pin will add more time to the transient.

The BYP pin is used to decouple the output stage at midsupply. Typically, for normal DOCSIS operation, the BYP pin should be decoupled to ground with a 0.1 μF capacitor. However, in applications that may require transient on/off times faster than 2 μs, smaller capacitors may be used, but it should be noted that the BYP pin should always be decoupled to ground.

Transmit Enable (TXEN) and $\overline{\text{SLEEP}}$

The asynchronous TXEN pin is used to place the AD8328 into between-burst mode. In this reduced current state, the output impedance of 75 Ω is maintained. Applying Logic 0 to the TXEN pin deactivates the on-chip amplifier, providing a 97.8% reduction in consumed power. For 5 V operation, the supply current is typically reduced from 120 mA to 2.6 mA. In this mode of operation, between-burst noise is minimized and high input to output isolation is achieved. In addition to the TXEN pin, the AD8328 also incorporates an asynchronous $\overline{\text{SLEEP}}$ pin, which may be used to further reduce the supply current to approximately 20 μA. Applying Logic 0 to the $\overline{\text{SLEEP}}$ pin places the amplifier into $\overline{\text{SLEEP}}$ mode. Transitioning into or out of $\overline{\text{SLEEP}}$ mode may result in a transient voltage at the output of the amplifier.

Distortion, Adjacent Channel Power, and DOCSIS

To deliver the DOCSIS required 58 dBmV of QPSK signal and 55 dBmV of 16 QAM signal, the PA is required to deliver up to 60 dBmV. This added power is required to compensate for losses associated with the diplex filter or other passive components that may be included in the upstream path of cable modems or set-top boxes. It should be noted that the AD8328 was characterized with a differential input signal. TPCs 1 and 4 show the AD8328 second and third harmonic distortion performance versus the fundamental frequency for various output power levels. These figures are useful for determining the in-band harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency (above 42 MHz for DOCSIS and above 65 MHz for EuroDOCSIS) will be sharply attenuated by the low-pass filter function of the diplexer.

Another measure of signal integrity is adjacent channel power, commonly referred to as ACP. DOCSIS 2.0, section 6.2.21.1.1

states, "Spurious emissions from a transmitted carrier may occur in an adjacent channel that could be occupied by a carrier of the same or different symbol rates." TPC 3 shows the measured ACP for a 60 dBmV QPSK signal taken at the output of the AD8328 evaluation board. The transmit channel width and adjacent channel width in TPC 3 correspond to the symbol rates of 160 kSym/s. Table I shows the ACP results for the AD8328 driving a QPSK, 60 dBmV signal for all conditions in DOCSIS Table 6-9, *Adjacent Channel Spurious Emissions.*

Noise and DOCSIS

At minimum gain, the AD8328 output noise spectral density is 1.2 nV/$\sqrt{\text{Hz}}$ measured at 10 MHz. DOCSIS Table 6-10, *Spurious Emissions in 5 MHz to 42 MHz*, specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 kSym/s is:

$$\left[20 \times \log\left(\sqrt{\left(\frac{1.2\,nV}{\sqrt{Hz}}\right)^2 \times 160\,kHz}\right)\right] + 60 = -66.4\,dBmV$$

Comparing the computed noise power of –66.4 dBmV to the +8 dBmV signal yields –74.4 dBc, which meets the required level set forth in DOCSIS Table 6-10. As the AD8328 gain is increased above this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal-to-noise ratio that improves with gain. In transmit disable mode, the output noise spectral density is 1.1 nV/$\sqrt{\text{Hz}}$, which results in –67 dBmV when computed over 160 kSym/s. The noise power was measured directly at the output of the AD8328AR-EVAL board.

Evaluation Board Features and Operation

The AD8328 evaluation board and control software can be used to control the AD8328 upstream cable driver via the parallel port of a PC. A standard printer cable connected to the parallel port of the PC is used to feed all the necessary data to the AD8328 using the Windows®-based control software. This package provides a means of controlling the gain and the power mode of the AD8328. With this evaluation kit, the AD8328 can be evaluated in either a single-ended or differential input configuration. A schematic of the evaluation board is provided in Figure 11.

Differential Signal Source

Typical applications for the AD8328 use a differential input signal from a modulator or a DAC. See Table II for common values of R4, or calculate other input configurations using the equation in Figure 6. This circuit configuration will give optimal distortion results due to the symmetric input signals. It should be noted that this is the configuration that was used to characterize the AD8328.

$$R4 = \frac{Z_{IN} \times 1.6k}{1.6k - Z_{IN}}$$

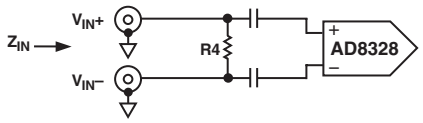


Figure 6. Differential Circuit

Differential Signal from Single-Ended Source

The default configuration of the evaluation board implements a differential signal drive from a single-ended signal source. This configuration uses a 1:1 balun transformer to approximate a differential signal. Because of the nonideal nature of real transformers, the differential signal is not purely equal and opposite in amplitude. Although this circuit slightly sacrifices even order harmonic distortion due to asymmetry, it does provide a convenient way to evaluate the AD8328 with a single-ended source.

The AD8328 evaluation board is populated with a TOKO 617DB-A0070 1:1 for this purpose (T1). Table II provides typical R4 values for common input configurations. Other input impedances may be calculated using the equation in Figure 7. Refer to Figure 10 for an evaluation board schematic. To utilize the transformer for converting a single-ended source into a differential signal, the input signal must be applied to V_{IN+}.

$$R4 = \frac{Z_{IN} \times 1.6k}{1.6k - Z_{IN}}$$

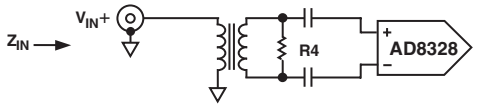


Figure 7. Single to Differential Circuit

Single-Ended Source

Although the AD8328 was designed to have optimal DOCSIS performance when used with a differential input signal, the AD8328 may also be used as a single-ended receiver, or an IF digitally controlled amplifier. However, as with the single-ended to differential configuration noted above, even order harmonic distortion will be slightly degraded.

When operating the AD8328 in a single-ended input mode, V_{IN+} and V_{IN-} should be terminated as illustrated in Figure 8. On the AD8328 evaluation boards, this termination method requires the removal of R2 and R3 to be shorted with R4 open, as well as the addition of 82.5 Ω at R1 and 39.2 Ω at R17 for 75 Ω termination. Table II shows the correct values for R11 and R12 for some common input configurations. Other input impedance configurations may be accommodated using the equations in Figure 8.

$$R1 = \frac{Z_{IN} \times 800}{800 - Z_{IN}} \quad R17 = \frac{Z_{IN} \times R1}{R1 + Z_{IN}}$$

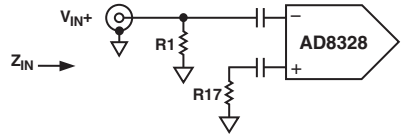


Figure 8. Single-Ended Circuit

Table II. Common Matching Resistors

Differential Input Termination			
Z_{IN} (Ω)	**R2/R3**	**R4 (Ω)**	**R1/R17**
50	Open	51.1	Open/Open
75	Open	78.7	Open/Open
100	Open	107.0	Open/Open
150	Open	165.0	Open/Open
Single-Ended Input Termination			
Z_{IN} (Ω)	**R2/R3**	**R4 (Ω)**	**R1/R17**
50	0 Ω/0 Ω	Open	53.6 Ω/25.5 Ω
75	0 Ω/0 Ω	Open	82.5 Ω/39.2 Ω

Overshoot on PC Printer Ports
The data lines on some PC parallel printer ports have excessive overshoot that may cause communications problems when presented to the CLK pin of the AD8328. The evaluation board was designed to accommodate a series resistor and shunt capacitor (R2 and C5 in Figure 11) to filter the CLK signal if required.

Installing Visual Basic Control Software
Install the CabDrive_28 software by running the setup.exe file on disk one of the AD8328 evaluation software. Follow the on-screen directions and insert disk two when prompted. Choose installation directory and then select the icon in the upper left to complete the installation.

Running AD8328 Software
To load the control software, go to START, PROGRAMS, CABDRIVE_28 or select the AD8328.exe file from the installed directory. Once loaded, select the proper parallel port to communicate with the AD8328 (Figure 9).

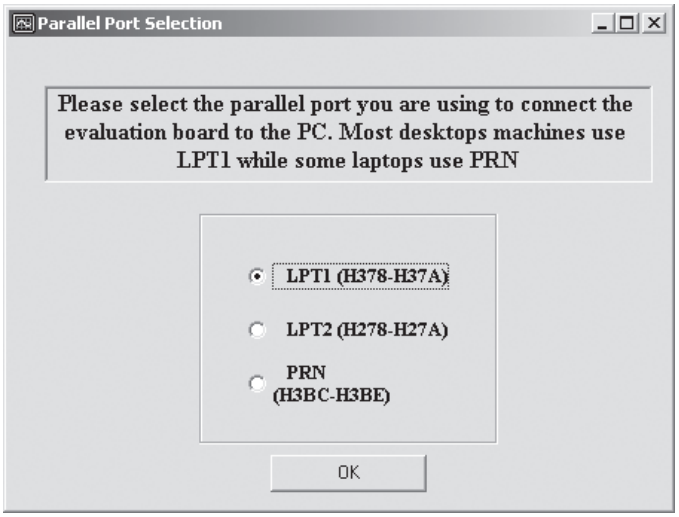


Figure 9. Parallel Port Selection

Controlling Gain/Attenuation of the AD8328
The slide bar controls the gain/attenuation of the AD8328, which is displayed in dB and in V/V. The gain scales 1 dB per LSB. The gain code from the position of the slide bar is displayed in decimal, binary, and hexadecimal (Figure 10).

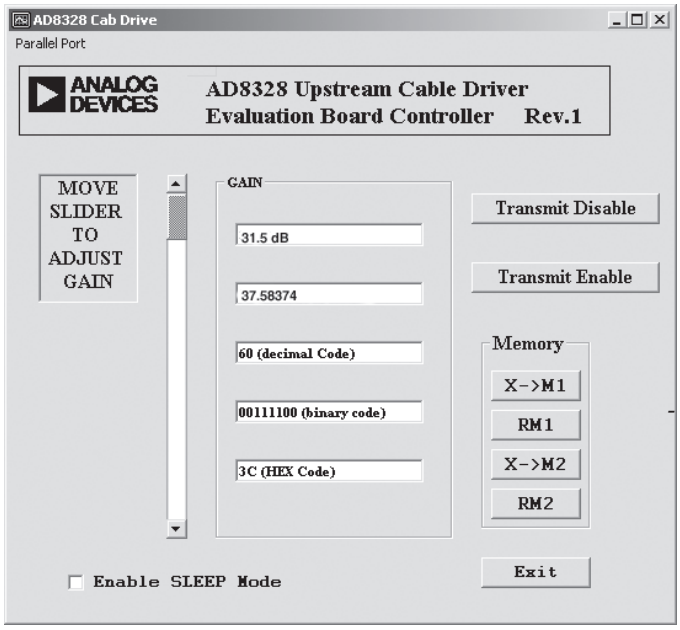


Figure 10. Control Software Interface

Transmit Enable and Sleep Mode
The Transmit Enable and Transmit Disable buttons select the mode of operation of the AD8328 by asserting logic levels on the asynchronous TXEN pin. The Transmit Disable button applies Logic 0 to the TXEN pin, disabling forward transmission. The Transmit Enable button applies Logic 1 to the TXEN pin, enabling the AD8328 for forward transmission. Checking the Enable $\overline{\text{SLEEP}}$ Mode checkbox applies Logic 0 to the asynchronous $\overline{\text{SLEEP}}$ pin, setting the AD8328 for $\overline{\text{SLEEP}}$ mode.

Memory Functions
The Memory section of the software provides a way to alternate between two gain settings. The X->M1 button stores the current value of the gain slide bar into memory, while the RM1 button recalls the stored value, returning the gain slide bar to the stored level. The same applies to the X->M2 and RM2 buttons.

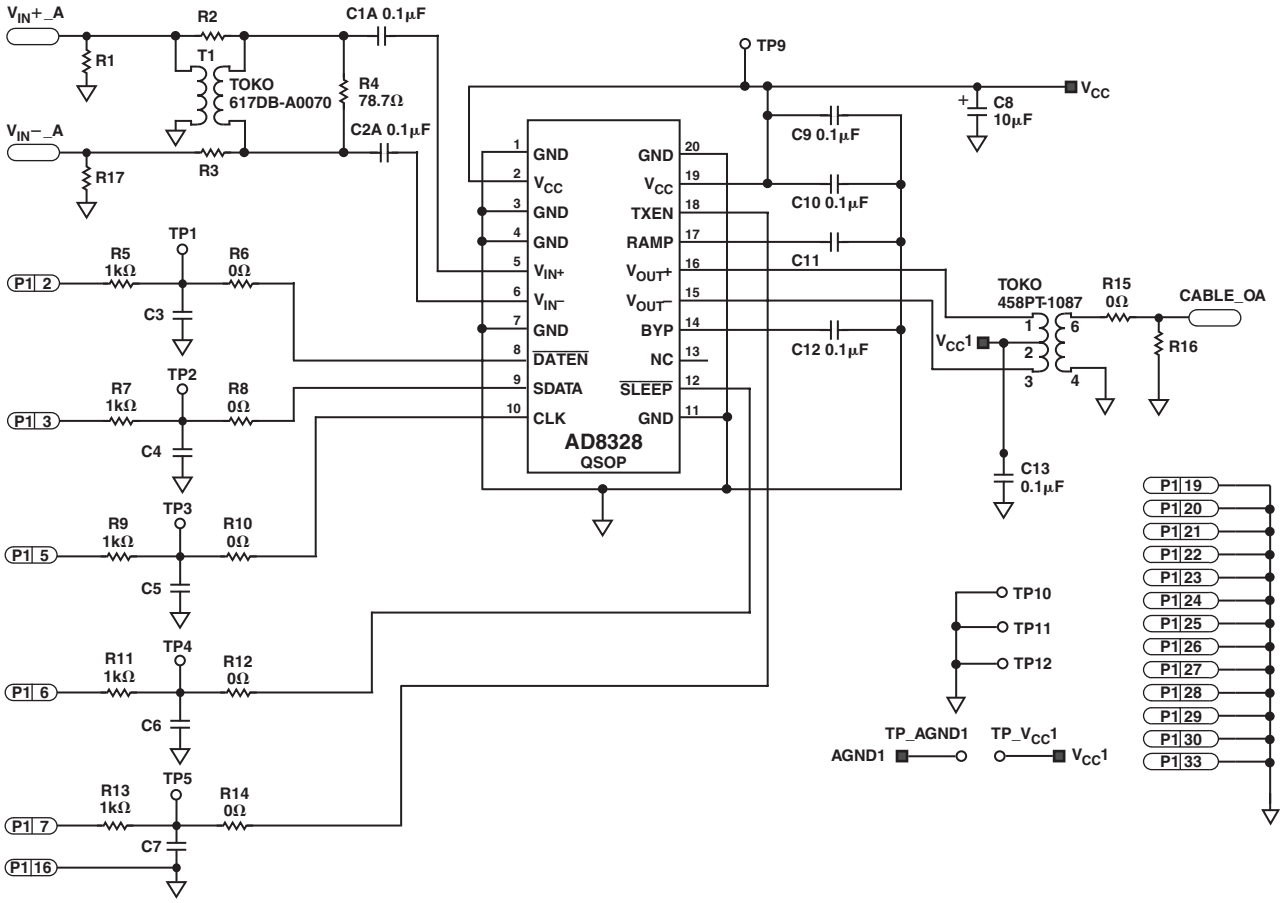


Figure 11. AD8328 Evaluation Board Schematic

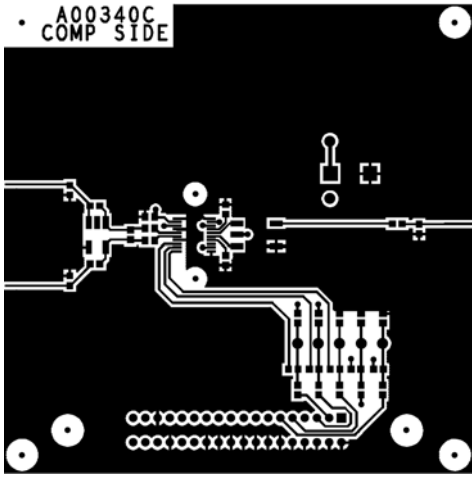


Figure 12. Primary Side

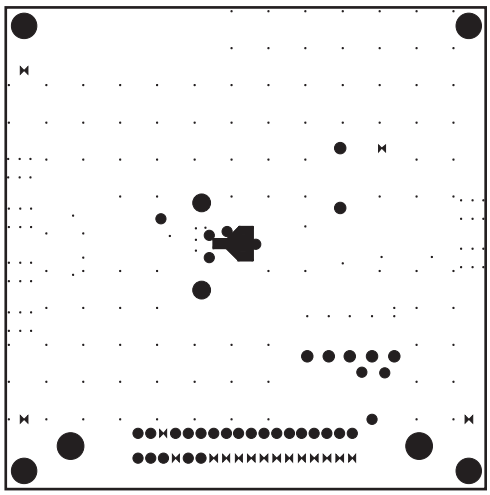


Figure 15. Internal Ground Plane

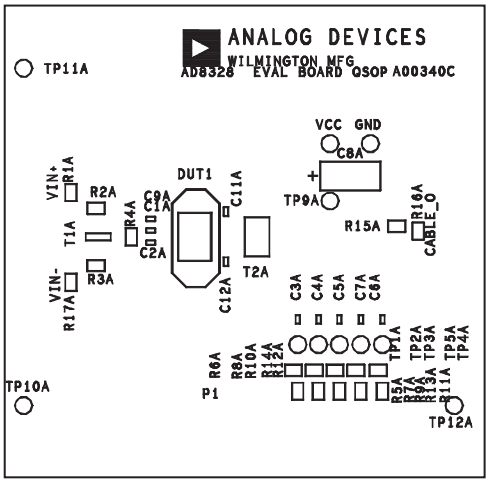


Figure 13. Component Side Silkscreen

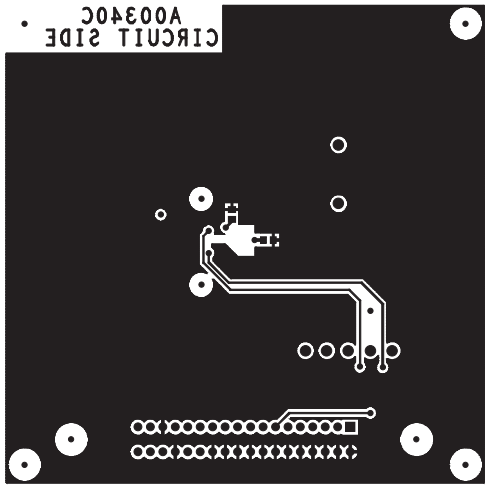


Figure 16. Secondary Side

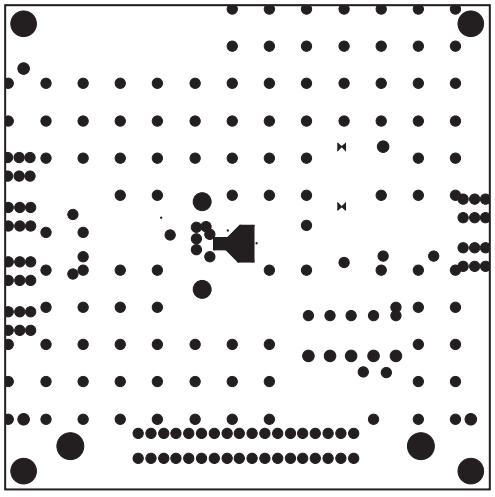


Figure 14. Internal Power Plane

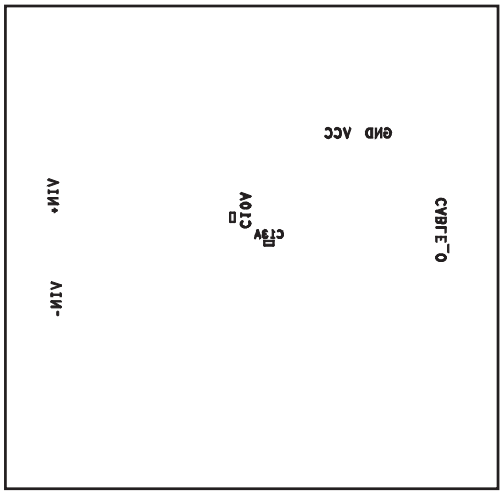
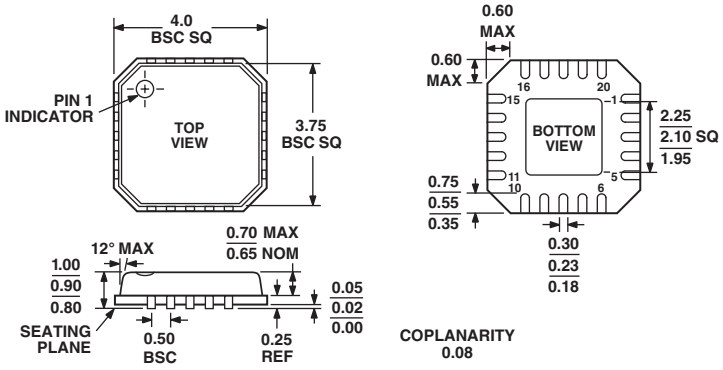


Figure 17. Secondary Side Silkscreen

OUTLINE DIMENSIONS

20-Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-20)

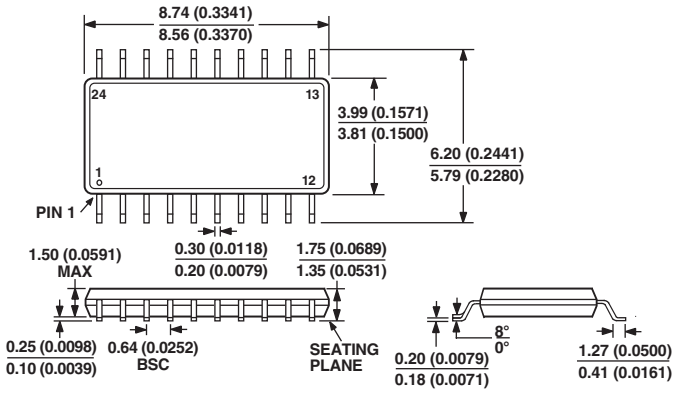
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1
CONTROLLING DIMENSIONS ARE IN MILLIMETERS

20-Lead SOIC, 0.025 Lead Pitch [QSOP]
(RQ-20)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

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