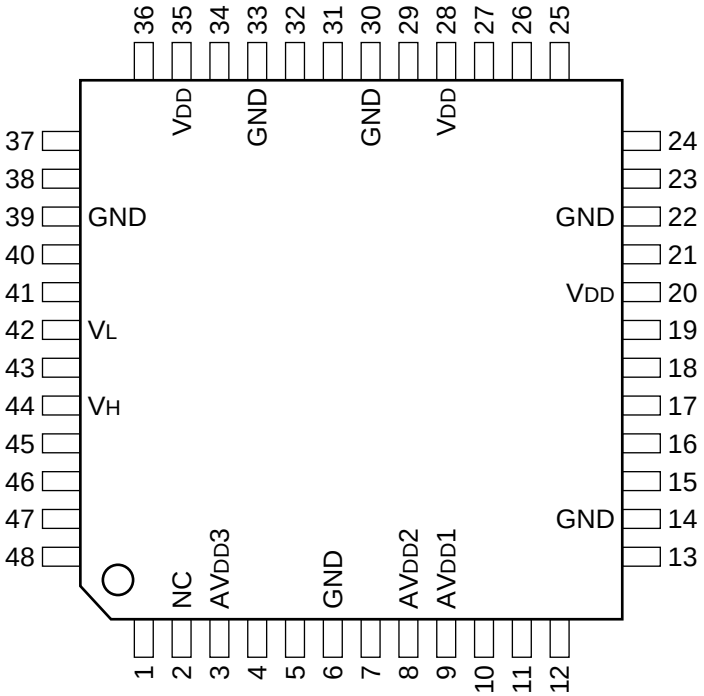
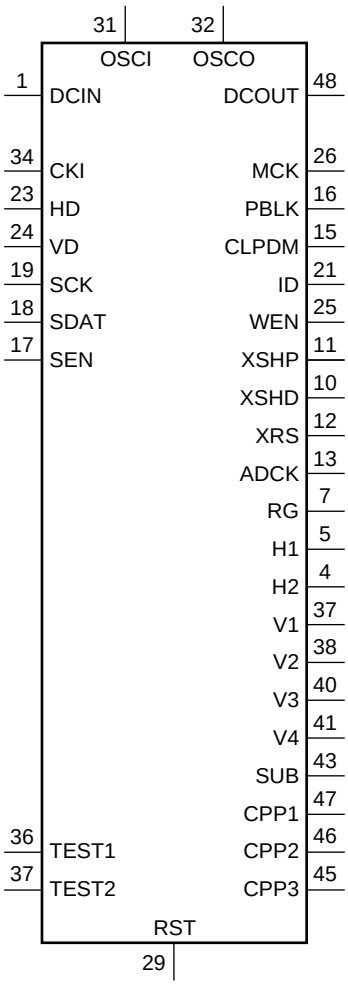
C-MOS TIMING CONTROLLER WITH CCD DRIVERS

—TOP VIEW—





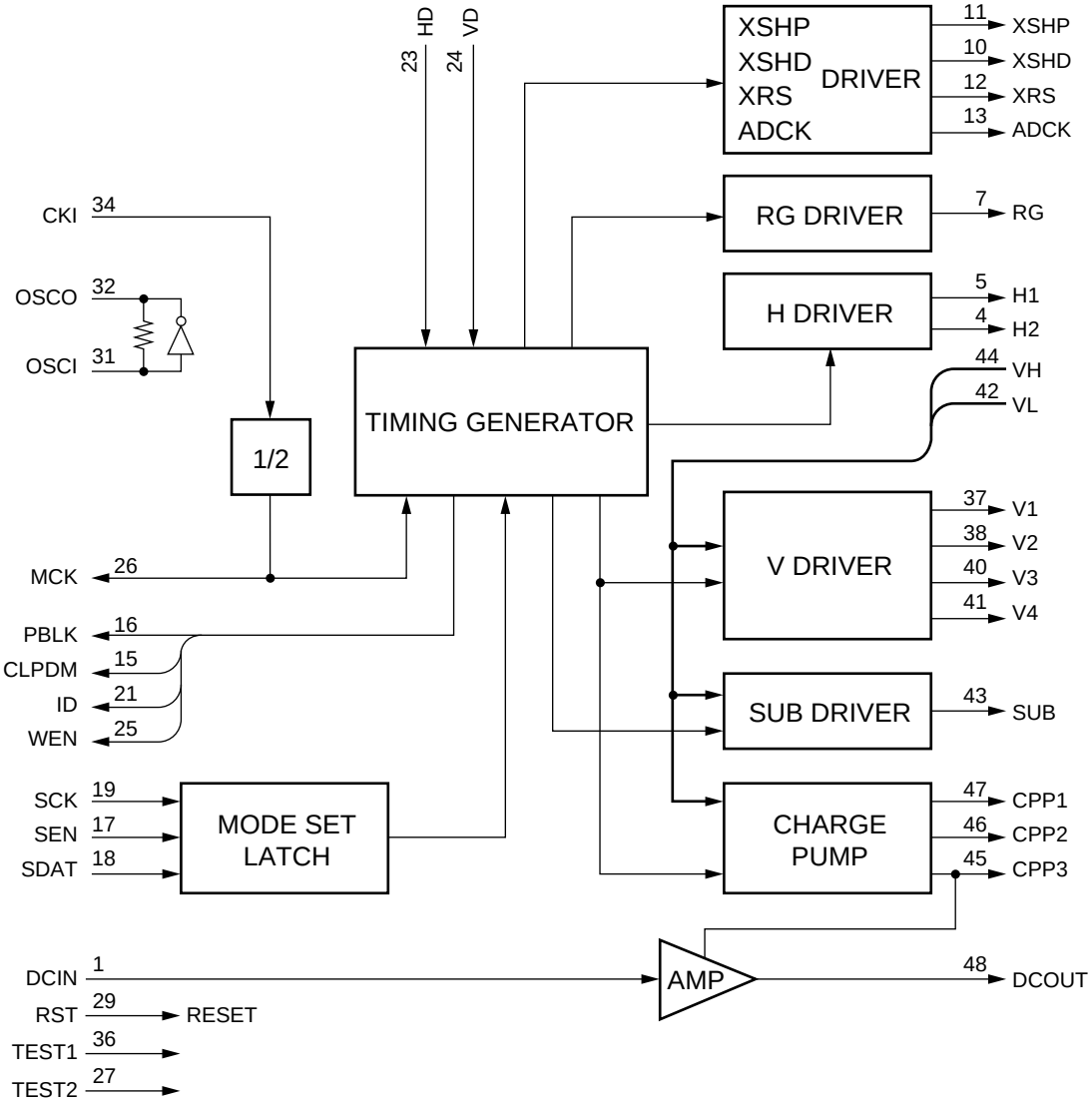
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	DCIN	25	O	WEN
2	—	NC	26	O	MCK
3	—	AVDD3	27	I	TEST2
4	O	H2	28	—	VDD
5	O	H1	29	I	RST
6	—	GND	30	—	GND
7	O	RG	31	I	OSCI
8	—	AVDD2	32	O	OSCO
9	—	AVDD1	33	—	GND
10	O	XSHD	34	I	CKI
11	O	XSHP	35	—	VDD
12	O	XRS	36	I	TEST1
13	O	ADCK	37	O	V1
14	—	GND	38	O	V2
15	O	LLPDM	39	—	GND
16	O	PBLK	40	O	V3
17	I	SEN	41	O	V4
18	I	SDAT	42	—	VL
19	I	SCK	43	O	SUB
20	—	VDD	44	—	VH
21	O	ID	45	O	CPP3
22	—	GND	46	O	CPP2
23	I	HD	47	O	CPP1
24	I	VD	48	O	DCOUT

INPUT

CKI	;	CLOCK
DCIN	;	OPERATIONAL AMPLIFIER INPUT FOR GENERATING THE SUB CLAMP VOLTAGE
HD	;	HORIZONTAL SYNC SIGNAL
OSCI	;	OSCILLATOR
RST	;	RESET
SCK	;	SERIAL COMMUNICATION CLOCK
SDAT	;	SERIAL COMMUNICATION DATA
SEN	;	SERIAL COMMUNICATION STROBE
TEST1, TEST2	;	TEST
VD	;	VERTICAL SYNC SIGNAL

OUTPUT

ADCK	;	A/D CONVERTER CLOCK
CLPDM	;	CLAMP PLUSE FOR CCD DUMMY SIGNAL
CPP1 - CPP3	;	CHARGE PUMP CAPACITORS
DCOUT	;	OPERATIONAL AMPLIFIER OUTPUT FOR GENERATING THE SUB CLAMP VOLTAGE
H1, H2	;	CCD HORIZONTAL REGISTER DRIVE PULSES
ID	;	LINE IDENTIFICATION SIGNAL
MCK	;	MODULATION CLOCK (1/2 CKI)
OSCO	;	OSCILLATOR
PBLK	;	BLANKING CLEANING PULSE
RG	;	CCD RESET GATE DRIVE PULSE
SUB	;	CCD ELECTRON-CHARGE DRAIN PULSE
V1 - V4	;	CCD VERTICAL REGISTER DRIVE PULSES
WEN	;	WRITE ENABLE SIGNAL (ONLY IN LOW-SPEED SHUTTER OPERATION)
XRS	;	A/D CONVERTER SAMPLE AND HOLD PULSE
XSHD	;	SAMPLE AND HOLD PULSE FOR DATA
XSHP	;	SAMPLE AND HOLD PULSE FOR PRECHARGING


HD
VD
23
24
XSHP
XSHD
XRS
ADCK
DRIVER
11
10
12
13
XSHP
XSHD
XRS
ADCK
CKI
34
RG DRIVER
7
RG
OSCO
32
OSCI
31
H DRIVER
5
4
H1
H2
44
42
VH
VL
TIMING GENERATOR
1/2
MCK
26
V DRIVER
37
38
40
41
V1
V2
V3
V4
PBLK
16
CLPDM
15
ID
21
WEN
25
SUB DRIVER
43
SUB
SCK
19
SEN
17
SDAT
18
MODE SET
LATCH
CHARGE
PUMP
47
46
45
CPP1
CPP2
CPP3
DCIN
1
AMP
48
DCOUT
RST
29
RESET
TEST1
36
TEST2
27