CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX883
Baseband Processor for 'Leisure Radios'

Provisional Issue

Full-Feature Audio-Processing and Signalling for Half Duplex FRS, MURS, GMRS and PMR446 'Leisure' Radios

Features

- Automatic signal type scanning and IRQ on detection of valid Rx signals, level or RSSI

- Tone generator for caller recognition tunes

- Programmable power down control

- Programmable signal detection thresholds

- Low Power operation with 'Zero Power' mode

- Uncommitted Aux ADC with switchable input to monitor signals

- Silent operation by removal of unwanted calls

- XTCSS channel and data signalling

- Voice processing facilities, including Tx and Rx gain setting and voice/subaudio filtering

- C-BUS serial host interface

- RF interface allowing 1 or 2 point modulation

- Programmable soft limiter

- Enhanced CTCSS and 23/24 bit DCS codecs

- Zero 'Talkdown' CTCSS decoder performance prevents dropouts

- All call code and monitor modes for CTCSS

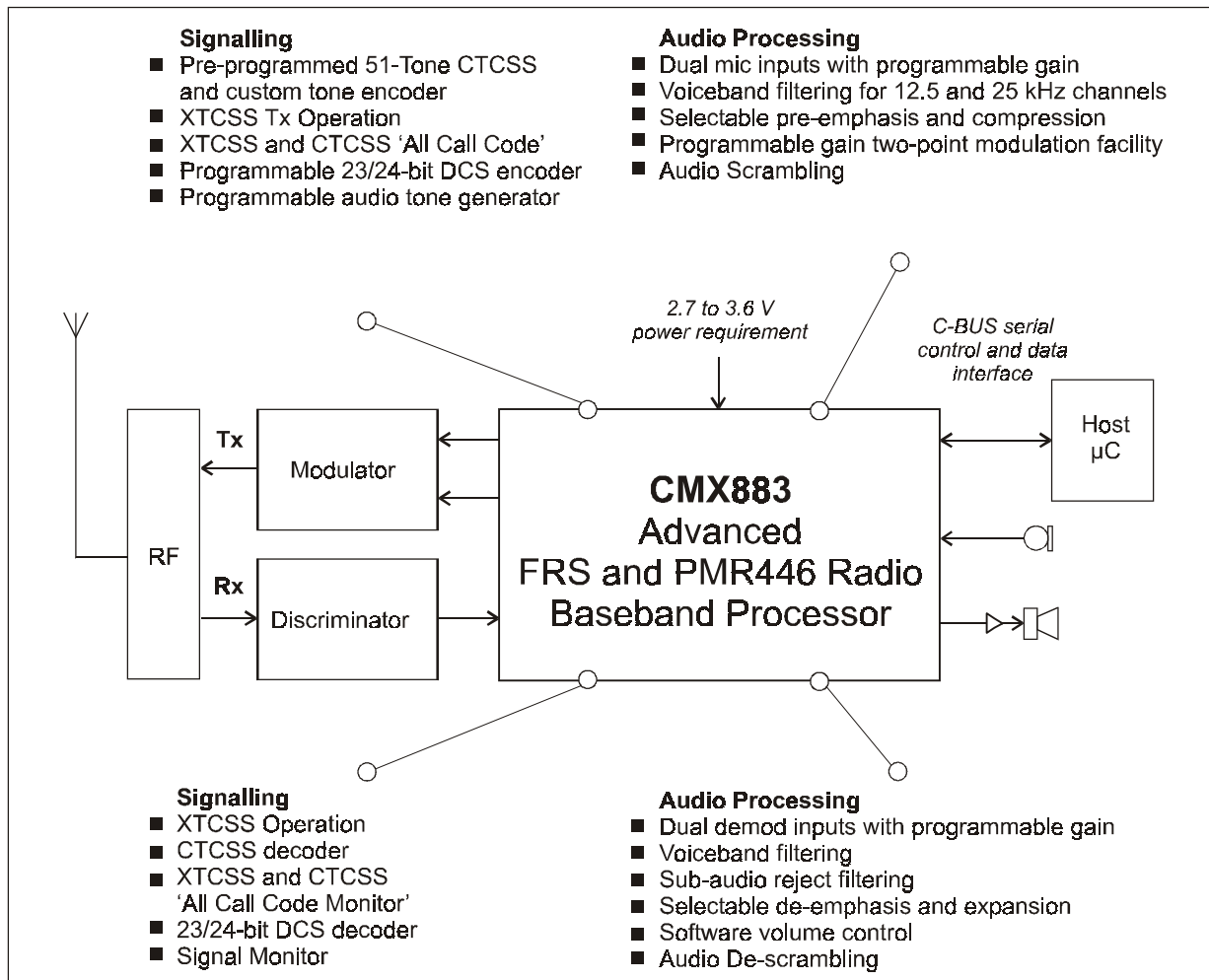- Audio scrambler

- Selectable voice companding
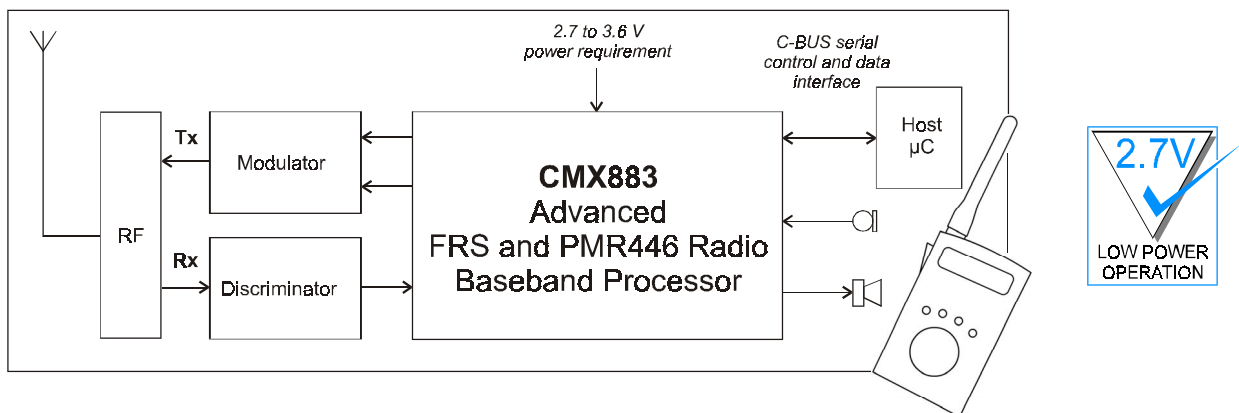
1.1   Brief Description

CMX883, a full-function half-duplex audio and signalling processor IC for FRS and PMR446 type facilities for both complex and simple end-designs. Under the control of the host µC, all voiceband requirements are catered for: voiceband and sub-audio filtering, pre/de-emphasis, compression and expansion and audio routing and global level setting with single or two-point modulation in the transmit path.

The combination of new and standard signalling functions of this product offer, under software control, increased functionality, versatility and privacy. Standard Extended-Code CTCSS and DCS are integrated with the new XTCSS code implementation. XTCSS provides additional and improved squelch-centred privacy codes with the added advantage of 'silent operation'; no annoying interference from other sub-audio users. XTCSS fitted radios enjoy more privacy and flexibility of operation.

With ultra low power requirements and graduated powersave, this product only requires a smaller, lower-power µC than existing FRS/PMR446 solutions. It is available in compact SSOP and TSSOP packages.

CMX883 Functions and Facilities

Signalling
- Pre-programmed 51-Tone CTCSS and custom tone encoder
- XTCSS Tx Operation
- XTCSS and CTCSS 'All Call Code'
- Programmable 23/24-bit DCS encoder
- Programmable audio tone generator

Audio Processing
- Dual mic inputs with programmable gain
- Voiceband filtering for 12.5 and 25 kHz channels
- Selectable pre-emphasis and compression
- Programmable gain two-point modulation facility
- Audio Scrambling

2.7 to 3.6 V power requirement

C-BUS serial control and data interface

Tx Modulator

Rx Discriminator

RF

CMX883 Advanced FRS and PMR446 Radio Baseband Processor

Host µC

Signalling
- XTCSS Operation
- CTCSS decoder
- XTCSS and CTCSS 'All Call Code Monitor'
- 23/24-bit DCS decoder
- Signal Monitor

Audio Processing
- Dual demod inputs with programmable gain
- Voiceband filtering
- Sub-audio reject filtering
- Selectable de-emphasis and expansion
- Software volume control
- Audio De-scrambling

Half Duplex Operation

Working in a half duplex mode, when the product is in Tx the Rx sections can be powered down to extend battery life, conversely in Rx major sections of the Tx can be treated in the same manner.

Serial Control and Data Interfaces

C-BUS: Serial control, data and command program interface compatible with SCI, SPI and Microwire type interfaces.

Power Requirements and Economy

With an ultra low power requirement, the CMX883 operates from a single 2.7 to 3.6 Volt supply with graduated 'Sleep Mode' powersaving facilities for both Rx and Tx modes.

Signalling:

XTCSS

A state-of-the-art (squelch) signalling format, employing both sub-audio (CTCSS) and in-band (XTC) signalling concurrently, which offers more than twice as many privacy codes as standard CTCSS operation and completely eliminates interference caused by other traffic on the channel (quiet operation). Additionally, the XTCSS signalling can be employed as an over-air control for such features as voice-compression. XTCSS is fully compatible with both conventional and enhanced CTCSS signalling operations and will implement the *All Call Code* function.
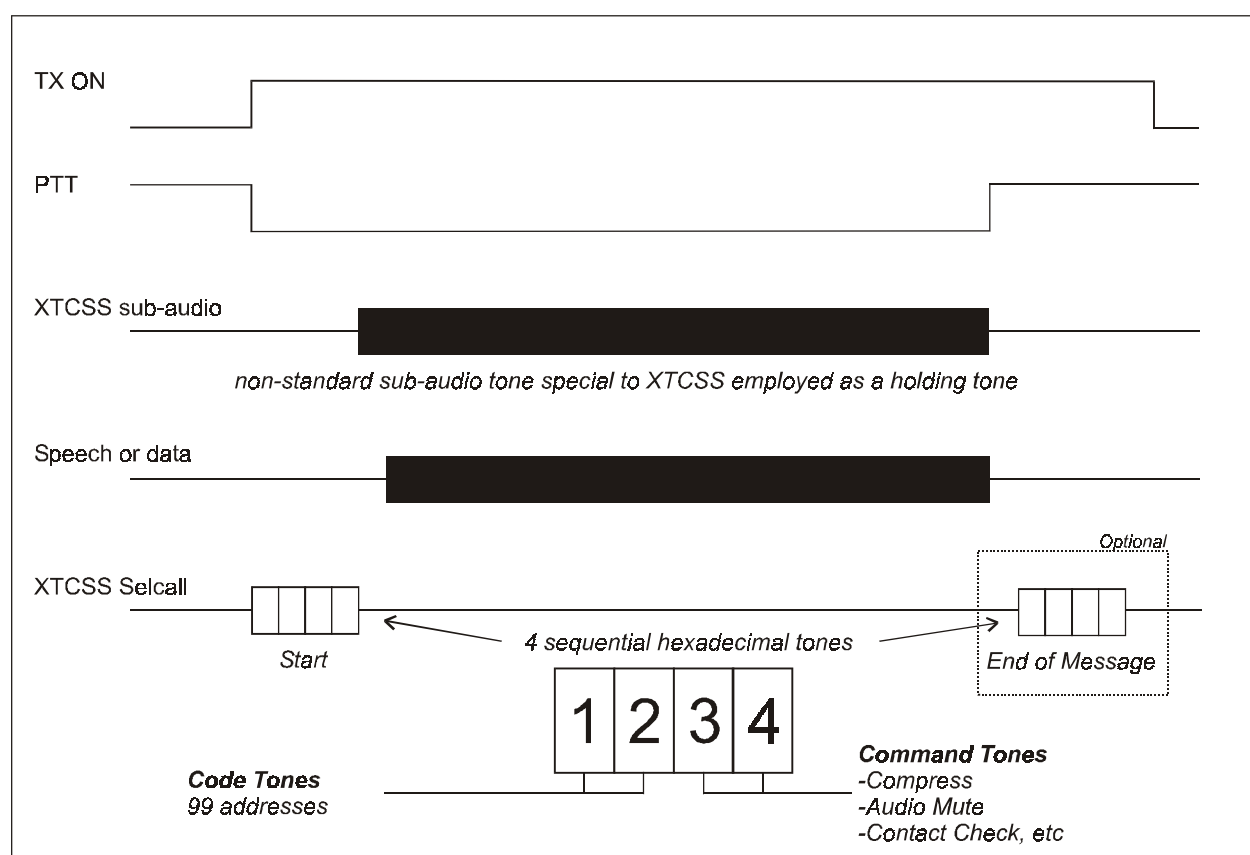
CTCSS

Zero 'talkdown' performance eliminates unwanted breaks in communication. The CMX883 is pre-programmed with 39 standard CTCSS (+ Notone and DCS 'turn off' tone) and 12 additional 'split-tone' frequencies. Any one of these can be selected for reception or transmission. Decoding is aided by the use of adjustable decode bandwidths and threshold levels. Decoding is carried out rapidly thus avoiding the loss of the beginning of speech or data signals. A CTCSS configuration of this product enables 'Tone Cloning'.

Two unique features of this product are its CTCSS 'All Call Code' and 'All Codes Monitor' modes:

All Call Code – transmissions using this code will be heard by all CMX883 enhanced radios regardless of their selected CTCSS code. This provides an important benefit to both safety and convenience.

All Codes Monitor – selection of this code at the receiver enables all transmissions that are using a CTCSS tone to be heard, and the tone number to be reported. Open channel noise or calls lacking coding, will go unheard. This is a superior method of 'channel monitoring', which allows miscoded calls from conventional CTCSS-party radios to be heard and directly responded to.

DCS

The DCS code is in NRZ format and is transmitted at 134.4b/s in either 23 or 24 bit patterns. The code, for transmission or reception is programmed via the host µC with the 'turn off' tone being supplied from the CTCSS facility. Decoding is carried out rapidly thus avoiding the loss of the beginning of speech or data signals.

Signal Monitor

An auxiliary circuit intended for the monitoring of any signal or level; both internal and external. This function can be used in conjunction with the host µC to allow such activities as: VOX operation and/or the 'wake-up' of powered-down circuitry.

Audio Processing:

Adjustable Gain Input Amplifiers

Selectable, component adjustable inputs are available for microphone or line voiceband or discriminator inputs. In either mode (Tx or Rx) the selected input can be further level adjusted under the control of the host µC prior to signal or audio- processing.

Voiceband and Sub-Audio Filtering with Limiting

Both Rx and Tx paths present voiceband filtering; the Tx path filter can be configured to either 12.5 or 25 kHz channel spacing whilst the Rx path also includes a sub-audio passband filter.

Voiceband Pre-emphasis and De-emphasis

Voiceband pre-emphasis is selectable to either 12.5 or 25 kHz channel configurations in the Tx path; de-emphasis at –6dB/ octave is selectable in the Rx path.

Software Adjustable Gains, Volume, Mixing and Routing

Providing total flexibility of operation, this product, under µC control has the ability to select and route functions and audio and signal paths, set bandwidths and threshold levels, mix audio and sub bands and vary both input and out gain/attenuation levels. Output levels from all analogue ports can be 'ramped' up and down at independently programmed rates.

Attenuation-Adjustable Single/Two-Point Modulation Outputs

To facilitate a wide range of transmitter types, the CMX883 has the ability to provide, independently programmable, modulation outputs; for single or two-point modulation schemes.

Scrambler

An optional frequency inversion scrambler is provided in both transmit and receive modes.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.2   Block Diagram
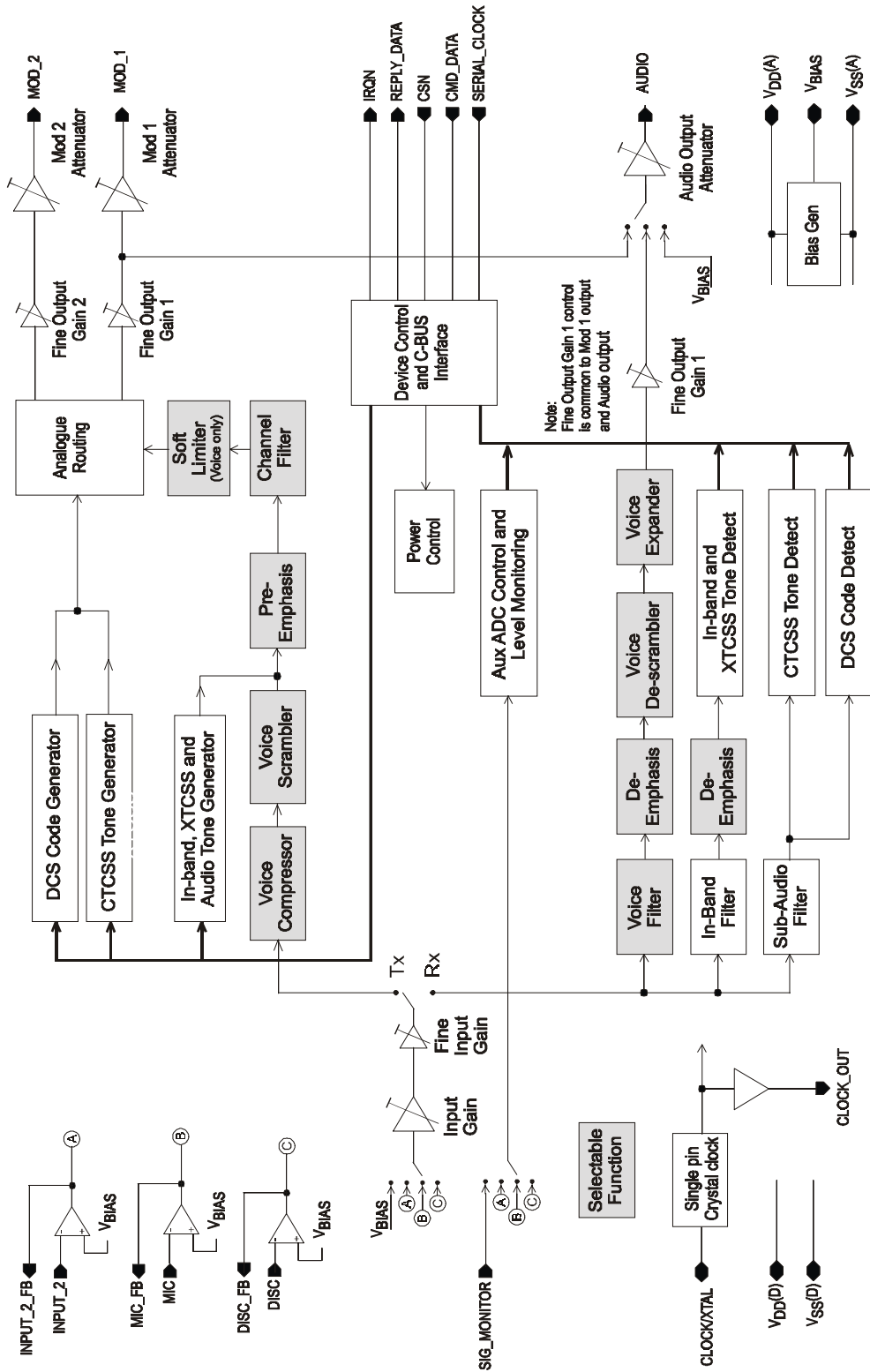
Figure 1 Block Diagram

1.3   Signal List

Package D6, E1	Signal		Description
Pin No.	**Name**	**Type**	
23	$V_{DD(D)}$	Power	The digital positive supply rail. This pin should be decoupled to $V_{SS(D)}$ by a capacitor mounted close to the device pins.
5	$V_{SS(D)}$	Power	The negative supply rail (digital ground).
18	$V_{DD(A)}$	Power	The analogue positive supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to $V_{SS(A)}$ by a capacitor mounted close to the device pins.
9, 21	$V_{SS(A)}$	Power	The negative supply rail. Both pins must be connected to analogue ground.
1, 2		NC	No connection should be made to these pins.
3	IRQN	O/P	A 'wire-ORable' output for connection to the Interrupt Request input of the host. This output is pulled down to $V_{SS(D)}$ when active and is high impedance when inactive. An external pull-up resistor is required.
4	REPLY_DATA	T/S	The C-BUS serial data output to the host. This output is held at high impedance when not sending data to the host.
6	SERIAL_CLOCK	I/P	The C-BUS serial clock input from the host.
7	CMD_DATA	I/P	The C-BUS serial data input from the host.
8	CSN	I/P	The C-BUS data loading control function. Data transfer sequences are initiated, and completed by the CSN signal.

1.3   Signal List (continued)

Package D6, E1	Signal		Description
Pin No.	**Name**	**Type**	
10	V_{BIAS}	O/P	Internally generated bias voltage of approximately $V_{DD(A)}/2$, except when bias is power-saved when V_{BIAS} will discharge to $V_{SS(A)}$. This pin should be decoupled to $V_{SS(A)}$ by a capacitor mounted close to the device pins.
11	DISC	I/P	Input terminal of discriminator input amplifier.
12	DISC_FB	O/P	Output / feedback terminal of discriminator input amplifier.
13	INPUT_2	I/P	Input terminal of amplifier 2, for either a second microphone or discriminator input.
14	INPUT_2_FB	O/P	Output / feedback terminal of input amplifier 2.
15	MIC	I/P	Input terminal of microphone input amplifier.
16	MIC_FB	O/P	Output / feedback terminal of microphone input amplifier.
17	SIG_MONITOR	I/P	Signal Monitor input to the internal level detecting circuit.
19	MOD_1	O/P	Modulator 1 output.
20	MOD_2	O/P	Modulator 2 output.
22	AUDIO	O/P	Output of the audio section.
24	CLOCK/XTAL	I/P	The input to the on-chip oscillator for an external crystal or a clock circuit.
25	CLOCK_OUT	O/P	Buffered (un-inverted) clock output available for use by other devices in the system.
26		I/P	Test input, connect to $V_{SS(D)}$.
27, 28		NC	No connection should be made to these pins.

Notes: I/P = Input
O/P = Output
T/S = 3-state Output
NC = No Connection
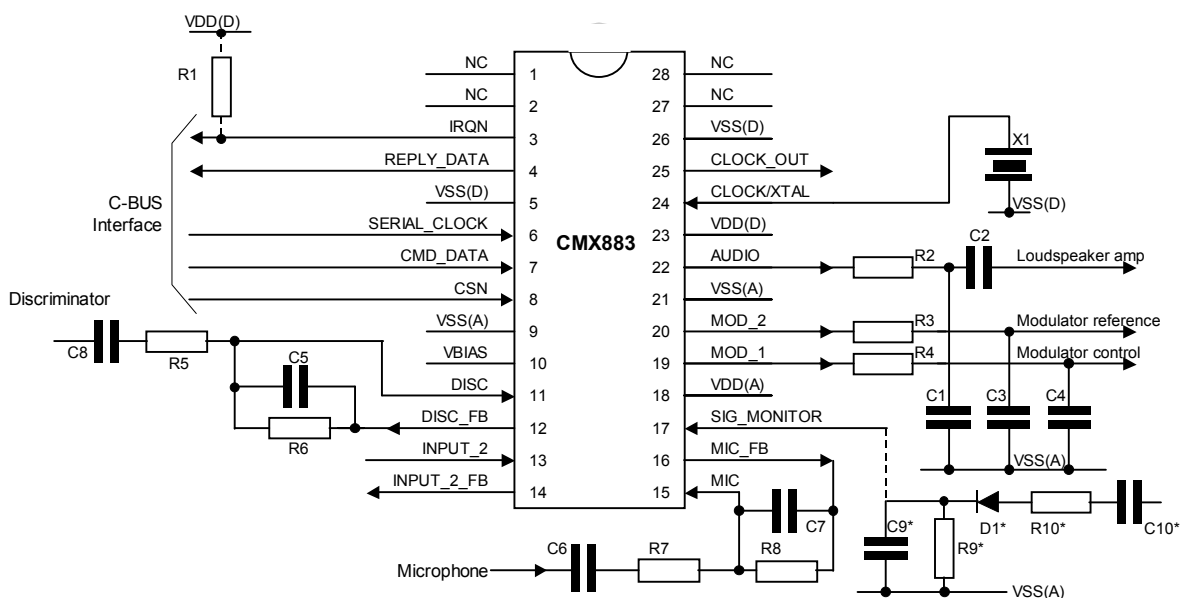
1.4 External Components

Figure 2 Recommended External Components

R1	100kΩ	R9	See note 6	C6	See note 4	
R2	100kΩ	R10	See note 6	C7	200pF	
R3	100kΩ			C8	See note 4	
R4	100kΩ	C1	100pF	C9/10	See note 6	
R5	See note 2	C2	1nF			
R6	100kΩ	C3	100pF	X1	18.432MHz	See note 1
R7	See note 3	C4	100pF			
R8	100kΩ	C5	100pF	D1	See note 6	

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The clock drift requirement is defined in section 1.8.1. The tracks between the crystal and pin 24 and pin 5 should be as short as possible to achieve maximum stability and best start up performance.

2. R5 should be selected to provide the desired dc gain (assuming C8 is not present) of the discriminator input, as follows:

$$\left|\text{GAIN}_{Disc}\right| = 100\text{k}\Omega \ / \ \text{R5}$$

The gain should be such that the resultant output at the DISC_FB pin is within the discriminator input signal range specified in section 1.8.1.

3. R7 should be selected to provide the desired dc gain (assuming C6 is not present) of the microphone input as follows:

$$\left|\text{GAIN}_{Mic}\right| = 100\text{k}\Omega \ / \ \text{R7}$$

The gain should be such that the resultant output at the MIC_FB pin is within the microphone input signal range specified in section 1.8.1.

4. C6 and C8 should be selected to maintain the lower frequency roll-off of the microphone and discriminator inputs as follows:

$$\text{C6} = 30\text{nF} \times \left|\text{GAIN}_{Mic}\right| \qquad \text{and C6} > 1000\mu\text{F} \ / \ \text{R7}$$
$$\text{C8} = 100\text{nF} \times \left|\text{GAIN}_{Disc}\right| \qquad \text{and C8} > \text{TBA}\mu\text{F} \ / \ \text{R5}$$

5. INPUT_2 and INPUT_2_FB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the networks around pins 11 and 12 or pins 15 and 16 respectively. If this input is not required pin 13 must be connected to pin 14.

6.   The circuit formed by D1, C9, C10, R9 and R10 is a peak detector, this is only required when the signal monitor is connected to an ac signal (e.g. microphone or received signal). For a dc type signal (e.g. RSSI) these components are not required. The values of C9 and R10 set the attack time, C9 and R9 set the decay time. D1 can be any suitable small signal diode. R10 should be a high enough value so as not to distort the signal source.

1.4.1   PCB Layout Guidelines and Power Supply Decoupling
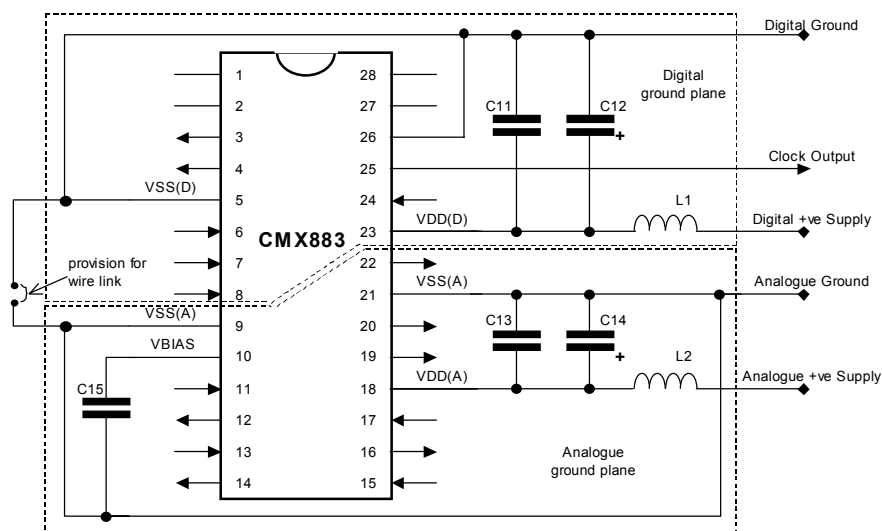
Figure 3 Power Supply Connections and De-coupling

C11	10nF		C14	10μF		L1	100nH	See note 7
C12	10μF		C15	100nF		L2	100nH	See note 7
C13	10nF							

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

7.   The inductors L1 and L2 can be omitted but this may degrade system performance.

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX883 and the supply and bias de-coupling capacitors. The de-coupling capacitors C11, C12, C13 and C14 should be as close as possible to the CMX883, particularly C11 and C13. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the V_{SS}(A) and V_{SS}(D) in the area of the CMX883, with provision to make a link between them close to the CMX883.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input(s) and audio output must be ac coupled as shown, so their return paths can be connected to V_{SS}(A) without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 can be replaced with an external clock source if required/desired. The internal clock generating circuit can be placed in power-save mode if the clock is provided externally.

1.4.2   Modulator Outputs

The combination of CMX883 and the modulator output components, R3/C3 and R4/C4, achieve roll-off rates better than –60dB/decade. If required this can be increased to better than –100dB/decade by replacing R3/C3 and R4/C4 with the active filter circuit shown in Figure 4.
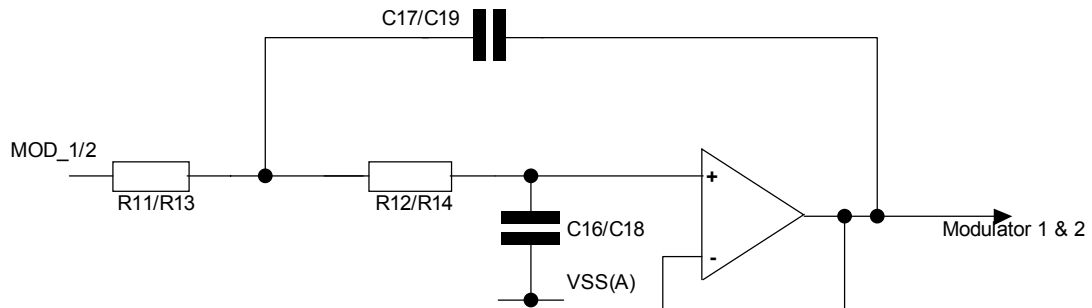
Figure 4 Modulator output components to achieve -100dB/decade roll-off

R11	120kΩ	C16	220pF	
R12	120kΩ	C17	440pF	(2 x C16)
R13	120kΩ	C18	220pF	
R14	120kΩ	C19	440pF	(2 x C18)

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:
8.   The external op-amp must be chosen to ensure that the required signal output level can be driven within acceptable distortion limits.

1.5   General Description

The CMX883 is intended for use in half duplex analogue two way land mobile radio (LMR) equipment and is particularly suited to enhanced MURS / GMRS / FRS terminal designs. The CMX883 provides radio signal encoder and decoder functions for: Voice, in-band tones, XTCSS, CTCSS and DCS permitting simple to sophisticated levels of tone control and data transfer. Power control facilities allow the device to be placed in varying levels of sleep allowing the user to fine tune the power depending on system requirements. The CMX883 includes a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX883 is shown in Figure 1.

Tx functions
- **Audio**
  - Single/dual microphone inputs with input amplifier and programmable gain adjustment
  - Filtering selectable for 12.5kHz and 25kHz channels
  - Selectable pre-emphasis
  - Selectable compression
  - Selectable frequency inversion voice scrambling
  - 2-point modulation outputs with programmable level adjustment
- **Signalling**
  - Pre-programmed 51 tone CTCSS encoder
  - Programmable 23/24bit DCS encoder
  - Programmable audio tone generator (for custom audio tones)
  - Pre-programmed XTCSS and in-band tone encoder

Rx functions
- **Audio**
  - Single/dual demodulator inputs with input amplifier and programmable gain adjustment
  - Voice-band and sub-audio rejection filtering
  - Selectable de-emphasis
  - Selectable expansion
  - Selectable frequency inversion voice de-scrambling
  - Software volume control
- **Signalling**
  - 1 from 51 CTCSS decoder + Tone Clone mode
  - 23/24bit DCS decoder
  - Pre-programmed in-band tone decode with XTCSS 4 tone addressing
  - Signal Monitor (RSSI / Microphone / Rx channel level monitor)

Voice Processing Combinations

Table 1 shows the valid voice processing combinations.

Table 1 Voice Processing Combinations

	TX				RX			
	Compress	Scramble	Pre-Emphasis	Filter	Filter	De-Emphasis	De-Scramble	Expand
1				✓	✓			
2			✓	✓	✓	✓		
3		✓	✓	✓	✓	✓	✓	
4		✓		✓	✓		✓	
5	✓		✓	✓	✓	✓		✓
6	✓			✓	✓			✓
Not Valid								
7	✓	✓	✓	✓	✓	✓	✓	✓
Not Recommended								
8[1]	✓	✓		✓	✓		✓	✓

Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX883 and the host μC; this interface is compatible with microwire, SPI etc. Interrupt signals notify the host μC when a change in status has occurred and the μC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 1.6.15.

Auxiliary (Signal Monitor) analogue signal

The CMX883 includes a Signal level monitor. This is an 8-bit successive approximation ADC and a two level signal sensor. The two level sensor facility can be used in conjunction with the power saving mode to wake up powered down blocks, and issue an interrupt on the IRQN line when the Signal exceeds the preset threshold level. The auxiliary ADC voltage reference is taken directly from the $V_{DD}(A)$ supply, so the Signal level being monitored should be derived from this supply voltage.

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[1] Audio quality is somewhat degraded.

1.5.1   Sleep Mode and Auto Start Up

Power-on reset or C-BUS general reset places the CMX883 into sleep mode, which results in all internal blocks, except the xtal clock circuit, being placed in power-saved mode. The xtal clock circuit can be power-saved but this must be done by an explicit C-BUS command. Power saving is achieved by turning off bias current sources or disabling local clocks, as appropriate.

During system standby periods, parts of the device can be put into sleep mode by the host to conserve power. The Auxiliary ADC can be programmed so that when the level exceeds a threshold, an interrupt is issued over the C-BUS and the selected mode (Tx or Rx) "woken up" within 400µs. If this time is too long to ensure no part of the signal is lost, the DISC or MIC input and ADC path can be kept powered up whilst in standby mode. The receive modes and transmit modes can also be activated by commands from the C-BUS. On wake up, activation of the various signal path stages are phased appropriately to avoid causing unwanted transients. More details are provided in section 1.6.4 on Signal Routing.

The CMX883 can be programmed to wake up its receive path automatically (automatic start-up) when the DISC input level exceeds the 'high' level threshold. While the CMX883 is in automatic receive start-up mode the DISC input must also be selected for the signal path. When not in automatic start-up mode it is recommended that the required input is selected during Auxiliary ADC operation to avoid subsequent switching of the input signal source.

1.5.2   Auxiliary ADC

This section of the CMX883 operates in both Tx and Rx modes and can be used to monitor one of 4 signal sources: Sig_Monitor pin, MIC1, Input_2 or DISC inputs. Activity on the selected input will optionally issue an interrupt if host intervention is required. During idle periods the majority of the CMX883 can be placed into low power mode. If monitoring ac signals connected to the Sig_Monitor pin they must be rectified and filtered using passive external circuitry.

The Auxiliary ADC facility comprises an 8-bit ADC, a comparator, an 8-bit result data word and two 8-bit threshold registers, one defining the 'Signal high' level and the other the 'Signal low' level. The two threshold registers are combined into one 16-bit C-BUS register word. The ADC measures the Signal level at intervals that are set by C-BUS command. It is advised that the interval be set to <125µs while waiting for a new incoming signal so that the CMX883 and host µC can be powered up and put into the correct mode in time to avoid missing any part of the signal. The default interval period following a reset is 20.8µs. Power dissipation of the Auxiliary ADC can be reduced by increasing the conversion interval time.

The result of the most recent Auxiliary ADC measurement can be read over the C-BUS whenever the Signal Processing and Aux ADC circuits are powered up.

The Auxiliary ADC compares each conversion result with the values in the 'Signal high' or the 'Signal low' threshold registers. The CMX883 can, for example, issue an interrupt to the host µC to wake up the receive path when the Auxiliary ADC input exceeds the 'high' level threshold. The CMX883 can also issue an interrupt to the host µC to indicate a weak or absent signal when it falls below the 'low' level threshold. This provides a user programmable hysteresis facility. The host must ensure that the value in the 'low' register is always less than that of the 'high' register. The options for issuing interrupts and for automatic start-up are selected by C-BUS command.

The Auxiliary ADC options are controlled by the $B2, $B3 and $C0 C-BUS registers.

The Auxiliary ADC requires the Auxiliary ADC, BIAS and Xtal clock to all be enabled in the Power Down Control register.

1.5.3 Receive Mode

The CMX883 can receive voice and various signal formats: CTCSS tone, DCS code and XTCSS / In-band tones. Reception of each of these signal types can be independently enabled/disabled by C-BUS command. If enabled, an interrupt will be issued to notify the host μC of the presence and type of the incoming signal.

In receive mode the CMX883 performs signal type identification in 2 frequency bands, sub-audio (60 - 260Hz) and voice band (300 - 3kHz), to determine what type of signal is being received. When an enabled signal is detected this will be indicated to the host over the C-BUS and the CMX883 will continue to process the received signal in its band. Identification / process mode will continue in the other band. The CMX883 can process voice and simultaneously identify and process at least 2 other signal types (one in the sub-audio in parallel with one in the voice band). See Table 2 for valid combinations. These combinations can be used with Voice Processing, if desired.

The receive gain and audio output amplifier gain can be adjusted by the host μC, via C-BUS command, to provide receive signal level adjustment and output volume control or muting.

Table 2 Concurrent Rx Signalling Modes Supported by the CMX883

Sub-Audio *All combinations of:*	Voice band signalling
DCS Inverted DCS CTCSS	XTCSS or In-band tones

By disabling all the decoding modes, the device can be configured to receive voice only signals with no decoding of the voice band, CTCSS or DCS signalling. This will result in reception of all signals as if they are voice. In this case it is up to the user/host μC to respond appropriately to incoming signals.

The CMX883 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Power-save level of the modulator outputs is the same as the V_{BIAS} pin, so the audio output level must also be at this level before switching.

1.5.3.1   Receiving Voice Band Signals

When a voice based signal is being received, it is up to the μC, in response to signal status information provided by the CMX883, to control muting/enabling of the voice band signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 5, to remove sub-audio components and to minimise high frequency noise. When appropriate the voice signal can then be routed to the AUDIO output.
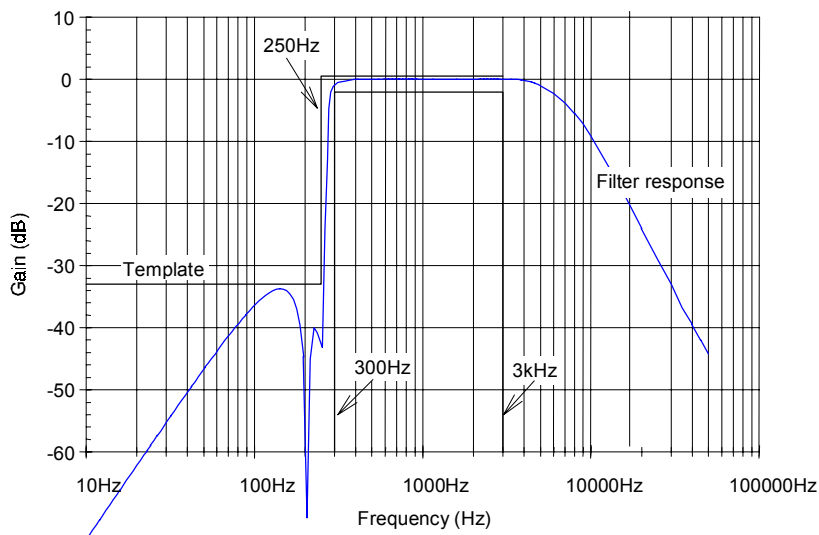
Figure 5 Rx Audio Filter Frequency Response

De-emphasis

Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 6) can be selected to facilitate compliance with TIA/EIA-603.
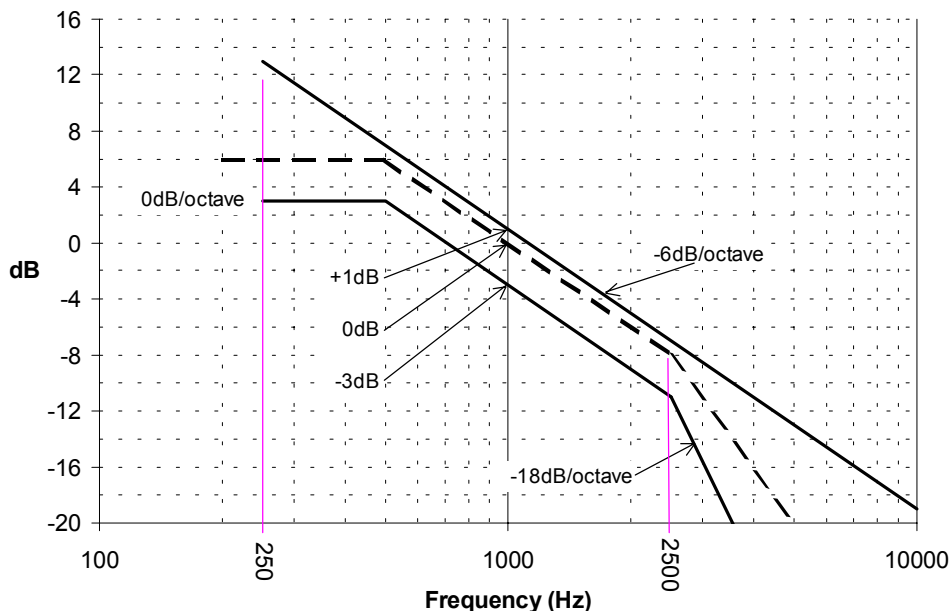
Figure 6 De-emphasis Curve for TIA/EIA-603 Compliance

Rx Companding (Expanding)
The CMX883 incorporates an optional syllabic compandor in both transmit and receive modes. This expands received voice band signals that have been similarly compressed in the transmitter to enhance dynamic range. The compandor attack, decay and 0dB point are defined in section 1.8.1. See section 1.6.9 for details of how to control this function.

Audio De-Scrambling
The CMX883 incorporates an optional frequency inversion de-scrambler receive mode. This de-scrambles received voice band signals that have been scrambled in the transmitter. See section 1.6.9 for details of how to control this function.

Voice Processing Combinations
Table 1 shows the valid voice processing combinations. (See section 1.5).

1.5.3.2   Receiving and Decoding CTCSS Tones

The CMX883 is able to accurately detect valid CTCSS tones quickly to avoid losing the beginning of voice or possibly data transmissions, and is able to continuously monitor the detected tone with minimal probability of falsely dropping out. The received signal is filtered in accordance with the template shown in Figure 7, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.
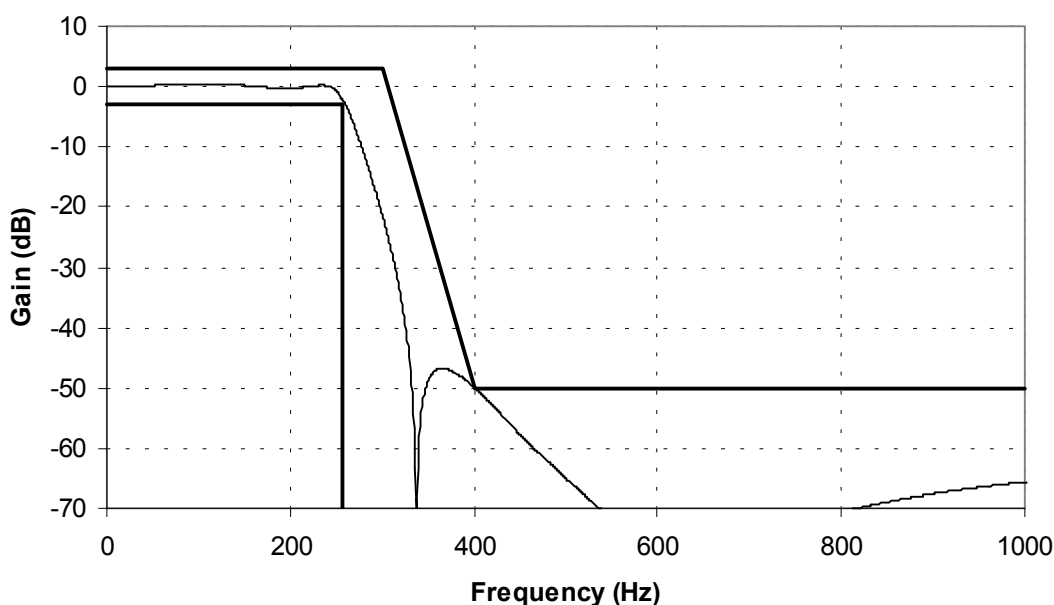
Figure 7 Low Pass Sub-Audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, the voice band signal can be passed to the audio output. The voice band signal is extracted from the received signal by band pass filtering as shown in Figure 5.

To help decode received CTCSS tones adjustable decoder bandwidths and threshold levels permit decode certainty and signal to noise performance to be traded when congestion or range limits the system performance. This entails setting the tone decoder bandwidth and threshold level in P2.1 of the Programming register ($C8) and programming the Audio & Tx CTCSS Control register with the desired tone.

Tone Cloning[TM]
Tone Cloning[TM] facilitates the detection of CTCSS tones 1 to 39 in receive mode. This allows the device to non-predictively detect any tone in this range. The range received tone number will be reported in the

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[TM] Tone Cloning is a trademark of CML Microsystems Plc.

Tones Status register. This tone code can then be programmed into the 'Audio and Device Address Control' register, by the host µC. The cloned tone will only be active when CTCSS is enabled in the Mode register.

Tone cloning should not be used in systems where tones 41 to 51 or other split tones (tones between the frequencies of tones 1 to 40) may be received. The all call tone 40 can still be used after tone cloning has been performed.

CTCSS Tones

Table 3 lists the CTCSS tones available. The tone numbers are decimal equivalents of the numbers written to the Audio & Device Address Control register ($C2) and reported in the Tone Status register ($CC).

Table 3 CTCSS Tones

Tone Number	Freq. (Hz)	Tone Number	Freq. (Hz)	Tone Number	Freq. (Hz)
00[1]	No Tone	20	131.8	40[2]	62.5*
01	67.0	21	136.5	41	159.8*
02	71.9	22	141.3	42	165.5*
03	74.4	23	146.2	43	171.3*
04	77.0	24	151.4	44	177.3*
05	79.7	25	156.7	45	183.5*
06	82.5	26	162.2	46	189.9*
07	85.4	27	167.9	47	196.6*
08	88.5	28	173.8	48	199.5*
09	91.5	29	179.9	49	206.5*
10	94.8	30	186.2	50	229.1*
11	97.4	31	192.8	51	254.1*
12	100.0	32	203.5	*52-54*	*Reserved*
13	103.5	33	210.7	*55[3]*	*Invalid*
14	107.2	34	218.1		*tone*
15	110.9	35	225.7	*>=56*	*Reserved*
16	114.8	36	233.6		
17	118.8	37	241.8		
18	123.0	38	250.3		
19	127.3	39	69.3		

* Subaudio tone not in TIA-603A standard.

Notes:
1   Tone number 00 in the Tone Status register ($CC) indicates that none of the above subaudio tones is being detected - see also section 1.6.19. If tone number 00 is programmed into the Audio & Device Address Control register ($C2) only tone 40 will be scanned for - see note 2. If CTCSS transmit is selected this tone setting will cause the CTCSS generator to output no signal.
2   Tone number 40 provides an all user CTCSS tone option; regardless of the subaudio tones set, the CMX883 will indicate to the host when this tone is detected whenever the CTCSS detector is enabled. This feature is useful for implementing emergency type calls. e.g. all call.
3   Tone number 55 is reported in the Tone Status register ($CC), when CTCSS receive is enabled and a subaudio tone is detected that does not correspond to the selected tone or the all-call tone (tone number 40). This could be a tone in the subaudio band which is not in the table or a tone in the table which is not the selected tone or all-call tone.

1.5.3.3   Receiving and Decoding DCS Codes

DCS Code is in NRZ format and transmitted at 134.4 ±0.4bps. The CMX883 is able to decode any 23 or 24 bit pattern in either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4. The CMX883 can detect a valid DCS Code quickly enough to avoid losing the beginning of voice transmissions.

Table 4 DCS Modulation Modes

Modulation Type:	Data Bit:	FM Frequency Change:
A	0	Minus frequency shift
	1	Plus frequency shift
B	0	Plus frequency shift
	1	Minus frequency shift

The CMX883 detects the DCS code that matches the programmed code defined in the 'DCS Code' words (P2.2-3) in the Programming register ($C8).

To detect the pre-programmed DCS code the signal is low pass filtered to suppress all but the sub-audio band using the filter shown in Figure 7. Further equalisation filtering, signal slicing and level detection are done to extract the code being received. The extracted code is then matched with the programmed 23 or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 5 shows a selection of valid 23-bit DCS codes, this does not preclude other codes being programmed. Recognition of a valid DCS Code will be flagged if the decode is successful (3 or less errors). A failure to decode is indicated by a '0' flag. This flag is updated after the decoding of every 4th bit of the incoming signal.

Once a valid DCS Code has been detected, the voice band signal can be passed to the AUDIO output under the control of the host μC. The voice signal is extracted from the received input signal by band pass filtering; see Figure 5.

More details for programming DCS Codes are provided in section 1.6.20.3.

The end of DCS transmissions is indicated by a 134.4 ±0.5Hz tone for 150-200ms. Detection of the turn off tone is enabled whenever DCS receive is active. To detect the DCS turn off tone while receiving DCS, the DCS turn off tone option must be selected in the Audio and CTCSS Control ($C2) register and CTCSS receive must also be enabled.

Table 5 DCS 23 Bit Codes

DCS Code	DCS bits 22-12	DCS bits 11-0	DCS Code	DCS bits 22-12	DCS bits 11-0	DCS Code	DCS bits 22-12	DCS bits 11-0
023	763	813	174	18B	87C	445	7B8	925
025	6B7	815	205	6E9	885	464	27E	934
026	65D	816	223	68E	893	465	60B	935
031	51F	819	226	7B0	896	466	6E1	936
032	5F5	81A	243	45B	8A3	503	3C6	943
043	5B6	823	244	1FA	8A4	506	2F8	946
047	0FD	827	245	58F	8A5	516	41B	94E
051	7CA	829	251	627	8A9	532	0E3	95A
054	6F4	82C	261	177	8B1	546	19E	966
065	5D1	835	263	5E8	8B3	565	0C7	975
071	679	839	265	43C	8B5	606	5D9	986
072	693	83A	271	794	8B9	612	671	98A
073	2E6	83B	306	0CF	8C6	624	0F5	994
074	747	83C	311	38D	8C9	627	01F	997
114	35E	84C	315	6C6	8CD	631	728	999
115	72B	84D	331	23E	8D9	632	7C2	99A
116	7C1	84E	343	297	8E3	654	4C3	9AC
125	07B	855	346	3A9	8E6	662	247	9B2
131	3D3	859	351	0EB	8E9	664	393	9B4
132	339	85A	364	685	8F4	703	22B	9C3
134	2ED	85C	365	2F0	8F5	712	0BD	9CA
143	37A	863	371	158	8F9	723	398	9D3
152	1EC	86A	411	776	909	731	1E4	9D9
155	44D	86D	412	79C	90A	732	10E	9DA
156	4A7	86E	413	3E9	90B	734	0DA	9DC
162	6BC	872	423	4B9	913	743	14D	9E3
165	31D	875	431	6C5	919	754	20F	9EC
172	05F	87A	432	62F	91A			

1.5.3.4   Receiving and Decoding In-band Tones

In-band tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid In-band tone is detected and when a present In-band tone turns off or changes (i.e. at the start and at the end of each In-band tone).

The CMX883 implements QTC coding using the EEA tone set. Other addressing and data formats can be implemented but will require more host intervention. The custom tones (1-4) permit other audio tones to be encoded or decoded, the frequency of each tone is defined in the program registers P1.2-5.

In receive the CMX883 scans through the tone table sequentially, the code reported will be the first one that matches the incoming frequency.

Adjustable decoder bandwidths, threshold levels are programmable via the Programming register and permits certainty of detection and signal to noise performance to be traded when congestion or range limits the system performance. The In-band signal is derived from the received input signal after the band pass filtering shown in Figure 5.

Table 6 In-band Tones

Special / Information Tones (5th bit = 0)			Normal Tones (5th bit = 1)		
4 bit Code		Freq.	4 bit Code		Freq.
Dec	Hex	(Hz)	Dec	Hex	(Hz)
0	0	No Tone	0	0	1981
1	1	Custom Tone 0 P1.2[1]	1	1	1124
2	2	Custom Tone 1 P1.3[1]	2	2	1197
3	3	Custom Tone 2 P1.4[1]	3	3	1275
4	4	Custom Tone 3 P1.5[1]	4	4	1358
5	5		5	5	1446
6	6		6	6	1540
7	7		7	7	1640
8	8		8	8	1747
9	9		9	9	1860
10	A	Reserved	10	A	1055
11	B		11	B	930
12	C		12	C	2247
13	D		13	D	991
14	E		14	E	2110[2]
15	F		15	F	No Tone

Notes:

1   Special tones 1-4 provide user programmable tone options for both transmit and receive modes as set in the indicated Program register, for programming information see section 1.6.20.2.

2   Normal tone 14 is the repeat tone, this code is must be used in transmit when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones the CMX883 will indicate the repeat tone when it is received, it is up to the host to interpret this and decode tones accordingly.

1.5.3.5   Receiving XTCSS Signals

The CMX883 can decode and monitor for XTCSS signalling. XTCSS is used to identify the start and optionally the end of voice/data/other calls. It provides additional information and control over the basic CTCSS method of channel coding.

XTCSS coding starts with a 4 tone sequence indicating the address and content of the following message. Immediately after the 4 tone sequence a sub-audio maintenance tone is sent for the duration of the call. At the end of the call the maintenance tone is removed and an optional 4 tone sequence sent indicating the end of message (EOM). For further details on XTCSS see section 1.5.5.

By enabling XTCSS reception the host instructs the CMX883 to search for a valid 4 tone sequence, an interrupt (if enabled) will be generated when this occurs. The 4 tone sequence will be indicated in the C-BUS register ($C9) for the host to read out using the tone numbers in Table 6.

The sub-audio tone will be searched for after a valid 4 tone In-band sequence if CTCSS detection is also enabled. CTCSS codes will be decoded and reported as defined in section 1.5.3.2. It is not necessary to enable CTCSS in the Mode Control register for the device to search for the XTCSS sub audio tone.

In receive, whenever the XTCSS detect bit is set the CMX883 will search for a valid 4 tone In-band sequence however detection of a CTCSS tone will inhibit the search for 4 tone sequences. To be valid the 4 tones must be preceded and followed by silence in the audio band (signals below the audio detect level - see program register P1.1) for the programmed no tone time. The presence (or absence) of the sub-audio maintenance tone will only be indicated to the host if the CTCSS detect bit is also set. After the 4 tone sequence is detected the maintenance tone can be used by the host to detect fades and the end of the message and hence can disable the audio path in sympathy with this tone being absent. At any time the XTCSS enable bit is set and maintenance tone is not decoded the 4 tone set will be automatically searched for.

It is possible (although unlikely) that a fade will exactly coincide and obliterate 2 lots of 4 tone sequence indicating an EOM and the start of a new message. In this case, the host could misinterpret the received signal as a long fade and enable the voice when the maintenance tone reappears. It is therefore recommended that the host operates a timer that is started on loss of maintenance tone. If this times out the host can then assume that the fade is long enough that the original call is lost or has become so corrupted that it is not worth continuing with. The host could then choose only to restore the audio path on the next occurrence of a valid XTCSS tone set. Note that the XTCSS detector operates independently and the host may enable or disable the audio path at any time.

1.5.4   Transmit Mode

The device operates in half duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host μC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation, separate sub-audio and voice band outputs. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid erroneous transmission of out of band frequencies when changing from Rx to Tx the MOD_1 and MOD_2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching. Similarly, when starting a transmission, the transmitted signal strength is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal strength is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Programming register P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

Table 7 Concurrent Tx Modes Supported by the CMX883

Sub-Audio		Voice band
CTCSS		
CTCSS	+	Voice
CTCSS	+	In-band tone
CTCSS^	+	XTCSS
DCS		
DCS	+	Voice
DCS	+	In-band tone
		Voice
		In-band tone
		XTCSS

^ Special subaudio tone only

For all transmissions the host must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX883 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability.

1.5.4.1 Processing Voice Signals for Transmission over Analogue Channels

The microphone input(s), with programmable gain, can be selected as the voice input source. Pre-emphasis is selectable with either version of the 2 analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in ETS-300-086 and/or TIA/EIA-603 compliant applications. Both filters attenuate sub-audio frequencies below 250Hz by more than 33dB wrt the signal level at 1kHz. These filters together with a built in limiter help ensure compliance with ETS-300-086 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.
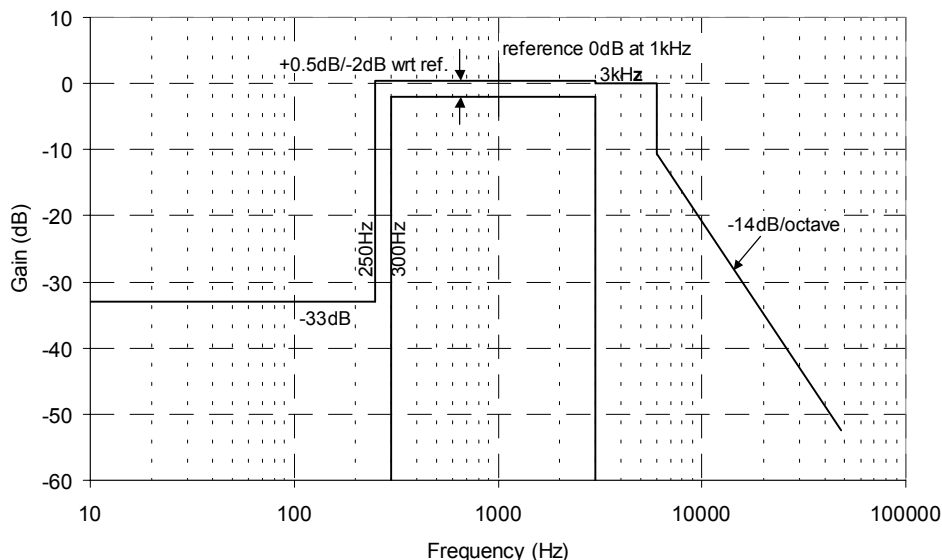
Figure 8 25kHz Channel Audio Filter Response Template

The filter characteristics of the 12.5kHz channel filter fits the filter template shown in Figure 9 (solid outline). This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' and 'B' bands. To achieve attenuation above 3kHz of better than −100dB/decade for TIA/EIA-603 'C' bands (dashed outline), additional external circuitry is required, such as suggested in section 1.4.2.
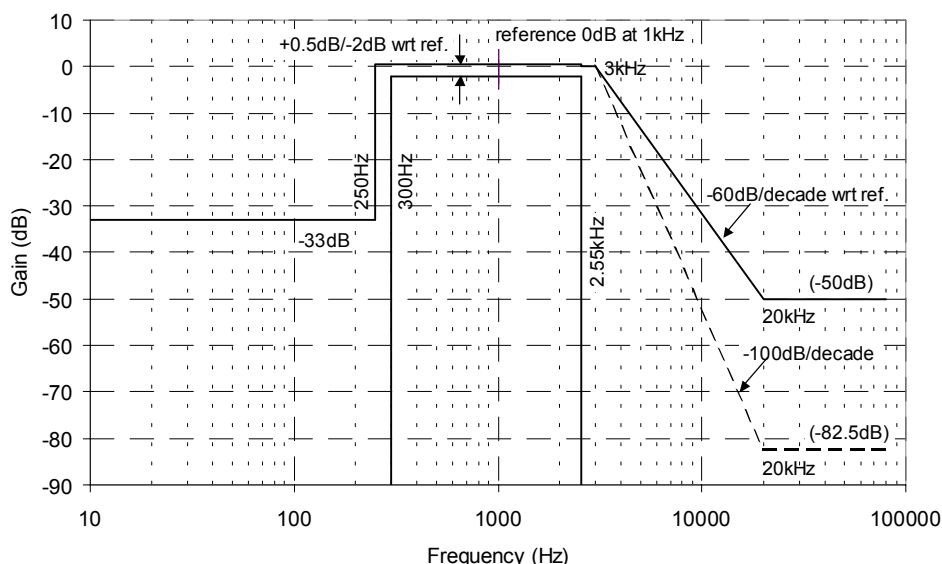
Figure 9 12.5kHz Channel Audio Filter Response Template

The CMX883 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 10.
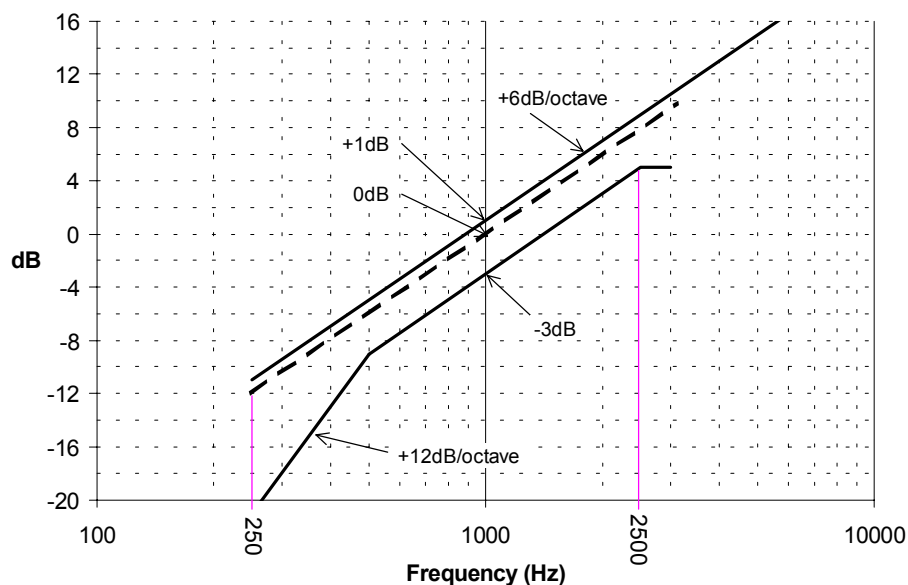
Figure 10 Audio Frequency Pre-emphasis Template

Modulator Output Routing
The sub-audio component can be combined with the voice band signal and this composite signal routed to both MOD_1 and MOD_2 outputs, or the sub-audio and voice band signal can be output separately (sub-audio to MOD_2 and voice band to MOD_1), in accordance with the settings of the Signal Routing register ($B1).

Tx Companding (Compressing)
The CMX883 incorporates an optional syllabic compandor in both transmit and receive modes. This compresses voice band signals before transmission to enhance dynamic range. The compandor attack, decay and 0dB point are defined in section 1.8.1. See section 1.6.9 for details of how to control this function.

Audio Scrambling
The CMX883 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles voice band signals to be de-scrambled in the receiver. See section 1.6.9 for details of how to control this function.

Voice Processing Combinations
Table 1 shows the valid voice processing combinations (see section 1.5).

1.5.4.2   CTCSS Tone
The sub-audio CTCSS tone generated is defined in the Tx CTCSS register ($C2). Table 3 lists the CTCSS tones and the corresponding value for programming the TX TONE bits.

1.5.4.3   DCS Code
A 23 or 24-bit sub-audio DCS Code can be generated, as defined by the 'DCS Code' words (P2.4-5) of the Programming register ($C8); the same DCS Code pattern is used for detection and transmission. The DCS Code is NRZ encoded at 134.4 ± 0.4 bits/s, low pass filtered and added to the voice band signal, prior to passing the signal to the modulator output stages. Valid 23-bit DCS codes and the corresponding settings for the DCS Code Register are shown in Table 5, this does not preclude other codes being programmed. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX883 is able to encode and transmit either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4.

To signal the end of the DCS transmission, the host should set the special sub-audio bits in the Audio & CTCSS Control register ($C2) to enable the DCS turn off tone for 150ms to 200ms. After this time period has elapsed the host should then disable DCS in the Mode register ($C1). Do not enable CTCSS in the Mode Control ($C1) register when transmitting the DCS turn off tone. To summarize, detection of DCS turn off tone requires the CTCSS decoder to be enabled, whereas generation of the DCS turn off tone requires the CTCSS encoder to be disabled.

1.5.4.4   Transmitting In-band Tones

The In-band tone to be generated is defined in the Tx Tone register ($C3). The tone level is set in the Programming register (P1.4). The In-band tone must be transmitted without other signals in the voice band, so the host µC must disable the voice path prior to initiating transmission of a In-band tone, and restore the voice path after the In-band tone transmission is complete. Table 6 shows valid In-band tones, together with the values for programming the In-band bits of the Tx Tone register.

Custom In-band tone frequencies are set in the program register ($C8) P1.6-9. See section 1.6.20.2 for programming details.

1.5.4.5   Transmitting XTCSS Signalling

XTCSS signals can be transmitted by loading the 4 tone pattern and CTCSS tone into the C-BUS registers and enabling XTCSS. The device will transmit the 4 tones in sequence, raise an interrupt when this is complete and then automatically generate the CTCSS tone (if enabled). At the end of the message the CTCSS tone can be disabled by setting the CTCSS enable bit to '0'. The XTCSS 4 tone sequence must be transmitted on its own, so if a voice or a data signal is being transmitted, this must be disabled during the XTCSS 4 tone transmission. See section 1.5.5 for more information.

1.5.5   XTCSS Coding

The CMX883 allows addressed calling using a 4 tone In-band tone burst followed by an optional sub-audio 'XTCSS maintenance tone' (at 64.7Hz). In transmit the CMX883 handles the transmission of the 4 tone sequence and the sub-audio tone. In receive the CMX883 will search for valid In-band tone sequences containing the previously programmed address.

The over air signalling of XTCSS is shown below:

```
XTCSS sub-audio    ----¦                  ┌───────────────┐
                   ----¦                  │               │
                 ──────┴──────────────────┘               └───────

                                          A

In-band tones      ----¦  ┌──┬──┬──┬──┐
                   ----¦  │A1│A0│S0│S1│
                 ──────┴──┴──┴──┴──┴──┴───────────────────────────

                                          B
Voice / Data       ----¦                  ┌───────────────┐
                   ----¦                  │░░░░░░░░░░░░░░░│
                 ──────┴──────────────────┴───────────────┴───────
```
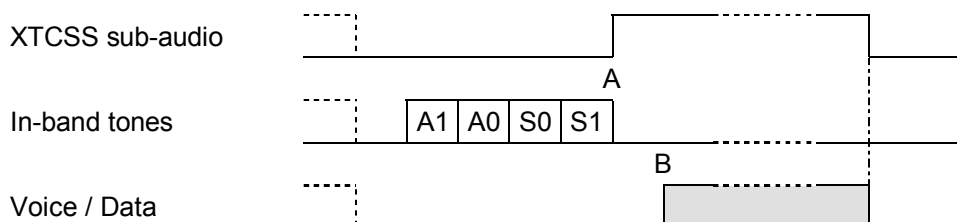
Notes:
- To reduce 'cut on' time with XTCSS voice calls, the host can enable the receive audio path at 'B' (as soon as the 4 tone sequence is available), before the sub-audio is detected.
- XTCSS 4 tone sequences must be prefixed and suffixed with a silent 'no-tone' period of at least the length of each tone. See also programming register P1.1.

In-band tones A1 and A0 are the BCD (binary coded decimal) representation of the Device Address bits of $C2 register, the valid XTCSS address range is 01 to 99, A0 is the least significant digit. The XTCSS address '40' is reserved for an all call address - regardless of the XTCSS address being searched for the CMX883 will always indicate when a valid 4 tone set containing address '40' has been received.

In transmit the CMX883 will only generate the sub-audio maintenance tone when the CTCSS enable bit is set to '0'. The sub-audio tone (if enabled) will be automatically output after the 4th XTCSS tone has been transmitted. An XTCSS interrupt is generated (if enabled) at point 'A' - see diagram above, the host should then wait before enabling the audio path (or transmitting data) to ensure sufficient no-tone suffix to the XTCSS 4 tone set. To summarize, detection of XTCSS sub-audio maintenance tone requires the

CTCSS decoder to be enabled, whereas generation of the XTCSS sub-audio maintenance tone requires the CTCSS encoder to be disabled.

In-band tone S0 is selected from the normal tone range of $B - $D to maintain compatibility with HSC type addressing. In-band tone S1 is selected from the normal tone range $0 - $9. The bit patterns for S0 and S1 indicate the type of information to follow according to the following tables:

In-band tone S0		
Dec	Hex	
0-10	0-$A	Reserved, do not use for S0
11	$B	Silent (non-voice) call to follow, see S1a
12	$C	Voice to follow - see S1b
13	$D	Reserved, do not use for S0

In-band tone S1a		
Dec	Hex	
0-3	0-3	User option for S1a
4-7	4-7	Reserved - do not use for S1a
8	8	End of XTCSS coded message (EOM)
9-13	9-$D	Reserved - do not use for S1a

In-band tone S1b		
Dec	Hex	Voice message Compressed
0	0	No
1	1	Yes
2-13	2-$D	Reserved, do not use for S1b

Note: Tone numbers in the above tables refer to the Normal tone column as defined in Table 6.

Examples:

Device address	Over air 4 tones	Meaning
$22	34C0	Address 34, Un-compressed voice to follow
$03	03C1	Address 03, Compressed voice to follow
$2C	4EB0	Address 44, Non voice, user option 0, (E is repeat character)

Note: For all XTCSS coding the CMX883 will add (in Tx) and strip out (in Rx) the repeat tone as required. The host µC need only load or read out the normal tones listed in Table 6.

1.5.6   C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX883's internal registers and the µC over the C-BUS serial interface. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX883's Write Only Registers, or one or more data byte(s) read out from one of the CMX883's Read Only Registers, as illustrated in Figure 11.

Data sent from the µC on the Command Data line is clocked into the CMX883 on the rising edge of the Serial_Clock input. Reply Data sent from the CMX883 to the µC is valid when the Serial_Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an A/C byte is dependent on the value of the A/C byte. The most significant bit of the address or data are sent first. For detailed timings see section 1.8.1.

C-BUS Write:

CSN   See Note 1   See Note 2

Serial_Clock

CMD_DATA | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 7 | 6 | ... | 0 | | 7 | ... | 0 |
           MSB   LSB   MSB   LSB   MSB   LSB
           Address / Command byte   Upper 8 bits   Lower 8 bits

REPLY_DATA
                       High Z state

C-BUS Read:

CSN   See Note 2

Serial_Clock

CMD_DATA | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
           MSB   LSB
           Address byte   Upper 8 bits   Lower 8 bits

REPLY_DATA | 7 | 6 | ... | 0 | | 7 | ... | 0 |
                       High Z state   MSB   LSB   MSB   LSB
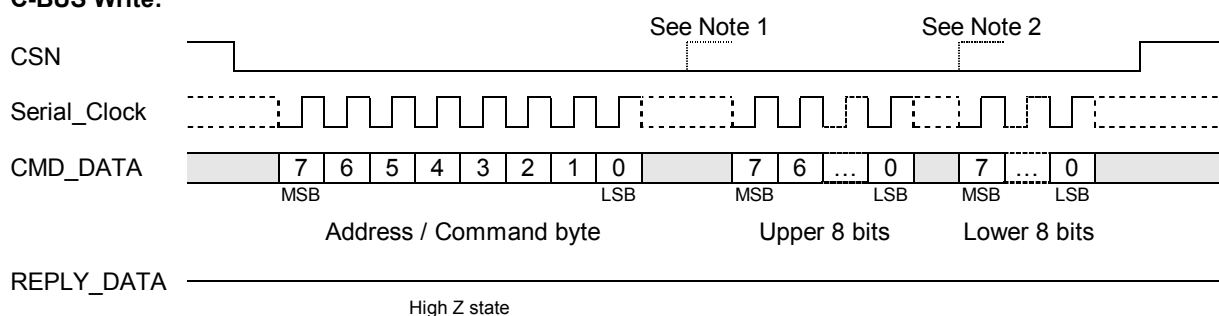
☐ Data value unimportant   ⌐ Repeated cycles   ⌐ Either logic level valid
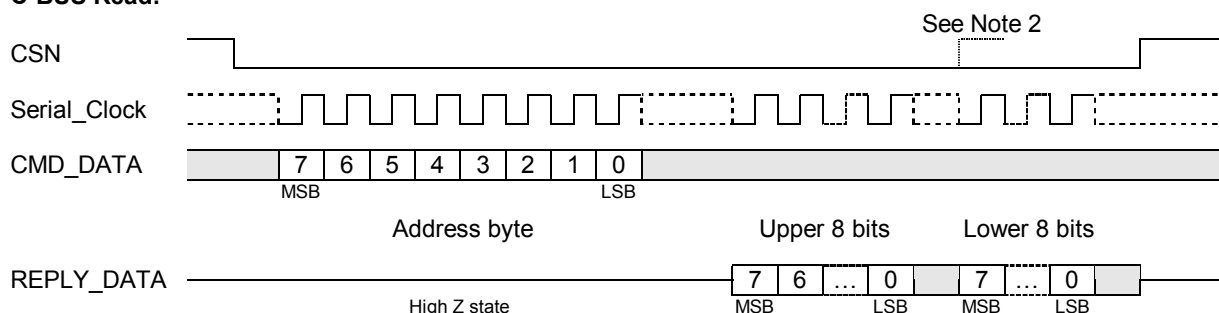
Figure 11 C-BUS Transactions

Notes:
1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CMD_DATA and REPLY_DATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The Serial_Clock input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CMD_DATA and REPLY_DATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

1.6   C-BUS Register Description

1.6.1   C-BUS Register Summary

C-BUS Write Only Registers

ADDR. (hex)	REGISTER	Word Size (bits)
$01	C-BUS RESET	0
$B0	ANALOGUE GAIN	16
$B1	SIGNAL ROUTING	16
$B2	AUXILIARY ADC THRESHOLDS	16
$B3	AUXILIARY ADC CONTROL	8
$C0	POWER DOWN CONTROL	16
$C1	MODE CONTROL	16
$C2	AUDIO & DEVICE ADDRESS CONTROL	16
$C3	TX TONE	16
$C7	RESERVED REGISTER ADDRESS	16
$C8	PROGRAMMING REGISTER	16
$CA	RESERVED REGISTER ADDRESS	16
$CB	XTCSS TX DATA	16
$CD	AUDIO TONE	16
$CE	INTERRUPT MASK	16
$CF	RESERVED REGISTER ADDRESS	16

The C-BUS addresses $C7, $CA and $CF are allocated for production testing and must not be accessed in normal operation.

C-BUS Read Only Registers

ADDR (hex)	REGISTER	Word Size (bits)
$B4	AUXILIARY ADC DATA	8
$C5	RESERVED REGISTER ADDRESS	16
$C6	STATUS	16
$C9	XTCSS RX DATA	16
$CC	TONE STATUS	16

Interrupt Operation

The CMX883 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to '1'. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a '0' to a '1' and the corresponding mask bit(s) in the Interrupt Mask register is(are) set.

All interrupt flag bits in the Status register except the Programming Flag (bit 0) are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the flag register. The Programming Flag bit is cleared only when it is permissible to write a new word to the Programming register.

### 1.6.2	$01 C-BUS RESET: address only.

The reset command has no data attached to it. It sets the device registers into the states listed below.

Addr.	REG.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$B0	ANALOGUE GAIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B1	SIGNAL ROUTING	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B2	AUXILIARY ADC THRESHOLDS	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
$B3	AUXILIARY ADC CONTROL									0	0	0	0	0	0	0	0
$B4	AUXILIARY ADC DATA									X	X	X	X	X	X	X	X
$C0	POWER DOWN CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C1	MODE CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C2	AUDIO & DEVICE ADDRESS CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C3	TX TONE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C6	STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C7	Reserved Register Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C8	PROGRAMMING REGISTER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C9	XTCSS RX DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CB	XTCSS TX DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CC	TONE STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CD	AUDIO TONE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CE	INTERRUPT MASK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CF	Reserved Register Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
P4.7	Transmit Limiter Control	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-

Following a C-BUS reset all of the programming registers (P0 – P4) are reset to zero.

The transmit limiter value is initialised to the maximum limit.

To initialise the device following power-up, or to clear the current device state, apply the following sequence of C-Bus actions:
1.	Send a C-Bus Reset command.
2.	Send $2001 to the Mode Control register (C-Bus address $C1).
3.	Send $0000 to the Mode Control register.
The device is now ready to be configured for its next application.

1.6.3 $B0 ANALOGUE GAIN: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Inv_1	MOD_1 Attenuation			Inv_2	MOD_2 Attenuation			0	Input Gain			Audio Output Attenuation			

Bits 15 and 11 set the phase of the MOD_1 and MOD_2 outputs. When set to '0' the 'true' signal (0° phase shift) will be produced, when set to '1' the signal will be inverted (180° phase shift). This can be useful when interfacing with rf circuitry or when generating an inverted turn off tone for CTCSS. Any change will take place immediately after these bits are changed.

The output paths provide user programmable attenuation stages to independently adjust the output levels of the modulators. Finer level control of the MOD_1 and MOD_2 outputs can be achieved with the FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2 registers (P4.2-3).

Bit 14	Bit 13	Bit 12	MOD_1 Output Attenuation
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bit 10	Bit 9	Bit 8	MOD_2 Output Attenuation
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bit 7 is reserved - set to 0.

Bits 6 to 4 control the input path programmable gain stage - useful when amplifying low power voice signals from the microphone inputs. Finer gain control can be achieved with the 'FINE INPUT GAIN' control register (P4.0). In receive mode it is recommended to set the gain to 0dB.

Bit 6	Bit 5	Bit 4	Input Gain
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

Bit 3	Bit 2	Bit 1	Bit 0	Audio Output Attenuation
0	0	0	0	>60dB
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Bits 3 to 0 control the output path programmable attenuation stage to adjust the volume of the audio output signal. Finer volume control can be achieved with the 'FINE OUTPUT GAIN 1' control register (P4.2).

1.6.4 $B1 SIGNAL ROUTING: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Tx MOD_1 and MOD_2 Routing		0	0	0	0	0	0	Analogue i/p select		AUDIO o/p select		Ramp Up	Ramp Down

Bits 15 and 14 reserved - set to 0.

Bits 13 and 12 select the routing of the transmit signals allowing 1 or 2 point modulation and interfaces.

Bit 13	Bit 12	Tx MOD_1 and MOD_2 routing
0	0	Tx, MOD_1 and MOD_2 outputs set to bias.
0	1	Tx, In-band signals to MOD_1, Subaudio signals to MOD_2
1	0	Tx, In-band and Subaudio to MOD_1, MOD_2 set to vbias
1	1	Tx, In-band and Subaudio to both MOD_1 and MOD_2

'In-Band' in this context refers to any of the signals; Voice, In-band tone etc.

Bits 11 to 6 are reserved - set to 0.

Bit 5	Bit 4	Analogue Input select
0	0	No input selected (Input = V_{BIAS})
0	1	Input amplifier 2 (Input_2 i/p)
1	0	Microphone (MIC i/p)
1	1	Discriminator (DISC i/p)

Bit 3	Bit 2	AUDIO Output select
0	0	No output selected (Output = V_{BIAS})
0	1	Received Voice signal
1	0	MOD_1 signal (for Tx monitoring)
1	1	Reserved, do not use

When bits 1 or 0 are set to '1' output signals are ramped up (bit 1) or ramped down (bit 0) to reduce transients in the transmitted signal. Time to ramp up / down is set in the 'Ramp Rate Control' section of the Programming register (P4.6).

1.6.5 $B2 AUXILIARY ADC THRESHOLDS: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	High Threshold [Range: 0 to 255]								Low Threshold [Range: 0 to 255]							

If the selected signal level exceeds the High Threshold, the 'Signal High' bit of the Status register will be set to 1. If the Signal level falls below the Low Threshold, the 'Signal Low' bit of the Status register will be set to 1. If the corresponding interrupt bit is enabled, a C-BUS interrupt will be generated. These status bits are cleared when the Status register is read. The behaviour of the CMX883 is not defined if the high threshold is less than the low threshold.

Threshold resolution: V_{DD}(A)/256 per LSB
Threshold accuracy: $\pm$2 LSB
Differential linearity: $\pm$1 LSB [monotonic]

The 'Auxiliary ADC Thresholds' register must not be updated whilst the Auxiliary ADC is enabled.

1.6.6 $B3 AUXILIARY ADC CONTROL: 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	Aux ADC i/p select		Conversion Interval					

The 'Conversion Interval' (bits 5 to 0) defines the time between measurements whilst the Auxiliary ADC is enabled. This allows the user to trade-off device power consumption with response time.

$$\text{Auxiliary ADC power} = 0.5\text{mW}/V_{DD}(A)/\text{conversion} \quad \text{(approximate)}$$
$$\text{Conversion Interval} = 20.8\mu s \text{ per LSB.} \quad \text{(approximate)}$$

The user should set an interval to ensure that no part of a received signal is missed, so that the signal type can be correctly identified. If using the Rx Auto start-up feature the recommended maximum Conversion Interval is 125µs. The 'Auxiliary ADC' register must not be updated whilst the Aux ADC is enabled.

The Aux ADC i/p select (bits 7 to 6) control the input to the Auxiliary ADC. Control is independent of the Analogue i/p select bits and hence the Aux ADC can monitor any one of the 4 inputs independently.

Bit 7	Bit 6	Auxiliary ADC input from:
0	0	Signal monitor (Sig_Monitor i/p)
0	1	Input amplifier 2 (Input_2 i/p)
1	0	Microphone (MIC i/p)
1	1	Discriminator (DISC i/p)

1.6.7 $C0 POWER DOWN CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	Input_2 amp	MIC amp	Disc amp	Input Gain	Output Fine Gain 1	Output Fine Gain 2	O/P Coarse Gain 1	O/P Coarse Gain 2

Bit:	7	6	5	4	3	2	1	0
	Audio Output	BIAS	Signal Processing	Prog Reg Save	Xtal_N	Clock_Out_N	Enable Aux ADC	Rx Auto start-up

Bits 15 to 5 provide the power control of the specified blocks. If a bit is '1', the corresponding block is on, else it is powered down. A C-BUS or Power up reset clears all bits in this register to '0'.

If bit 5 is '0' the internal signal processing blocks are reset and placed into a power-save mode.

Bit 4 should be set to a '1' if any of the program registers (1.6.20) have been programmed as this prevents them being reset after a Rx Auto start-up or when the Signal Processing blocks come out of power save. If bit 4 is set to '0' the program registers will be reset to the C-BUS or Power-up reset state whenever the Signal Processing blocks come out of power save.

Bits 3 and 2 control the xtal clock circuit. The xtal circuit is powered down by setting bit 3 to '1'. Note: The Clock/Xtal pin may be driven by an external clock source regardless of the setting of these bits. The Clock_Out pin is disabled (held low) by setting bit 2 to '1'. After a Power-up or C-BUS reset bits 2 and 3 are cleared to '0', so that both the xtal circuit and clock output are enabled.

Bit 1 controls the Auxiliary ADC. If set to '1' the Auxiliary ADC will generate interrupts in accordance with the settings of the interrupt mask bits. If bit 1 is '0' the Auxiliary ADC is disabled and powered down.

Bit 0 controls Rx Auto start up. If bit 0 is set to '1' and the Aux ADC input rises above the 'High Threshold' the device will automatically enter receive mode and initiate Rx signal type identification for those signals enabled in the Mode register. The correct Aux ADC input, Rx signal routing and power down bits must be set for automatic receive start up to operate, the mode control bits should be set to '00' in this case. If bit 0 is cleared to '0' the CMX883 will not automatically start-up and it is up to the host to respond to Aux ADC interrupts in this case. Bit 0 must be set to '0' whilst writing through register $C8 - Programming Register.

1.6.8 $C1 MODE CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	Enable Voice	In band signalling: In-band tone, XTCSS		Generate Audio Tone	Enable CTCSS	Enable DCS	Enable DCS Inverse	0

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Mode Select	

Bits 1 and 0 control the overall mode of the CMX883 according to the table below:

Bit 1	Bit 0	Device Mode
0	0	Idle
0	1	Receive Mode
1	0	Transmit Mode
1	1	Reserved - do not use

During transmit, only one signal type may be enabled for each of the sub-audio and voice bands, see Table 7. During receive the CMX883 will search for all signals enabled in this register and report those that are successfully decoded. See also Table 2 in section 1.5.3.

In transmit mode the CMX883 begins transmission of a selected signal immediately after it has been enabled. The host µC must ensure all associated data and control bits have been set to their required values before enabling the signal in this register.

Bits 2 to 8 are reserved - set to '0'.

Bits 11 to 9 determine the sub-audio transmission / reception signalling:

Bit 11	Bit 10	Bit 9	Tx - Transmitted signal:	Rx - Monitored signal(s):
0	0	0	No Sub-Audio Transmitted	No Sub-audio Monitoring
0	0	1	Inverted DCS*	Inverted DCS*
0	1	0	DCS	DCS
0	1	1	Do not use	DCS + inv DCS*
1	0	0	CTCSS	CTCSS
1	0	1	Do not use	CTCSS + inv DCS*
1	1	0	Do not use	CTCSS + DCS
1	1	1	Do not use	CTCSS + DCS + inv DCS*

  * See Table 4 DCS Modulation Modes.

Bit 12 enables Audio tone generation (see section 1.6.14). This operates in transmit and receive modes. In transmit mode this bit will only enable the Audio Generator when no other voice band signals are being transmitted i.e. bits 14 and 13 set to '0'.

Bits 14 and 13 determine the voice band tone transmission and reception. When transmitting or receiving audio band signals the voice path must be disabled by clearing 'Voice Enable' bit 15 to '0'.

Bit 14	Bit 13	Tx - Transmitted signal	Rx - Monitored signal
0	0	No voice band tone transmitted	No voice band tones monitored
0	1	In-band tone	In-band tone
1	0	Reserved	Reserved
1	1	XTCSS	XTCSS

When set to '1', bit 15 enables the voice path. In transmit mode the selected audio input is routed to the modulator outputs. In receive mode the voice processing path is enabled to the audio output. In transmit mode bit 15, if set to '1', will be temporarily disabled (cleared to '0') whenever any of the bits 12, 13 and 14 are set to '1'. In receive mode bit 15, if set to '1', will be temporarily disabled (cleared to '0') whenever bit 12 is set to '1'. It is up to the host µC to control bit 15 when voice band signals are received.

The Mode Control register ($C1) may be written to at any time (subject to C-BUS timing restrictions). If the enable bit of the currently decoded signal is disabled whilst in phase 2 the CMX883 will return to phase 1 for that band. If the same signal needs to be searched for again then the appropriate bit needs to be set back to '1' in $C1. However, to de-emphasise in-band tones, bit 15 must be set to '1'.

The CMX883 will only detect signals when their amplitude is above the threshold set for each band (sub-audio and voice), as set in the program registers. Therefore even if valid tones or signals are present the CMX883 will ignore them unless they exceed the detect threshold. Time and level hysteresis is applied to reduce chattering in marginal conditions.

1.6.9 $C2 AUDIO & DEVICE ADDRESS CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Scramble	Compand	Voice filter mode			Special Sub-Audio		Device Address							

Bit 14 controls the audio band scrambler. When set to '1' voice signals are scrambled, by frequency inversion, in transmit and receive modes. When set to '0' no scrambling is performed.

Bits 7 to 0 define the device address. This setting is used for the CTCSS and XTCSS address in both Tx and Rx modes. The range of valid addresses is: CTCSS tone (1-51 in decimal) and XTCSS (1-99 in decimal). In Tx this number will be used to select the addressing of the enabled signal, if the address is outside the valid range no signalling will occur. In Rx this address (along with the all call address of '40') will be searched for each signalling format enabled in the Mode register, the detected signal type will be reported in the Status register $C6 and the address will be indicated in the XTCSS Rx Data register $C9 or the Tone Status register $CC.

Bits 9 to 8 select special sub-audio tones in accordance with the following table. Selecting the 'DCS turn off tone' during DCS transmit will cause the DCS turn off tone to be transmitted; this will override the DCS data being transmitted. 'DCS turn off tone' must be selected in this register to enable detection of the DCS turn off tone during receive. To transmit the 64.7Hz XTCSS maintenance tone, XTCSS transmit must be selected in the Mode Control register and XTCSS maintenance tone must be selected in this register. Transmission of the maintenance tone overrides any other CTCSS tone being transmitted. The XTCSS maintenance tone decoder is enabled by selecting XTCSS receive mode, so it is not necessary to select the XTCSS maintenance tone in this register when receiving. If the Tone Clone[TM] mode is selected this allows the device in Rx to non-predictively detect any CTCSS frequency in the range of valid tones, the received tone number will be reported in the Tone Status register $CC.

Bit 9	Bit 8	Freq (Hz)	Special Sub-Audio tone
0	0	-	None
0	1	134.4	DCS turn off tone
1	0	64.7	XTCSS maintenance tone
1	1	Clone	CTCSS Tone clone mode (Rx only)

The voice filter control bits 12 and 11 determine the Voice Band Filter mode applied to the voice signal before it is transmitted or after it has been received. Bit 10 controls the de-emphasis (Rx) or pre-emphasis (Tx) mode of the voice band filtering.

Bit 12	Bit 11	Bit 10	Voice filter mode
X	X	0	Disable de/pre-emphasis
X	X	1	Enable de/pre-emphasis
0	0	X	No filtering applied
0	1	X	12.5kHz channel filtering
1	0	X	25.0kHz channel filtering
1	1	X	Reserved – do not use

Bit 13 controls the audio band compandor. When set to '1' audio band signals are compressed in transmit mode and expanded in receive mode. When set to '0' no companding is performed.

Bits 14 to 15 are reserved, set to '0'.

1.6.10 $C3 Tx In-Band Tones: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx In-band tone					0	0	0	0	0	0	0	0	0	0	0

Bits 15 to 11 define the tone transmitted when Tx In-band tone is enabled. The frequency is as defined in Table 6 In-band Tones.

1.6.11 $C7 Reserved - Do not write to this register

1.6.12 $C8 PROGRAMMING REGISTER: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First Word	Block Number	Block / Data		Programming Data											

See section 1.6.20 for a description of this register.

1.6.13 $CB XTCSS Codes: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)			0	0	0	0	0	0	0	0

$CB holds the codes to be used when transmitting an XTCSS type tone set. Each 4 bits define the In-band tone used, see Table 6 In-band Tones. S0 and S1 are the information section of the 4 tone set. This register must be set to the required value before XTCSS transmission is enabled. For more details see section 1.5.6. Note The address used is defined in the Audio & Device Address Control register.

1.6.14 $CD AUDIO TONE: 16-bit write only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	Audio Tone											

When the required bits of the Mode Control register ($C1) are set an audio tone will be generated with the frequency set by bits (11-0) of this register in accordance with the formula below. If bits 11-0 are programmed with '0' no tone (i.e. Vbias) will be generated when the Audio Tone is enabled.

$$\text{frequency} = \text{Audio Tone}\quad\text{(i.e. 1Hz per LSB)}$$

The Audio Tone frequency must only be set to generate frequencies from 300Hz to 3000Hz.

The host must suppress other voice band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is also controlled by the host μC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD1/2 pins).

1.6.15 $CE INTERRUPT MASK: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	IRQ MASK	0	Rx In-band detect MASK	XTCSS MASK	Rx CTCSS detect MASK	Rx DCS detect MASK	Aux ADC High MASK	Aux ADC Low MASK

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Prog Flag MASK

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14		Reserved – Set to 0
13	1	Enable interrupt when a change to a In-band tone is detected as indicated by a '0' to '1' change of bit 13 of the Status register
	0	Disabled
12	1	Enable interrupt when a valid XTCSS 4 tone set is detected or has finished being transmitted as indicated by a '0' to '1' change on bit 12 of the Status register
	0	Disabled
11	1	Enable interrupt when a change to a programmed CTCSS tone is detected as indicated by a '0' to '1' change of bit 11 of the Status register
	0	Disabled
10	1	Enable interrupt on a change in the detect status of the DCS decoder as indicated by a change of state on bit 10 of the Status register
	0	Disabled
9, 8	1	Enable interrupt when the corresponding Aux ADC status bit changes
	0	Disabled
7 - 1		Reserved - Set to 0
0	1	Enable interrupt when Prog Flag bit of the Status register changes from '0' to '1' (see Programming register $C8)
	0	Disabled

The following 4 registers are read only

1.6.16 $B4 AUX ADC MONITOR DATA: 8-bit read-only

Bit:	7	6	5	4	3	2	1	0
	Signal Monitor Data							

This data holds the result of the last measurement performed by the auxiliary ADC.

The signal processor must be on to read Auxiliary ADC data, so Power Down Control register b5 must be set to '1'. This is independent of whether Tx or Rx modes are selected.

1.6.17 $C6 STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8
	IRQ	0	In-band tone state change	XTCSS 4 tone set complete	CTCSS state change	DCS state change	Aux ADC Monitor High	Aux ADC Monitor Low

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Programming Flag

This word holds the current status of the CMX883: the value read out is only valid when bit 5 of the Power Down Control register ($C0) is set to '1'. Changes in the Status register will cause the IRQ bit (bit 15) to be set to '1' if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when the IRQ bit is '1' and the IRQ MASK bit (bit 15 of register $CE) is set to '1'.

Bits 1 to 15 of the Status register are cleared to '0' after the Status register is read. Bit 0 is only cleared by writing to the Programming Register.

Bits 14 and 7 to 1 are reserved.

Bits 13, 11 and 10 indicate that a In-band tone, CTCSS or DCS event caused the interrupt, the host should then read the Tones Status register ($CC) for further information. In transmit these bits will be set to '0'. Detection of the DCS turn off tone and removal of DCS turn off tone are both flagged as DCS events in the Status register not as CTCSS events. The assertion or removal of the 'XTCSS Maintenance Tone' (64.7Hz) is flagged as a CTCSS event.

In receive bit 12 indicates that a valid XTCSS 4 tone set with the correct addressing (see $C2) has been detected, the 4 received tones are indicated in $CB. In Tx mode bit 12 will be set to '1' at the end of the 4th XTCSS tone transmitted.

Aux ADC High (bit 9) and Aux ADC Low (bit 8) reflect the recent history of the Aux ADC level, with respect to the high and low thresholds. The most recent Aux ADC reading can be read from $B4.

Aux ADC Monitor High	Aux ADC Monitor Low	Aux ADC history since last reading:
0	0	Neither threshold crossed
0	1	Signal gone below low threshold
1	0	Signal gone above high threshold
1	1	Signal gone below low threshold and above high threshold

Programming Flag, bit 0: The Programming Register ($C8) should only be written to when bit 0 is set to '1' (with both Mode select bits set low – See register $C8). Writing to the Programming Register ($C8) clears bit 0 to '0'. Bit 0 is restored to '1' when the programming action is complete, normally within 250µs, when it is then safe to write to the Programming Register.

1.6.18 $C9 XTCSS RX DATA: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	XTCSS Tone 3 (S1)				XTCSS Tone 2 (S0)				XTCSS received address							

$C9 holds the information decoded after receiving an XTCSS type tone set. Bits 7 to 0 represent the received address in hex based on the XTCSS tones A1 and A0. This register will only be updated if the received address matches the one programmed in the Audio and Device Address Control register or is the all call address of '40'. Bits 15 to 12 and 11 to 8 defines the received S1 and S0 tones, see Table 6 In-band Tones and section 1.5.6.

1.6.19 $CC TONES STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Detected In-band tone frequency					Sub-Audio Status			0	0	Detected CTCSS code					

This word holds the current status of the CMX883 sub-audio and In-band tone sections. This word should be read by the host after an interrupt caused by a DCS, CTCSS or In-band tone event.

The value in bits 5 to 0, Detected CTCSS code, identifies the detected sub-audio tone by its position in Table 3 CTCSS Tones. If bits 5 to 0 = '000000' there is no CTCSS tone currently being detected. If bits 5 to 0 = '110111' (= 55 in decimal) this indicates that an Invalid Tone has been detected. An Invalid Tone is any tone in the subaudio band which is not the selected subaudio tone nor the all-call tone, or is a tone not listed in Table 3. A change in the state of bits 5-0 to Invalid Tone from the no tone condition will not cause Status register ($C6), b11 to be set to '1'. Any other change in the state of bits 5-0 will cause the Status register ($C6), b11 to be set to '1'.

A detected In-band frequency is indicated by the value in bits 15 to 11, 'Detected In-band tone frequency', identifies the frequency by its position in Table 6 In-band Tones. If bits 15 to 11 = '00000' there is no In-band tone currently being detected. A change in the state of bits 15 to 11 will cause bit 13 of the Status register ($C6), 'In-band tone State Change', to be set to '1'.

Bits 10 to 8 indicate the DCS and special sub-audio tone status. The Status register ($C6) will indicate the type of signal detected. If DCS or special CTCSS tones are detected they will be indicated in bits 10 to 8 according to the table below and bits 7 to 0 will be set to '00000000'. If a normal CTCSS tone is detected bits 10 to 8 will be set to '000' and bits 7 to 0 will indicate the decoded tone. A change in the state of bits 10 to 8 will cause the relevant bit (10 or 11) of the Status register to be set to '1'.

Bit 10	Bit 9	Bit 8	Sub-Audio status	
0	0	0	No DCS or special CTCSS detected	
0	0	1	Reserved	
0	1	0	DCS sequence detected	Only enabled with DCS
0	1	1	inverted DCS sequence detected	Only enabled with DCS
1	0	0	Reserved	
1	0	1	134.4Hz DCS turn off tone detected	Only enabled with DCS
1	1	0	64.7Hz XTCSS sub-audio tone detected	Only enabled with XTCSS
1	1	1	Reserved	

When the relevant detection mode is not enabled, the associated bits will be set to '0'. In Tx mode this register will be set to '0'.

During the DCS receive, the device can flag an interrupt when the DCS code fails to be recognised. This may be due to code dropout. The turn off tone may be flagged shortly after, if the transmission is ending. Alternatively the DCS link may be restored and DCS detection will be flagged again.

1.6.20 $C8 PROGRAMMING REGISTER: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First Word	Block Num.	Block Num. or Data		Programming Data											

This register is used for programming various gains, levels, offset compensations, tones and codes. If the user programs any of these values then bit 4 of $C0 (Power Down Control) must be set to '1'. Following a C-BUS Reset or a Power Up Reset, the programmed values are initialised in accordance with the settings described in section 1.6.2 (C-BUS Reset).

The Signal Processing function and the XTAL clock circuit must both be enabled in order to write to the Programming Register, so Power Down Control register bit 5 must be set to '1' and bit 3 must be set to '0'.

The Programming Register should only be written to when the Programming Flag bit (bit 0) of the Status register is set to '1' and the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both '0'). The Programming Flag is cleared when the Programming Register is written to. When the corresponding programming action has been completed (normally within 250µs) the CMX883 will set the flag back to '1' to indicate that it is now safe to write the next programming value. The Programming Register must not be written to while the Programming Flag bit is '0'. Programming is done by writing a sequence of 16-bit words to the Programming Register, in the order shown in the following tables. Writing data to the Programming Register must be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g. If only 'Fine output gain 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block. The word P4.8 is allocated for production testing and must not be accessed in normal operation.

The high order bits of each word define which block the word belongs to, and if it is the first word of that block:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 – Bit 0
1	X	X	X	1st data for each block
0	X	X	X	2nd and following data
X	1	0	0	Reserved - do not use
X	1	0	1	Write to block 1 (12 bit words)
X	1	1	0	Write to block 2 (12 bit words)
X	1	1	1	Reserved - do not use
X	0			Write to block 4 (14 bit words)

Block 0 – Reserved. Do not use.

Block 1 – XTCSS and In-band tone Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio band Tx level											Emph
P1.1	0	1	0	1	XTCSS tone length		Audio band detect threshold						In-band tone detect bandwidth			
P1.2	0	1	0	1	0	Programmable In-band Tone 0										
P1.3	0	1	0	1	0	Programmable In-band Tone 1										
P1.4	0	1	0	1	0	Programmable In-band Tone 2										
P1.5	0	1	0	1	0	Programmable In-band Tone 3										

Block 2 – CTCSS and DCS Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Tx level											
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			
P2.2	0	1	1	0	DCS Code bits 11 – 0											
P2.3	0	1	1	0	DCS Code bits 23/22 – 12											
P2.4	0	1	1	0	Sub-audio drop out time				0							

Block 3 – Reserved. Do not use.

Block 4 – Gain and Offset Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain													
P4.1	0	0	Reserved - set to '0'													
P4.2	0	0	Fine Output Gain 1													
P4.3	0	0	Fine Output Gain 2													
P4.4	0	0	Output 1 Offset Control													
P4.5	0	0	Output 2 Offset Control													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting (all 1's = Vbias +/- 0.5 Vdd)													
P4.8	0	0	Special Programming Register (Production Test Only)													

1.6.20.1   PROGRAMMING REGISTER Block 0 – Reserved

1.6.20.2   PROGRAMMING REGISTER Block 1 – XTCSS and In-band tone Setup:

$C8 (P1.0)   Voice band tones Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Voice band tones Tx level											Emph

Bits 11 (MSB) to 1 (LSB) set the transmitted In-band tone and Audio Tone signal level (pk-pk) with a resolution of $V_{DD}(A)/2048$ per LSB (1.465mV per LSB at $V_{DD}(A)=3V$). Valid range for this value is 0 to 1536.

Bit 0 controls Rx In-band tone de-emphasis. When set to '0' the signal going to the In-band tone detector is not de-emphasised. When voice processing is enabled in the Mode register, de/pre-emphasis is enabled in the Audio & Device Address register and this bit (b0) is set to '1', signals going to the In-band tone detector are de-emphasised in accordance with Figure 6.

$C8 (P1.1)   In-band tone Detect Bandwidth and Audio Band Detect Threshold

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.1	0	1	0	1	XTCSS tone length		Audio band detect threshold						In-band tone detect bandwidth		

XTCSS tone length (bits 11 to 10) set the transmit tone length for each of the 4 tones in a XTCSS sequence. In receive these bits define the minimum silent prefix and suffix qualification periods for successful reception, also the maximum receive tone length is double the time set (e.g. for 60ms setting each received tone must be less than 120ms in length for successful XTCSS decoding). '00' = 40ms, '01' = 60ms, '10' = 80ms and '11' = 100ms.

The 'detect threshold' bits (bits 9 to 4) set the minimum In-band tone signal level that will be detected. The levels are set according to the formula:

Minimum Level = Detect Threshold $\times$ 3.63mV rms at $V_{DD}(A) = 3V$ (2.93mV per LSB at $V_{DD}(A)=3V$)

The In-band detected bandwidth is set in accordance with the following table:

	Bit 3	Bit 2	Bit 1	Bit 0	BANDWIDTH	
					Will Decode	Will Not Decode
	1	0	0	0	±1.1%	±2.4%
Recommended for EEA ⇒	**1**	**0**	**0**	**1**	**±1.3%**	**±2.7%**
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P1.2-5)   Programmable In-band Tones

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.2-5	0	1	0	1	0	Programmable In-band Tone										
						N (see below)						R (see below)				

These words set the programmable In-band tones used in transmit and receive. The frequency is set in bits 11-0 for each word according to the formula:

N = Integer part of (0.042666 x frequency)
R = (0.042666 x frequency - N) x 6000 / frequency (round to nearest integer)

Example: For 1010Hz, N = 43, R = 1. The programmed tones must only be set to frequencies from 400Hz to 3000Hz.

1.6.20.3 PROGRAMMING REGISTER Block 2 – CTCSS and DCS Setup:

$C8 (P2.0)   CTCSS and DCS TX LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Level											

Bits 11 (MSB) to 0 (LSB) set the transmitted CTCSS or DCS sub-audio signal level (pk-pk) with a resolution of $V_{DD}(A)/16384$ per LSB (0.183mV per LSB at $V_{DD}(A)=3V$, giving a range 0 to 749.8mV pk-pk).

$C8 (P2.1)   CTCSS TONE BW AND LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS detect threshold						CTCSS detect bandwidth			

Bit 11, DCS 24, sets the length of DCS code transmitted or searched for. When this bit is set to '1' 24 bit codes are transmitted and decoded. When this bit is set to '0' 23 bit codes are used.

The 'detect threshold' bits (bits 9 to 4) set the minimum CTCSS or DCS signal level that will be detected. The levels are set according to the formula:

Minimum Level = Detect Threshold $\times$ 2mV rms at $V_{DD}(A)$ = 3V   [0.37mV per LSB at $V_{DD}(A)=3V$]

The CTCSS detected tone bandwidth is set in accordance with the following table:

				BANDWIDTH	
	Bit 3	Bit 2	Bit 1	Bit 0	Will Decode	Will Not Decode
Recommended for use with split tones	0	1	1	0	±0.5%	±1.8%
	0	1	1	1	±0.8%	±2.1%
Recommended for CTCSS ⇒	**1**	**0**	**0**	**0**	**±1.1%**	**±2.4%**
	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P2.2-3)   DCS CODE (LOWER) and DCS CODE (UPPER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.2	0	1	1	0	DCS Data (bits 11-0)											
P2.3	0	1	1	0	DCS Data (bits 23/22-12)											

These words set the DCS code to be transmitted or searched for. The least significant bit (bit 0) of the DCS code is transmitted or compared first and the most significant bit is transmitted or compared last. Note that DCS Data bit 23 is only used when bit 11 (DCS 24) of P2.1 is set to '1'.

$C8 (P2.4)   SUBAUDIO DROP OUT TIME

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.4	0	1	1	0	Subaudio Drop Out Time				0							

The Subaudio Drop Out Time defines the time that the sub-audio signal detection can drop out before loss of sub-audio is asserted. The period is set according to the formula:

Time = Subaudio Drop Out Time $\times$ 8.0ms   [range 0 to 120ms]

The setting of this register defines the maximum drop out time that the device can tolerate. The setting of this register also determines the de-response time, which is typically 40ms longer than the programmed drop out time.

1.6.20.4 PROGRAMMING REGISTER Block 3 – Reserved

1.6.20.5 PROGRAMMING REGISTER Block 4 – Gain and Offset Setup

$C8 (P4.0)   FINE INPUT GAIN

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain (unsigned integer)													

Gain = $20 \times \log([32768{-}IG]/32768)$ IG is the unsigned integer value in the 'Fine Input Gain' field

Fine input gain adjustment should be kept within the range 0 to -3.5dB.

$C8 (P4.1)   Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.1	0	0	Reserved - set to '0'													

This register is reserved and should be set to '0'.

$C8 (P4.2-3)   FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 (unsigned integer)													

Gain = $20 \times \log([32768{-}OG]/32768)$ OG is the unsigned integer value in the 'Fine Output Gain' field

Fine output gain adjustment should be kept within the range 0dB to -3.5dB.

$C8 (P4.4-5)   OUTPUT 1 OFFSET and OUTPUT 2 OFFSET

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's complement offset for MOD_1, resolution = $V_{DD}(A)/16384$ per LSB													
P4.5	0	0	2's complement offset for MOD_2, resolution = $V_{DD}(A)/16384$ per LSB													

Can be used to compensate for inherent offsets in the output path via MOD_1 (Output 1 Offset) and MOD_2 (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV.

$C8 (P4.6)   RAMP RATE CONTROL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down control (RRD)						

The ramp-up rate and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

$$\text{Time to ramp-up to full gain} = (1 + RRU) \times 1.333\text{ms}$$
$$\text{Time to ramp down to zero gain} = (1 + RRD) \times 1.333\text{ms}$$

$C8 (P4.7)   TRANSMIT LIMITER CONTROL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting, resolution = V_{DD}(A)/16384 LSB													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD_1 and MOD_2 pins. The maximum setting ($2000) is +/- V_{DD}(A)/2 i.e. output limited from 0 to V_{DD}(A).

Any settings above $2000 will limit to the $2000 setting. The limiter is set to maximum following a C-BUS Reset or a Power Up Reset. The limiter is only applied to voice signals, not internally generated audio band signals. The levels of internally generated signals must be limited by setting appropriate transmit levels.

$C8 (P4.8)   Special Programming Register – do not access.
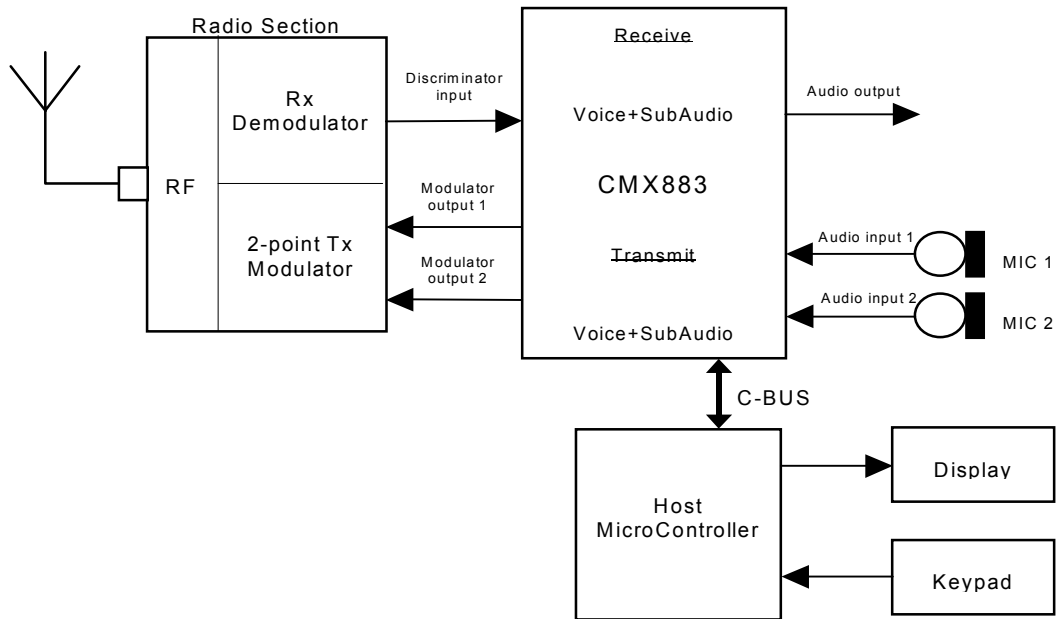
1.7 Application Notes

Figure 12 Possible FRS Configuration

1.8 Performance Specification

1.8.1   Electrical Performance

The performance data are target figures, that may change subject to the outcome of device evaluation.

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: $V_{DD}(D)$- $V_{SS}(D)$	−0.3	7.0	V
$V_{DD}(A)$- $V_{SS}(A)$	−0.3	7.0	V
Voltage on any pin to $V_{SS}(D)$	−0.3	$V_{DD}(D) + 0.3$	V
Voltage on any pin to $V_{SS}(A)$	−0.3	$V_{DD}(A) + 0.3$	V
Current into or out of $V_{DD}(A)$, $V_{SS}(A)$, $V_{DD}(D)$ and $V_{SS}(D)$	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
$V_{DD}(D)$ and $V_{DD}(A)$	0	0.3	V
$V_{SS}(D)$ and $V_{SS}(A)$	0	50	mV

D6 Package (SSOP)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

E1 Package (TSSOP)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C		400	mW
... Derating		5.3	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})		2.7	3.6	V
Operating Temperature		−40	+85	°C
Clock/Xtal Frequency	11	18.3	18.6	MHz

Notes: 11   Nominal clock frequency is 18.432MHz.

Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 18.432MHz $\pm$0.01% (100ppm).
V_{DD} = 2.7V to 3.6V; Tamb = $-40°C$ to +85°C.
Reference Signal Level = 308mV rms at 1kHz with V_{DD} = 3V.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB.
Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
$I_{DD}(D)$ (V_{DD} = 3.0V)	21		4.5	8.0	mA
$I_{DD}(A)$ (V_{DD} = 3.0V)	21		1.0	2.0	mA
$I_{DD}(D)$ (All Power-saved) (V_{DD} = 3.0V)	21		2.0	10	µA
$I_{DD}(A)$ (All Power-saved) (V_{DD} = 3.0V)	21		2.0	10	µA
C-BUS Interface					
Input Logic '1'		70%			V_{DD}
Input Logic '0'				30%	V_{DD}
Input Leakage Current (Logic '1' or '0')		-1.0		1.0	µA
Input Capacitance		-		7.5	pF
Output Logic '1' (I_{OH} = 120µA)		90%			V_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current				10	µA
IRQN (Vout = V_{DD}(D))		-1.0		1.0	µA
REPLY_DATA (output HiZ)		-1.0		1.0	µA
CLOCK_OUT					
Output Logic '1' (I_{OH} = 120µA)		90%			V_{DD}
(I_{OH} = 1mA)		80%			V_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	V_{DD}
(I_{OL} = -1.5mA)				15%	V_{DD}
CLOCK/XTAL	22				
Input Logic '1'		70%			V_{DD}
Input Logic '0'				30%	V_{DD}
Input current (Vin = V_{DD})				40	µA
Input current (Vin = V_{SS})		-40			µA
V_{BIAS}	23				
Output voltage offset wrt V_{DD}/2 (I_{OL} < 1µA)		-2%		+2%	V_{DD}
Output impedance			22		kΩ

Notes:

21   Not including any current drawn from the device pins by external circuitry.

22   Characteristics when driving the CLOCK/XTAL pin with an external clock source.

23   Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
CLOCK/XTAL Input						
'High' pulse width		31	21			ns
'Low' pulse width		31	21			ns
Input impedance (at 18.432MHz)						
Powered-up	Resistance			150		kΩ
	Capacitance			20		pF
Powered-down	Resistance			300		kΩ
	Capacitance			20		pF
Clock frequency				18.432		MHz
Clock stability/accuracy					±100	ppm
Clock start up (from power-save)				400		ms
CLOCK_OUT Output						
CLOCK/XTAL input to CLOCK_OUT timing:						
(in high to out high)		32		15		ns
(in low to out low)		32		15		ns
'High' pulse width		33	22	27.13	33	ns
'Low' pulse width		33	22	27.13	33	ns
V$_{BIAS}$						
Start up time (from power-save)				30		ms
Microphone, Input_2 and Disc Inputs (MIC, INPUT_2, DISC)						
Input impedance		34		1		MΩ
Input signal range		35	10		90	%V$_{DD}$
Load resistance (pin 12, 14 and 16)			80			kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)				60		dB
Unity gain bandwidth				1.0		MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)			−0.5	0	0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)			−1.0		1.0	dB

Notes:
	31	Timing for an external input to the CLOCK/XTAL pin.
	32	CLOCK/XTAL input driven by external source.
	33	18.432MHz XTAL fitted.
	34	With no external components connected
	35	After multiplying by gain of input circuit, with external components connected.
	36	Gain applied to signal on output of buffer amplifier, pin 12, 14 or 16

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1 and 2 and Audio Output (MOD_1, MOD_2, AUDIO)					
Power-up to output stable	37		50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)		−0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6		0.6	dB
Output Impedance Enabled	38		600		Ω
Output Impedance Disabled	38		500		kΩ
Audio Attenuator					
Attenuation (at 0dB)		−0.5	0	0.5	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0		1.0	dB
Output Impedance Enabled	38		600		Ω
Output Impedance Disabled	38		500		kΩ
Feedback load resistance		80			kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)			60		dB
Unity gain bandwidth			1.0		MHz

Notes: 37 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in power-save mode.

38 Small signal impedance, at V_{DD} = 3.0V and Tamb = 25°C.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary ADC (Signal Monitor)					
8 Bit ADC Mode					
Resolution			8		Bits
Input Range		10%		90%	$V_{DD}(A)$
Conversion time	41		20.8		μs
Input impedance					
Resistance			10		$M\Omega$
Capacitance			5		pF
Zero error					
(input offset to give ADC output = 0)		−20		+20	mV
Integral Non-linearity	42			2	LSB
	43			4	LSB
Differential Non-linearity	42			1	LSB
	43			3	LSB
Source output impedance	44			24	$k\Omega$
Level Threshold Detect Mode					
Threshold Resolution			8		Bits
Upper threshold range (VTH)	45	VTL		$V_{DD}(A)$	V
Lower threshold range (VTL)	45	$V_{SS}(A)$		VTH	V
Signal Monitor change to IRQ	46			120	μs
Signal Monitor change to Receiver-Turn-On	47			60	μs
Audio Compandor					
Attack time			4.0		ms
Decay time			13		ms
0dB point	48		100		mVrms
Compression / Expansion ratio			2:1		

Notes:

41	With clock frequency of 18.432MHz.
42	$V_{DD}(A) >= 3.0V$
43	$V_{DD}(A) < 3.0V$
44	Denotes output impedance of the driver of the Signal Monitor input, to ensure < 1 bit additional error under nominal conditions.
45	Upper threshold > Lower threshold
46	Time from Signal Monitor input rising above Upper Threshold or falling below Lower Threshold, to IRQN being asserted.
47	Time from Signal Monitor input rising above Upper Threshold to receiver path powering up, settling and starting automatic signal type identification.
48	$V_{DD}(A) = 3.0V$

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification					
Probability of correctly identifying signal type					
(SNR = 12dB)			>>99.9		%
CTCSS Detector					
Sensitivity (Pure Tone)	51		-26		dB
Response Time (Composite Signal)	52		140	250	ms
De-response Time (Composite Signal)	52, 54		210		ms
Dropout immunity (Composite Signal)	52, 54		160		ms
Frequency Range		60		260	Hz
IN-BAND TONE Detector					
Sensitivity (Pure Tone)	53		-26		dB
Response Time (Good Signal)			35		ms
De-response Time (Good Signal)				45	ms
Dropout immunity (Good Signal)				20	ms
Frequency Range (In-band tone)		400		3000	Hz
DCS Decoder					
Sensitivity	51	58			mVp-p
Bit-Rate Sync Time			2		edges
Response Time (Good Signal)			TBD		ms

Notes:
51   Sub-Audio Detection Level threshold set to 16mV.
52   Composite signal = 308mV rms at 1kHz + 75mV rms Noise + 31mV rms Sub-Audio signal. Noise bandwidth = 5kHz Band Limited Gaussian.
53   In-band Tone Detection Level threshold set to 16mV.
54   With sub-audio dropout time (P2.4) set to $\geq$ 120ms. The typical dropout immunity is approximately 40ms more than the programmed dropout immunity. The typical de-response time is approximately 90ms longer than the programmed dropout immunity. See section 1.6.20.3, P2.4.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
CTCSS Encoder					
Frequency Range		60.0		260	Hz
Tone Frequency Accuracy				±0.3	%
Tone Amplitude Tolerance	61	-1.0		+1.0	dB
Total Harmonic Distortion	62		2.0	4.0	%
In-band tone Encoder					
Frequency Range		400		3000	Hz
Tone Frequency Accuracy				±0.3	%
Tone Amplitude Tolerance	63	-1.0		+1.0	dB
Total Harmonic Distortion	62		2.0	4.0	%
DCS Encoder					
Bit Rate			134.4		bits/s
Amplitude Tolerance	61	-1.0		+1.0	dB
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received voice	64	300		3000	Hz
12.5kHz channel transmitted voice	65	300		2550	Hz
25kHz channel transmitted voice	66	300		3000	Hz
Pass-band Gain (at 1.0kHz)			0		dB
Pass-band Ripple (wrt gain at 1.0kHz)		-2		+0.5	dB
Stop-band Attenuation		33.0			dB
Residual Hum and Noise	69		-50		dBp
Pre-emphasis	67		6		dB/oct
De-emphasis	68		−6		dB/oct
Audio Scrambler					
Inversion frequency			3300		Hz
Pass band		300		3000	Hz

Notes:

61	$V_{DD}(A)$ = 3.0V and Tx Sub-Audio Level set to 88mV p-p (31mV rms).
62	Measured at MOD_1 or MOD_2 output.
63	$V_{DD}(A)$ = 3.0V and Tx Audio Level set to 871mV p-p (308mV rms).
64	The receiver voice filter complies with the characteristic shown in Figure 5. The high pass filtering removes sub-audio components from the audio signal.
65	The 12.5kHz channel filter complies with the characteristic shown in Figure 9.
66	The 25kHz channel filter complies with the characteristic shown in Figure 8.
67	The pre-emphasis filter complies with the characteristic shown in Figure 10.
68	The de-emphasis filter complies with the characteristic shown in Figure 6.
69	dBp represents a psophometrically weighted measurement.

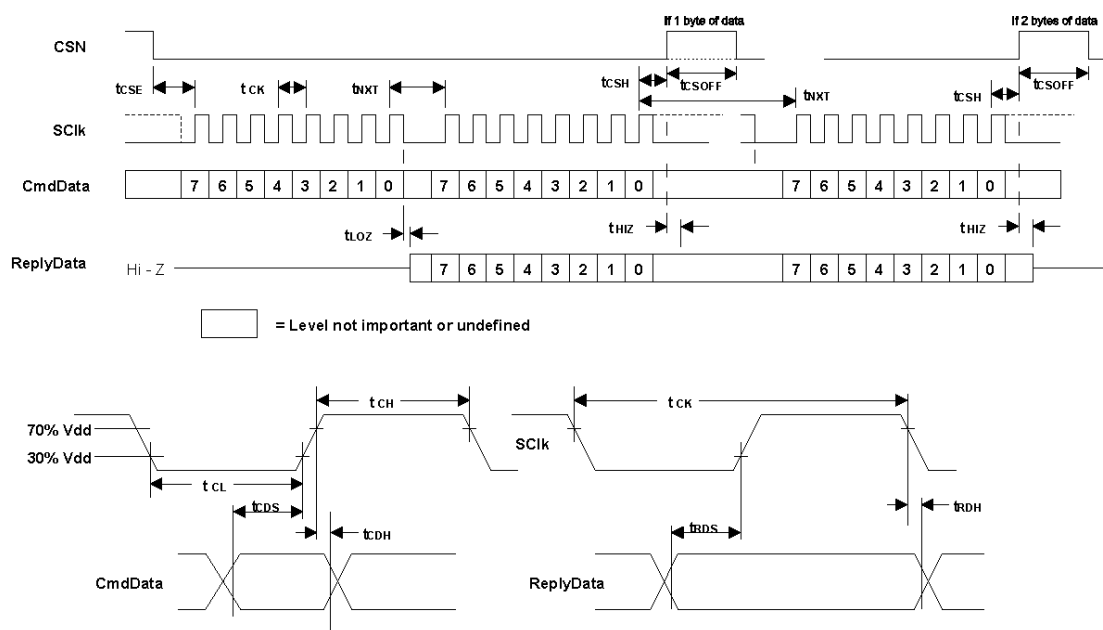## C-BUS Timing

Figure 13 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SClk high time		100			ns
t_{CSH}	Last SClk high to CSN high time		100			ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0			ns
t_{HIZ}	CSN high to ReplyData high impedance				1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0			µs
t_{NXT}	Inter-byte time		200			ns
t_{CK}	SClk cycle time		200			ns
t_{CH}	SClk high time		100			ns
t_{CL}	SClk low time		100			ns
t_{CDS}	Command Data setup time		75			ns
t_{CDH}	Command Data hold time		25			ns
t_{RDS}	Reply Data setup time		50			ns
t_{RDH}	Reply Data hold time		0			ns

Notes: 1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX883 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.
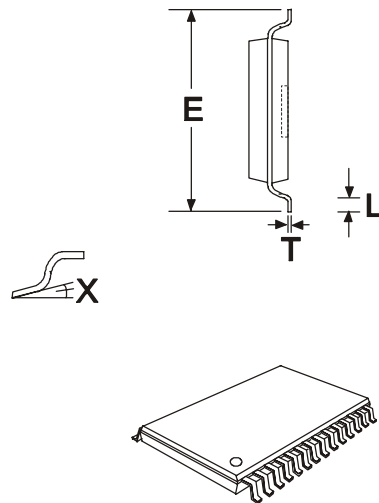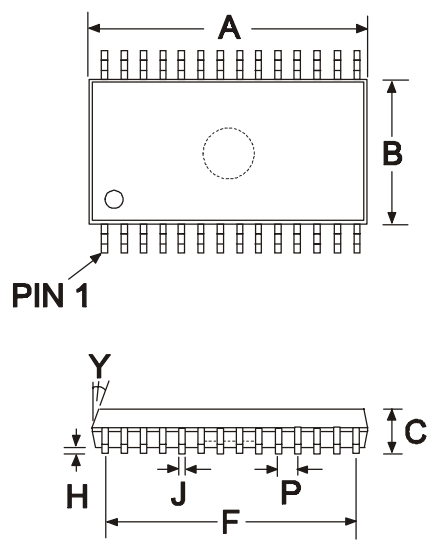
1.8.2 Packaging
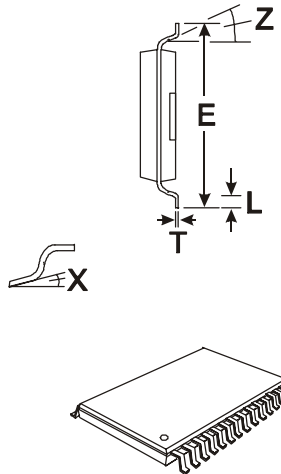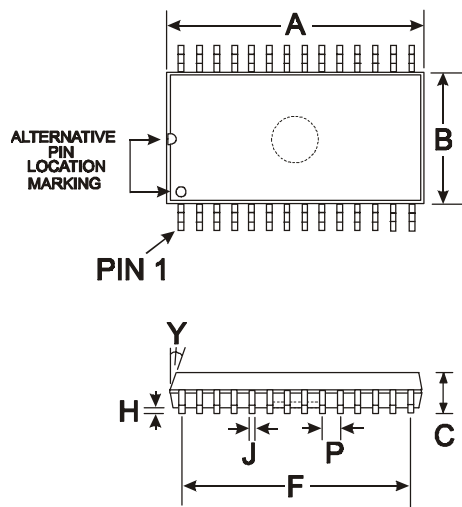
DIM.	MIN.	TYP.	MAX.
* A	9.90		10.50
* B	5.00		5.60
C	1.67		2.00
E	7.40		8.20
F		8.45	
H	0.05		0.21
J	0.22		0.38
L	0.55		0.95
P		0.65	
T	0.09		0.25
X	0°		8°
Y	7°		9°
Z	4°		12°

NOTE :

* A & B are reference data and do
not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 14 Mechanical Outline of 28-pin SSOP (D6): *Order as part no. CMX883D6*

DIM.	MIN.	TYP.	MAX.
* A	9.60		9.80
* B	4.30		4.50
C	-------		1.20
E	6.30		6.50
F		8.45	
H	0.05		0.15
J	0.17		0.30
L	0.45		0.75
P		0.65	
T	0.08		0.20
X	0°		8°
Y		12°	

NOTE :

* A & B are reference data and do not
include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 15 Mechanical Outline of 28-pin TSSOP (E1): *Order as part no. CMX883E1*

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For a full data sheet listing see: www.cmlmicro.com/products/datasheets/download.htm

For detailed application notes: www.cmlmicro.com/products/applications/

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