

STW30NM60D

N-CHANNEL 600V - 0.125Ω - 30A TO-247 Fast Diode MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW30NM60D	600 V	< 0.145 Ω	30 A

- TYPICAL $R_{DS}(on) = 0.125 \Omega$
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE RATED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- FAST INTERNAL RECOVERY DIODE

DESCRIPTION

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

APPLICATIONS

 ZVS PHASE-SHIFT FULL BRIDGE CONVERTERS FOR SMPS AND WELDING EQUIPMENT

Figure 1: Package

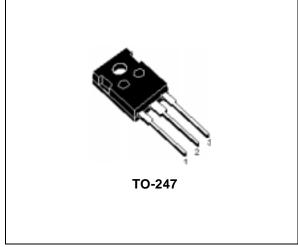


Figure 2: Internal Schematic Diagram

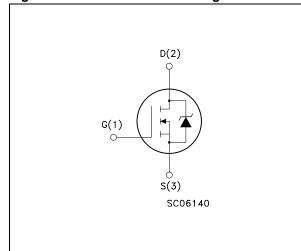


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW30NM60D W30NM60D		TO-247	TUBE

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Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	600	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	30	А
ID	Drain Current (continuous) at T _C = 100°C	18.9	А
I _{DM} (•)	Drain Current (pulsed)	120	А
P _{TOT}	Total Dissipation at T _C = 25°C	312	W
	Derating Factor	2.5	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150	°C °C

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.4	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	15	Α
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	740	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED) Table 6: On /Off

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125°C			10 100	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			± 10	μA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R _{DS(on}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 15 A		0.125	0.145	Ω

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^(•) Pulse width limited by safe operating area (1) $I_{SD} \le 30A$, di/dt $\le 400A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$.

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V , I _D = 15 A		16		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		2520 800 75		pF pF pF
Coss eq (3).	Equivalent Output Capacitance	V _{GS} = 0 V, V _{DS} = 0 to 480 V		390		pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 300 \text{ V, } I_{D} = 15 \text{ A,}$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 15)		32 33 75 35		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480 \text{ V}, I_{D} = 30 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 18)		82 24 42	115	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				30 120	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 30 A, V _{GS} = 0			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 30 A, di/dt = 100 A/ μ s V_{DD} = 50V (see Figure 16)		165 1.1 14		ns nC A
t _{rr} Q _{rr} IRRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 30 \text{ A, di/dt} = 100 \text{ A/µs}$ $V_{DD} = 50\text{V, T}_{j} = 150^{\circ}\text{C}$ (see Figure 16)		312 3.3 21		ns nC A

⁽¹⁾ Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

 ⁽²⁾ Pulse width limited by safe operating area.
 (3) C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Figure 3: Safe Operating Area

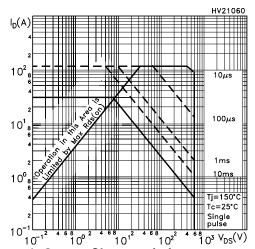


Figure 4: Output Characteristics

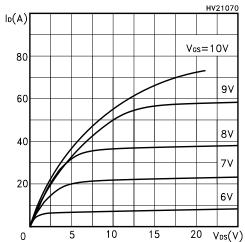


Figure 5: Transconductance

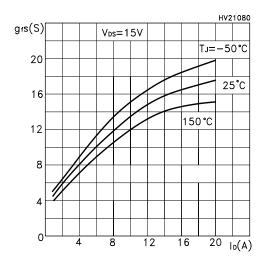


Figure 6: Thermal Impedance

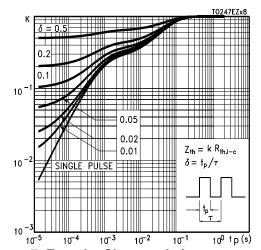


Figure 7: Transfer Characteristics

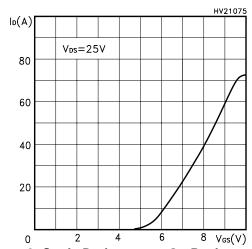
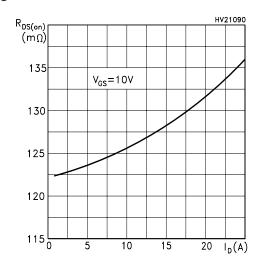


Figure 8: Static Drain-source On Resistance



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Figure 9: Gate Charge vs Gate-source Voltage

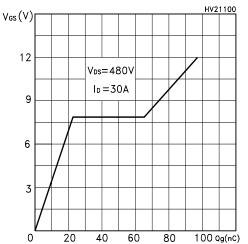


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

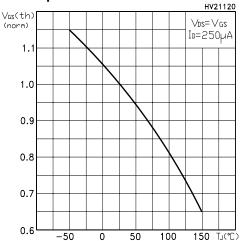


Figure 11: Dource-Drain Diode Forward Characteristics

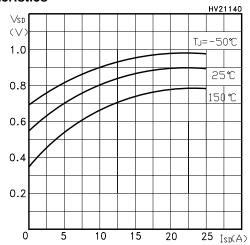


Figure 12: Capacitance Variations

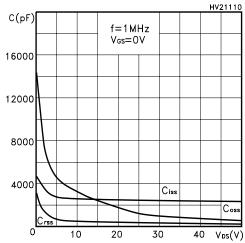


Figure 13: Normalized On Resistance vs Temperature

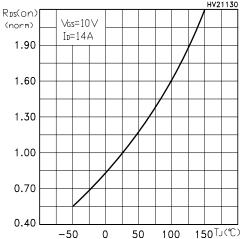


Figure 14: Unclamped Inductive Load Test Circuit

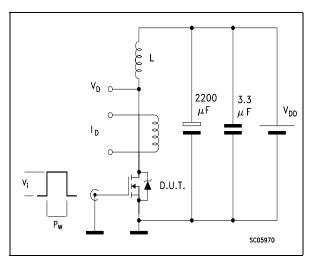


Figure 15: Switching Times Test Circuit For Resistive Load

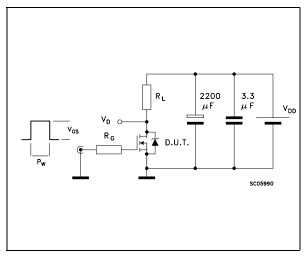


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

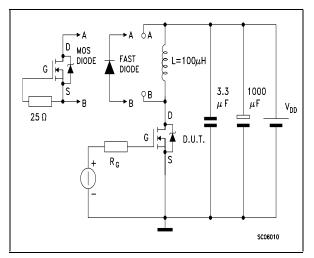


Figure 17: Unclamped Inductive Wafeform

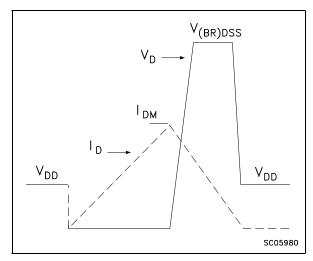
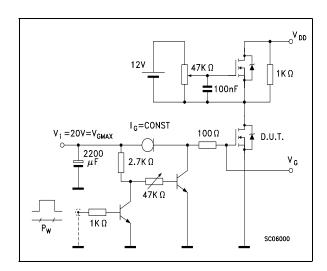


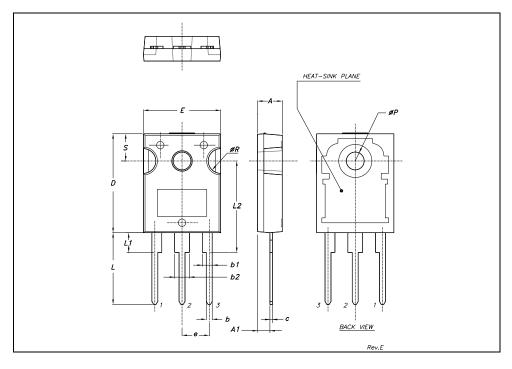
Figure 18: Gate Charge Test Circuit



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TO-247	MECHANICA	I DATA

DIM.		mm.		i		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
С	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
е		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øΡ	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



STW30NM60D

Table 9: Revision History

Date	Revision	Description of Changes
24-June-2004	3	The document change from "ADVANCED" to "COMPLETE".
		New Stylesheet.
		Rds(on) Max@10V changed. See Table 6.

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