MU9C4320L ATMCAM

APPLICATION BENEFITS

- High performance VPI/VCI translation for ATM switches and routers, up to OC-48
- Fully deterministic translation, independent from the size of the list and the length of VPI/VCI
- Pipelined architecture for increased throughput
- No limitation of the range of legal values for VPI/VCI, guaranteeing full interoperability
- Cell tagging can be performed without any time penalty
- Easy buffer management in “Find and Replace” mode because of the ability to check CLP field during VPI/VCI translation
- No limitation in the amount of associated information stored with each connection
- No time penalty when checking both VPI/VCI and VPI only connections

DISTINCTIVE CHARACTERISTICS

- 4096 x 32-bit Content Addressable Memory (CAM)
- 70 ns compare and output time per VPI/VCI
- 32-bit Data I/O port
- 16-bit Match Address Output port directly addresses external RAM containing associated data of any width
- Address/Control bus directly controls CAM operations for faster throughput
- Instruction and Status registers for optional software control
- Simultaneously compares Virtual Paths and Virtual Channels
- Cascadable for increased depth
- Extensive set of control states for flexibility
- JTAG interface
- 100-pin TQFP package; 3.3 volt operation

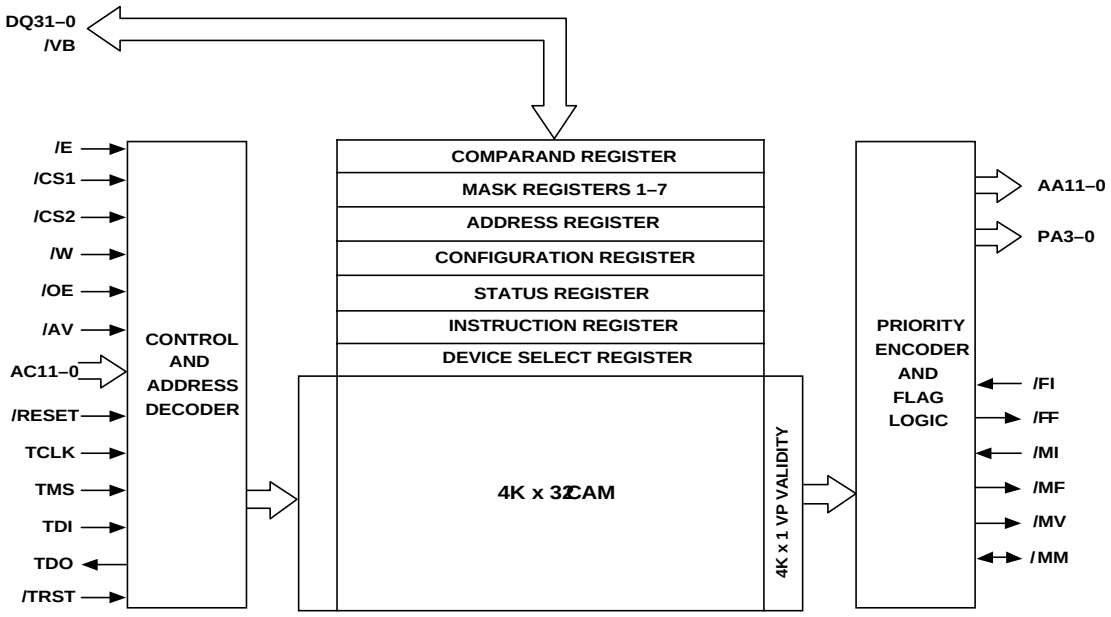


Figure 1: Block Diagram

GENERAL DESCRIPTION

The MU9C4320L ATMCAM is a 4K x 32 Content Addressable Memory (CAM) with a 32-bit wide data interface. The device is designed for use in ATM switches and routers to provide very high throughput VPI/VCI translation through lookup tables held in external RAM. VPI/VCI fields from the ATM cell header are compared against a list of current connections stored in the CAM array. As a result of the comparison, the ATMCAM generates an address that is used to access an external RAM where VPI/VCI mapping data and other information associated with the connection are stored.

The ATMCAM simultaneously compares the VPI/VCI in the CAM array as well as the VPI in a separate VP table. This capability provides support for both VPCs and VCCs, and halves the number of cycles needed to compare VPI and VCI information. A set of control states provides a powerful and flexible control interface to the ATMCAM. This control structure allows memory read and write, register read and write, data move, comparison, validity control, addressing control, and initialization operations.

The ATMCAM architecture uses a non-multiplexed data bus, direct hardware control of the device, and an independent bus for returning match results. Software control is also supported for systems where optimum performance is not needed.

OPERATIONAL OVERVIEW

The ATMCAM is designed to act as an address translator for lookup tables in ATM switch and router systems. It takes incoming VP/VC identifiers in ATM cell headers and generates addresses that access data in an external RAM. The RAM holds translated VPI/VCI information and other data relating to the particular connection. Refer to Figure 2 for a simplified block diagram of an ATM switch.

When a new connection is set up, the VPI/VCI of the connection is written to the ATMCAM. The write cycle can be to either a specific address within the device, or to the next free address. The address at which the write takes place is driven onto the Output Address bus, so VPI/VCI mapping data can be written simultaneously into the external RAM at the correct address.

With the connection established, the controller strips the VPI/VCI information off an arriving cell to form the Comparand, which is then compared against the contents of the ATMCAM. The ATMCAM generates an address that is used to access the VPI/VCI mapping data in the external RAM. The controller reads the data from the RAM and prefixes the translated header to the cell payload.

If the switch operates on VPI only, as well as on full VPI/VCI, the ATMCAM can compare both the VPI and VPI/VCI fields simultaneously. The option to test VPI fields is selected in the Configuration register of the ATMCAM. When selected, the VPI field is used to form an address that accesses a single-bit RAM array in the ATMCAM. This area of memory is referred to as the VP Table, and holds a single bit of information indicating the validity of a VP value.

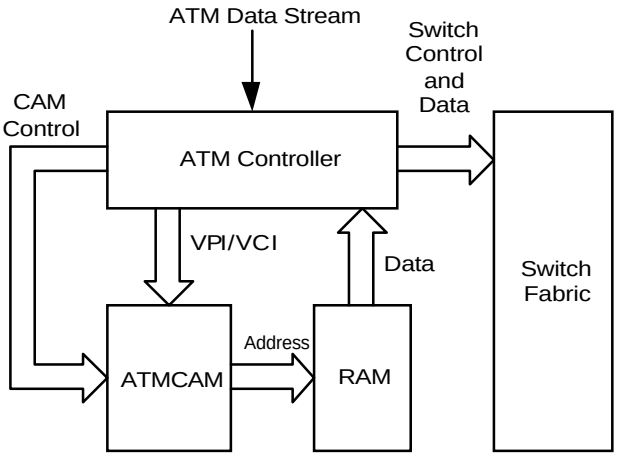


Figure 2: Switch Block Diagram

The VP Table contains 4K entries, corresponding to the 12 bits in the VPI field of the ATM header. In a multiple device system, only the lowest-priority device holds the VP Table. A hit in the VP Table takes lower priority than a match in the CAM array where the VPI/VCI fields are compared associatively. If there is a mismatch in the CAM array, but a hit in the VP Table, the VPI value is driven onto the Address Output bus. Flags indicate whether a CAM match or VP Table hit has occurred.

The VP Table eliminates the need to do two sequential compares, one on the full VPI/VCI fields, and the other on the VPI fields. The test of both sets of fields is accomplished by the ATMCAM in a single compare cycle.

The validity of a location in the CAM array is determined by an extra bit called the Validity bit. This bit is set and reset either with an address or an associative match. Therefore, when a new VPI/VCI entry is written to the CAM, its Validity bit is set valid.

When a connection is removed, the Validity bit for that entry is reset, and the address of the location is driven onto the Active Address bus. This simple mechanism allows easy maintenance of the connection list in both the CAM array and the external RAM.

The ATMCAM supports simple daisy chained vertical cascading that serves to prioritize multiple devices and provides system-level match and full indication. If the slight timing overhead associated with the daisy chain is unacceptable in the fastest systems, the ATMCAM is designed to facilitate external prioritization across multiple devices.

PIN DESCRIPTIONS

Note: *Signal names that start with a slash ("/") are active LOW. All signals are 3.3V CMOS level. Never leave inputs floating. The CAM architecture draws large currents during compare operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.*

DQ31–0 (Data Bus, Three-state, Common Input/Output)

The DQ31–0 lines convey data to and from the ATMCAM. When the /E input is HIGH the DQ31–0 lines are held in their high-impedance state. The /W input determines whether data flows to or from the device on the DQ31–0 lines. The source or destination of the data is determined by the AC11–0 lines and the /AV line. During a Write cycle, data on the DQ31–0 lines is registered by the falling edge of /E.

AC11–0 (Address/Control Bus, Input)

When Hardware control is selected, the AC11–0 lines convey address or control information to the ATMCAM, depending on the state of the /AV input. When /AV is LOW then AC11–0 carry an address; when /AV is HIGH AC11–0 carry control information. Data on the AC11–0 lines are registered by the falling edge of /E. When software control is selected, the state of the AC11–0 lines does not affect the operation of the device.

AA11–0 (Active Address, Output)

The AA11–0 lines convey the CAM Match address, the VP Table address, the Next Free address, or Random Access address, depending on the most recent memory cycle. The /OE input enables the AA11–0 outputs; when the /OE input is HIGH, the AA11–0 outputs are in their high-impedance state; when /OE is LOW the AA11–0 lines are active. In a vertically cascaded system after a Comparison cycle, Write at Next Free Address cycle or Read/Write at Highest-Priority match, only the highest-priority device will enable its AA11–0 lines, regardless of the state of the /OE input. In the event of a mismatch in both CAM array and VP Table after a Compare cycle, or after a Write at Next Free Address cycle into an already full system, the lowest-priority device will drive the AA11–0 lines with all 1s. The AA11–0 lines are latched when /E is LOW, and are free to change only when /E is HIGH.

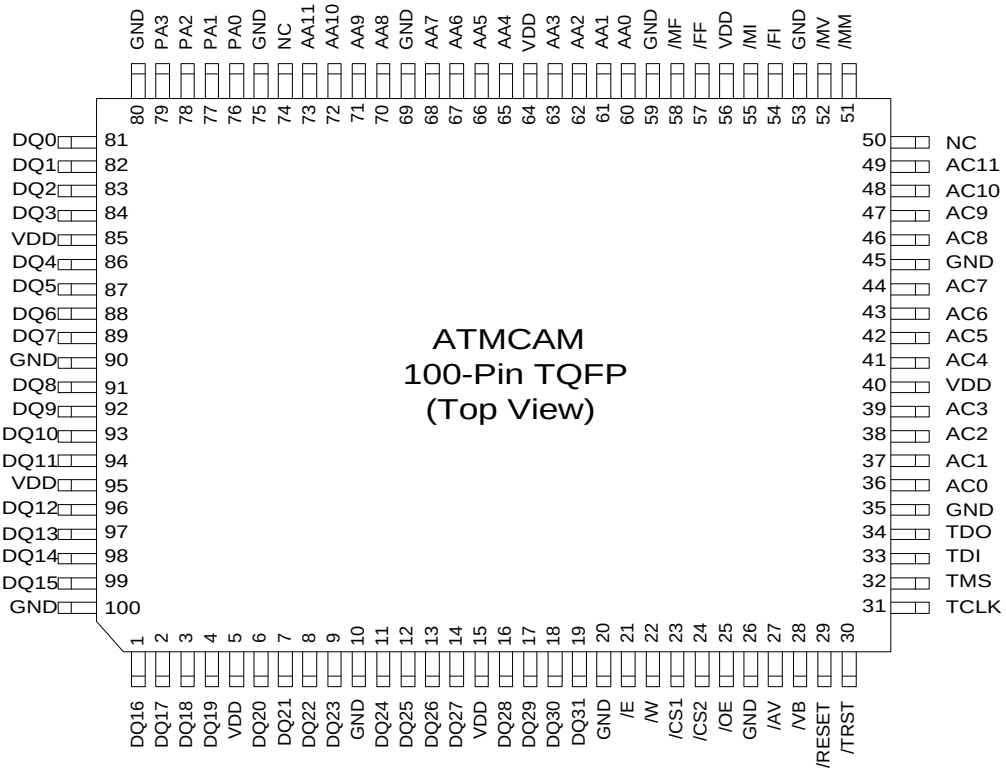


Figure 3: ATMCAM Pinout

PA3–0 (Page Address, Output)

The PA3–0 lines convey Page Address information. When the /OE input is HIGH, the PA3–0 outputs are in their high-impedance state; when /OE is LOW the PA3–0 lines carry the Page Address value held in the Configuration register. The PA3–0 lines are latched when /E is LOW, and are free to change only when /E is HIGH. The Page Address value of the currently active or highest-priority responding device is output at the same time, and under the same conditions, as the AA11–0 lines are active.

/E (Chip Enable, Input)

The /E input is the main chip enable and synchronizing control for the ATMCAM. When /E is HIGH, the chip is disabled and the DQ31–0 lines are held in their high-impedance state. The falling edge of /E registers the /W, /CS1, /CS2, /AV, /AC11–0 lines, and the /VB and DQ31–0 lines for a Write cycle. /E being LOW causes the results of the previous comparison or memory access to be latched on the PA3–0:AA11–0 lines; when /E goes HIGH the latches open allowing the new comparison results or random access memory address to flow to the PA3–0:AA11–0 lines.

/CS1, /CS2 (Chip Select 1, Chip Select 2, Inputs)

The /CS1 and /CS2 inputs enable the ATMCAM. If either /CS1 or /CS2 are LOW, the device is selected for a Read, Write, or Compare cycle through the DQ31–0 lines, or for an internal data transfer. The /CS1 and /CS2 lines do not have any effect on the PA3–0:AA11–0 outputs. The state of the /CS1 and /CS2 lines is registered by the falling edge of /E.

/W (Write Enable, Input)

The /W input determines the direction of data transfer on the DQ31–0 lines during Read, Write, and Data Move cycles. When /W is LOW, data flows into the DQ31–0 lines; when /W is HIGH, data flows out. The /W line also conditions the control state present on the AC11–0 lines. The state of the /W line is registered by the falling edge of /E.

/OE (Output Enable, Input)

The /OE input enables the PA3–0:AA11–0 outputs. When /OE is HIGH, PA3–0:AA11–0 are in their high-impedance state. When /OE is LOW, PA3–0:AA11–0 outputs are active, and convey the results of the last Comparison Cycle Match address or Memory Access address. In a vertically cascaded system, only the PA3–0:AA11–0 outputs of the highest-priority device will be activated by /OE being LOW; in lower-priority devices, the PA3–0:AA11–0 outputs remain in high impedance regardless of the state of /OE.

/AV (Address Valid, Input)

When Hardware control is selected, the /AV input determines whether the AC11–0 lines carry address or control information. When /AV is LOW, the AC11–0 lines convey a memory address; when /AV is HIGH, the AC11–0 lines convey control information. The state of the /AV line is registered by the falling edge of /E. When software control is selected, the /AV line distinguishes between instructions and data on the DQ31–0 lines; when /AV is LOW, data is present on the DQ31–0 lines; when /AV is HIGH, an instruction is present on the DQ11–0 lines.

/VB (Validity Bit, Three-state, Common Input/Output)

During accesses over the DQ31–0 lines, the /VB line conveys validity information to and from the ATMCAM. During a Write cycle (/W=LOW), when /VB is LOW the addressed location is set valid; when /VB is HIGH it is set empty. During a Read cycle (/W=HIGH), the validity of the addressed location is read on the /VB line. During a Write cycle, the state of the /VB line is registered by the falling edge of /E.

/MF (Match Flag, Output)

The /MF output indicates whether a valid match has occurred during the previous Comparison cycle. If the /MF output is HIGH at the end of a Comparison cycle, then no match occurred; if it is LOW then either a match occurred within the device, or the /MI input is LOW, conditioned by the /MF output from a higher-priority device in the system. The /MF line is used in conjunction with the /MV line to indicate when a match occurred in the CAM array or the VP Table. If /MF is LOW, then the match occurred in the CAM array; if /MF is HIGH and /MV is LOW, then the match occurred in the VP Table. Both /MF and /MV lines are HIGH after a Compare cycle that results in a mismatch. The state of the /MF line will not change until after the rising edge of /E during the Comparison cycle. Note that /MF indicates the results of the most recent Comparison cycle; it will not change when the PA3–0:AA11–0 lines carry an address other than the Match address.

/MI (Match Input, Input)

The /MI input receives match information from the next higher-priority ATMCAM in a vertically cascaded system to provide system-level prioritization. When the /MI input is HIGH, the /MF output will only go LOW if there is a match during a Comparison cycle; when the /MI input is LOW, the /MF output will go LOW. The /MF output from one device is connected to the /MI input of the next lower-priority device. The /MI pin of the highest-priority device must be tied HIGH.

/FF (Full Flag, Output)

The /FF output indicates when all the memory locations have their Validity bits set valid (LOW). When there is at least one location with its Validity bit set HIGH, the /FF output will be HIGH; when all locations have their Validity bits set LOW, and the /FI input is LOW, the /FF output will be LOW. If the /FI input is HIGH, the /FF output will be HIGH. The state of the /FF line will not change until after the rising edge of /E during a Write cycle.

/FI (Full Input, Input)

The /FI input receives full information from the next higher-priority ATMCAM in a vertically cascaded system to provide system-level full information. When the /FI input is LOW the /FF output will be HIGH if there is at least one location whose Validity bit is set invalid; when all locations have their Validity bits set valid, the /FF output goes LOW. When the /FI input is HIGH, the /FF output will remain HIGH. The /FF output from one device is connected to the /FI input of the next lower-priority device to give system-full indication. The /FI pin of the highest-priority device must be tied LOW.

/MM (Multiple Match, Open Drain Output)

The /MM line indicates that there is a multiple match within the system. When the /MI input is HIGH, the /MM line is pulled LOW if there are at least two matches within the ATMCAM as a result of the previous Comparison cycle; when there are less than two matches, the /MM line floats HIGH. When the /MI input is LOW, the /MM line is pulled LOW if there are one or more matches within the ATMCAM as a result of the previous Comparison cycle; when there are no matches, the /MM line floats HIGH. The /MM lines have open-drain outputs, so all /MM lines within the system are connected together to give system-level multiple match indication. The state of the /MM line will not change until after the rising edge of /E during a Comparison cycle. The /MM line is unaffected by matches in the VP Table.

/MV (Match Valid, Output)

After a Compare cycle, the /MV line indicates whether there has been a valid match in this device in either the CAM array or the VP Table. When /MV is LOW then a match has occurred in either the CAM array or the VP Table; when /MV is HIGH then a mismatch has occurred in both the CAM array and the VP Table. The /MF output is used to distinguish between the two types of matches. The state of the /MV line will not change until after the rising edge of /E during a Comparison cycle. /MV represents local conditions written in the device; it is not conditioned by the /MI input.

/RESET

The /RESET input is used to reset the ATMCAM to a known state. When the /RESET line is pulled LOW it causes the ATMCAM to enter its reset state. After power is applied to the ATMCAM, the /RESET line must be held LOW for a time equal to or greater than the minimum RESET pulse width before the device can operate correctly.

TCLK (JTAG Test Clock, Input)

The TCLK input is the Test Clock input.

TMS (JTAG Test Mode Select, Input)

The TMS input is the Test Mode Select input.

TDI (JTAG Test Data Input, Input)

The TDI input is the Test Data input.

TDO (JTAG Test Data Output, Output)

The TCLK output is the Test Data output.

/TRST (JTAG Reset, Input)

The /TRST input is the Reset input, and serves to reset the Test Access Port circuitry to its reset condition.

VDD, GND (Positive Power Supply, Ground)

These pins are the main power supply connections to the ATMCAM. VDD must be held at +3.3 Volt ± 0.3 Volt relative to the GND pin, which is at 0 Volt, system reference potential, for correct operation of the device.

Note: *The TCLK, TMS, TDI, TDO, and /TRST lines are defined in the IEEE Standard Test Access Port and Boundary-scan Architecture IEEE Std. 1149.1-1990 and IEEE Std. 1149.1a-1993.*

FUNCTIONAL DESCRIPTION

Data is read from and written to the ATMCAM through the DQ31–0 lines. The ATMCAM is controlled through the Control bus, which comprises Chip Enable (/E), two Chip Selects (/CS1, /CS2), Write Enable (/W), Output Enable (/OE), Validity Bit Control (/VB), Address Valid (/AV), and Address/Control inputs (AC11–0). When the /AV line is LOW, the AC11–0 lines carry an address for random access into the Memory array; when it is HIGH, the AC11–0 lines convey control information. The ATMCAM control states perform Read/Write Memory, Read/Write Register, Data Move, Comparison, Set Validity, VP Table Control, and Initialization. These functions are summarized in Table 1 on page 19.

Random access to memory locations occurs when the /AV line is LOW; during a Write cycle, the validity of the location is set by the /VB input. When the /AV line is HIGH the control states allow read and write access to the register set comprising Comparand register, seven mask registers, a Configuration register, a Status register, an Address register, a Device Select register, and an Instruction register. The Configuration register sets the persistent operating conditions of the device: the Page address of the device, selection of mask register for directly addressed memory writes, selection between hardware and software control, enabling VP Table lookup, selection of VP Table masking, and VP Table Page address.

When Hardware control is selected, control is through the AC11–0 bus. When software control is selected, control is through the Instruction register, which is loaded from the DQ bus. Under software control the /AV line is used to distinguish between data and an instruction on the DQ bus. Therefore, in Software Control mode, random access to the Memory array can only take place through indirect addressing using the Address register.

The two Chip Select lines /CS1, /CS2 enable the device and simplify access to a multi-chip system, if either Chip Select line is LOW the device is selected. The ATMCAM also can be selected through the Device Select register when its value is set to that of the Page address of the device, and the enable bit in the Device Select register is set LOW. The /OE input enables the output signals and is used to synchronize devices in a multi-chip system, and to prevent race conditions between devices during priority resolution.

The output signals comprise the Active address (AA11–0), and the Page address (PA3–0). The PA3–0:AA11–0 bus carries the current Active address which is either the Match address, VP Table address, Next Free address, or the Random Access address, concatenated with the Device Page address. The source of Active address is dependent on the previous control state, allowing access to associated data in the external RAM at the same location as an access in the ATMCAM for all types of cycles.

The Output Enable /OE controls the PA3–0:AA11–0 bus: when it is LOW after a Compare cycle, the highest-priority responding device outputs its Page and Match addresses on PA3–0:AA11–0. Only the highest-priority responding device is enabled, all other lower-priority devices will have their PA3–0:AA11–0 lines in their high-impedance state, regardless of the state of their respective /OE lines; when /OE is HIGH, the PA3–0:AA11–0 lines remain in their high-impedance state.

When a mismatch occurs in the system, the lowest-priority device, as defined in the Configuration register, will drive the PA3–0:AA11–0 bus with all 1s. When any Read or Write cycle occurs, the address of the accessed location is output on the PA3–0:AA11–0 bus. The address output on the PA3–0:AA11–0 bus is persistent, and is held latched until /E goes HIGH during the next cycle that changes the Active address. The PA3–0:AA11–0 lines are free to change only while /E is HIGH. Once /E goes LOW, the state of the PA3–0:AA11–0 bus is latched.

After a Compare cycle, the /MV, /MF, and /MM flags are free to change after /E has gone HIGH. Once the Match Flag daisy chain has resolved device prioritization, the /OE lines can be asserted to enable the PA3–0:AA11–0 lines from the highest-priority matching device.

In a multi-CAM system, when a device remains deselected during a Compare cycle through /CS1 and /CS2 being HIGH and there being no match between the Device Select register and the Page Address register that device will clear any previous positive match results. In other words, if it had previously been indicating a match from an earlier Comparison cycle, it will now be set to indicate a mismatch, even though it was not selected during the most recent Compare cycle.

For pure software control of the ATMCAM, instructions can be loaded into the Instruction register, and results read from the Status register. The Status register holds the results of comparison: PA3–0:AA11–0, /MF, /FF, /MV, and /MM plus two PA:AA Validation bits which indicate the type of cycle that generated the PA3–0:AA11–0 value.

The ATMCAM supports VP Table lookup in parallel with VPI/VCI comparison in the CAM array. This option is selected through the Configuration register. When active, Comparand Register bits CR31–20 are used to address the 4K x 1 VP Table simultaneously with the Compare cycle.

The results of the Compare cycle have higher priority than the VP Table lookup, and take precedence over it. In the absence of a match in the CAM, the single bit accessed in the VP Table is used to indicate whether there was a VP Table match. Results of the Comparison cycle and VP Table lookup are indicated through the /MV and /MF outputs. Only the lowest-priority device in the system is configured to hold the VP Table.

Vertical cascading is supported through a daisy chain architecture. There are two daisy chains, one each for the Match flag and the Full flag; the Multiple Match flag is connected between devices with an open-drain line. The Match flag (/MF) from a higher-priority device is connected to the Match input (/MI) of the next lower-priority device to provide prioritization throughout a multiple device system. The /MF output from the lowest priority device provides a system Match flag. If the delay through the daisy chain is unacceptable, the /OE input can be used by external priority-resolution circuitry to enable the highest-priority responder in the system.

The match conditions on the Match, Match Valid, and Multiple Match flag lines are persistent indicating the results of the most recent Compare cycle. The Match flags are free to change after the rising edge of /E during a Compare cycle, at which time the daisy chain starts to resolve device prioritization. Once the daisy chain has settled, the /OE lines can be pulled LOW to access the Highest-Priority Match address on the PA3–0:AA11–0 bus.

The Multiple Match open-drain output (/MM) provides multiple match indication when there are two or more matches in a single device, or a device has its /MI input LOW and has a match; the /MM flags of all devices in the system are wire-ORed. Multiple responders can be accessed sequentially by resetting the Highest-Priority Match latch with the control state “Advance Match Address to Next Match.”

The Full flag (/FF) is cascaded from one device to the Full Flag input (/FI) of the next lower-priority device in the system. The /FF output from the lowest-priority device provides a system Full flag. The Full flag is free to change after the rising edge of /E during a Write cycle. The daisy chains are persistent and are not conditioned by the /OE input.

The ATMCAM supports JTAG boundary-scan testing through the pins TCK, TMS, TDI, TDO, and /TRST, according to the IEEE 1149 Standard: Test Access Port and Boundary-scan Architecture.

OPERATIONAL CHARACTERISTICS

Processor Interface

The processor interface is through a 32-bit data bus DQ31–0 and control signals comprising Chip Enable (/E), two Chip Selects (/CS1, /CS2), Write Enable (/W), Output Enable (/OE), Validity Bit Control (/VB), Address Valid (/AV), and Address/Control inputs (AC11–0). When the /AV line is LOW, the AC11–0 lines carry an address for random access into the Memory array; when it is HIGH, the AC11–0 lines convey control information.

Most of the functionality of the ATMCAM is accessed through the control states on AC11–0 when /AV is HIGH. The processor maps the control structure into memory space and controls the ATMCAM through memory Read and Write cycles. Using this memory mapping scheme, the /AV line should be driven from logic that generates a HIGH level within the mapped range of the control states, and a LOW level outside it. Other control inputs /E, /W, /CS1, and /CS2 are analogous to SRAM control inputs.

The /VB line acts like an extra data bit during memory Read and Write cycles and is used to read and write the validity of any memory location.

The ATMCAM is enabled either through hardware through /CS1 or /CS2 being LOW, or it is enabled by the value written to the Device Select register matching with the Page Address field of the Configuration register. One extra bit in the Device Select register enables the comparison between the Page Address value and the Device Select register. These Chip Select mechanisms operate in parallel. If any one is active, the device is enabled.

The ATMCAM can be controlled directly through software. The Software Control mode is selected through settings in the Configuration register.

When the Software Control mode is selected, control states are written to the Instruction register from DQ11–0 during a Write cycle with the /AV line held HIGH. If the control state does not involve any data transaction on the DQ31–0 lines, the instruction is executed during the same cycle; the state of DQ12 modifies the instruction, its state is equivalent to the /W line during the execution of a control state under Hardware control. If the instruction calls for a data transaction on the DQ31–0 lines, then it is latched into the Instruction register but no further action takes place during that cycle. Subsequent Data Read or Write cycles with the /AV line LOW will cause the instruction to be executed with the data on the DQ31–0 lines.

A Read cycle with the /AV line HIGH will access the Status register, allowing results to be read back without loading a new instruction. After a Comparison cycle, Write at Next Free Address cycle or Read/Write at Highest-Priority match in a vertically cascaded system, only the highest-priority device will enable its DQ31–0 lines and output the contents of its Status register. After a Comparison cycle, in the event of a mismatch in the CAM, the DQ31–0 lines of the lowest-priority device will be enabled. After a random access Read or Write cycle, the Status register of any selected device will be enabled. Under these circumstances, it is up to the user to ensure that only a single device is enabled through /CS1, /CS2, or the Device Select register.

The instruction is persistent, so that all subsequent data transactions will be executed according to the control state held in the Instruction register. The results of a Comparison cycle can be read back from the Status register, and include PA3–0:AA11–0, /MF, /MM, /MV, and /FF. The following sequence of events provides the fastest operation of the ATMCAM in Software Control mode:

/AV	Operation
1	Load ‘Compare DQ with CAM’ instruction
0	Comparand on DQ31–0
1	Read Status register
0	Next Comparand on DQ31–0
1	Read Status register, etc.

Note: *It is up to the system designer to ensure that the correct cycle type follows the loading of an instruction in Software Control mode. If the instruction expects a Read cycle, and a Write cycle is executed, or vice versa, the function of the ATMCAM is undefined. Such an error may lead to data loss, but will not damage the device physically.*

The ATMCAM supports VP Table lookup. This function is selected through the Configuration register. By default the VP Table lookup is disabled. When selected, the function is implemented through a 4K x 1 table addressed by the upper-order 12 bits of the Comparison Data bits 31–20. The lowest-priority device within a vertically cascaded system holds the VP Table. The function is disabled in all other devices through the setting in the Configuration register. Because the VPI field is 12 bits, the VP Table is entirely contained within the 4K depth of a single ATMCAM. Note that when the VP Table is disabled, the VP Table control states are still active. In other words, even when disabled, the VP Table bits can be read, set, and reset.

The table is accessed during a Compare cycle. The single bit that is accessed in the VP Table by the address formed from Comparison data bits 31–20 is used to indicate whether there is a VP Table match at that address. The

individual bits in the VP Table are set and reset through control states. A LOW value in the VP Table indicates a match, while a HIGH value indicates a mismatch. The results of comparison in the CAM array have a higher priority than the VP Table result. In other words, if there is a match in the CAM array, the VP Table result is ignored, and the match is flagged by /MV and /MF going LOW. If there is a mismatch in the CAM array, then a VP Table match is indicated by /MV going LOW and /MF remaining HIGH. In the event of a mismatch in both the CAM array and the VP Table, both /MV and /MF remain HIGH. The following truth table shows how match conditions are flagged:

/MV	/MF	Compare Cycle Result
0	0	Match in CAM
0	1	Match in VP Table
1	0	/MI = LOW (CAM match in higher priority device)
1	1	No Match

Note: *The /MV line will be LOW in any device with a match, regardless of its priority. Only when the /MV line is LOW and the /MF line is HIGH in the lowest-priority device will there be a VP Table match and no CAM array match.*

The VPI field can be masked through the Configuration register. The VPI values are ANDed with the VP Table Address Mask bit; therefore, “zeros” can be forced into any of the VP Table Address bits. This facility is useful in cases where the VPI values are coded on less than 12 bits. For example, for 8-bit VPI processing, the Table Address Mask field would have “zeros” in the upper-order four bits and “ones” in the rest. This masked address is the value output on the AA11–0 bus while the VP Page address is output on the PA3–0 bus during a VP Table match. Note that the VP Table Address Mask bits are only active for Comparison cycles, and not for other VP Table accesses.

The ATMCAM supports JTAG boundary-scan testing through the pins TCK, TMS, TDI, and TDO, according to the IEEE 1149 Standard: Test Access Port and Boundary-scan Architecture. The following JTAG support is provided: BYPASS, SAMPLE/PRELOAD, IDCODE, CLAMP, INTEST, and EXTEST. Signals on input pins can be captured and signals on output pins can be driven, allowing testing of board-level interconnection and internal device testing.

Hardware Control

Performance of the ATMCAM is enhanced by direct hardware control through a set of control states through the AC11–0 lines. The Hardware Control mode is selected when Configuration Register bits FR27–26 are set LOW. The AC11–0 inputs are qualified by the /W, /AV, and /VB. When /AV is LOW, the AC11–0 lines carry the address for a random Read or Write cycle, depending on the state of /W, and /VB carries the validity of the location. During a Write cycle, /VB is written to the Validity bit of the addressed location; during a Read cycle, the validity of the location is read on the /VB line. When /VB is LOW, the location contains valid data; when /VB is HIGH the location is empty.

When /AV is HIGH, the AC11–0 lines carry address and control information. The control information is conveyed on AC8–0. If masking is not used, and all random addressing of the memory is indirect through the Address register, then only the AC5–0 lines are needed for full control of the device.

In applications where a restricted number of control lines are available, or where speed is not critical, the ATMCAM can be controlled in Software Control mode where the control states are loaded into the Instruction register through the DQ31–0 lines. The control states are identical in both Hardware and Software Control modes, although DQ12 takes on special significance in Software mode.

Software Control

For optimum performance, the ATMCAM is controlled through the AC11–0 lines, allowing data transactions through the DQ31–0 lines during a control cycle. In cases where the overhead of a separate data load cycle can be accommodated, the ATMCAM can be operated through the Instruction register.

Control through the Instruction register is selected by the FR27–26 bits of the Configuration register being set HIGH. Under this circumstance, the AC11–0 lines are not used, instead the instruction is loaded from the DQ11–0 lines into the Instruction register during a Write cycle with the /AV line HIGH. The instructions are directly analogous to the control states for any operation that does not involve data transfer on the DQ31–0 lines, in which case the instruction is executed during the same cycle as the instruction is loaded. To distinguish between Read and Write control states, DQ12 is used to indicate which type of instruction should be executed. When DQ12 is LOW at the beginning of the cycle, the instruction executed is the Write Cycle instruction (/W = LOW when control state is conveyed on AC11–0); when DQ12 is HIGH at the beginning of the cycle, the instruction executed is the Read Cycle instruction (/W = HIGH when control state is conveyed on AC11–0).

When the instruction calls for data to be written or read from the DQ31–0 lines, the instruction is loaded into the Instruction register during the cycle, and the next Data Read or Write cycle with /AV LOW executes the instruction using the DQ31–0 bus for the data transaction. The instruction is persistent; i.e., if no other instruction is loaded into the Instruction Register, subsequent data transactions with the /AV line LOW will be executed according to the instruction currently loaded in the Instruction register. When there is a data access to a memory location on DQ31–0 associated with the instruction, the /VB line carries the validity of that location.

Instructions that involve data transactions on DQ31–0, and are therefore executed on a subsequent Read or Write cycle with the /AV line LOW, are all Read/Write Memory and Read/Write Register instructions, Read Validity, Write DQ3–0 to PA in Configuration register of Highest-Priority Empty device, and Set /FF. All other instructions are executed in a single cycle with the state of DQ12 being interpreted as the state of the /W line during the equivalent hardware control state. A Read cycle with /AV HIGH accesses the Status register.

Active Address Interface PA3–0:AA11–0

The Active Address interface PA3–0:AA11–0 carries the currently active address. The address source depends on the most recent control state that caused it to change. The possible address sources that are output on PA3–0:AA11–0 are: Highest-Priority CAM Match address, VP Table Match address, Next Free address, CAM Read address, CAM Write address, VP Table Read address, and VP Table Write address.

PA3–0:AA11–0 After a Comparison Cycle

After a Comparison cycle, or access to the Highest-Priority address, the PA3–0:AA11–0 lines carry one of three possible results:

- The CAM Match address if the Comparison cycle resulted in a match in the CAM. Only the device containing the highest-priority match enables its PA3–0:AA11–0 lines. All other devices with either no match or a lower-priority match, as indicated by the Match Flag daisy chain, keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.
- The VP Table Match address if the Comparison cycle resulted in a mismatch in the CAM but a match in the VP Table. Only the lowest-priority device, as indicated by bit FR25 in the Configuration register, enables its PA3–0:AA11–0 lines. All other devices keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.
- All 1s if there was no match in either CAM or VP Table, or there was no match in the CAM and the VP Table was disabled by Configuration register bit FR24 being HIGH. The lowest-priority device, as indicated by bit FR25 in the Configuration register, enables its PA3–0:AA11–0 lines and provides the source of all 1s. All other devices will keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.

PA3–0:AA11–0 After a Write at Next Free Address Cycle

After a Write at Next Free Address cycle the PA3–0:AA11–0 lines carry the address that was written to during that cycle. Only the device in which the write occurred enables its PA3–0:AA11–0 lines. All other devices keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.

In the event that the system was full prior to the Write at Next Free Address cycle being executed, so that the write operation was suppressed, the PA3–0:AA11–0 lines carry all 1s. The lowest-priority device, as indicated by bit FR25 in the Configuration register, enables its PA3–0:AA11–0 lines and provides the source of all 1s. All other devices keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.

PA3–0:AA11–0 After a Random Access Read or Write to the CAM

After a random Read or Write cycle to the CAM, the PA3–0:AA11–0 lines carry the address that was accessed during that cycle. Only the device in which the access occurred enables its PA3–0:AA11–0 lines. All other devices keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs. Note that the access to the PA3–0:AA11–0 bus differs in this respect from the operation of the Status register which is accessible in any selected device under this particular circumstance.

In the event that the Write cycle was broadcast to multiple devices, all devices that have their /OE lines held LOW will enable their PA3–0:AA11–0 lines. Under this circumstance, it is up to the system designer to ensure that only one /OE line is driven LOW to prevent bus contention on the PA3–0:AA11–0 lines.

PA3–0:AA11–0 After a Random Access Read or Write to the VP Table

After a Read or Write cycle to the VP Table, the PA3–0:AA11–0 lines carry the address of the location accessed in the VP Table. The VP Table is held in the lowest-priority device, which therefore is the only device to enable its PA3–0:AA11–0 lines. All other devices keep their PA3–0:AA11–0 lines in high impedance regardless of the state of their /OE inputs.

PA3–0:AA11–0 Conditions of Operation

- During a control state that does not have any effect on the device address, such as a Write Register cycle, the PA3–0:AA11–0 lines remain unchanged. In other words, the state of the PA3–0:AA11–0 lines persists until another cycle causes it to change.
- When enabled by /OE being LOW, the PA3–0:AA11–0 lines are only free to change while /E is HIGH. When /E goes LOW the PA3–0:AA11–0 lines are latched.
- The PA3–0:AA11–0 lines are enabled when /OE is LOW provided that the previous cycle causes them to be active. When /OE is HIGH, the PA3–0:AA11–0 lines are in high impedance. Note that /OE is asynchronous with respect to /E, and is independent of Chip Select from either /CS1, /CS2, or through the Device Select register, except in the case of non-broadcast random Read and Write cycles to the CAM.

PA3–0:AA11–0 and the Match Flags

The Match flags /MV, /MF, /MM reflect the results of the most recent Comparison cycle. During a Comparison cycle, they do not change until after /E has gone HIGH after which they are free to change combinatorially; their state is not latched when /E is LOW. This condition allows some pipelining to occur and is useful in systems with long daisy chains. A Comparison cycle can be followed by another cycle that does not affect the PA3–0:AA11–0 lines before the daisy chain is resolved. For example:

```
CMP CR
WR CR
```

The WR CR control state can be executed before the daisy chain has resolved device prioritization after the CMP CR control state. The /OE is then asserted at a suitable time, depending on the length of the daisy chain. The Match address of the highest-priority responding device is then driven onto the PA3–0:AA11–0 lines.

The /MV, /MF, /MM lines continue to indicate the results of the most recent match, even when the PA3–0:AA11–0 lines carry an address other than the Match address. This condition allows rapid return to the Match address value on the PA3–0:AA11–0 lines through a RD[HPM] cycle, without the daisy chain having to re-resolve device-level prioritization.

PA3–0:AA11–0 and the Status Register

The Status Register bits SR15–0 reflect the PA3–0:AA11–0 lines under all conditions. The Status Register flags /MV, /MF, /MM, and /FF represent the local conditions within the device, and are not conditioned by the /MI and /FI inputs.

After a Comparison cycle, Write at Next Free address, or access to the Highest-Priority Matching device, a Status Register Read cycle is executed in the same device as the active PA3–0:AA11–0 lines. In the case of a random access Read or Write cycle, the Status register of any selected device can be accessed by a Read Status Register cycle. The system designer must ensure that a Status Register Read cycle after a random Read or Write cycle is into a single device using Chip Select /CS1, /CS2, or the Device Select register to prevent bus contention on the DQ31–0 bus.

REGISTER DESCRIPTIONS

The register set contains a Comparand register, seven mask registers, Address register, Configuration register, Status register, Next Free Address register, Device Select register, and Instruction register. Note that all RESERVED bits can be read and written without affecting the operation of the device. However, for forward compatibility with future product enhancements, system designers should not rely on any particular RESERVED bit having no effect on the operation of the device in future revisions. Therefore, all RESERVED bits should be set to logical zero.

Comparand Register

The 32-bit Comparand register holds the value to be compared with the valid contents of the CAM array, although the DQ lines can be compared directly, and then optionally written into the Comparand register.

Mask Registers

There are seven 32-bit mask registers which are used to mask Compare and Write cycles. When a bit is set LOW in a selected mask register, the corresponding bit enters into comparison during a Compare cycle, or is written during a Write cycle. When a bit is set HIGH in a selected mask register, the corresponding bit does not enter into comparison during a Compare cycle, or remains unchanged after a Write cycle.

Address Register

The 32-bit Address register is used for indirect addressing of the CAM array. When random access to the CAM array is restricted to indirect addressing, the width of the control bus can be reduced to 9 bits if masking is used or 6 bits if it is not. Control states allow increment and decrement of the Address register as well as auto-increment and auto-decrement Read and Write cycles. Bits AR11–0 hold the address while bits AR31–12 are reserved and should be set LOW.

Configuration Register

The 32-bit Configuration register sets the persistent operating conditions of the ATMCAM. Bits FR31–29 select which mask register is used for direct Write cycles to the CAM array when the address is conveyed on the AC11–0 lines (/AV=LOW), a value of 000 in this field results in unmasked direct Write cycles. Bits FR27–26 select the mode of operation: Hardware Control mode or Software Control mode. Bit FR25 is used to identify the lowest priority device in a vertically cascaded system. Bit 24 is used to enable or disable the VP Table in the lowest-priority device. Bits FR23–12 hold the VP Table Address mask. Bits FR7–4 hold the VP Table Page address. Bits FR3–0 hold the device Page address. All other bits are reserved and should be set LOW. See Table 3 on page 26.

Status Register

The 32-bit Status register holds the results of the most recent control state that caused the PA:AA lines to change. It is intended for use in Software Control mode where results of an operation are read from the CAM through the DQ31–0 lines. Bit SR31 holds the Match Valid flag, /MV, which goes LOW if there is a match in the CAM array or a hit in the VP Table. Bit SR31 holds the Match flag, /MF, which goes LOW when there is a match in the CAM array. Bit SR29 holds an internal version of the Multiple Match flag, /MM, which is LOW if there is a multiple match in the particular device; note that this is not a system-level multiple match indication. Bit SR28 holds the Full flag, /FF, which goes LOW when all the CAM array locations are set valid, and the /FI line is LOW. Bits SR25–24 indicate the type of result held in the Active Address field: Match address, Memory Access address, VP Table address, or Reset state. Bits SR19–16 hold the Page address, PA3–0, for the device. Bits SR11–0 hold the Active address, AA11–0. All other bits are reserved and are set LOW. See Table 4 on page 26.

Next Free Address Register

The 32-bit Next Free Address register holds the highest-priority address that has its Validity bit set empty (LOW). System-level prioritization ensures that only the device with the highest-priority empty address in a vertically cascaded system will respond to a Read Next Free Address Register Control state. Bits NF19–16 hold the device Page address, PA3–0. Bits NF11–0 hold the next free address value. All other bits are reserved, and are set LOW. See Table 5 on page 26.

Device Select Register

The 32-bit Device Select register is used for software selection of the ATMCAM. A particular device is selected when the value in bits DS3–0 are the same as the Page Address value PA3–0 and the Device Select Enable bit, DS8, is set LOW. Setting DS8 HIGH prevents the Device Select register from enabling the ATMCAM. All other bits are reserved and should be set LOW. See Table 6 on page 26.

Instruction Register

In Software Control mode, control states are written to the 32-bit Instruction register instead of being fed to the ATMCAM through the AC11–0 lines. Bits IR11–0 are equivalent to the AC11–0 lines and the control states they invoke are identical to those of the Hardware Control mode. The remaining bits are reserved and should be set LOW.

The Memory Array

The Memory Array is organized as 4096 32-bit locations. Location 0000H as the highest-priority location, and location 0FFFH as the lowest-priority location. Write cycles to the next free address start at location 0000H when the ATMCAM is empty, and continue down to 0FFFH when it becomes full.

Each 32-bit location in the CAM array has one extra bit, the Validity bit, which is used to indicate whether the location is empty or has valid contents. When the Validity bit is HIGH, the location is empty and is not compared during Comparison cycles; when it is LOW the contents are valid and will be compared during a Comparison cycle. The Validity bits are set or reset during Write cycles through the /VB line. The Validity bit of a location is accessed on the /VB line during a Read cycle. The Validity bits can be set and reset through control states.The Validity bits are also used in the generation of the next free address value.

Memory Access

Data is written to or read from the Memory array either randomly by address, or associatively by comparison and next free address. Random addressing can be either direct with the address on the AC11–0 lines (/AV=LOW) or indirect with the address held in the Address register. Memory access is controlled through the control states on the AC11–0 lines (/AV=HIGH) in Hardware Control mode, or through the Instruction register in Software Control mode.

VP Table

The VP Table is a separate area of RAM, organized as 4K x 1 and addressed by the upper order 12 bits of the comparand which hold the VPI field of the ATM header. The VP Table is contained in the lowest-priority device, and is enabled by Configuration Register bit FR24. Each VP Table location holds a flag bit to indicate whether there is a VP match at that address. A VP Table value of 0 indicates a match, or hit.

The VP Table is not initialized by hardware or software resets. Before enabling the VP Table, all VP bits must be initialized by writing to each bit using the VP Table control states.

The VP Table is accessed during a Compare cycle. If there is a match in the CAM, it takes priority over a hit in the VP Table. The /MV flag goes LOW if there is a match in the CAM or a hit in the VP Table, the /MF line goes LOW if there is a match in the CAM. The address fed to the VP Table can be masked by forcing zeros into the address bits. The VP Table address mask is held in Configuration Register bits FR23–12. When there is a VP Table hit and no match in the CAM, the masked VP Table address is output on the AA11–0 bus while the VP Page address is output on the PA3–0 bus.

Chip Select

There are two methods of selecting an ATMCAM: through Hardware control inputs /CS1 and /CS2, and through software control using the Data Select register.

Chip Select Inputs

The Chip Select lines /CS1 and /CS2 enable an ATMCAM to participate in a control cycle. If either /CS1 or /CS2 are LOW the device is selected. By connecting all the /CS1 lines together in a multi-CAM system, and decoding the lines to each individual device's /CS2 line, control states can operate locally within a single device or globally in all devices. Control states can be broadcast to all devices within the system by pulling the /CS1 lines LOW, for operations such as Write Comparand register; individual devices can be selected to respond to a control state such as Write at Address by pulling a single decoded /CS2 line LOW.

Device Select Register

One dedicated line is needed per device to do local selection of one device within a multi-CAM system. In cases where control lines are at a premium, the Device Select register can be used as the method of selection. If Device Select Register bit DS8 is LOW, only the device or devices whose Page Address value, held in Configuration Register bits FR3-0, match with the Device Select Register bits DS3–0 will be selected. Note that the match condition of the Device Select register is ORed with the state of the /CS1 and /CS2 lines. If DS8 is HIGH, the device remains unselected through the Device Select register.

The conditions of the Device Select register, the /CS1 and /CS2 lines are sampled at the time of the falling edge of /E. In a particular ATMCAM within a system, that CAM will be selected under the following conditions:

(/CS1=LOW) OR (/CS2=LOW)
OR ((DS8 = LOW) AND (DS3–0 = PA3–0))

Therefore, the /CS1 lines of all devices are tied together for global cycles that broadcast control states to all devices within the system; then, for local cycles, an individual device is selected by loading all the Device Select Registers bit DS8 LOW and bits DS3–0 with the Page Address value of the device to be selected. On a subsequent cycle, /CS1 and /CS2 remain HIGH, and only the device whose Page Address value matches with its DS3–0 will respond. After an individual device has been selected, a global Write cycle to the Device Select register using /CS1 line is executed to select another device, or to disable the software chip select mechanism altogether.

Vertical Cascading

A system can be designed to any practical depth by vertically cascading ATMCAMs. The scheme uses a daisy chain to provide system level prioritization as well as Match, Multiple Match, and Full flags. There are three daisy chains: Match, Multiple match, and Full, plus a Match Valid line indicates both the CAM and VP Table matches.

When a control state is broadcast that accesses the highest-priority matching location or Status register, the daisy chain ensures that only the device that responds is the one with the highest-priority match in the system. All other devices will have their DQ31–0 lines and PA3–0:AA11–0 outputs held in high impedance. Therefore, the Match Flag daisy chain controls access to the system resources for control states that are conditional on the results of the previous Compare cycle.

During a Comparison cycle, the Match and Multiple Match flags will not change until /E goes HIGH during that cycle. At this time, the daisy chain starts to resolve system-level prioritization. Once sufficient time has elapsed for the daisy chain to be resolved, the PA3–0:AA11–0 lines can be enabled with /OE, and Status Register Read cycles will access only the highest-priority matching device. Note that the daisy chain resolves system-level prioritization combinatorially once initiated by /E going HIGH. Other cycles that do not affect the daisy chain or match results can take place in the ATMCAM while the daisy chain is resolving, for example, WR CR, allowing some degree of pipelining. During a Write cycle, the Full flag will not change until /E goes HIGH during that cycle.

There is a small propagation delay per device in the daisy chain. Alternatively, vertical cascading can be done with external logic that provides prioritization and select lines back into each device. The ATMCAM architecture supports external prioritization for cases where the daisy chain overhead proves unacceptable. Figure 4 shows a system in which a number of ATMCAMs are vertically cascaded.

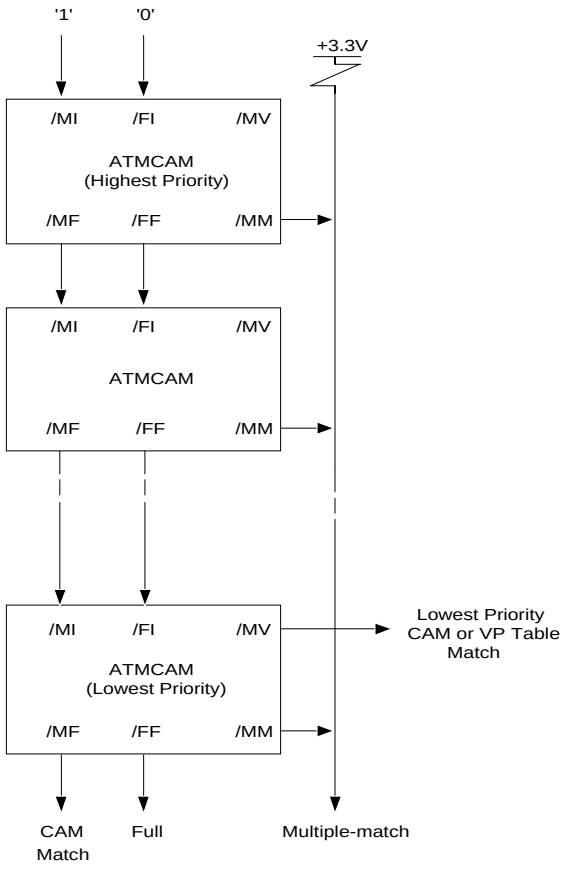


Figure 4: Vertically Cascading ATMCAMs

FULL Cascading

The Full flag is set LOW in a particular ATMCAM if the /FI line is LOW, and that device is full. During a Write cycle, the Full flag will not change until /E goes HIGH during that cycle. When the /FI line is HIGH, one or more locations are free in the higher-priority devices; therefore, when the /FI line is HIGH, whether or not that particular device is full, its /FF output will remain HIGH. This method allows the Full Flag daisy chain to recognize noncontiguous empty locations throughout the entire ATMCAM system.

The daisy chain gives System Full indication. When the device at the end of the chain has its /FF output LOW, the entire CAM system is full. The first device in the daisy chain has its /FI line tied LOW to ensure data can be written into the system.

The daisy chain also controls Write at Next Free Address cycles as well as Read Next Free Address cycles so that they work globally across the system, and not just locally in a specific device. Only the device in which the /FI line is LOW, and which is not full, will respond to the Write cycle. Therefore, deletions and insertions can be made in the memory, without the need to keep track of empty locations.

Match Cascading

The Match flag /MF will be LOW in a particular device within a vertically cascaded system when its /MI input is LOW, or when there is a match in that device. During a Comparison cycle, the Match flag will not change until /E goes HIGH during that cycle. When the /MI line is LOW, one or more locations in higher-priority devices have a match; when the /MI line is LOW, the /MF output will be forced LOW. This method allows the Match Flag daisy chain to respond to and prioritize matches throughout the entire ATMCAM system.

The daisy chaining gives a System Match indication, when the device at the end of the daisy chain has its /MF output LOW there is a match within the CAM system. The first device in the daisy chain has its /MI input tied HIGH.

The daisy chain also controls access to the device by controlling the outputs during a Read Highest-Priority Match data, or Read Status register, onto the DQ31–0 lines. The device must be selected with either /CS1, or /CS2, or the Data Select register. After a Comparison or Read/Write at Highest-Priority Match Address cycle, only the device whose /MI line is HIGH, and which has a valid match, will drive data onto DQ31–0 or onto PA3–0:AA11–0; any device that has its /MI line set LOW will have its outputs in their high-impedance state, even if it has a valid match. Therefore, Reads from and Writes to the Highest-Priority Matching address operate over the entire system; only the device in which the /MI line is HIGH and which has a match will respond to the cycle. This scheme automatically prioritizes a system of vertically cascaded devices, the highest up in the chain has the highest priority. Note however, that cycles which do not access highest-priority match data or the Status register will operate without regard to the state of the Match daisy chain.

Multiple Match Flag Daisy Chain

The Multiple Match flag, /MM is an open-drain output, and it will be pulled LOW by a particular device when its /MI input is HIGH and there is more than one match within the device, or when the /MI input is LOW and there is one match within the device. During a Comparison cycle, the Multiple Match flag will not change until /E goes HIGH during that cycle. This wired-OR output provides system level indication of the multiple match condition within a vertically cascaded system of ATMCAMs.

Match Flag Timing Overhead

There is a propagation delay for the match results to ripple down through the daisy chain. All the ATMCAMs within the system execute a Comparison cycle in parallel, so the local results are available at the end of a Comparison cycle. The local Match flags do not change during a Comparison cycle until /E goes HIGH. The logical combination of the results then propagates down the daisy chain with a delay through each stage. The compare time in each device operating in parallel is added to the ripple delay through the daisy chain. Before reading the results of a comparison from the System Match flag, the daisy chain must be given time to settle to a valid state. If there are N devices vertically cascaded in a system, and the time to get a valid output on /MF for one device is t(MF), and the propagation delay for the flag to ripple through one device from /MI valid to /MF valid is t(PD), then the time t(DC) for the daisy chain to develop a valid output condition is:

$$t(DC) = t(MF) + (N-1) * t(PD)$$

This period of time must elapse before the flagged results of the comparison are available, and before /OE is driven LOW or a Status Register Read cycle is performed.

There is a similar but shorter delay for the Full Flag daisy chain, but this only limits the rate at which back-to-back Write at Next Free Address cycles can be performed.

External Prioritization

For systems where the propagation delay associated with the Match Flag daisy chain is unacceptable, the ATMCAM supports external prioritization. Using external prioritization, each /MF output is fed to a 1-of-N prioritizing circuit whose outputs are fed back to the /CS and /OE inputs of the respective ATMCAMs. Access to the Highest-Priority Match Memory location or Status register is accomplished by only enabling the /CS to the Highest-Priority Match device based on the status of the /MF flags in the system. Likewise, access to the Highest-Priority Match device's PA3–0:AA11–0 match address result is accomplished by enabling the /OE line only to the Highest-Priority Match device.

Initialization

After power is applied to the ATMCAM the /RESET line must be pulled LOW for at least 50ns to ensure that the device establishes its correct initial operating conditions. There are control states to initialize the system-level operating conditions that can be run once the device or devices in the system have been reset after power has been applied.

Reset

The Reset condition occurs when the /RESET line is pulled LOW (Hardware reset), or when the Reset Control state is executed (Software reset). The conditions after a reset are shown in Table 2 on page 25.

The Instruction register is enabled for Software Control mode. To activate Hardware control, the appropriate value should be written to the Configuration register in two cycles from the DQ31–0 lines.

For a Hardware reset, FR25, which defines the lowest priority device, is set HIGH. This means that either FR25 must be set LOW in the lowest-priority device, or a Memory access cycle or a Compare cycle that generates a match must be executed for there to be any response when reading the PA:AA bus or the Status register.

Note: *The VP Table is not reset and must be initialized by the user prior to being enabled.*

System Initialization

Once the ATMCAM devices in the system have been reset, the system operating conditions must be set up. The ATMCAM is reset to Software Control mode, so a value must be written to the Configuration register to set the persistent operating state of the device. This first write to the devices in the system must be through Software control. The following sequence writes a new value to the Configuration register under software control:

1. Write 006H to ATMCAMs (/AV=HIGH, DQ12=LOW). The value 006H is the control state WR FR (Write to Configuration register with no mask). /AV being HIGH indicates that this is the instruction to be written to the Instruction register, and DQ12 being LOW indicates that it is a Write cycle.
2. Write XXXXXXXXH to ATMCAMs (/AV=LOW). The value XXXXXXXXH is written to the Configuration register, and if FR27–26=00 then the devices are set to operate in Hardware Control mode. /AV being LOW causes the control state to execute using the data present on the DQ31–0 lines.

If the devices in a vertically cascaded system are to be selected solely through the Device Select register, then the Page addresses must be set to unique values in each device. However, to set the Page address in each Configuration register in turn would require that each device already had a unique Page Address value. To overcome this dilemma, there are two special control states that allow the Page Address registers to be set individually in this circumstance. Once the general operating conditions have been established by broadcasting a configuration value to all the ATMCAMs in the system, the Page Address values must be set to a unique value in each device. This is done through a sequence of WR PA control states, each executed with a unique value on the DQ3–0 lines. This control state writes the DS3–0 value into the Page Address field of the Configuration register of the highest-priority empty device, and then sets the Full flag of that device to indicate full (LOW). The next WR PA will therefore be directed to the next lower-priority device within the system. The sequence continues until all Page Address values have been written. The RST FF control state is then broadcast to all devices to set the Full flags back to Empty, and the system is then ready for normal operation.

JTAG

For detailed information on JTAG testing, refer to the IEEE Standard Test Access Port and Boundary-scan Architecture IEEE Std. 1149.1-1990 and 1149.1a-1993. The ATMCAM JTAG Instruction register is 3 bits long, giving eight possible JTAG instructions. The least significant bit is clocked in first. The JTAG instructions are as follows:

JTAG Function	Instruction
EXTEST	000
RESERVED	001
RESERVED	010
RESERVED	011
IDCODE	100
INTEST	101
SAMPLE/PRELOAD	110
BYPASS	111

The ATMCAM IDCode is: X4320133H. (X is the 4-bit revision code)

BSDL files are available; check the MUSIC Semiconductors website or contact MUSIC Technical Support.

CONTROL STATE OVERVIEW

Table 1: Control State Overview

	/W = LOW	PA:AA	Scope	/W = HIGH	PA:AA	Scope
Write/Read Memory						
A11–0 [/AV = LOW]	WR aaa	aaa	AS	RD aaa	aaa	S
xxx nnn 000 000	WR [AR] {MRnnn}	aaa	AS	RD [AR]	aaa	S
xxx nnn 100 110	WR [AR]+ {MRnnn}	aaa	AS	RD [AR]+	aaa	S
xxx nnn 100 111	WR [AR]- {MRnnn}	aaa	AS	RD [AR]-	aaa	S
xxx nnn 000 001	WR [NFA] {MRnnn}	NFA	NFD	RD [HPM]; INC MA	HPMA	HPD
xxx nnn 000 010	WR [HPM] {MRnnn}	HPMA	HPD	RD [HPM]	HPMA	HPD
Write/Read Register						
xxx nnn 000 100	WR AR {MRnnn}	n/c	AS	RD AR	n/c	S
xxx xxx 000 011	NOP	n/c	n/a	RD NFA	n/c	NFD
xxx nnn 000 110	WR FR {MRnnn}	n/c	AS	RD FR	n/c	S
xxx nnn 001 000	WR DS {MRnnn}	n/c	AS	RD DS	n/c	S
xxx xxx 000 111	RESERVED	n/c	n/a	RD SR	n/c	HPD/S
xxx nnn 000 101	WR CR {MRnnn}	n/c	AS	RD CR	n/c	S
xxx nnn 001 001	WR MRnnn	n/c	AS	RD MRnnn	n/c	S
Data Move						
xxx nnn 001 100	MOV [AR],CR {MRnnn}	aaa	AS	MOV CR,[AR] {MRnnn}	aaa	AS
xxx nnn 001 101	MOV [NFA],CR {MRnnn}	NFA	NFD	RESERVED	n/c	n/a
xxx nnn 001 110	MOV [HPM],CR {MRnnn}	HPMA	HPD	MOV CR,[HPM] {MRnnn}	HPMA	HPD
Comparison						
xxx nnn 011 000	CMP CR {MRnnn}	HPMA	AS	RESERVED	n/c	n/a
xxx nnn 011 001	CMP DQ {MRnnn}	HPMA	AS	RESERVED	n/c	n/a
xxx nnn 011 010	CMPW DQ {MRnnn}	HPMA	AS	RESERVED	n/c	n/a
xxx xxx 011 011	INC MA	HPMA	HPD	RESERVED	n/c	n/a
Set Validity						
xxx xxx 100 000	SET V@[AR]	aaa	AS	RD V@[AR]	aaa	S
xxx xxx 100 001	RST V@[AR]	aaa	AS	RESERVED	n/c	n/a
xxx xxx 100 010	RST V@[HPM]	HPMA	HPD	RESERVED	n/c	n/a
xxx xxx 100 011	RST V@AML	HPMA	AS	RESERVED	n/c	n/a
Address Register Control						
xxx xxx 100 100	Inc AR	n/c	AS	RESERVED	n/c	n/a
xxx xxx 100 101	Dec AR	n/c	AS	RESERVED	n/c	n/a
VP Table Control						
xxx xxx 101 000	SET VP@[AR]	aaa	AS	RD VP@[AR]	aaa	S
xxx xxx 101 001	RST VP@[AR]	aaa	AS	RESERVED	n/c	n/a
Initialization						
xxx xxx 111 100	WR PA	n/c	NFD	RESERVED	n/c	n/a
xxx xxx 111 101	RST FF	n/c	AS	RESERVED	n/c	n/a
xxx xxx 111 111	RST	All 1s	AS	RESERVED	n/c	n/a

Key: aaa = Random access address
All 1s = All PA:AA outputs HIGH
AS = All selected devices
HPD = Highest-Priority device
HPMA = Highest-Priority Match address
n/a = Not applicable
n/c = No change
NFA = Next Free address
NFD = Highest-Priority device with a Free location
S = Selected device

The ‘Scope’ of a control state describes which devices respond in a multi-CAM system.
The ‘PA:AA’ field describes what is output on the PA3–0:AA11–0 bus as a result of the control state.
/AV is HIGH unless otherwise noted.

CONTROL STATE DESCRIPTIONS

Read/Write Memory

Control State: Direct Write at Address
Mnemonic: WR[aaa]
Binary Op Code: aaa
/W: LOW /AV: LOW PA:AA: aaa Scope: AS
Description: Writes data from the DQ31–0 bus to the location defined by the address value present on the AC11–0 bus. The write optionally can be masked by the mask register selected through the Configuration register; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. This control state provides direct random access memory writes. This control state, along with the Read cycle equivalent is the only one that uses direct addressing. It is selected by the /AV line being LOW. All other control states have the /AV line HIGH whereby the AC11–0 bus carries a control code. This control state is not available in software mode.

Control State: Direct Read at Address
Mnemonic: RD[aaa]
Binary Op Code: aaa
/W: HIGH /AV: LOW PA:AA: aaa Scope: S
Description: Reads data from the location defined by the address value present on the AC11–0 bus to the DQ31–0 bus. This control state provides direct random access memory reads. This control state, along with the Write cycle equivalent is the only one that uses direct addressing. It is selected by the /AV line being LOW. All other control states have the /AV line HIGH whereby the AC11–0 bus carries a control code. During the Read cycle, the /VB line carries the Validity Bit value of the addressed location. This control state is not available in software mode.

Control State: Indirect Write at Address
Mnemonic: WR[AR]{MRnnn}
Binary Op Code: XXX nnn 000 000
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Writes data from the DQ31–0 bus to the location defined by the contents of the Address register. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. This control state provides indirect random access memory writes.

Control State: Indirect Read at Address
Mnemonic: RD[AR]
Binary Op Code: XXX nnn 000 000
/W: HIGH /AV: HIGH PA:AA: aaa Scope: S
Description: Reads data from the location defined by the contents of the Address register to the DQ31–0 bus. This control state provides indirect random access memory reads. During the Read cycle, the /VB line carries the Validity bit value of the addressed location.

Control State: Indirect Write at Address; Increment Address Register
Mnemonic: WR[AR]+{MRnnn}
Binary Op Code: XXX nnn 100 110
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Writes data from the DQ31–0 bus to the location defined by the contents of the Address register. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. The contents of the Address register are incremented.

Control State: Indirect Read at Address; Increment Address Register
Mnemonic: RD[AR]+
Binary Op Code: XXX XXX 100 110
/W: HIGH /AV: HIGH PA:AA: aaa Scope: AS
Description: Reads data from the location defined by the contents of the Address register to the DQ31–0 bus. This control state provides indirect random access memory reads. During the Read cycle, the /VB line carries the Validity Bit value of the addressed location. The contents of the Address register are incremented.

Control State: Indirect Write at Address; Decrement Address Register
Mnemonic: WR[AR]-{MRnnn}
Binary Op Code: XXX nnn 100 111
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Writes data from the DQ31–0 bus to the location defined by the contents of the Address register. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. The contents of the Address register are decremented.

Control State: **Indirect Read at Address; Decrement Address Register**
Mnemonic: **RD[AR]**
Binary Op Code: **XXX XXX 100 111**
/W: HIGH /AV: HIGH PA:AA: aaa Scope: S
Description: Reads data from the location defined by the contents of the Address register to the DQ31–0 bus. This control state provides indirect random access memory reads. During the Read cycle, the /VB line carries the Validity Bit value of the addressed location. The contents of the Address register are decremented.

Control State: **Write at Next Free Address**
Mnemonic: **WR[NFA]{MRnnn}**
Binary Op Code: **XXX nnn 000 001**
/W: LOW /AV: HIGH PA:AA: NFA Scope: NFD
Description: Writes data from the DQ31–0 bus to the next free location in the Memory array. In a vertically cascaded system, the write will take place in the device whose /FI=LOW and /FF=HIGH, and at the highest-priority location whose Validity bit is set HIGH. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Highest-Priority Matching Location; Increment Match Address**
Mnemonic: **RD[HPM];INC MA**
Binary Op Code: **XXX XXX 000 001**
/W: HIGH /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Reads data from the location defined by the highest-priority matching location to the DQ31–0 bus. In the event that the previous Comparison cycle resulted in a mismatch, the DQ31–0 bus will remain in high impedance. The Next Highest-Priority Matching location is selected and its address appears on the PA3–0:AA11–0 lines.

Control State: **Write to Highest-Priority Matching Location**
Mnemonic: **WR[HPM]{MRnnn}**
Binary Op Code: **XXX nnn 000 010**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Writes data from the DQ31–0 bus to the highest-priority matching location in the Memory array. The validity of the location is set by the state of the /VB input, /VB=LOW: Valid, /VB=HIGH: Empty. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Highest-Priority Matching Location**
Mnemonic: **RD[HPM]**
Binary Op Code: **XXX XXX 000 010**
/W: HIGH /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Reads data from the location defined by the highest-priority matching location to the DQ31–0 bus. In the event that the previous Comparison cycle resulted in a mismatch, the DQ31–0 bus will remain in high impedance.

Register Read/Write

Control State: **Write Address Register**
Mnemonic: **WR AR{MRnnn}**
Binary Op Code: **XXX nnn 000 100**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Writes data from the DQ31–0 bus to the Address register. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Address Register**
Mnemonic: **RD AR**
Binary Op Code: **XXX XXX 000 100**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: S
Description: Reads the contents of the Address register to the DQ31–0 bus.

Control State: **No Operation**
Mnemonic: **NOP**
Binary Op Code: **XXX XXX 000 011**
/W: LOW /AV: HIGH PA:AA: n/c Scope: n/a
Description: No operation. The device performs no operation during the cycle. No existing states change.

Control State: **Read Next Free Address**
Mnemonic: **RD NFA**
Binary Op Code: **XXX XXX 000 011**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: NFD
Description: Reads the value of the Next Free address on the DQ11–0 bus. In a vertically cascaded system this will be in the device whose /FI=LOW and /FF=HIGH, and at the highest-priority location whose Validity bit is set HIGH. This value is the address of the location where a subsequent Write at Next Free Address cycle will be written. The Page address of the device value is output on DQ15–12; DQ31–16 are LOW.

Control State: **Write Configuration Register**
Mnemonic: **WR FR{MRnnn}**
Binary Op Code: **XXX nnn 000 110**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Writes data from the DQ31–0 bus to the Configuration register. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Configuration Register**
Mnemonic: **RD FR**
Binary Op Code: **XXX XXX 000 110**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: S
Description: Reads the contents of the Configuration register to the DQ31–0 bus.

Control State: **Write Device Select Register**
Mnemonic: **WR DS{MRnnn}**
Binary Op Code: **XXX nnn 001 000**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Writes data from the DQ31–0 bus to the Device Select register. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Device Select Register**
Mnemonic: **RD CR**
Binary Op Code: **XXX XXX 001 000**
/W: HIGH AV: HIGH PA:AA: n/c Scope: S
Description: Reads the contents of the Device Select register to the DQ31–0 bus.

Control State: **Read Status Register**
Mnemonic: **RD SR**
Binary Op Code: **XXX XXX 000 111**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: HPD/S
Description: Reads the contents of the Status register to the DQ31–0 bus. After a Comparison or Read/Write at Highest-Priority Matching Address cycle only the highest-priority device with a match responds to this control state; in the event of a mismatch, the lowest-priority device responds. After a random access Read or Write cycle into the Memory array, RD SR will take place in any selected device.

Control State: **Write Comparand Register**
Mnemonic: **WR CR{MRnnn}**
Binary Op Code: **XXX nnn 000 101**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Writes data from the DQ31–0 bus to the Comparand register. The write is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Read Comparand Register**
Mnemonic: **RD CR**
Binary Op Code: **XXX XXX 000 101**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: S
Description: Reads the contents of the Comparand register to the DQ31–0 bus.

Control State: **Write Mask Register**
Mnemonic: **WR MRnnn**
Binary Op Code: **XXX nnn 001 001**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Writes data from the DQ31–0 bus to the Mask register. If nnn=000 then no data is written.

Control State: **Read Mask Register**
Mnemonic: **RD MRnnn**
Binary Op Code: **XXX nnn 001 001**
/W: HIGH /AV: HIGH PA:AA: n/c Scope: S
Description: Reads the contents of the Mask register to the DQ31–0 bus. If nnn=000 then the output is undefined.

Data Move

Control State: **Move Data from Comparand Register to Memory Indirect**
Mnemonic: **MOV [AR],CR{MRnnn}**
Binary Op Code: **XXX nnn 001 100**
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Moves data from the Comparand register to the memory address defined by the contents of the Address register. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The move is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Move Data from Memory to Comparand Register Indirect**
Mnemonic: **MOV CR,[AR]{MRnnn}**
Binary Op Code: **XXX nnn 001 100**
/W: HIGH /AV: HIGH PA:AA: aaa Scope: AS
Description: Moves data from the memory address defined by the contents of the Address register to the Comparand register. The move is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. Note that the /VB line is not driven during this operation.

Control State: **Move Data from Comparand Register to Next Free Address**
Mnemonic: **MOV [NFA],CR{MRnnn}**
Binary Op Code: **XXX nnn 001 101**
/W: LOW /AV: HIGH PA:AA: NFA Scope: NFD
Description: Moves data from the Comparand Register to the Next Free address. In a vertically cascaded system, the write will take place in the device whose /FI=LOW and /FF=HIGH, and at the highest-priority location whose Validity bit is set HIGH. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The move is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Move Data from Comparand Register to Highest-Priority Matching Location**
Mnemonic: **MOV [HPM],CR{MRnnn}**
Binary Op Code: **XXX nnn 001 110**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Moves data from the Comparand register to the Highest-Priority Matching address from the previous Comparison cycle. The validity of the location is set by the state of the /VB input, /VB = LOW: Valid, /VB = HIGH: Empty. The move is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated.

Control State: **Move Data from Highest-Priority Matching Location to Comparand Register**
Mnemonic: **MOV CR,[HPM]{MRnnn}**
Binary Op Code: **XXX nnn 001 110**
/W: HIGH /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Moves data from the Highest-Priority Match address from the previous Comparison cycle to the Comparand register. The move is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits in the addressed location that correspond to LOW values in the selected mask register are updated. Note that the /VB line is not driven during this operation.

Comparison

Control State: **Compare Comparand Register with Memory Array**
Mnemonic: **CMP CR,{MRnnn}**
Binary Op Code: **XXX nnn 011 000**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: AS
Description: The Comparand register is compared with all locations in the Memory array that have their Validity bits set LOW. The comparison is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits that correspond to LOW values in the selected mask register are compared.

Control State: **Compare Data Bus with Memory Array**
Mnemonic: **CMP DQ,{MRnnn}**
Binary Op Code: **XXX nnn 011 001**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: AS
Description: The data from the DQ bus is compared with all locations in the Memory array that have their Validity bits set LOW. The comparison is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits that correspond to LOW values in the selected mask register are compared.

Control State: **Compare Data Bus with Memory Array; Write Data Bus to Comparand Register**
Mnemonic: **CMPW DQ,{MRnnn}**
Binary Op Code: **XXX nnn 011 010**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: AS
Description: The data from the DQ bus is compared with all locations in the Memory array that have their Validity bits set LOW. The data from the DQ31–0 bus is written to the Comparand register. The comparison is masked by the contents of Mask Register nnn. When nnn=000 no mask is used; when masking is selected, only bits that correspond to LOW values in the selected mask register are compared. Note that the selected mask register masks the comparison and not the write to Comparand register.

Control State: **Advance to Next Matching Location**
Mnemonic: **INC MA**
Binary Op Code: **XXX nnn 011 011**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Advances the Match address to the next matching location when the previous Comparison cycle resulted in a multiple match. The /MF flag will go HIGH when all matches have been exhausted, therefore the scheme operates in vertically cascaded systems through the priority daisy chain.

Set Validity

Control State: **Set Valid Indirect**
Mnemonic: **SET V@[AR]**
Binary Op Code: **XXX XXX 100 000**
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Set the Validity bit LOW at the location pointed to by the contents of the Address register. The location is set valid and will enter into comparisons during a Comparison cycle, and will not be written to during a Write at Next Free Address cycle.

Control State: **Read Validity Indirect**
Mnemonic: **RD V@[AR]**
Binary Op Code: **XXX XXX 100 000**
/W: HIGH /AV: HIGH PA:AA: aaa Scope: S
Description: Reads the Validity bit at the location addressed by the contents of the Address register onto DQ0. When the validity value is LOW, the location is valid; when the validity value is HIGH, the location is empty. DQ31–1 will read as logical 0s.

Control State: **Set Empty Indirect**
Mnemonic: **RST V@[AR]**
Binary Op Code: **XXX XXX 100 001**
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Set the Validity bit HIGH at the location pointed to by the contents of the Address register. The location is set empty and will not enter into comparisons during a Comparison cycle, and may be written to during a Write at Next Free Address cycle.

Control State: **Set Empty at Highest-Priority Matching Location**
Mnemonic: **RST V@[HPM]**
Binary Op Code: **XXX XXX 100 010**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: HPD
Description: Set the Validity bit HIGH at the highest-priority matching location from the previous Comparison cycle. The location is set empty and will not enter into comparisons during a Comparison cycle, and may be written to during a Write at Next Free Address cycle.

Control State: **Set Empty at All Matching Locations**
Mnemonic: **RST V@[AML]**
Binary Op Code: **XXX XXX 100 011**
/W: LOW /AV: HIGH PA:AA: HPMA Scope: AS
Description: Set the Validity bit HIGH at all matching locations from the previous Comparison cycle. The locations are set empty and will not enter into comparisons during a Comparison cycle, and will be written to during a Write at Next Free Address cycle.

Address Register Control

Control State: **Increment Address Register**
Mnemonic: **INC AR**
Binary Op Code: **XXX XXX 100 100**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Increments the value held in the Address register. Used for automatic sequencing through addresses in the Memory array.

Control State: **Decrement Address Register**
Mnemonic: **DEC AR**
Binary Op Code: **XXX XXX 100 101**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Decrements the value held in the Address register. Used for automatic sequencing through addresses in the Memory array.

VP Table Control

Control State: **Set VP Table Valid Indirect**
Mnemonic: **SET VP@[AR]**
Binary Op Code: **XXX XXX 101 000**
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Sets the VP Table bit valid (LOW) at the location pointed to by the contents of the Address register.

Control State: **Read VP Table Indirect**
Mnemonic: **RD VP@[AR]**
Binary Op Code: **XXX XXX 101 000**
/W: HIGH /AV: HIGH PA:AA: aaa Scope: S
Description: Reads the VP Table bit at the location pointed to by the contents of the Address register onto DQ0. DQ31–1 will read as logical 0s.

Control State: **Set VP Table Invalid Indirect**
Mnemonic: **RST VP@[AR]**
Binary Op Code: **XXX XXX 101 001**
/W: LOW /AV: HIGH PA:AA: aaa Scope: AS
Description: Resets the VP Table bit invalid (HIGH) at the location pointed to by the contents of the Address register.

Initialization

Control State: **Write Page Address to Highest-Priority Empty Device; Set Full**
Mnemonic: **WR PA**
Binary Op Code: **XXX XXX 111 100**
/W: LOW /AV: HIGH PA:AA: n/c Scope: NFD
Description: Writes DQ3–0 to the Page Address field of the Configuration register, and sets the /FF LOW. This control state is intended for sequential loading of Page addresses in vertically cascaded systems that do not have explicit lines controlling the /CS inputs to the individual devices.

Control State: **Reset Full Flag**
Mnemonic: **RST FF**
Binary Op Code: **XXX XXX 111 101**
/W: LOW /AV: HIGH PA:AA: n/c Scope: AS
Description: Resets /FF HIGH. Used after sequentially loading the PA fields with previous control state to set the system back to empty.

Control State: **Reset**
Mnemonic: **RST**
Binary Op Code: **XXX XXX 111 111**
/W: LOW /AV: HIGH PA:AA: All '1's Scope: AS
Description: Performs a software reset of the ATMCAM. See Table 2.

Control State: **Undefined Operations**
Mnemonic: **RESERVED**
Description: Binary Op codes that are not documented are reserved control states. The results of these control states are undefined.

Table 2: Reset Conditions

Resource			Hardware Reset	Software Reset
Memory Array			All locations set Empty	All locations set Empty
VP Table			Not reset	No Change
Comparand Register			00000000H	00000000H
Mask Registers 1–7			00000000H	00000000H
Address Register			00000000H	00000000H
Instruction Register			00000000H	No Change
Next Free Address Register			00000000H	00000000H
Device Select Register				
	DS31–9	Reserved	000000H	000000H
	DS8	SELEN	1 = Disabled	1 = Disabled
	DS7–4	Reserved	0000	0000
	DS3-0	Device Select	1111	No Change
Status Register				
	SR31–28	Flags	1111 = No Match, Not Full	1111
	SR27–26	Reserved	00	00
	SR25–24	Active Address Type	11 = Reset State	11 = Reset State
	SR23–20	Reserved	0000	0000
	SR19–16	Page Address	1111	1111
	SR15–12	Reserved	0000	0000
	SR11–0	Active Address	111111111111	111111111111
Configuration Register				
	FR31–29	Direct Write Mask Source	000 = No Mask	No Change
	FR28	Reserved	0	0
	FR27–26	Control Mode	11 = Software Control Mode	No Change
	FR25	LPC	1 = Not Low Priority CAM	No Change
	FR24	EN VP	1 = Disable VP Table	No Change
	FR23–12	VP Table Address Mask	111111111111	No Change
	FR11–8	VP Table Page Address	1111	No Change
	FR7–4	Reserved	0000	0000
	FR3–0	Page Address	1111	No Change

Table 3: Configuration Register Bit Assignments

Bit(s)	Name	Description
31:29	Direct Write Mask Source	000 = No Mask 001 = Mask Register 1 010 = Mask Register 2 011 = Mask Register 3 100 = Mask Register 4 101 = Mask Register 5 110 = Mask Register 6 111 = Mask Register 7
28	Reserved	Set to 0
27:26	Control Mode	00 = Hardware Control Mode 01 = Reserved 10 = Reserved 11 = Software Control Mode. (If /AV = 1, access Status Register.)
25	LPC	0 = Low priority CAM 1 = Not low priority CAM
24	EN VP	0 = Enable VP table 1 = Disable VP table
23:12	VP Table Address Mask	VP Table Address Mask value
11:8	VP Table Page Address	VP Table Page Address value
7:4	Reserved	Set to 0
3:0	Page Address PA3-0	Page Address value

Table 4: Status Register Bit Assignments

Bit(s)	Name	Description
31	/MV	0 = Match in CAM or VP table 1 = No match in CAM or VP table
30	/MF	0 = Match in CAM 1 = No match in CAM
29	/MM	0 = Multiple match in CAM 1 = No multiple match in CAM
28	/FF	0 = Full 1 = Not full
27:26	Reserved	Set to 0
25:24	Active Address Type	00 = Match address 01 = Memory access 10 = VP table address 11 = Reset state
23:20	Reserved	Set to 0
19:16	Page Address PA3-0	Page Address
15:12	Reserved	Set to 0
11:0	Active Address A11-0	Active Address

Table 5: Next Free Register Bit Assignments

Bit(s)	Name	Description
31:20	Reserved	Set to 0
19:16	Page Address PA3-0	Page Address
15:12	Reserved	Set to 0
11:0	Next Free Address NF11-0	Next Free Address

Table 6: Device Select Register Bit Assignments

Bit(s)	Name	Description
31:9	Reserved	Set to 0
8	SELEN	0 = Enable Select 1 = Disable Select
7:4	Reserved	Set to 0
3:0	Device Select DS3-0	Device Select when PA3-0 = DS3-0 and SELEN = 0

ELECTRICAL

Absolute Maximum Ratings

Supply Voltage	-0.5 to 4.6 Volts
Voltage on all other pins	-0.5 to VDD +0.5 Volts (-2 Volts for 10 ns, measured at the 50% point)
Temperature under bias	-55° C to +125° C
Storage Temperature	-55° C to +125° C
DC Output Current	20 mA (per output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages referenced to GND.

Operating Conditions

Voltages referenced to GND at the device pin.

Symbol	Parameter		Min.	Typical	Max.	Units	Notes
V_{DD}	Operating supply voltage		3.0	3.3	3.6	Volts	
V_{IH}	Input voltage logic 1		2.0		V_{DD} + 0.3	Volts	
V_{IL}	Input voltage logic 0		-0.3		0.8	Volts	1, 2
T_A	Ambient operating temperature	Comercial	0		70	° C	Still air
		Industrial	-40		85	° C	

Electrical Characteristics

Symbol	Parameter		Min.	Typical	Max.	Units	Notes
I_{DD}	Average power supply current	-70		115	160	mA	$t_{ELEL} = t_{ELEL}$ (min.); 10
		-90		90	140		
		-12		70	120		
$I_{DD(SB)}$	Stand-by power supply current				7	mA	/E = HIGH
V_{OH}	Output voltage logic 1		2.4			Volts	I_{OH} = -2.0 mA
V_{OL}	Output voltage logic 0				0.4	Volts	I_{OL} = 4.0 mA
I_{IZ}	Input leakage current	Others	-2		2	µA	$GND \le V_{IN} \le V_{DD}$
		Internal Pull-Ups	6	9	15	Kohms	V_{IN} = 0 V; 11
I_{OZ}	Output leakage current		-10		10	µA	$GND \le V_{OUT} \le V_{DD}$ DQ_N = High -Z

Capacitance

Symbol	Parameter	Max.	Units	Notes
C_{IN}	Input capacitance	6	pF	f = 1 MHz, V_{IN} = 0V
C_{OUT}	Output capacitance	7	pF	f = 1 MHz, V_{OUT} = 0V

AC Test Conditions

Table 7: AC Test Conditions

Input Signal Transitions	0.0 Volts to 3.0 Volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 Volts
Output Timing Reference Level	1.5 Volts

Switching Test Figures

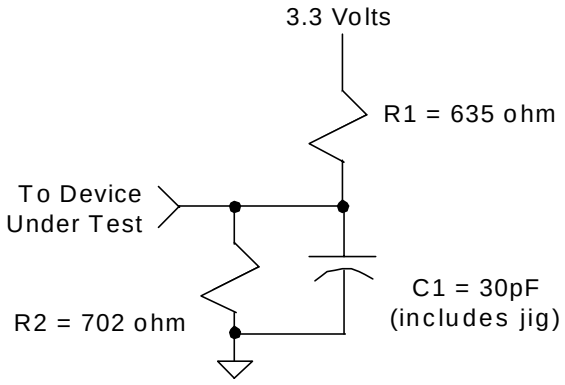


Figure 5: AC Test Load A

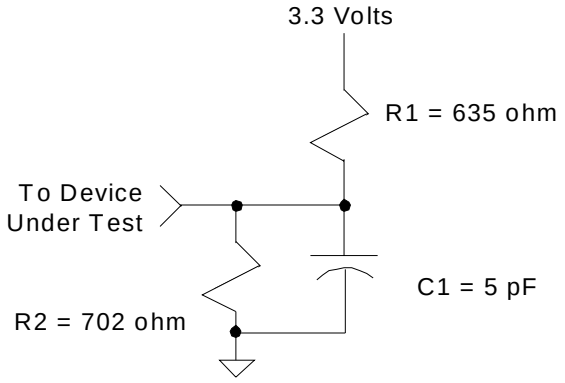


Figure 6: AC Test Load B

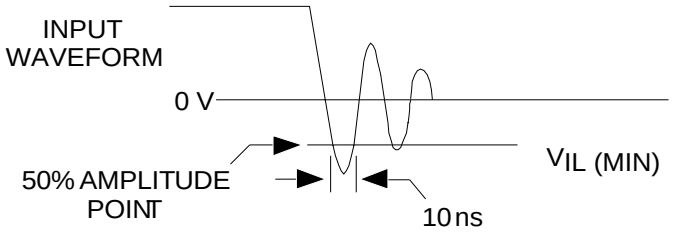


Figure 7: Input Signal Waveform

Switching Characteristics

				-70		-90		-12		
No	**Symbol**	**Parameter (all times in nanoseconds)**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Notes**
1a	tELEL	Chip Enable Cycle Time (Short Cycle)		50		50		75		3
1b	tELEL	Chip Enable Cycle Time (Compare Cycle)		70		90		120		4
2a	tELEH	Chip Enable LOW Pulse Width (Short Cycle)		40		40		55		3
2b	tELEH	Chip Enable LOW Pulse Width (Compare Cycle)		60		75		90		4
3	tEHEL	Chip Enable HIGH Pulse Width		10		10		10		
4	tCVEL	Control Input to Chip Enable LOW Setup Time		5		8		10		5
5	tELCX	Control Input to Chip Enable LOW Hold Time		3		3		5		5
6	tELQX	Chip Enable LOW to Outputs Active		5		5		5		6
7	tELQV	Chip Enable LOW to Outputs Valid	Register		40		40		50	6
			Memory		50		70		80	6
8	tEHQZ	Chip Enable HIGH to Outputs High-Z		2	10	2	10	2	15	7
9	tDVEL	Data to Chip Enable LOW Setup Time		3		3		5		6
10	tELDX	Data from Chip Enable LOW Hold Time		3		3		5		
11	tFIVEL	Full In Valid to Chip Enable LOW Setup Time		0		0		3		
12	tFIVFFV	Full In Valid to Full Flag Valid			8		9		12	
13	tEHFFV	Chip Enable HIGH to Full Flag Valid			16		16		25	
14	tEHQX	Chip Enable HIGH to Output Change		2		2		2		
15	tEHQV	Chip Enable HIGH to Output Valid			22		25		30	
16	tMIVEL	Match In Valid to Chip Enable LOW Setup		8		10		12		
17	tEHMX	Chip Enable HIGH to Match Flag Change		2		2		2		
18	tEHMV	Chip Enable HIGH to Match Flag Valid			17		20		25	
19	tMIVMV	Match In Valid to Match Flag Valid	/MF, /MV		8		9		12	
			/MM		10		10		12	
20	tOEHQZ	Output Enable HIGH to Outputs High-Z		2	10	2	10	2	15	
21	tOELQV2	Output Enable LOW to Match Address Outputs Valid			12		14		16	
22	tMIVOEL	Match in Valid to Output Enable LOW		3		3		4		
23	tFIVOEL	Full in Valid to Output Enable LOW		3		3		4		
24	tEHRSTL	Chip Enable HIGH to Reset LOW		20		20		25		
25	tRSTLRSTH	Reset Pulse Width		50		50		70		8
26	tRSTHEL	Reset HIGH to Chip Enable LOW		20		20		25		
27	tTIVTCLKH	Test Input Valid to TCLK HIGH Setup Time		20		20		25		9
28	tTCLKHTIX	TCLK HIGH to Test Input Hold Time		20		20		25		9
29	tTCLKLTDOX	TCLK LOW to TDO Change		2	10	2	10	2	15	
30	tTCLKLTDOV	TCLK LOW to TDO Valid			20		20		25	
31	tTCLKLTDOZ	TCLK LOW to TDO High-Z		20		20		25		

Notes:

1. *-1.0V for a duration of 10ns measured from the 50% amplitude points for input-only lines.*
2. *Common I/O lines are clamped so that transients cannot fall below -0.5V.*
3. *Applies to all cycle types except Compare cycles and Memory Read cycles.*
4. *Applies to Compare cycles.*
5. *Control signals are /CS1, /CS2, /W, /AV, and AC11–0.*
6. *With loads specified in Figure 5.*
7. *With loads specified in Figure 6.*
8. */E should be HIGH during /RESET active to ensure proper device defaults.*
9. *Test inputs are the TDI and TMS signals.*
10. *With output and I/O pins unloaded.*
11. *Pins with internal pull-ups are /RESET, TCLK, TMS, TDI, and /TRST.*

TIMING DIAGRAMS

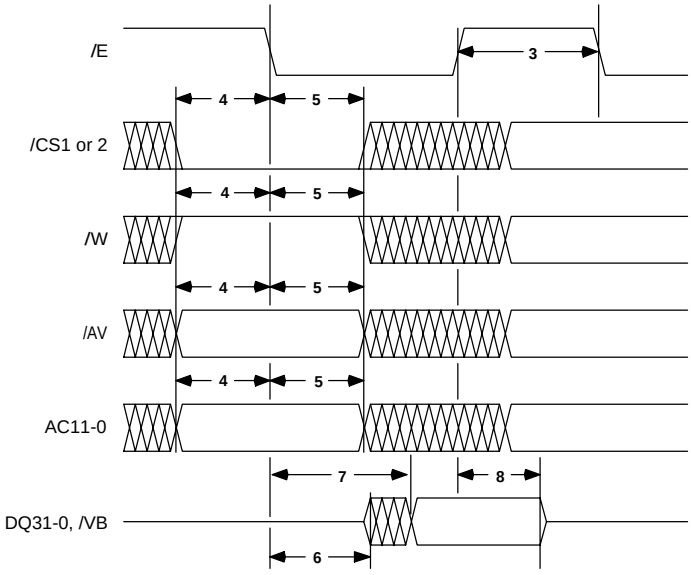


Figure 8: Read Cycle

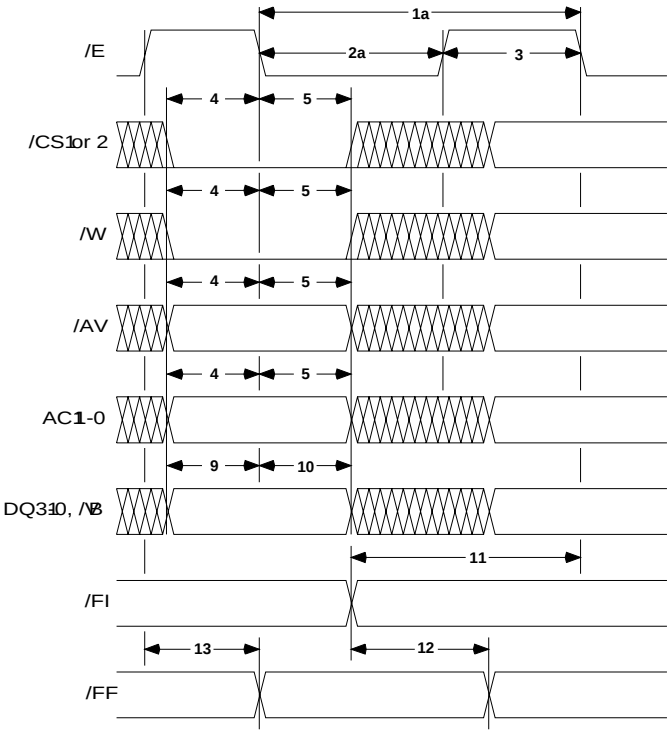


Figure 9: Write Cycle

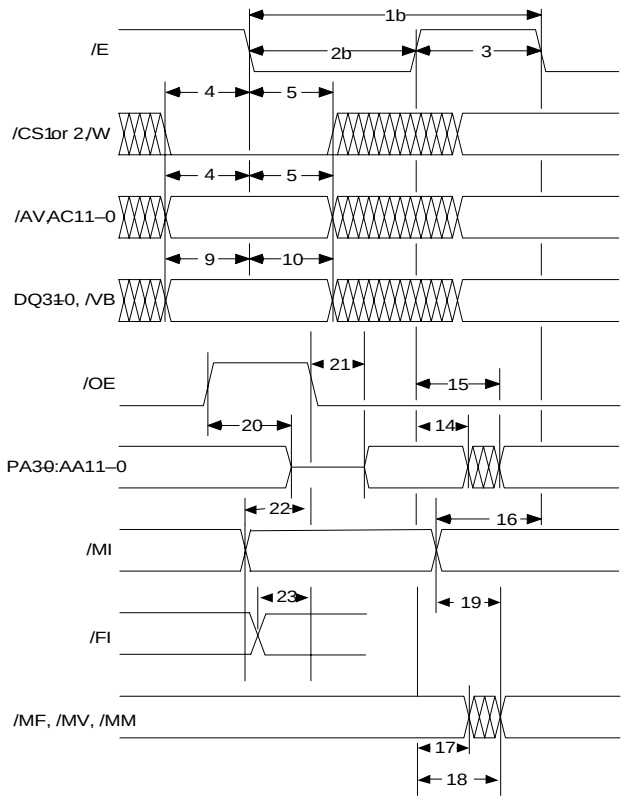


Figure 10: Compare Cycle

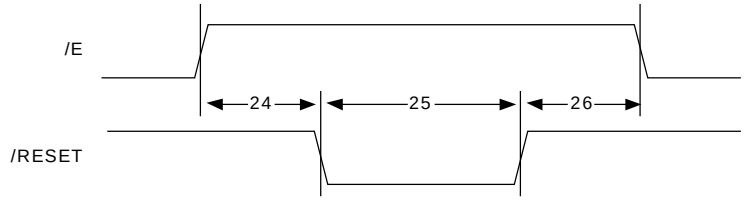


Figure 11: Reset Cycle

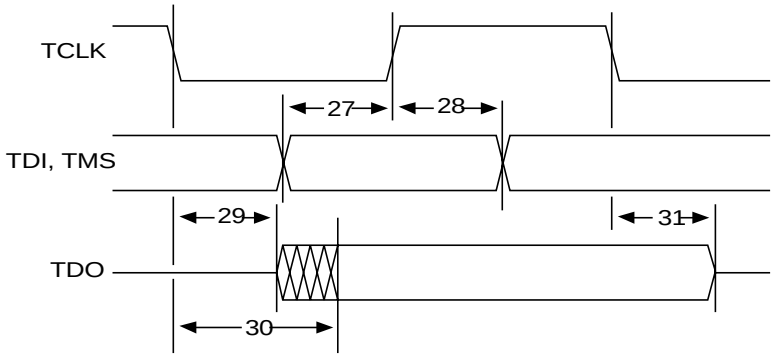
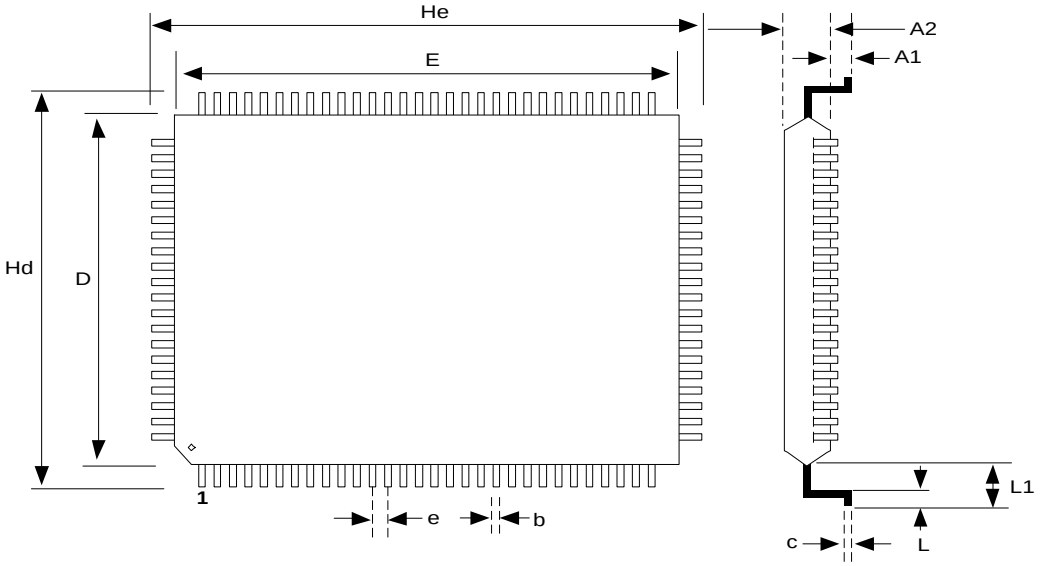


Figure 12: JTAG Test Cycle

ORDERING INFORMATION

Part Number	Cycle Time	Package	Temperature	Voltage
MU9C4320L-70TDC	70ns	100-PIN TQFP	0–70° C	3.3 ± 0.3V
MU9C4320L-90TDC	90ns	100-PIN TQFP	0–70° C	3.3 ± 0.3V
MU9C4320L-12TDC	120ns	100-PIN TQFP	0–70° C	3.3 ± 0.3V
MU9C4320L-70TDI	70ns	100-PIN TQFP	-40–85° C	3.3 ± 0.3V
MU9C4320L-90TDI	90ns	100-PIN TQFP	-40–85° C	3.3 ± 0.3V
MU9C4320L-12TDI	120ns	100-PIN TQFP	-40–85° C	3.3 ± 0.3V

PACKAGE



100-pin TQFP	Dim. A1	Dim. A2	Dim. b	Dim. c	Dim. D	Dim. E	Dim. e	Dim. Hd	Dim. He	Dim. L1	Dim. L
Min.	0.05	1.35	0.22	0.09	13.90	19.90	0.65 nom	15.90	21.90	1.0 nom	0.45
Max.	0.15	1.45	0.38	0.20	14.10	20.10		16.10	22.10		0.75

MUSIC Semiconductors' agent or distributor:

http://www.music-ic.com
email: info@music-ic.com

Worldwide Headquarters
MUSIC Semiconductors
2290 N. First St., Suite 201
San Jose, CA 95131
USA
Tel: 408 232-9060
Fax: 408 232-9201
USA Only: 800 933-1550 Tech Support
888 226-6874 Product Info

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549-1480
Fax: +63 49 549-1024
Sales Tel/Fax: +632 723-6215

European Headquarters
MUSIC Semiconductors
P. O. Box 184
6470 ED Eygelshoven
The Netherlands
Tel: +31 43 455-2675
Fax: +31 43 455-1573