Ordering number : EN*6145

Bi-CMOS IC

LV2151V

2.0 GHz PLL Frequency Synthesizer IC

Preliminary

Overview

The SANYO LV2151V is a 2.0 GHz PLL frequency synthesizer IC that features low-voltage operation and low current drain and is suitable for CATV, DAB, and mobile phone systems.

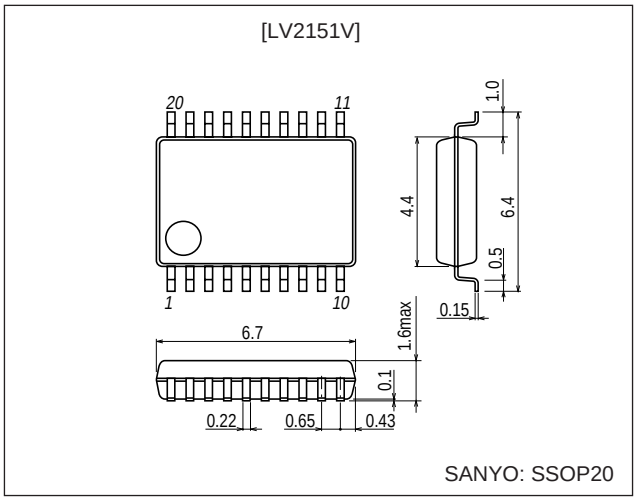
Features

- A wide range of operating frequency from 0.2 to 2.0 GHz
- I²C bus/ 3-wire bus selective. (For I²C bus WRITE mode only)
- Includes three ports for band switch
- Includes unlock detect indicator.
- Battery saving mode
- 2.7V to 3.5 V operation
- Small package 20-pin SSOP (Lead pitch 0.65mm)

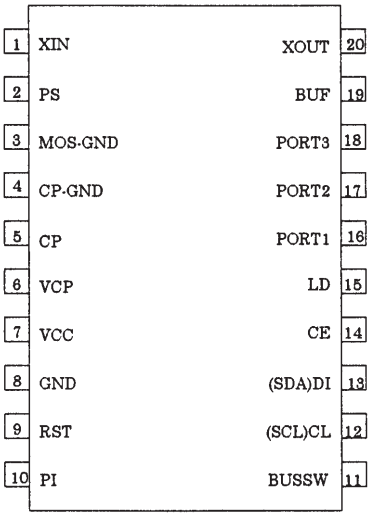
Package Dimensions

unit: mm

3179A-SSOP20



Pin Assignment



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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Pin	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}, VCP		4.5	V
Maximum input voltage	Vin max	SCL(CL), SDA(DI) CE, PS, RST, BUSSW		–0.3 to V_{CC} + 0.3	V
Maximum output voltage	Vout max	LD, PORT1 to 3, SDA(DI)		–0.3 to V_{CC} + 0.3	V
Maximum output current1	I_{OUT} max1	PORT1 to 3, SDA(DI)		4	mA
Maximum output current2	I_{OUT} max2	LD		0.7	mA
Allowable power dissipation	Pd max		Ta ≤ 85°C	50	mW
Operating temperature	Topr			–30 to +85	°C
Storage temperature	Tstg			–50 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Pin	Ratings			Unit
			min	typ	max	
Recommended power supply voltage	V_{CC}	V_{CC}, VCP		3.0		V
Operating voltage range	V_{CCOP}	V_{CC}, VCP	2.7		3.5	V

Allowable Operating Ranges at Ta = –30 to +85°C

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{CC}	V_{CC}, VCP		2.7		3.5	V
High-level input voltage	V_{IH}	SCL(CL), SDA(DI), CE, PS, RST, BUSSW		V_{CC}*0.7		V_{CC}	V
Low-level input voltage	V_{IL}	SCL(CL), SDA(DI), CE, PS, RST, BUSSW		0		0.6	V
Input frequency	fin(1)	XIN	AC Coupled	4		22	MHz
	fin(2)	PI	*	0.2		2.0	GHz
Input amplitude	Vin(1)	XIN	AC Coupled	–12		10	dBm
	Vin(2)	PI	*	–12		0	dBm
Guaranteed crystal oscillation	Xtal	XIN, XOUT		4		22	MHz

Note: *50 Ω terminate (0 dBm = 0.224 Vrms)

Electrical Characteristics at Ta = 25°C, V_{CC} = 3.0 V

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Low-level output voltage1	V_OL1	LD	I_O = 0.5 mA			0.4	V
Low-level output voltage2	V_OL2	SDA(DI), PORT1 to 3	I_O = 3.0 mA			0.4	V
Output off leak current	I OFF	LD, PORT1 to 3	V_O = 3.0 V			1	µA
CP Output off leak current	I OFCP	CP	V_O = 1.5 V			100	nA
CP output current	Icp	CP	V_O = 1.5 V		±6.5		mA
High-level input current1	IH1	SCL(CL), SDA(DI), CE, PS, RST, BUSSW	Vi = 3.0 V			5	µA
High-level input current2	IH2	XIN			3		µA
Low-level input current1	IL1	SCL(CL), SDA(DI), CE, PS, RST, BUSSW	Vi = 0 V			5	µA
Low-level input current2	IL2	XIN			3		µA
Supply current	Icco	V_{CC} + VCP	*1		7.0		mA
Standby current	Isb	No signal input	Power saving mode		0.4		mA

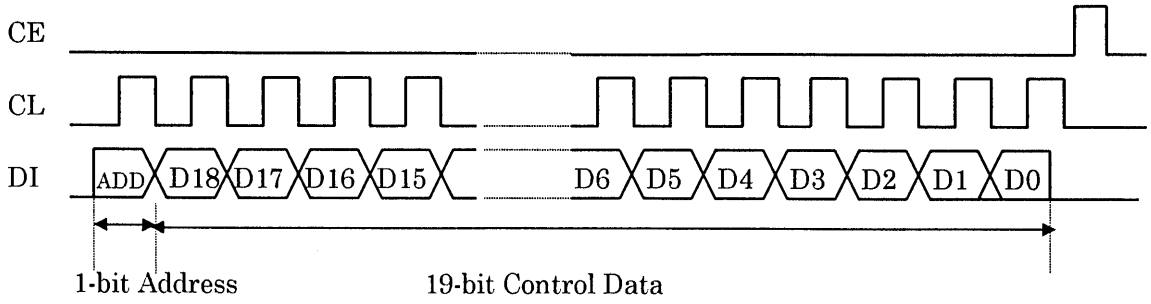
Note: *PI = 2000 MHz, Vpi = 0 dBm, RI = 19.2 MHz, Vri = 0 dBm
Other input pins = 0 V, I/O pins = open, CP off, output pins = high

Pin Descriptions

Pin	Symbol	I/O	Description
1 20	XIN XOUT	CMOS input	Crystal oscillator connection pins.
2	PS	CMOS input with a pull-down resistor built in.	Power saving switch. "Open or Low": Power saving mode "High": Active mode
3	V_{SS}		Ground pin for logic system
4	CP-GND		Ground pin for charge pump. (Fixed current output)
5	CP	BIP output	Charge pump output. (Fixed current output)
6	VCP		V_{CC} supply for charge pump.
7	V_{CC}		V_{CC} supply. (Except charge pump circuit)
8	GND		Ground pin for RF block.
9	RST	CMOS input with a pull-up resistor built in.	Reset pin for I²C bus. Connect capacitor to GND. "Open or High" Release "Low" Reset
10	PI	Bipolar input	Comparator signal input. VCO output must be AC coupled to input.
11	BUSSW	CMOS input with a pull-up resistor built in.	Serial data select input. "Open or High" I²C bus "Low" 3-wire bus
12 13 14	SCL(CL) SDA(DI) CE	CMOS input	Data input pins CE is used as an address selector pin if I²C bus is used.
15	LD	NPN transistor open collector output	PLL unlock detector output pin.
16 17 18	PORT1 PORT2 PORT3		Output port pins for band switch.
19	BUF	Bipolar output	Buffer output pin for crystal oscillator.

Data Format

(1) 3-Wire Bus (BUSSW pin set low.)



1. Programmable Counter and Test Mode
   ADD latch address data must be set to 1.

(MSB) (LSB)

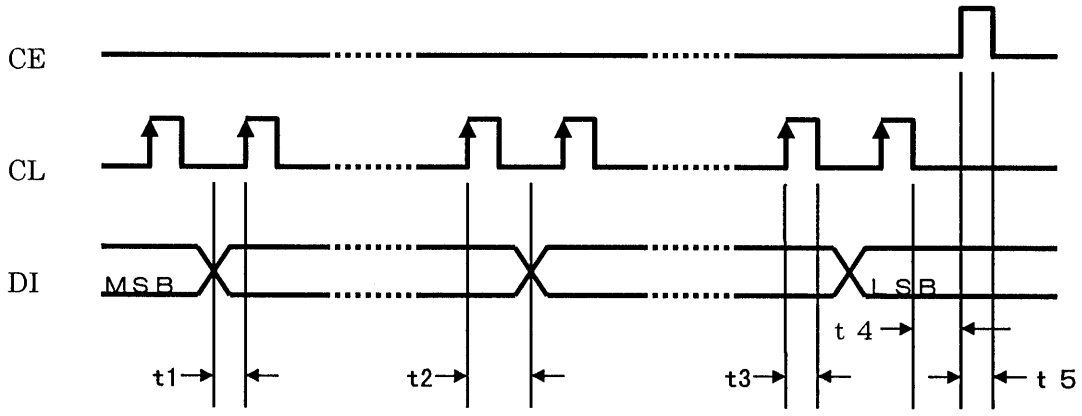
ADD	TS1	TS0	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

2. Reference Counter and Other Control
   ADD latch address data must be set to 0

(MSB) (LSB)

ADD	CPD	ULD	UE1	UE0	PORT 3	PORT 2	PORT 1	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

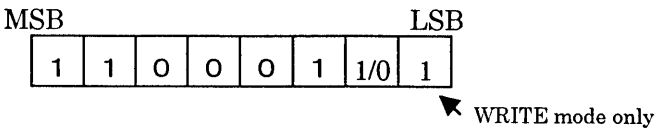
Serial Data Timing



t1, t2, t3, t4, t5 ≥ 100 ns

(2) I²C bus BUSSW pin set open or high.

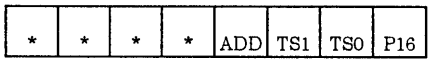
Address Byte



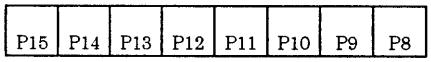
CE pin is high when the data is set to 1.
CE pin is low when the data is set to 0.

1. Programmable Counter and Testing Mode

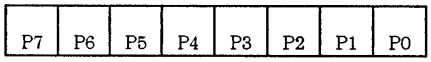
Data1 Byte



Data2 Byte

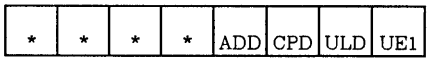


Data3 Byte

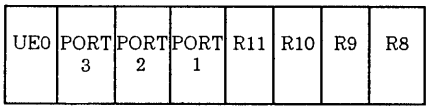


2. Reference Counter and Other Control

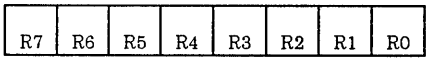
Data1 Byte



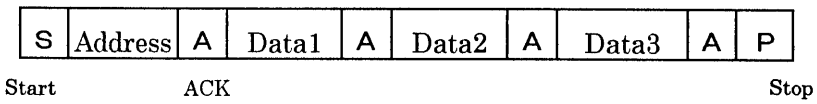
Data2 Byte



Data3 Byte



Receiving Data Diagrams



Serial Data Description

(1) Programmable Counter and Test Mode

Bit "ADD(Latch Address Data)" = 1

(MSB) (LSB)

ADD	TS1	TS0	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

1. Programmable Counter
   Bits P0 to P16 determine programmable divider ratios. Binary value with P0 as the LSB.
   The division ratio can be set in the range of 4032 to 131071.
   Ex. Settable division ratio factor is 8192

ADD	TS1	TS0	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Test Mode
   TS0 and TS1 are testing bits. These bits must normally be set to 0.

(2) Reference Counter and Other Control

ADD is the latch address bit. This bit must be set to 0.

(MSB) (LSB)

ADD	CPD	ULD	UE1	UE0	PORT 3	PORT 2	PORT 1	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

1. Reference Counter
   Bits R0 to R11 determine programmable divider ratios. Binary value with R0 as the LSB.
   The division ratio can be set in the range of 20 to 4095.
   Ex. Settable division ratio factor is 2048 ("*" = Don't care)

ADD	CPD	ULD	UE1	UE0	PORT	PORT	PORT	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
0	*	*	*	*	*	*	*	1	0	0	0	0	0	0	0	0	0	0	0

2. Phase Comparator Output Control
   Bit CPD is phase comparator polarity switching data.

CPD	Phase comparator polarity
0	(1) Shown Fig.1
1	(2) Shown Fig.1

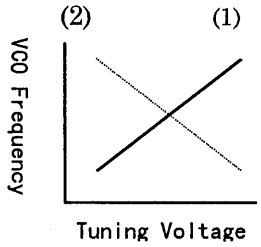


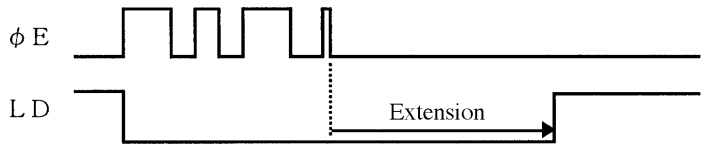
Fig.1

3. Unlock Detection Control
   ULD is used to control the signal length which determines whether or not the PLL is locked. PLL is determined as unlocked if a phase error signal longer than that in the table below is detected.

ULD	Thresholds	fXIN = 10.24 MHz
0	±4/fXIN	390 ns
1	±8/fXIN	780 ns

4. Unlock Output Signal Extension Control
   UE0 and UE1 are used to control the extension of LD signal detected in the unlock detector circuit.

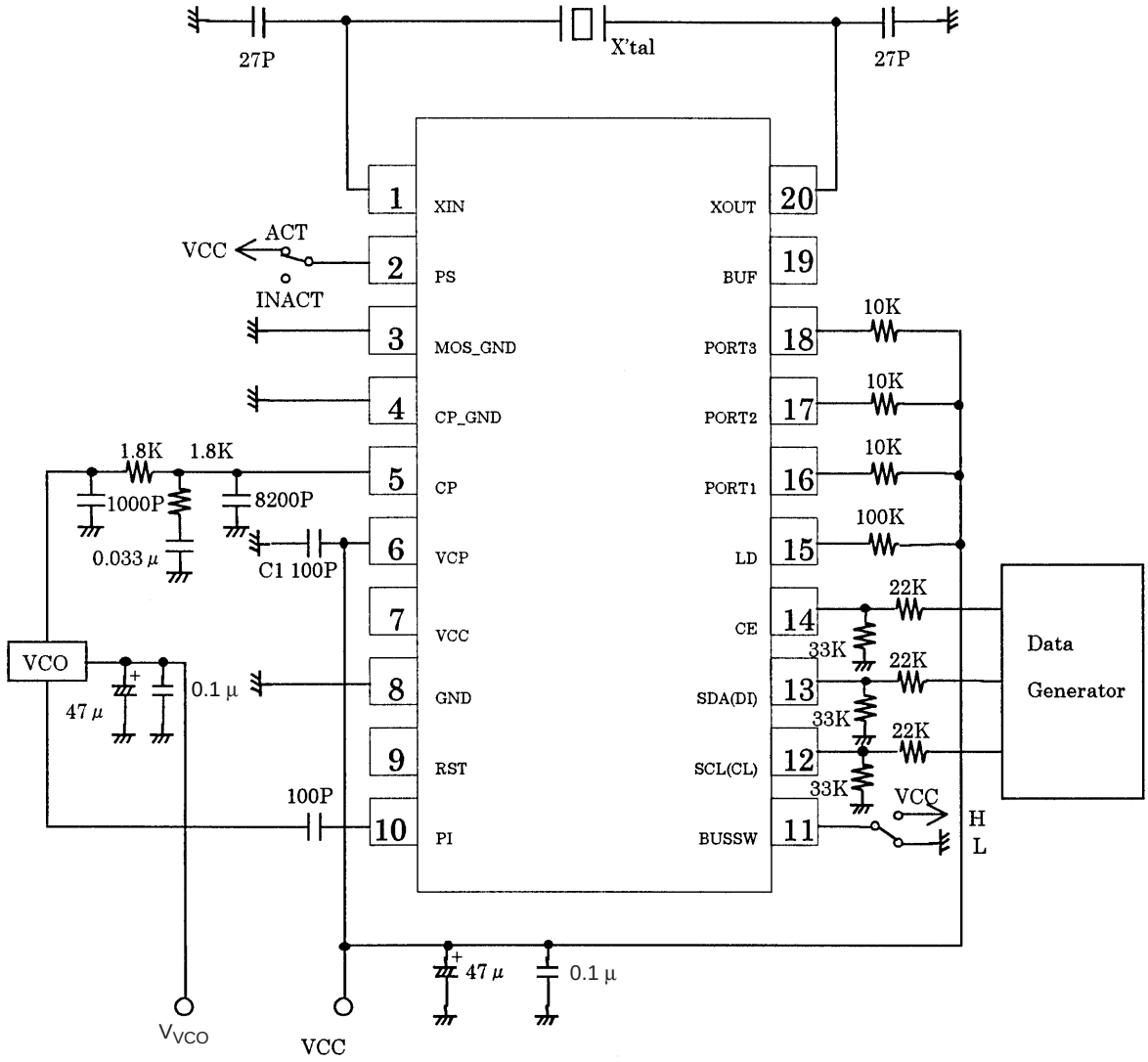
UE1	UE0	Extension Time	fref = 50 k
0	0	4*(1/fref)	80 µs
0	1	8*(1/fref)	160 µs
1	0	16*(1/fref)	320 µs
1	1	32*(1/fref)	640 µs



5. Band Switching Output Ports
   PORT1 to PORT3 are used to switch the outputs for pin16 to pin18, respectively. The pins go to high when the data is set to 0, and go to low when set to 1.

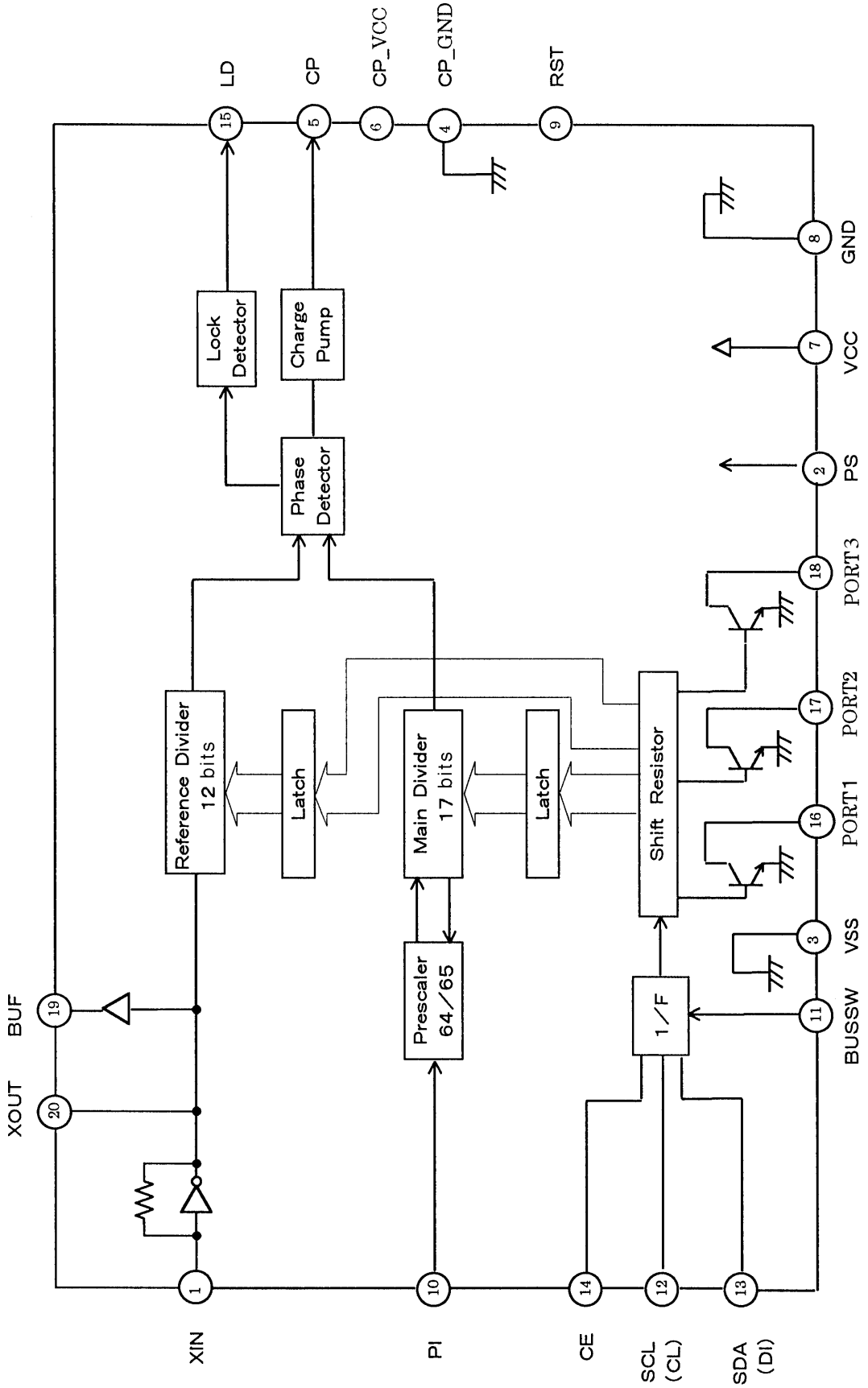
PORT*	Output
0	High
1	Low

LV2151V Evaluation Circuit



Unit (resistance: Ω, capacitance:F)

Block Diagram



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