32MBIT (2MBIT × 16) PAGE MODE DUAL WORK FLASH MEMORY

1. GENERAL DESCRIPTION

The W28F321, a 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, cost efficiency, nonvolatile read/write storage solution for a wide range of applications. The product can be operated at V_{DD} = 2.7V to 3.6V and V_{PP} = 1.65V to 3.6V or 11.7V to 12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The W28F321 provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time-consuming wait states. Furthermore, its configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program. Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

2. FEATURES

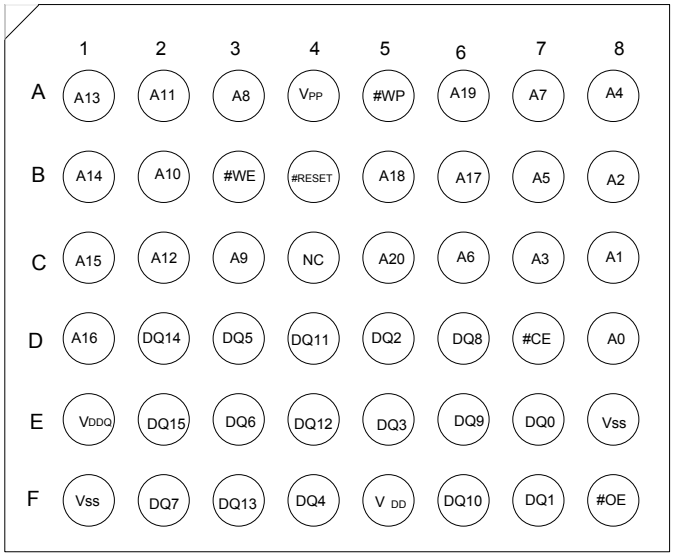
- 32M Density with 16 Bit I/O Interface
- High-Performance Reads
  - 70/25 nS 8-Word Page Mode
- Configurative 4-Plane Dual Work
  - Flexible Partitioning
  - Read operations during Block Erase or (Page Buffer) Program
  - Status Register for Each Partition
- Low Power Operation
  - 2.7V Read and Write Operations
  - V_{DDQ} for Input/Output Power Supply Isolation
  - Automatic Power Savings Mode Reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
  - 5 μS Typical Erase/Program Suspends
- OTP (One Time Program) Block
  - 4-Word Factory-Programmed Area
  - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
  - 16-Word Page Buffer
  - 5 μS/ Word (Typ.) at 12V V_{PP}
- Operating Temperature
  - -40°C to +85°C
- CMOS Process (P-type silicon substrate)
- Flexible Blocking Architecture
  - Eight 4k-word Parameter Blocks
  - Sixty-three 32k-word Main Blocks
  - Top or Bottom Parameter Location
- Enhanced Data Protection Features
  - Individual Block Lock and Block Lock-Down with Zero-Latency
  - All blocks are locked at power-up or device reset
  - Absolute Protection with $V_{PP} \le V_{PPLK}$

– Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions

- Automated Erase/Program Algorithms
  – 3.0V Low-Power 11 μS/ Word (Typ.) Programming
  – 12V No Glue Logic 9 μS/ Word (Typ.) Production Programming and 0.5s Erase (Typ.)
- Cross-Compatible Command Support
  – Common Flash Interface (CFI)
  – Basic Command Set
- Extended Cycling Capability
  – Minimum 100,000 Block Erase Cycles
- Chip-Size Packaging
  – 0.75 mm pitch 48-Ball TFBGA(7mm x 7mm)
- ETOX™ Flash Technology
- No designed or rated as radiation hardened

** ETOX is a trademark of Intel Corporation.*

3. PIN CONFIGURATION



0.75mm pitch
48-Ball TFBGA
Pinout

7 x 7 mm
TOP VIEW

Figure 1. 0.75 mm pitch TFBGA 48-Ball Pinout

Table 1. Pin Descriptions

SYMBOL	TYPE	NAME AND FUNCTION
A0 – A20	INPUT	**ADDRESS INPUTS**: Inputs for addresses. 32M: A0 – A20.
DQ0 – DQ15	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS**: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
#CE	INPUT	**CHIP ENABLE**: Activates the device's control logic, input buffers, decoders and sense amplifiers. #CE-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
#RESET	INPUT	**RESET**: When low (V_{IL}), #RESET resets internal automation and inhibits write operations, which provides data protection. #RESET-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. #RESET must be low during power-up/down.
#OE	INPUT	**OUTPUT ENABLE**: Gates the device's outputs during a read cycle.
#WE	INPUT	**WRITE ENABLE**: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of #CE or #WE (whichever goes high first).
#WP	INPUT	**WRITE PROTECT**: When #WP is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When #WP is V_{IH}, lock-down is disabled.
V_{PP}	INPUT	**MONITORING POWER SUPPLY VOLTAGE:** V_{PP} is not used for power supply pin. With $V_{PP} \le V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.
V_{DD}	SUPPLY	**DEVICE POWER SUPPLY (2.7V to 3.6V)**: With $V_{DD} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{DD} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{DDQ}	SUPPLY	**INPUT/OUTPUT POWER SUPPLY (2.7V to 3.6V):** Power supply for all input/output pins.
V_{SS}	SUPPLY	**GROUND**: Do not float any ground pins.
NC		**NO CONNECT**: Lead is not internally connected; it may be driven or floated.

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Table 2. Simultaneous Operation Modes Allowed with Four Planes(1,2)

	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
IF ONE PARTITION IS	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

Notes:

1. "X" denotes the operation available.

2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
   Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (PARAMETER PLANE)	70	4K-WORD	1FF000h - 1FFFFFh
	69	4K-WORD	1FE000h - 1FEFFFh
	68	4K-WORD	1FD000h - 1FDFFFh
	67	4K-WORD	1FC000h - 1FCFFFh
	66	4K-WORD	1FB000h - 1FBFFFh
	65	4K-WORD	1FA000h - 1FAFFFh
	64	4K-WORD	1F9000h - 1F9FFFh
	63	4K-WORD	1F8000h - 1F8FFFh
	62	32K-WORD	1F0000h - 1F7FFFh
	61	32K-WORD	1E8000h - 1EFFFFh
	60	32K-WORD	1E0000h - 1E7FFFh
	59	32K-WORD	1D8000h - 1DFFFFh
	58	32K-WORD	1D0000h - 1D7FFFh
	57	32K-WORD	1C8000h - 1CFFFFh
	56	32K-WORD	1C0000h - 1C7FFFh
	55	32K-WORD	1B8000h - 1BFFFFh
	54	32K-WORD	1B0000h - 1B7FFFh
	53	32K-WORD	1A8000h - 1AFFFFh
	52	32K-WORD	1A0000h - 1A7FFFh
	51	32K-WORD	198000h - 19FFFFh
	50	32K-WORD	190000h - 197FFFh
	49	32K-WORD	188000h - 18FFFFh
	48	32K-WORD	180000h - 187FFFh
PLANE2 (UNIFORM PLANE)	47	32K-WORD	178000h - 17FFFFh
	46	32K-WORD	170000h - 177FFFh
	45	32K-WORD	168000h - 16FFFFh
	44	32K-WORD	160000h - 167FFFh
	43	32K-WORD	158000h - 15FFFFh
	42	32K-WORD	150000h - 157FFFh
	41	32K-WORD	148000h - 14FFFFh
	40	32K-WORD	140000h - 147FFFh
	39	32K-WORD	138000h - 13FFFFh
	38	32K-WORD	130000h - 137FFFh
	37	32K-WORD	128000h - 12FFFFh
	36	32K-WORD	120000h - 127FFFh
	35	32K-WORD	118000h - 11FFFFh
	34	32K-WORD	110000h - 117FFFh
	33	32K-WORD	108000h - 10FFFFh
	32	32K-WORD	100000h - 107FFFh

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	31	32K-WORD	0F8000h - 0FFFFFh
	30	32K-WORD	0F0000h - 0F7FFFh
	29	32K-WORD	0E8000h - 0EFFFFh
	28	32K-WORD	0E0000h - 0E7FFFh
	27	32K-WORD	0D8000h - 0DFFFFh
	26	32K-WORD	0D0000h - 0D7FFFh
	25	32K-WORD	0C8000h - 0CFFFFh
	24	32K-WORD	0C0000h - 0C7FFFh
	23	32K-WORD	0B8000h - 0BFFFFh
	22	32K-WORD	0B0000h - 0B7FFFh
	21	32K-WORD	0A8000h - 0AFFFFh
	20	32K-WORD	0A0000h - 0A7FFFh
	19	32K-WORD	098000h - 09FFFFh
	18	32K-WORD	090000h - 097FFFh
	17	32K-WORD	088000h - 08FFFFh
	16	32K-WORD	080000h - 087FFFh
PLANE0 (UNIFORM PLANE)	15	32K-WORD	078000h - 07FFFFh
	14	32K-WORD	070000h - 077FFFh
	13	32K-WORD	068000h - 06FFFFh
	12	32K-WORD	060000h - 067FFFh
	11	32K-WORD	058000h - 05FFFFh
	10	32K-WORD	050000h - 057FFFh
	9	32K-WORD	048000h - 04FFFFh
	8	32K-WORD	040000h - 047FFFh
	7	32K-WORD	038000h - 03FFFFh
	6	32K-WORD	030000h - 037FFFh
	5	32K-WORD	028000h - 02FFFFh
	4	32K-WORD	020000h - 027FFFh
	3	32K-WORD	018000h - 01FFFFh
	2	32K-WORD	010000h - 017FFFh
	1	32K-WORD	008000h - 00FFFFh
	0	32K-WORD	000000h - 007FFFh

Figure 2.1 Top Parameter Memory Map

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
PLANE2 (UNIFORM PLANE)	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
	39	32K-WORD	100000H - 107FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	38	32K-WORD	0F8000H - 0FFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
PLANE0 (PARAMETER PLANE)	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
	7	4K-WORD	007000H - 007FFFH
	6	4K-WORD	006000H - 006FFFH
	5	4K-WORD	005000H - 005FFFH
	4	4K-WORD	004000H - 004FFFH
	3	4K-WORD	003000H - 003FFFH
	2	4K-WORD	002000H - 002FFFH
	1	4K-WORD	001000H - 001FFFH
	0	4K-WORD	000000H - 000FFFH

Figure 2.2 Bottom Parameter Memory Map

Table 3. Identifier Codes and OTP Address for Read Operation

	CODE	ADDRESS [A15 – A0] (1)	DATA [DQ15 – DQ0]	NOTES
Manufacture Code	Manufacture Code	0000H	00B0H	
Device Code	Top Parameter	0001H	00B4H	2
	Bottom Parameter		00B5H	2
Block Lock Configuration Code	Block is Unlocked	Block Address +2	DQ0 = 0	3
	Block is Locked		DQ0 = 1	3
	Block is not Locked-Down		DQ1 = 0	3
	Block is Locked-Down		DQ1 = 1	3
Device Configuration Code	Partition Configuration register	0006H	PCRC	4
OTP	OTP Lock	0080H	OTP-LK	5
	OTP	0081-0088H	OTP	6

Notes:

1. The address A20 – A16 are shown in below table for reading the manufacturer, device, lock configuration, device configuration code and OTP data.
2. Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
   Top parameter device has its parameter blocks in the plane3 (The highest address).
3. DQ15 – DQ2 are reserved for future implementation.
4. PCRC = Partition Configuration Register Code.
5. OTP – LK = OTP Block Lock configuration.
6. OTP = OTP Block data.

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1)

PARTITION CONFIGURATION REGISTER(2)			ADDRESS (32M-BIT DEVICE) [A20 – A16]
PCR.10	PCR.9	PCR.8	
0	0	0	00H
0	0	1	00H or 08H
0	1	0	00H or 10H
1	0	0	00H or 18H
0	1	1	00H or 08H or 10H
1	1	0	00H or 10H or 18H
1	0	1	00H or 08H or 18H
1	1	1	00H or 08H or 10H or 18H

Notes:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
2. Refer to Table 12 for the partition configuration register.

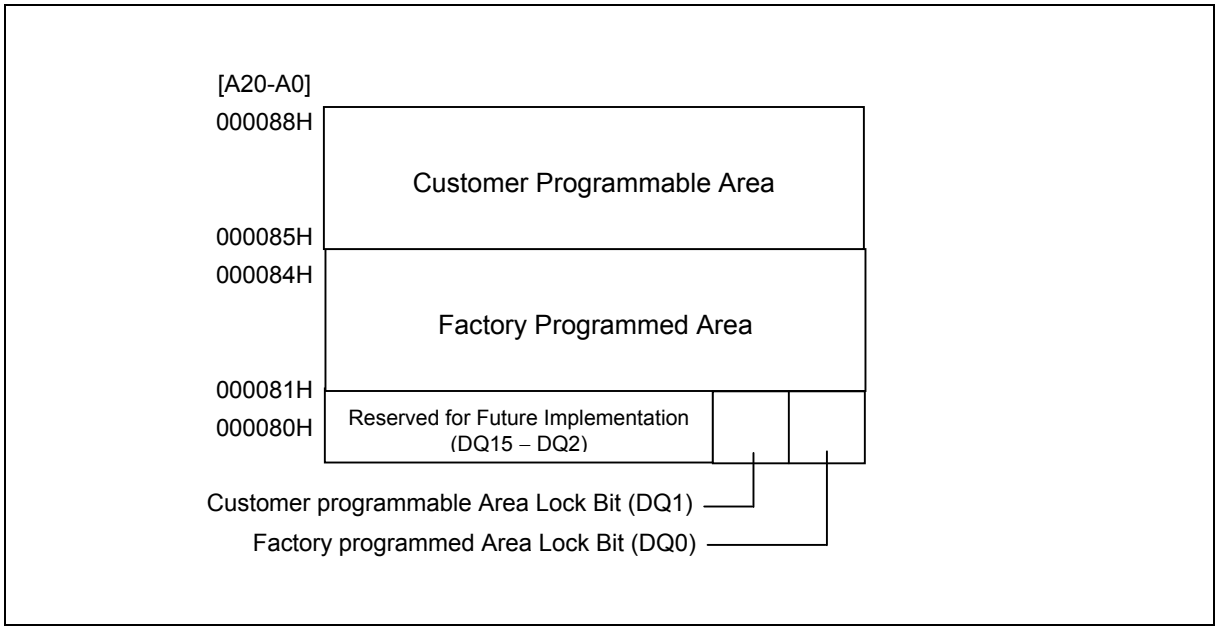


Figure 3. OTP Block Address Map for OTP Program (The area outside 80H – 88H cannot be used.)

Table 5. Bus Operations (1, 2)

MODE	NOTE	#RESET	#CE	#OE	#WE	ADDRESS	V_{PP}	DQ0 – 15
Read Array	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	DOUT
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z
Reset	3	V_{IL}	X	X	X	X	X	High Z
Read Identifier Codes/OTP	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Table 3, 4	X	See Table 3, 4
Read Query	6, 7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Appendix	X	See Appendix
Write	4, 5, 6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	DIN

Notes:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. #RESET at $V_{SS} \pm 0.2V$ ensures the lowest power consumption.
4. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when $V_{PP} = V_{PPH1/2}$ and V_{DD} = 2.7V to 3.6V.
   Command writes involving full chip erase are reliably executed when $V_{PP} = V_{PPH1}$ and V_{DD} = 2.7V to 3.6V.
5. Refer to Table 6 for valid DIN during a write operation.
6. Never hold #OE low and #WE low at the same timing.
7. Refer to Appendix for more information about query code.

Table 6. Command Definitions(11)

COMMAND	BUS CYCLES REQ'D.	NOTE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array	1	2	Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	2, 3, 4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	2, 3, 4	Write	PA	98H	Read	QA	QD
Read Status Register	2	2, 3	Write	PA	70H	Read	PA	SRD
Clear Status Register	1	2	Write	PA	50H			
Block Erase	2	2, 3, 5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	2, 5, 9	Write	X	30H	Write	X	D0H
Program	2	2, 3, 5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	2, 3, 5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	2, 8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	2, 8, 9	Write	PA	D0H			
Set Block Lock Bit	2	2	Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	2, 10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2	2	Write	BA	60H	Write	BA	2FH
OTP Program	2	2, 3, 9	Write	OA	C0H	Write	OA	OD
Set Partition configuration Register	2	2, 3	Write	PCRC	60H	Write	PCRC	04H

Notes:

1. Bus operations are defined in Table 5.
2. The address which is written at the first bus cycle should be the same as the address which is written at the second bus cycle.
   X = Any valid address within the device.
   PA = Address within the selected partition.
   IA = Identifier codes address (See Table 3 and Table 4).
   QA = Query codes address. Refer to Appendix for details.
   BA = Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA = Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA = Address of OTP block to be read or programmed (See Figure 3).
   PCRC = Partition configuration register code presented on the address A0 – A15.
3. ID = Data read from identifier codes. (See Table 3 and Table 4).
   QD = Data read from query database. Refer to Appendix for details.
   SRD = Data read from status register. See Table 10 and Table 11 for a description of the status register bits.
   WD = Data to be programmed at location WA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
   OD = Data to be programmed at location OA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
   N-1 = N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4). The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when #RESET is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when #WP is V_{IL}. When #WP is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by Winbond for future device implementations and should not be used.

Table 7. Functions of Block Lock(5) and Block Lock-Down

CURRENT STATE					
State	**#WP**	**DQ1(1)**	**DQ0(1)**	**State Name**	**Erase/Program Allowed(2)**
[000]	0	0	0	Unlocked	Yes
[001](3)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](3)	1	0	1	Locked	No
[110](4)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

1. DQ0 = 1: a block is locked; DQ0 = 0: a block is unlocked.
   DQ1 = 1: a block is locked-down; DQ1 = 0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (#WP = 0) or [101] (#WP = 1), regardless of the states before power-off or reset operation.
4. When #WP is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function, which is different from those described above.

Table 8. Block Locking State Transitions upon Command Write(4)

CURRENT STATE				RESULT AFTER LOCK COMMAND WRITTEN (Next State)		
State	**#WP**	**DQ1**	**DQ0**	**Set Lock(1)**	**Clear Lock(1)**	**Set Lock-down(1)**
[000]	0	0	0	[001]	No Change	[011](2)
[001]	0	0	1	No Change(3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111](2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111](2)
[111]	1	1	1	No Change	[110]	No Change

Notes:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ0 = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that #WP is not changed and fixed V_{IL} or V_{IH}.

Table 9. Block Locking State Transitions upon #WP Transition(4)

Previous State	Current State				Result after #WP Transition (Next State)	
	State	#WP	DQ1	DQ0	#WP = 0→1(1)	#WP = 1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

Notes:

1. "#WP = 0→1" means that #WP is driven to V_{IH} and "#WP = 1→0" means that #WP is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When #WP is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 10. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
- 1 = Ready
- 0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
- 1 = Error in (Page Buffer) Program or OTP Program
- 0 = Successful (Page Buffer) Program or OTP Program

SR.3 = V_{PP} STATUS (VPPS)
- 1 = V_{PP} LOW Detect, Operation Abort
- 0 = V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 – SR.1 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, V_{PPH2} or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 11. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	NOTES: After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Table 12. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15–11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2 – 0)
- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1 – 3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane2 – 3 are merged into one partition respectively.
- 100 = Plane 0 – 2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2 – 3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0 – 1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1 – 2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7 – 0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After power-up or device reset, PCR10-8 (PC2 – 0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See Figure 4 for the detail on partition configuration.

PCR.15 – 11 and PCR.7 – 0 are reserved for future use and should be masked out when polling the partition configuration register.

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	PARTITION0: PLANE3, PLANE2, PLANE1, PLANE0	0 1 1	PARTITION2: PLANE3, PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0
0 0 1	PARTITION1: PLANE3, PLANE2, PLANE1; PARTITION0: PLANE0	1 1 0	PARTITION2: PLANE3; PARTITION1: PLANE2; PARTITION0: PLANE1, PLANE0
0 1 0	PARTITION1: PLANE3, PLANE2; PARTITION0: PLANE1, PLANE0	1 0 1	PARTITION2: PLANE3; PARTITION1: PLANE2, PLANE1; PARTITION0: PLANE0
1 0 0	PARTITION1: PLANE3; PARTITION0: PLANE2, PLANE1, PLANE0	1 1 1	PARTITION3: PLANE3; PARTITION2: PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0

Figure 4. Partition Configuration

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Operating Temperature
During Read, Erase and Program ..... -40°C to +85°C(1)

Storage Temperature
During under Bias ..... -40°C to +85°C
During non Bias ..... -65°C to +125°C

Voltage On Any Pin
(except V_{DD} and V_{PP}) ..... -0.5V to V_{DD} +0.5V(2)

V_{DD} and V_{DDQ} Supply Voltage..... -0.2V to +3.9V(2)

V_{PP} Supply Voltage..... -0.2V to +12.6V(2,3,4)

Output Short Circuit Current..... 100 mA(5)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Notes:

1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to V_{SS}. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{DD} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20 nS. Maximum DC voltage on input/output pins and V_{DD} is V_{DD} +0.5V, which, during transitions, may overshoot to V_{DD} +2.0V for periods <20 nS.
3. Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20 nS.
4. V_{PP} erase/program voltage is normally 2.7V to 3.6V. Applying 11.7V to 12.3V to V_{PP} during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. V_{PP} may be connected to 11.7V to 12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Conditions

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	NOTE
Operating Temperature	T_A	-40	+25	+85	°C	
V_{DD} Supply Voltage	V_{DD}	2.7	3.0	3.6	V	1
I/O Supply Voltage	V_{DDQ}	2.7	3.0	3.6	V	1
V_{PP} Voltage when Used as a Logic Control	V_{PPH1}	1.65	3.0	3.6	V	1
V_{PP} Supply Voltage	V_{PPH2}	11.7	12	12.3	V	1, 2
Main Block Erase Cycling: V_{PP} = 3.0V		100,000			Cycles	
Parameter Block Erase Cycling: V_{PP} = 3.0V		100,000			Cycles	
Main Block Erase Cycling: V_{PP} = 12V, 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: V_{PP} = 12V, 80 hrs.				1,000	Cycles	
Maximum V_{PP} hours at 12V				80	Hours	

Notes:

1. See DC Characteristics tables for voltage range-specific specification.
2. Applying V_{PP} = 11.7V to 12.3V during an erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to V_{PP} =11.7V to 12.3V is not allowed and can cause damage to the device.

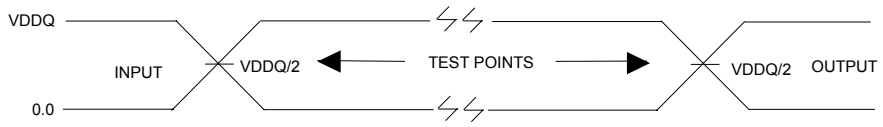
Capacitance(1)

TA = +25° C, f = 1 MHz

PARAMETER	SYM.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	CIN	6	8	pF	VIN = 0.0V
Output Capacitance	COUT	10	12	pF	VOUT = 0.0V

Note: Sampled, not 100% tested.

AC Input/Output Test Conditions



AC test inputs are driven at V_{DD}(min) for a Logic "1" and 0.0V for a Logic "0".
Input timing begins, and output timing ends at V_{DD}/2. Input rise and fall times (10% to 90%) < 5 nS.
Worst case speed conditions are when V_{DD} =V_{DD}(min).

Figure 5. Transient Input/Output Reference Waveform for V_{DD} =2.7V to 3.6V

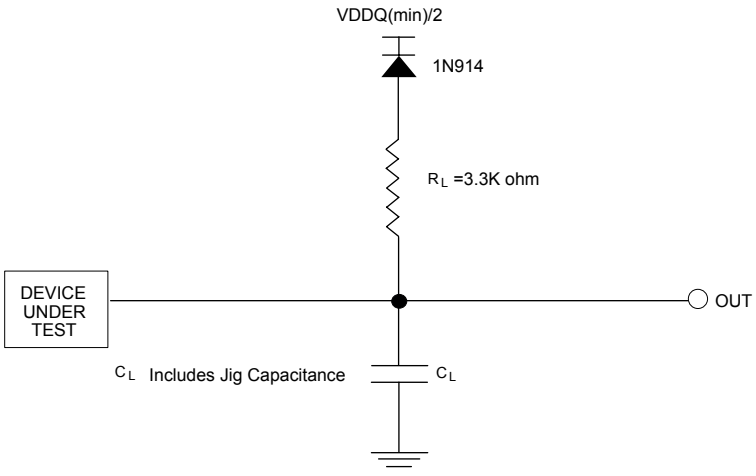


Figure 6. Transient Equivalent Testing Load Circuit

Table 13. Configuration Capacitance Loading Value

TEST CONFIGURATION	CL(PF)
V_{DD} = 2.7V to 3.6V	50

DC Characteristics

PARAMETER		SYM.	TEST CONDITIONS	V_{DD} = 2.7V to 3.6V			UNIT
				Min.	Typ.	Max.	
Input Load Current (note 1)		I_{LI}	$V_{DD} = V_{DD}$ Max., $V_{DDQ} = V_{DDQ}$ Max., $V_{IN}/V_{OUT} = V_{DDQ}$ or V_{SS}	-1.0		+1.0	µA
Output Leakage Current (note1)		I_{LO}		-1.0		+1.0	µA
V_{DD} Standby Current (note 1)		I_{CCS}	$V_{DD} = V_{DD}$ Max. #CE = #RESET = V_{DDQ} ±0.2V, #WP = V_{DDQ} or V_{SS}		4	20	µA
V_{DD} Automatic Power Saving Current (note 1, 4)		I_{CCAS}	$V_{DD} = V_{DD}$ Max. #CE = V_{SS} ±0.2V, #WP = V_{DDQ} or V_{SS}		4	20	µA
V_{DD} Reset Power-Down Current (note 1)		I_{CCD}	#RESET = V_{SS} ±0.2V		4	20	µA
Average V_{DD} Read Current Normal Mode (note1, 7)		I_{CCR}	$V_{DD} = V_{DD}$ Max., #CE = V_{IL}, #OE = V_{IH}, f = 5 MHz		15	25	mA
Average V_{DD} Read Current Page Mode (note1, 7)	8 Word Read				5	10	mA
V_{DD} (Page Buffer) Program Current (note 1, 5, 7)		I_{CCW}	$V_{PP} = V_{PPH1}$		20	60	mA
			$V_{PP} = V_{PPH2}$		10	20	mA
V_{DD} Block Erase, Full Chip Erase Current (note 1, 5, 7)		I_{CCE}	$V_{PP} = V_{PPH1}$		10	30	mA
			$V_{PP} = V_{PPH2}$		10	30	mA
V_{DD} (Page Buffer) Program or Block Erase Suspend Current (note 1, 2, 7)		I_{CCWS} I_{CCES}	#CE = V_{IH}		10	200	µA
V_{PP} Standby or Read Current (note 1, 6, 7)		I_{PPS} I_{PPR}	$V_{PP} \leq V_{DD}$		2	5	µA
V_{PP} (Page Buffer) Program Current (note 1, 5, 6, 7)		I_{PPW}	$V_{PP} = V_{PPH1}$		2	5	µA
			$V_{PP} = V_{PPH2}$		10	30	mA
V_{PP} Block Erase, Full Chip Erase Current (note 1, 5, 6, 7)		I_{PPE}	$V_{PP} = V_{PPH1}$		2	5	µA
			$V_{PP} = V_{PPH2}$		5	15	mA
V_{PP} (Page Buffer) Program Suspend Current (note 1, 6, 7)		I_{PPWS}	$V_{PP} = V_{PPH1}$		2	5	µA
			$V_{PP} = V_{PPH2}$		10	200	µA
V_{PP} Block Erase Suspend Current (note 1, 6, 7)		I_{PPES}	$V_{PP} = V_{PPH1}$		2	5	µA
			$V_{PP} = V_{PPH2}$		10	200	µA

DC Characteristics (continued)

PARAMETER	SYM.	TEST CONDITIONS	V_{DD} = 2.7V – 3.6V			UNIT
			Min.	Typ.	Max.	
Input Low Voltage (note 5)	V_{IL}		-0.4		0.4	V
Input High Voltage (note 5)	V_{IH}		V_{DDQ} -0.4		V_{DDQ} +0.4	V
Output Low Voltage (note 5)	V_{OL}	V_{DD} = V_{DD} Min., V_{DDQ} = V_{DDQ} Min., I_{OL} = 100 μA			0.2	V
Output High Voltage (note 5)	V_{OH}	V_{DD} = V_{DD} Min., V_{DDQ} = V_{DDQ} Min., I_{OH} = -100 μA	V_{DDQ} -0.2			V
V_{PP} Lockout during Normal Operations (note 3, 5, 6)	V_{PPLK}				0.4	V
V_{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations (note 6)	V_{PPH1}		1.65	3.0	3.6	V
V_{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations (note 6)	V_{PPH2}		11.7	12	12.3	V
V_{DD} Lockout Voltage	V_{LKO}		1.5			V

Notes:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{DD} = 3.0V and T_A = +25° C unless V_{DD} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program while in block erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Block erases, full chip erase, (page buffer) program and OTP program are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.) and above V_{PPH2} (max.).
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when address are changed.
5. Sampled, not 100% tested.
6. V_{PP} is not used for power supply pin. With $V_{PP} \le V_{PPLK}$, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
   Applying 12V±0.3V to V V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{DD} power bus.
   Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum.
7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

AC Characteristics - Read-only Operations(1)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Read Cycle Time	t_{AVAV}	70		nS
Address to Output Delay	t_{AVQV}		70	nS
#CE to Output Delay (note 3)	t_{ELQV}		70	nS
Page Address Access Time	T_{APA}		25	nS
#OE to Output Delay (note 3)	t_{GLQV}		20	nS
#RESET High to Output Delay	T_{PHQV}		150	nS
#CE or #OE to Output in High Z, whichever Occurs First (note 2)	t_{EHQZ}, $t_{GHQZ,}$		20	nS
#CE to Output in Low Z (note 2)	T_{ELQX}	0		nS
#OE to Output in Low Z (note 2)	t_{GLQX}	0		nS
Output Hold from first Occurring Address, #CE or #OE Change (note 2)	t_{OH}	0		nS

Notes:

1. See AC Input/Output Reference Waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. #OE may be delayed up to t_{ELQV} to t_{GLQV} after the falling edge of #CE without impact to t_{ELQV}.

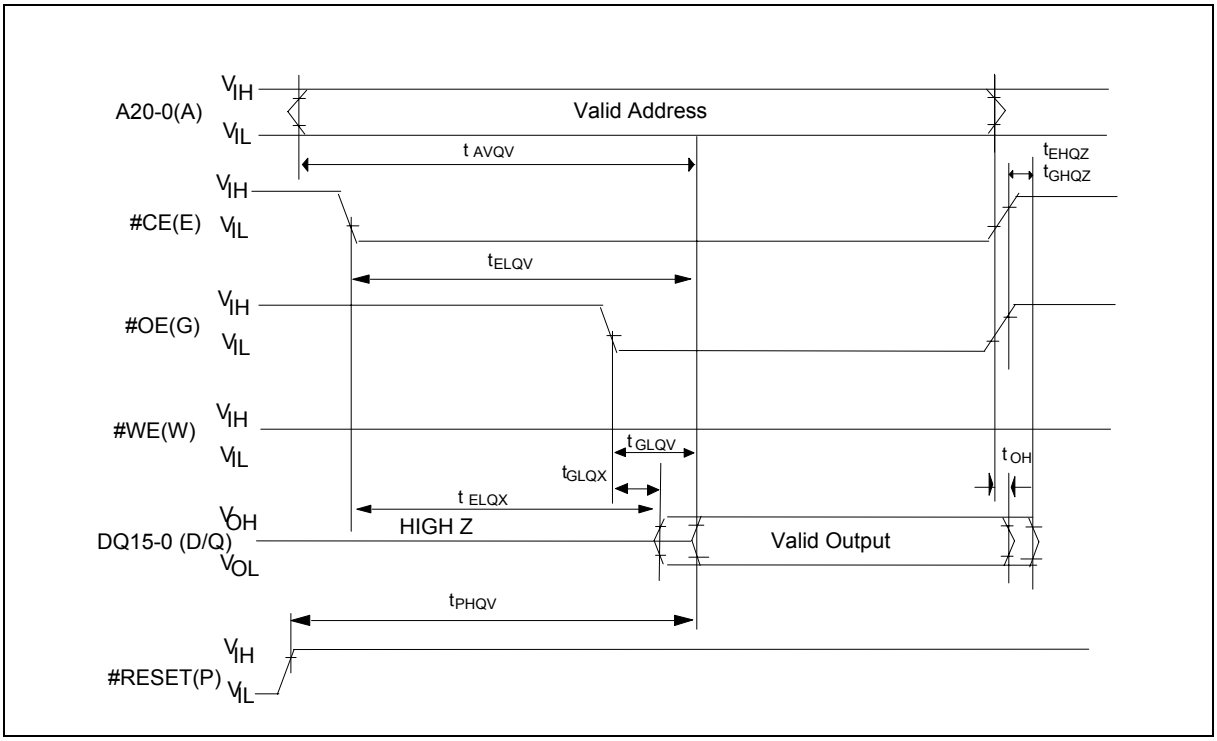


Figure 7. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier codes, OTP Block or Query Code

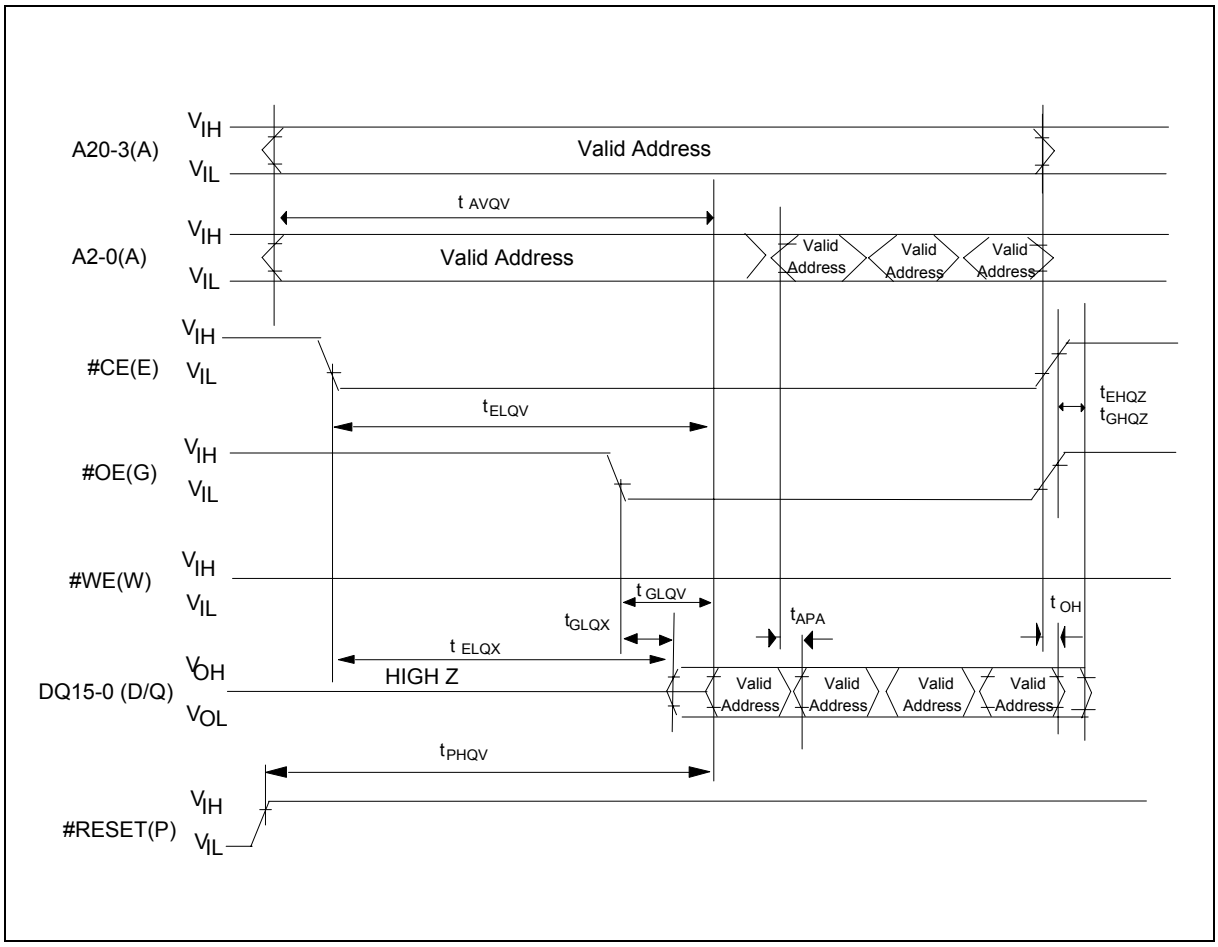


Figure 8. AC Waveform for Asynchronous Page Mode Read Operations from Main Blocks or Parameter Blocks

AC Characteristics - Write Operations[1,2]

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	70		nS
#RESET High Recovery to #WE(#CE) Going Low (note 3)	$t_{PHWL}(t_{PHEL})$	150		nS
#CE(#WE) Setup to #WE(#CE) Going Low (note 4)	$t_{ELWL}(t_{WLEL})$	0		nS
#WE(#CE) Pulse Width (note 4)	$t_{WLWH}(t_{ELEH})$	60		nS
Data Setup to #WE(#CE) Going High (note 8)	$t_{DVWH}(t_{DVEH})$	40		nS
Address Setup to #WE(#CE) Going High (note 8)	$t_{AVWH}(t_{AVEH})$	50		nS
#CE(#WE) Hold from #WE(#CE) High	$t_{WHEH}(t_{EHWH})$	0		nS
Data Hold from #WE(#CE) High	$t_{WHDX}(t_{EHDX})$	0		nS
Address Hold from #WE(#CE) High	$t_{WHAX}(t_{EHAX})$	0		nS
#WE(#CE) Pulse Width High (note 5)	$t_{WHWL}(t_{EHEL})$	30		nS
#WP High Setup to #WE(#CE) Going High (note 3)	$t_{SHWH}(t_{SHEH})$	0		nS
V_{PP} Setup to #WE(#CE) Going High (note 3)	$t_{VVWH}(t_{VVEH})$	200		nS
Write Recovery before Read	$t_{WHGL}(t_{EHGL})$	30		nS
#WP High Hold from Valid SRD (note 3, 6)	t_{QVSL}	0		nS
V_{PP} Hold from Valid SRD (note 3, 6)	t_{QVVL}	0		nS
#WE(#CE) High to SR.7 Going "0" (note 3, 7)	$t_{WHR0}(t_{EHR0})$		t_{AVQV}+40	nS

Notes:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either #CE or #WE.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of #CE or #WE (whichever goes low last) to the rising edge of #CE or #WE (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of #CE or #WE (whichever goes high first) to the falling edge of #CE or #WE (whichever goes low last). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
6. V_{PP} should be held at $V_{PP} = V_{PPH1/2}$ until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5 = 0) and held at $V_{PP} = V_{PPH1}$ until determination of full chip erase success (SR.1/3/5 = 0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.
8. Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.

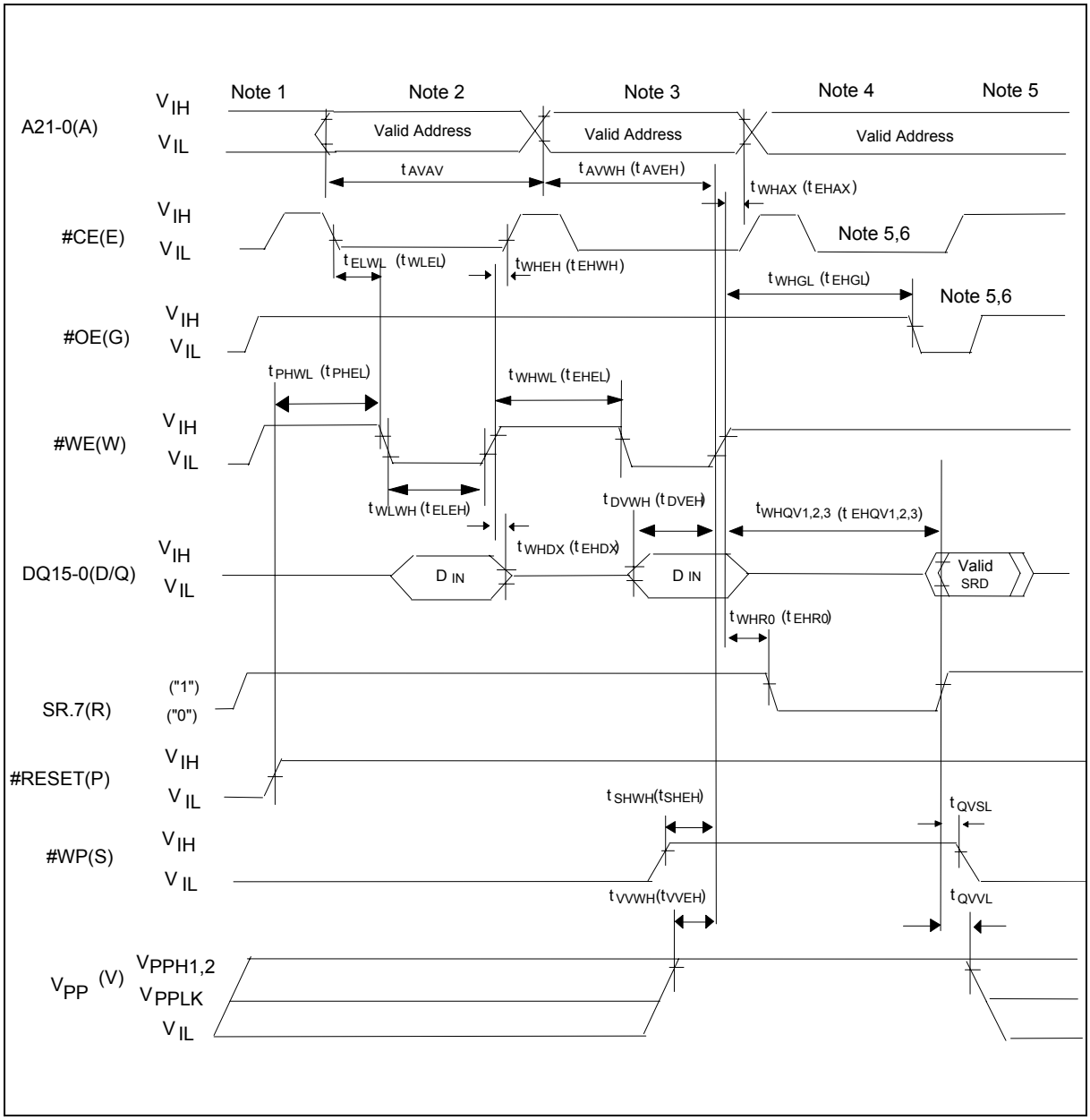


Figure 9. AC Waveform for Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, #OE and #CE must be driven active, and #WE de-asserted.

Reset Operations

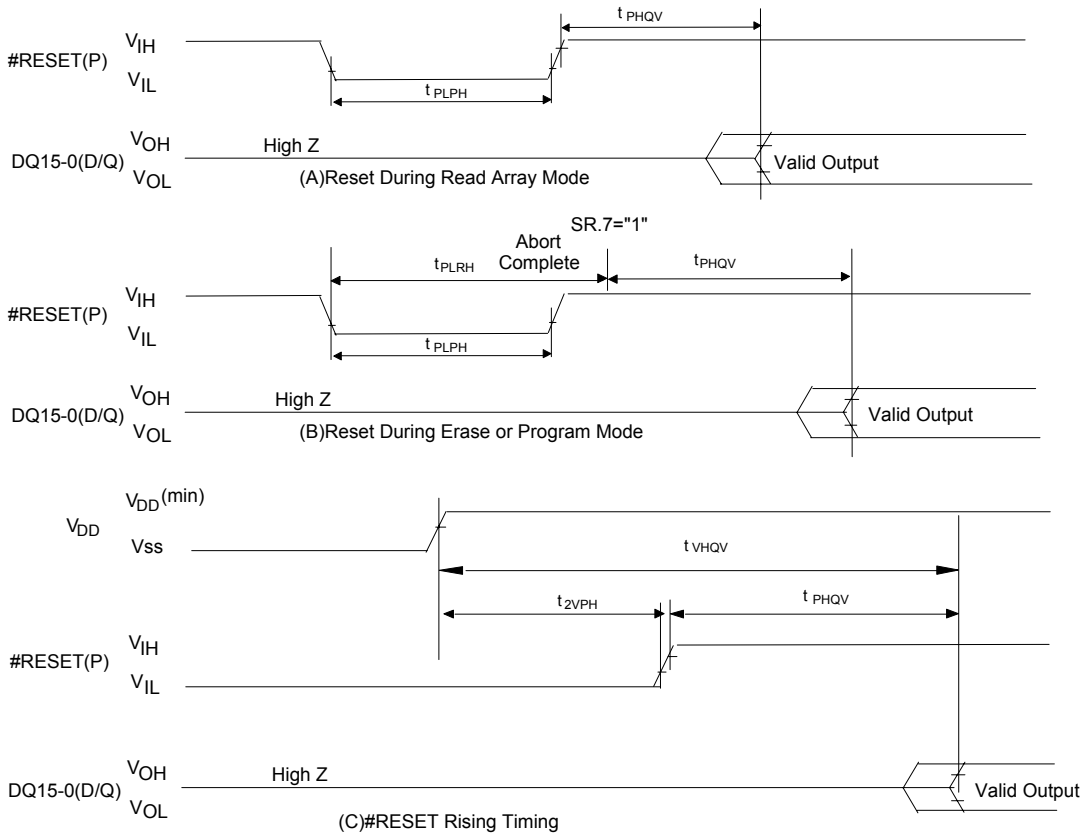


Figure 10. AC Waveform for Reset Operation

Reset AC Specifications

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET Low to Reset during Read (#RESET should be low during power-up.) (note 1, 2, 3)	t_{PLPH}	100		nS
#RESET Low to Reset during Erase or Program (note 1, 3, 4)	t_{PLRH}		22	µS
V_{DD} 2.7V to #RESET High (note 1, 3, 5)	t_{2VPH}	100		nS
V_{DD} 2.7V to Output Delay (note 3)	t_{VHQV}		1	mS

Notes:

1. A reset time, t_{PHQV}, is required from the later of SR.7 going "1"(High Z) or #RESET going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.

4. If #RESET asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding #RESET low minimum 100ns is required after V_{DD} has been in predefined range and also has been in stable there.

Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance(3)

V_{DD} = 2.7V to 3.6V, TA = -40°C to +85°C

PARAMETER	SYM.	PAGE BUFFER COMMAND IS USED OR NOT USED	$V_{PP} = V_{PPH1}$ (IN SYSTEM)			$V_{PP} = V_{PPH2}$ (IN MANUFACTURING)			UNIT
			MIN.	TYP.(1)	MAX.(2)	MIN.	TYP.(1)	MAX.(2)	
4K-Word Parameter Block Program Time (note 2)	t_{WPB}	Not Used		0.05	0.3		0.04	0.12	S
		Used		0.03	0.12		0.02	0.06	S
32K-Word Main Block Program Time (note 2)	t_{WMB}	Not Used		0.38	2.4		0.31	1.0	S
		Used		0.24	1.0		0.17	0.5	S
Word Program Time (note 2)	t_{WHQV1}/ t_{EHQV1}	Not Used		11	200		9	185	µS
		Used		7	100		5	90	µS
OTP Program Time (note 2)	t_{WHOV1}/ t_{EHOV1}	Not Used		36	400		27	185	µS
4K-Word Parameter Block Erase Time (note 2)	t_{WHQV2}/ t_{EHQV2}	-		0.3	4		0.2	4	S
32K-Word Main Block Erase Time (note 2)	t_{WHQV3}/ t_{EHQV3}	-		0.6	5		0.5	5	S
Full Chip Erase Time (note 2)				40	350				S
(Page Buffer) Program Suspend Latency Time to Read (note 4)	t_{WHRH1}/ t_{EHRH1}	-		5	10		5	10	µS
Block Erase Suspend Latency Time to Read (note 4)	t_{WHRH2}/ t_{EHRH2}	-		5	20		5	20	µS
Latency Time from Block Erase Resume Command to Block Erase Suspend Command (note 5)	t_{ERES}	-	500			500			µS

Notes:

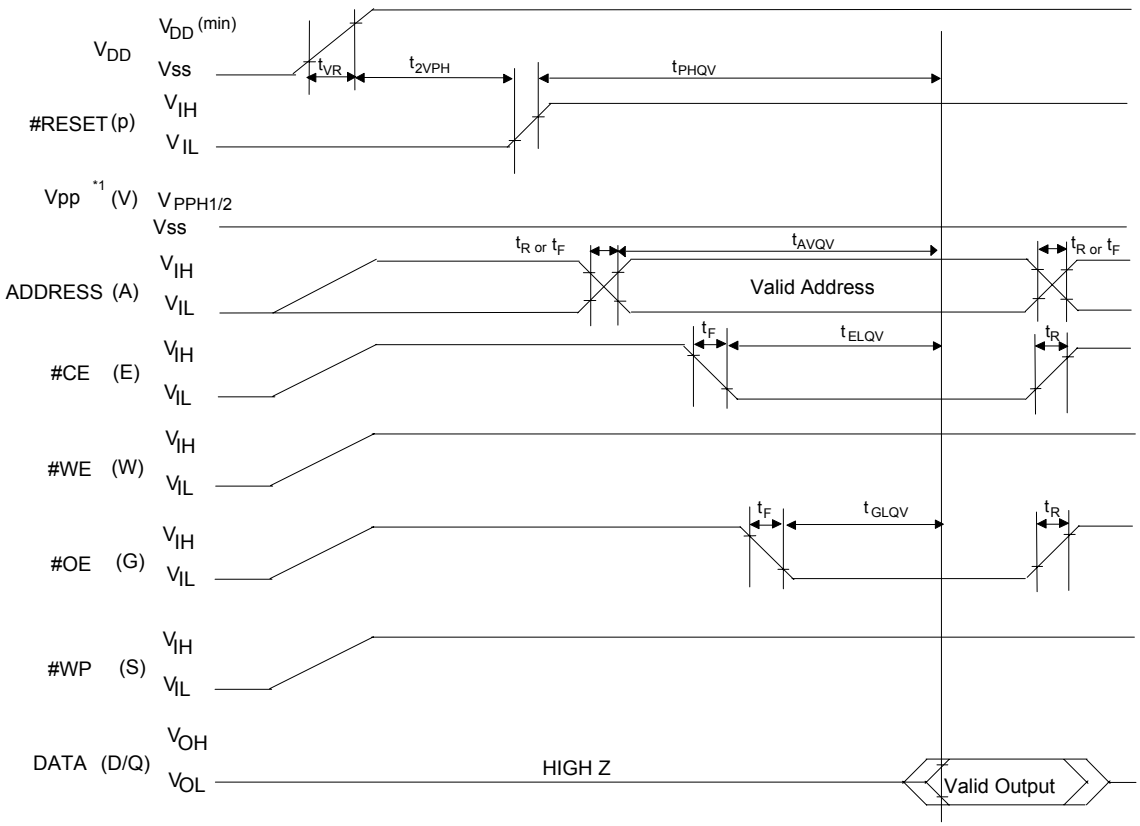
1. Typical values measured at V_{DD} = 3.0V, V_{PP} = 3.0V or 12V, and TA=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (#WE or #CE going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

5. ADDITIONAL INFORMATION

Recommended Operating Conditions

At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PP} to 0V during read operations and $V_{PPH1/2}$ during write or erase operations.

Figure A-1. AC Timing at Device Power-up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

Rise and Fall Time

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time (note 1)	t_{VR}	0.5	30000	µS/ V
Input Signal Rise Time (note1, 2)	t_R		1	µS/ V
Input Signal Fall Time (note1, 2)	t_F		1	µS/ V

Notes:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

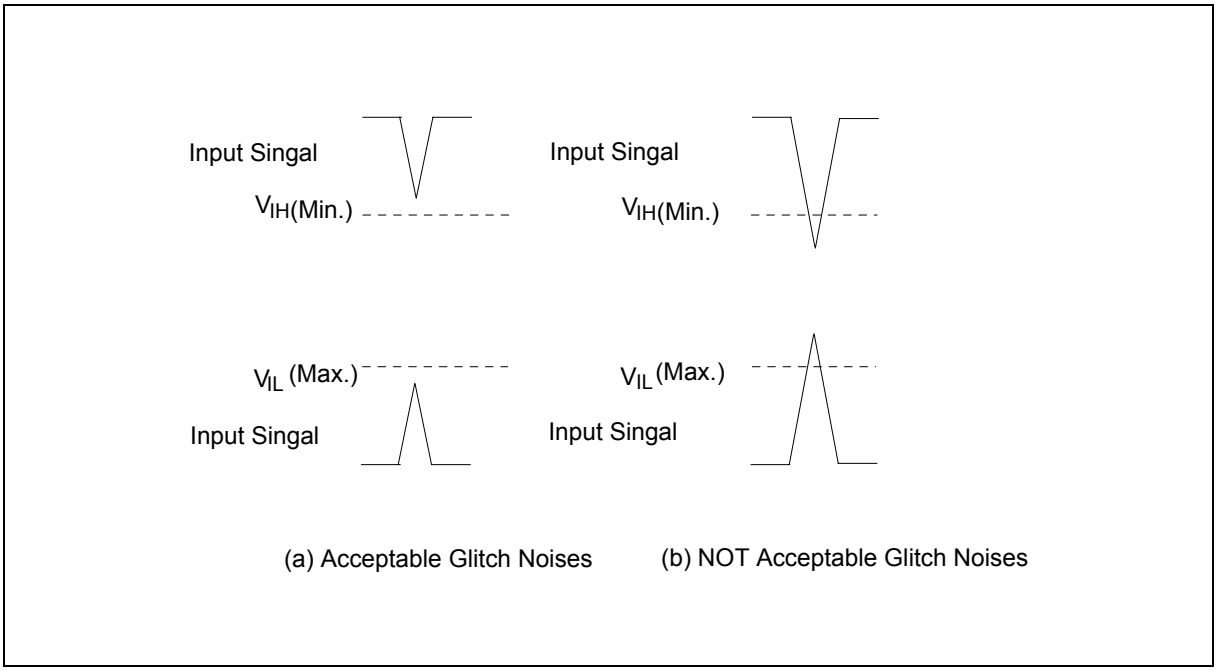


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

6. ORDERING INFORMATION

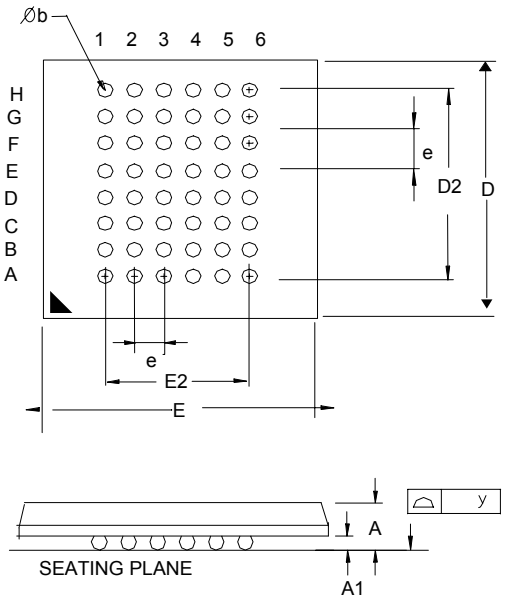
PART NO.	ACCESS TIME (nS)	OPERATING TEMPERATURE (°C)	BOOT BLOCK	PACKAGE
W28F321BB70L	70	-40° C to 85° C	Bottom Boot	48-Ball TFBGA
W28F321TB70L	70	-40° C to 85° C	Top Boot	48-Ball TFBGA

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

7. PACKAGE DIMENSION

48-Ball TFBGA (7mm x 7mm) (measurements in millimeters)



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.05	-	-	0.042
A1	0.20	0.25	0.30	0.008	0.010	0.012
D	6.80	7.00	7.20	0.272	0.280	0.288
D2	3.75 BASIC			0.150 BASIC		
E	6.80	7.00	7.20	0.272	0.280	0.288
E2	5.25 BASIC			0.210		
y	0.10 BASIC			0.004 BASIC		
Øb	0.37	0.40	0.43	0.015	0.016	0.017
e	0.75 BASIC			0.030 BASIC		

8. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 3, 2003	-	Initial Issued
A2	Feb. 17, 2003	27	Modify the package dimension drawing

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