



PIC16HV540

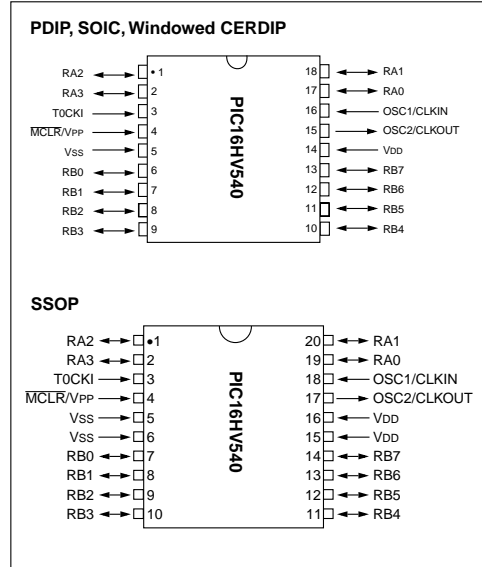
Enhanced PIC16C54 EPROM-Based 8-Bit CMOS Microcontroller With On-Chip Voltage Regulator

High-Performance RISC CPU:

Device	Pins	I/O	EPROM	RAM
PIC16HV540	18	12	512	25

- Only 33 single word instructions to learn
 - All instructions are single cycle (200 ns) except for program branches which are two-cycle
 - Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
 - 12-bit wide instructions
 - 8-bit wide data path
 - Seven special function hardware registers
 - ★ • Four-level deep hardware stack
 - Direct, indirect and relative addressing modes for data and instructions
- ### Peripheral Features:
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
 - Power-On Reset (POR)
 - ★ • Brown-Out Protection
 - Device Reset Timer (DRT) with short RC-oscillator start up time
 - ★ • Programmable Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
 - Sleep Timer
 - ★ • 8 High Voltage I/O
 - ★ • 4 Regulated I/O
 - ★ • Wake up from SLEEP on pin change
 - Programmable code-protection
 - Power saving SLEEP mode
 - Selectable oscillator options:
 - RC: Low-cost RC oscillator
 - XT: Standard crystal/resonator
 - HS: High speed crystal/resonator
 - LP: Power saving, low frequency crystal
 - ★ • Glitch filtering on $\overline{\text{MCLR}}$ and pin change inputs

Pin Configurations



CMOS Technology:

- ★ • Selectable on-chip 3V/5V Regulator
- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
 - 3.5V to 15V
- Temperature range:
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
- Low-power consumption
 - < 2 mA typical @ 5V, 4 MHz
 - 15 μA typical @ 3V, 32 kHz
 - < 4.5 μA typical standby current @ 15V (with WDT disabled), 0°C to 70°C

★ = Enhanced Features

1.0 GENERAL DESCRIPTION

The PIC16HV540 from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, EPROM-based CMOS microcontroller. It is pin and software compatible with the PIC16C5X family of devices. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16HV540 delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly orthogonal resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC16HV540 is the first One-Time-Programmable (OTP) microcontroller with an on-chip 3 Volt and 5 Volt regulator. This eliminates the need for an external regulator in many applications powered from 9 Volt or 12 Volt batteries or unregulated 6 Volt, 9 Volt or 12 Volt mains adapters. The PIC16HV540 is ideally suited for applications that require very low standby current at high voltages. These typically require expensive low current regulators.

The PIC16HV540 is equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator, cost saving RC oscillator, and XT and HS for crystal oscillators. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective OTP versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC16HV540 will in future be supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines. Functions that correspond to the PIC16C54 (such as assembly and programming) can utilize existing tools.

1.1 Applications

The PIC16HV540 fits perfectly in low-power battery applications such as CO and smoke detection, toys, games, security systems and automobile modules. The EPROM technology makes customizing of application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint package, for through hole or surface mounting, make this microcontroller perfect for applications with space limitations. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the PIC16HV540 very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

1.2 Enhanced Features

1.2.1 REGULATED I/O PORTA INDEPENDENT OF CORE REGULATOR

PORTA I/O pads and OSC2 output are powered by the regulated internal voltage V_{IO} . A maximum of 10mA per output is allowed, or a total of 40mA. The core itself is powered from the independently regulated supply VREG.

1.2.2 HIGH VOLTAGE I/O PORTB

All eight PORTB I/Os are high voltage I/O. The inputs will tolerate input voltages as high as the V_{DD} and outputs will swing from V_{SS} to the V_{DD} . The input threshold voltages vary with supply voltage. (See DC characteristics.)

1.2.3 WAKE UP ON PIN CHANGE ON PORTB [0:3]

Four of the PORTB inputs latch the status of the pin at the onset of sleep mode. A level change on the inputs resets the device, implementing wake up on pin change (via warm reset). The PC bit in the status register is reset to indicate that a pin change caused the reset condition. Any pin change (glitch insensitive) of the opposite level of the initial value wakes up the device. This option can be enabled/disabled in OPTION2 register. (See OPTION2 register, Figure 4-3.)

1.2.4 WAKE UP ON PIN CHANGE WITH A SLOWLY-RISING VOLTAGE ON PORTB [7]

PORTB [7] also implements wake up from sleep, however this input is specifically adapted so that a slowly rising voltage does not cause excessive power consumption. This input can be used with external RC circuits for long sleep periods without using the internal timer and prescaler. This option is also enabled/disabled in OPTION2 register. (The enable/disable bit is shared with the other 4 wake up inputs.) The new wake up status bit in the status register is also shared with the other four wake up inputs.

1.2.5 LOW-VOLTAGE (BROWN-OUT) DETECTION

A low voltage (Brown-out) detect circuit optionally resets the device at a voltage level higher than that at which Brown-out events occur. The nominal trip voltages are 3.1 Volt (for 5 Volt operation) and 2.2 Volt (for 3 Volt operation), respectively. The core remains in the reset state as long as this condition holds (as if a MCLR external reset was given). The Brown-out trip level is user selectable, with built-in interlocks. The Brown-out detector is disabled at power-up and is activated by clearing the appropriate bit (BE) in OPTION2 register.

1.2.6 INCREASED STACK DEPTH

The stack depth is 4 levels to allow modular program implementation by using functions and subroutines.

1.2.7 ENHANCED WATCHDOG TIMER (WDT) OPERATION

The WDT is enabled by setting FUSE 2 in the configuration word. The WDT setting is latched and the fuse disabled during SLEEP mode to reduce current consumption.

If the WDT is disabled by FUSE 2, it can be enabled/disabled under program control using bit 4 in OPTION2 (SWE). The software WDT control is disabled at power-up.

The current consumption of the on-chip oscillator (used for the watchdog, oscillator startup timer and sleep timer) is less than 1 μ A (typical) at 3 Volt operation.

1.2.8 REDUCED EXTERNAL RC OSCILLATOR STARTUP TIME

If the RC oscillator option is selected in the Configuration word (FOSC1=1 and FOSCO=1) the oscillator startup time is 1.0 ms nominal instead of 18 ms nominal. This is applicable after power-up (POR), either WDT interrupt or wake-up, external reset on MCLR, WPC (wake on pin change) and Brown-out.

1.2.9 LOW-VOLTAGE OPERATION OF THE ENTIRE CPU DURING SLEEP

The voltage regulator can automatically lower the voltage to the core from 5 Volt to 3 Volt during sleep, resulting in reduced current consumption. This is an option bit in OPTION2 register.

1.2.10 GLITCH FILTERS ON WAKEUP PINS AND MCLR

Glitch sensitive inputs for wakeup on pin change are filtered to reduce susceptibility to interference. A similar filter reduces false reset on MCLR.

1.2.11 PROGRAMMABLE CLOCK GENERATOR

When used in RC mode the CLKOUT pin can be used as a programmable clock output. The output is connected to TMR0, bit 0 and by setting the prescaler, clock out frequencies of CLKIN/8 to CLKIN/1024 can be generated. The CLKOUT pin can also be used as a general purpose output by modifying to TMR0, bit 0.

TABLE 1-1: PIC16HV540 DEVICE

		PIC16HV540
Clock	Maximum Frequency (MHz)	20
Memory	EPROM Program Memory	512
	RAM Data Memory (bytes)	25
Peripherals	Timer Module(s)	TMR0
Packages	I/O Pins	12
	Voltage Range (Volts)	3.5V-15V
	Number of Instructions	33
	Packages	18-pin DIP SOIC 20-pin SSOP

All PICmicro[®] devices have Power-on Reset, selectable WDT, selectable code protect and high I/O current capability.

2.0 PIC16HV540 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. When placing orders, please use the PIC16HV540 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable versions, offered in Cerdip packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART[®] and PRO MATE[®] programmers both support programming of the PIC16HV540. Third party programmers also are available; refer to Literature Number DS00104 for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

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3.0 ARCHITECTURAL OVERVIEW

This section provides information on the architecture of the PIC16HV540. For information on operation of the peripherals, electrical specifications, etc., please refer to the PIC16C5X data sheet (DS30453).

FIGURE 3-1: PIC16HV540 BLOCK DIAGRAM

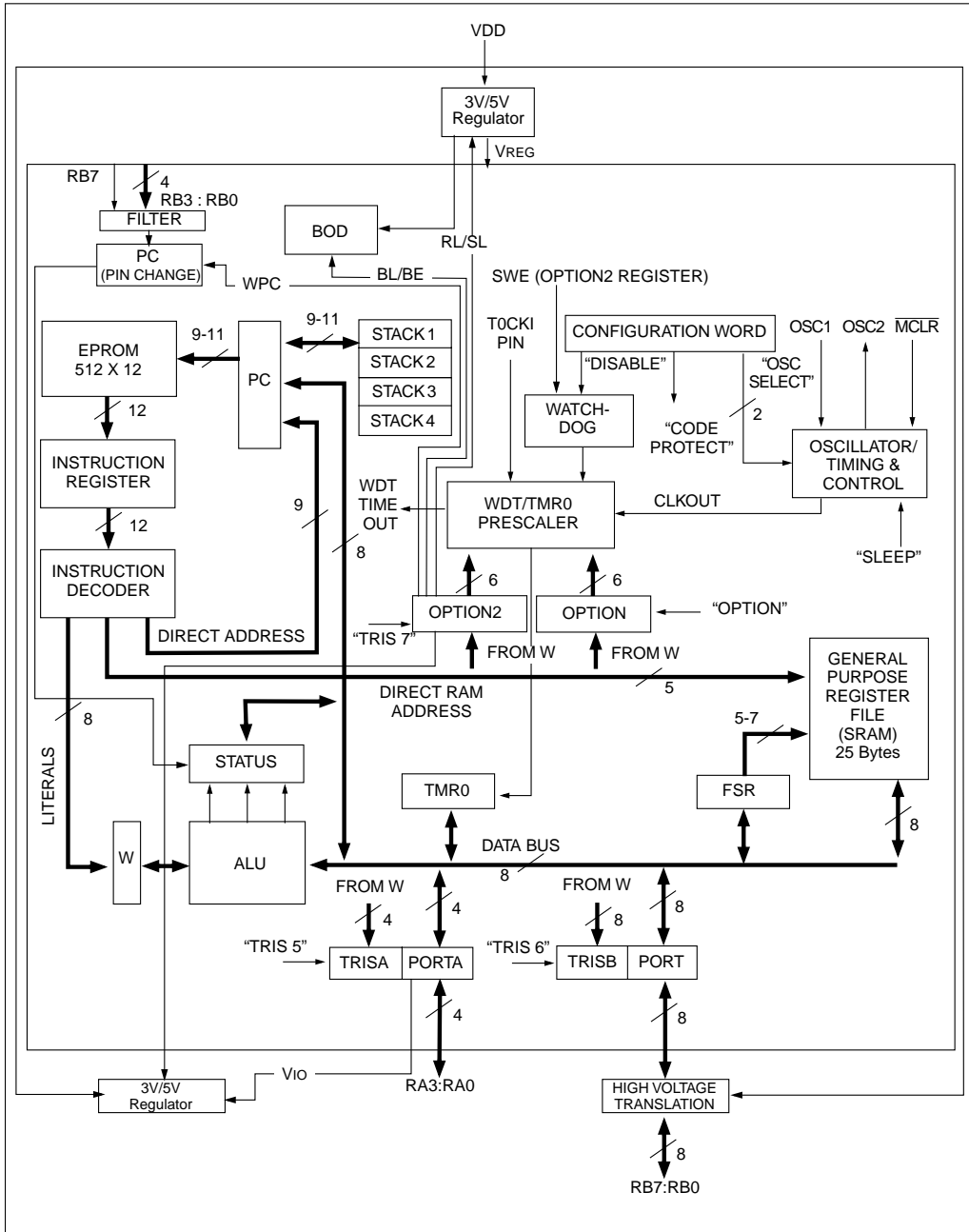


TABLE 3-1: PINOUT DESCRIPTION - PIC16HV540

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description	
RA0 RA1 RA2 RA3	17 18 1 2	19 20 1 2	I/O I/O I/O I/O	TTL TTL TTL TTL	Independently regulated Bi-directional I/O port — V _{IO}	
RB0 RB1 RB2 RB3	6 7 8 9	7 8 9 10	I/O I/O I/O I/O	TTL TTL TTL TTL	High-voltage Bi-directional I/O port. Sourced from V _{DD} .	Wake up on pin change.
RB4 RB5 RB6	10 11 12	11 12 13	I/O I/O I/O	TTL TTL TTL		
RB7	13	14	I/O	TTL		Wake up on SLOW rising pin change.
T0CKI	3	3	I	ST	Clock input to Timer 0. Must be tied to V _{SS} or V _{DD} , if not in use, to reduce current consumption.	
MCLR/VPP	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the MCLR/VPP pin must not exceed V _{DD} to avoid unintended entering of programming mode.	
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.	
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.	
VDD	14	15,16	P	—	Positive supply.	
VSS	5	5,6	P	—	Ground reference.	

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used, TTL = TTL input,
ST = Schmitt Trigger input

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4.0 MEMORY ORGANIZATION

FIGURE 4-1: PIC16HV540 PROGRAM MEMORY MAP AND STACK

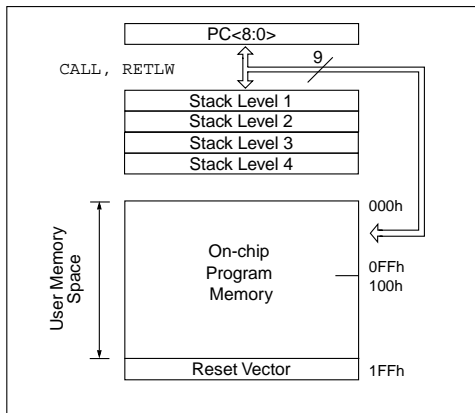


FIGURE 4-2: PIC16HV540 REGISTER FILE MAP

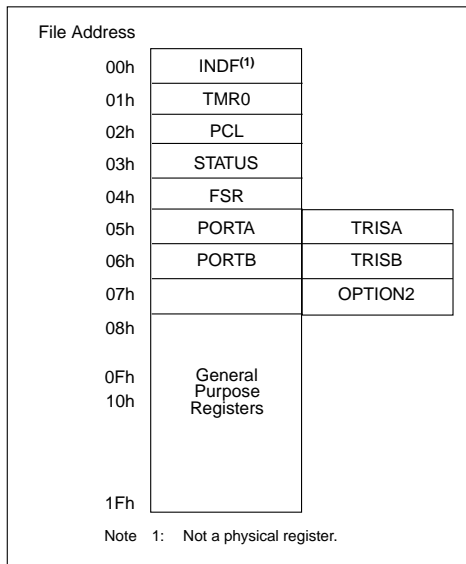


TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
N/A	OPTION2	Contains control bits to configure pin changes, software enabled WDT, regulation and brown-out								xx11 1111	xx11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PCF	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C	1001 1xxx	100q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, — = unimplemented, read as '0' (if applicable)
 x = unknown, u = unchanged, q = value depends on condition.

- Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 of the PIC16C5X data sheet (DS30453) for an explanation of how to access these bits.
- File address 07h is a general purpose register on the PIC16HV540.
 - PCF This bit is set to 1 after power up-reset (POR) or sleep command.
 - PCF This bit is set to 0 after a wake up on pin change event.

Figure 4-3: OPTION2 REGISTER (TRIS 07h)

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
-	-	WPC	SWE	RL	SL	BL	BE
bit7	6	5	4	3	2	1	0

W = Writable bit
 U = Unimplemented bit
 -n = Value at POR reset

bit 7-6: **Unimplemented.**

bit 5: **WPC:** Wake up on pin change
 1 = Disabled
 0 = Enabled

bit 4: **SWE:** Software WDT enable
 1 = Disabled
 0 = Enabled

bit 3: **RL:** Regulated voltage level select bit
 1 = 5 Volt
 0 = 3 Volt

bit 2: **SL:** Sleep voltage level select bit
 1 = **RL** bit setting
 0 = 3 Volt

bit 1: **BL:** Brown-out voltage level select bit
 1 = **RL** bit setting, but **SL** during sleep
 0 = 3 Volt

bit 0: **BE:** Brown-out enabled
 1 = Disabled
 0 = Enabled

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5.0 INSTRUCTION SET SUMMARY

Each PIC16HV540 instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16HV540 instruction set summary in Table 5-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 5-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 5-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
\overline{TO}	Time-Out bit
\overline{PD}	Power-Down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 5-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 5-1: GENERAL FORMAT FOR INSTRUCTIONS

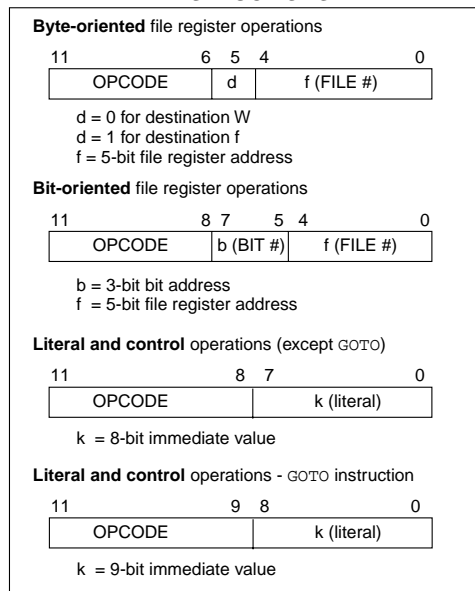


TABLE 5-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands	Description	Cycles	12-Bit Opcode			Status Affected	Notes
			MSb	LSb			
ADDWF f, d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF f, d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF f	Clear f	1	0000	011f	ffff	Z	4
CLRWF –	Clear W	1	0000	0100	0000	Z	
COMF f, d	Complement f	1	0010	01df	ffff	Z	
DECf f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ f, d	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
INCF f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ f, d	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
IORWF f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF f	Move W to f	1	0000	001f	ffff	None	1,4
NOP –	No Operation	1	0000	0000	0000	None	
RLF f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2,4
RRF f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2,4
SUBWF f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTfSC f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTfSS f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS							
ANDLW k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT k	Clear Watchdog Timer	1	0000	0000	0100	<u>TO, PD</u>	
GOTO k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION k	Load OPTION register	1	0000	0000	0010	None	
RETLW k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP –	Go into standby mode	1	0000	0000	0011	<u>TO, PD</u>	
TRIS f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for **GOTO**. (See individual device data sheets, Memory Section/Indirect Data Addressing, **INDF** and **FSR** Registers)

- When an I/O register is modified as a function of itself (e.g. **MOVf PORTB, 1**), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction **TRIS f**, where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of **PORTA** or **B** respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.
- If this instruction is executed on the **TMR0** register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to **TMR0**).

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ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff
------	------	------

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ADDWF FSR, 0

Before Instruction

W = 0x17
FSR = 0xC2

After Instruction

W = 0xD9
FSR = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0001	01df	ffff
------	------	------

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF FSR, 1

Before Instruction

W = 0x17
FSR = 0xC2

After Instruction

W = 0x17
FSR = 0x02

ANDLW **And literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \leq k \leq 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

1110	kkkk	kkkk
------	------	------

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW 0x5F

Before Instruction

W = 0xA3

After Instruction

W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

0100	bbbb	ffff
------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 31
 0 ≤ b ≤ 7

Operation: 1 → (f)

Status Affected: None

Encoding:

0101	bbbbf	ffff
------	-------	------

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example: BSF FLAG_REG, 7

Before Instruction
 FLAG_REG = 0x0A

After Instruction
 FLAG_REG = 0x8A

BTFSF **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSF f,b

Operands: 0 ≤ f ≤ 31
 0 ≤ b ≤ 7

Operation: skip if (f) = 1

Status Affected: None

Encoding:

0111	bbbbf	ffff
------	-------	------

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.

 If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE BTFSF FLAG, 1
 FALSE GOTO PROCESS_CODE
 TRUE •
 •
 •

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0,
 PC = address (FALSE);
 if FLAG<1> = 1,
 PC = address (TRUE)

BTFSF **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSF f,b

Operands: 0 ≤ f ≤ 31
 0 ≤ b < 7

Operation: skip if (f) = 1

Status Affected: None

Encoding:

0111	bbbbf	ffff
------	-------	------

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.

 If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE BTFSF FLAG, 1
 FALSE GOTO PROCESS_CODE
 TRUE •
 •
 •

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0,
 PC = address (FALSE);
 if FLAG<1> = 1,
 PC = address (TRUE)

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0,
 PC = address (FALSE);
 if FLAG<1> = 1,
 PC = address (TRUE)

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CALL Subroutine Call

Syntax: [*label*] CALL *k*

Operands: $0 \leq k \leq 255$

Operation: (PC) + 1 → Top of Stack;
k → PC<7:0>;
 (STATUS<6:5>) → PC<10:9>;
 0 → PC<8>

Status Affected: None

Encoding:

1001	kkkk	kkkk
------	------	------

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.

Words: 1

Cycles: 2

Example: HERE CALL THERE

Before Instruction
 PC = address (HERE)

After Instruction
 PC = address (THERE)
 TOS = address (HERE + 1)

CLRF Clear f

Syntax: [*label*] CLRF *f*

Operands: $0 \leq f \leq 31$

Operation: 00h → (f);
 1 → Z

Status Affected: Z

Encoding:

0000	011f	ffff
------	------	------

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example: CLRF FLAG_REG

Before Instruction
 FLAG_REG = 0x5A

After Instruction
 FLAG_REG = 0x00
 Z = 1

CLRW Clear W

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
 1 → Z

Status Affected: Z

Encoding:

0000	0100	0000
------	------	------

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example: CLRW

Before Instruction
 W = 0x5A

After Instruction
 W = 0x00
 Z = 1

CLRWDW Clear Watchdog Timer

Syntax: [*label*] CLRWDW

Operands: None

Operation: 00h → WDT;
 0 → WDT prescaler (if assigned);
 1 → \overline{TO} ;
 1 → PD

Status Affected: \overline{TO} , PD

Encoding:

0000	0000	0100
------	------	------

Description: The CLRWDW instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits \overline{TO} and PD are set.

Words: 1

Cycles: 1

Example: CLRWDW

Before Instruction
 WDT counter = ?

After Instruction
 WDT counter = 0x00
 WDT prescale = 0
 \overline{TO} = 1
 PD = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0010	01df	ffff
------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: COMF REG1, 0

Before Instruction

REG1 = 0x13

After Instruction

REG1 = 0x13

W = 0xEC

DECf **Decrement f**

Syntax: [*label*] DECf f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0000	11df	ffff
------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: DECf CNT, 1

Before Instruction

CNT = 0x01

Z = 0

After Instruction

CNT = 0x00

Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow d$; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff
------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
 If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE DECFSZ CNT, 1
 GOTO LOOP
 CONTINUE
 •
 •
 •

Before Instruction

PC = address (HERE)

After Instruction

CNT = CNT - 1;
 if CNT = 0,
 PC = address (CONTINUE);
 if CNT \neq 0,
 PC = address (HERE+1)

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \leq k \leq 511$

Operation: $k \rightarrow \text{PC}\langle 8:0 \rangle$;
 $\text{STATUS}\langle 6:5 \rangle \rightarrow \text{PC}\langle 10:9 \rangle$

Status Affected: None

Encoding:

101k	kkkk	kkkk
------	------	------

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits $\langle 8:0 \rangle$. The upper bits of PC are loaded from STATUS $\langle 6:5 \rangle$. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example: GOTO THERE

After Instruction

PC = address (THERE)

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INCF Increment f

Syntax: [*label*] INCF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0010	10df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: INCF CNT, 1

Before Instruction

CNT = 0xFF
Z = 0

After Instruction

CNT = 0x00
Z = 1

INCFSZ Increment f, Skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{dest})$, skip if result = 0

Status Affected: None

Encoding:

0011	11df	ffff
------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, then the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example: HERE INCFSZ CNT, 1
GOTO LOOP
CONTINUE
•
•
•

Before Instruction

PC = address (HERE)

After Instruction

CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT \neq 0,
PC = address (HERE + 1)

IORLW Inclusive OR literal with W

Syntax: [*label*] IORLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. (k) \rightarrow (W)$

Status Affected: Z

Encoding:

1101	kkkkk	kkkkk
------	-------	-------

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: IORLW 0x35

Before Instruction

W = 0x9A

After Instruction

W = 0xBF
Z = 0

IORWF Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{dest})$

Status Affected: Z

Encoding:

0001	00df	ffff
------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: IORWF RESULT, 0

Before Instruction

RESULT = 0x13
W = 0x91

After Instruction

RESULT = 0x13
W = 0x93
Z = 0

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

0010	00dF	ffff
------	------	------

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: MOVF FSR, 0

After Instruction
 W = value in FSR register

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \leq k \leq 255$

Operation: k → (W)

Status Affected: None

Encoding:

1100	kkkk	kkkk
------	------	------

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.

Words: 1

Cycles: 1

Example: MOVLW 0x5A

After Instruction
 W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

0000	001f	ffff
------	------	------

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example: MOVWF TEMP_REG

Before Instruction
 TEMP_REG = 0xFF
 W = 0x4F

After Instruction
 TEMP_REG = 0x4F
 W = 0x4F

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000
------	------	------

Description: No operation.

Words: 1

Cycles: 1

Example: NOP

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OPTION Load OPTION Register

Syntax: [label] OPTION
 Operands: None
 Operation: (W) → OPTION
 Status Affected: None
 Encoding:

0000	0000	0010
------	------	------

 Description: The content of the W register is loaded into the OPTION register.

Words: 1
 Cycles: 1
 Example: OPTION
 Before Instruction
 W = 0x07
 After Instruction
 OPTION = 0x07

RETLW Return with Literal in W

Syntax: [label] RETLW k
 Operands: $0 \leq k \leq 255$
 Operation: $k \rightarrow (W)$;
 TOS → PC
 Status Affected: None
 Encoding:

1000	kkkk	kkkk
------	------	------

 Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

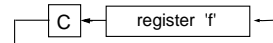
Words: 1
 Cycles: 2
 Example: CALL TABLE ;W contains
 ;table offset
 ;value.
 • ;W now has table
 • ;value.
 •
 •
 TABLE ADDWF PC ;W = offset
 RETLW k1 ;Begin table
 RETLW k2 ;
 •
 •
 •
 RETLW kn ; End of table
 Before Instruction
 W = 0x07
 After Instruction
 W = value of k8

RLF Rotate Left f through Carry

Syntax: [label] RLF f,d
 Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
 Operation: See description below
 Status Affected: C
 Encoding:

0011	01df	ffff
------	------	------

 Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1
 Cycles: 1
 Example: RLF REG1,0

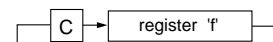
Before Instruction
 REG1 = 1110 0110
 C = 0
 After Instruction
 REG1 = 1110 0110
 W = 1100 1100
 C = 1

RRF Rotate Right f through Carry

Syntax: [label] RRF f,d
 Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
 Operation: See description below
 Status Affected: C
 Encoding:

0011	00df	ffff
------	------	------

 Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1
 Cycles: 1
 Example: RRF REG1,0

Before Instruction
 REG1 = 1110 0110
 C = 0
 After Instruction
 REG1 = 1110 0110
 W = 0111 0011
 C = 0

SLEEP **Enter SLEEP Mode**

Syntax: *[label]* SLEEP

Operands: None

Operation: 00h → WDT;
 0 → WDT prescaler;
 1 → \overline{TO} ;
 0 → PD

Status Affected: \overline{TO} , \overline{PD}

Encoding:

0000	0000	0011
------	------	------

Description: Time-out status bit (\overline{TO}) is set. The power down status bit (\overline{PD}) is cleared. The WDT and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP

SUBWF **Subtract W from f**

Syntax: *[label]* SUBWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{dest})$

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff
------	------	------

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1, 1

Before Instruction
 REG1 = 3
 W = 2
 C = ?

After Instruction
 REG1 = 1
 W = 2
 C = 1 ; result is positive

Example 2:

Before Instruction
 REG1 = 2
 W = 2
 C = ?

After Instruction
 REG1 = 0
 W = 2
 C = 1 ; result is zero

Example 3:

Before Instruction
 REG1 = 1
 W = 2
 C = ?

After Instruction
 REG1 = FF
 W = 2
 C = 0 ; result is negative

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SWAPF Swap Nibbles in f

Syntax: [label] SWAPF f,d
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)
Status Affected: None
Encoding:

0011	10df	ffff
------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.
Words: 1
Cycles: 1
Example SWAPF REG1, 0
Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0x5A

TRIS Load TRIS Register

Syntax: [label] TRIS f
Operands: f = 5, 6 or 7
Operation: (W) → TRIS register f
Status Affected: None
Encoding:

0000	0000	0fff
------	------	------

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register
Words: 1
Cycles: 1
Example TRIS PORTA
Before Instruction
W = 0xA5
After Instruction
TRISA = 0xA5

XORLW Exclusive OR literal with W

Syntax: [label] XORLW k
Operands: $0 \leq k \leq 255$
Operation: (W) .XOR. k → (W)
Status Affected: Z
Encoding:

1111	kkkk	kkkk
------	------	------

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words: 1
Cycles: 1
Example XORLW 0xAF
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF Exclusive OR W with f

Syntax: [label] XORWF f,d
Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
Operation: (W) .XOR. (f) → (dest)
Status Affected: Z
Encoding:

0001	10df	ffff
------	------	------

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words: 1
Cycles: 1
Example XORWF REG,1
Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

6.0 PIC16HV540 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16HV540 Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16HV540 family of devices, there is one device type, as indicated in the device number:

1. **HV**, as in PIC16HV540A. Refer to PIC16C5X data sheet (DS30453A) for an explanation of how to access these bits. These devices have EPROM program memory and operate over the standard voltage range of 3.5 to 13 volts.

6.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16HV540. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

6.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

6.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

6.4 Serialized Quick-Turnaround-Production (SQTPSM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

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7.0 ELECTRICAL CHARACTERISTICS - PIC16HV540

Absolute Maximum Ratings[†]

Ambient temperature under bias	-20°C to +85°C
Storage temperature	- 65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +16V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} ⁽²⁾	0 to +14V
Voltage on all other pins with respect to V _{SS}	-0.6V to (V _{DD} + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Max. current out of V _{SS} pin.....	150 mA
Max. current into V _{DD} pin.....	100 mA
Max. current into an input pin (TOCKI only).....	±500 µA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	±20 mA
Max. output current sunk by any I/O pin.....	25 mA
Max. output current sourced by any I/O pin.....	10 mA
Max. output current sourced by a single I/O port (PORTA or B).....	40 mA
Max. output current sunk by a single I/O port (PORTA or B).....	50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to V_{SS}

[†] NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

7.1 DC Characteristics: **PIC16HV540-04, 20 (Commercial)** **PIC16HV540-04I, 20I (Industrial)**

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified)					
	Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage HS, XT, RC and LP options	VDD	3.5		15	V	
RAM Data Retention Voltage⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05 VDD			V/ms	See section on Power-On Reset for details
Supply Current⁽³⁾ HS, XT and RC ⁽⁴⁾ options LP option, Commercial	IDD		0.5 11	27	mA μA	FOSC = 4.0 MHz, VDD = 15V FOSC = 32 kHz, VDD = 15V, WDT disabled
Power Down Current⁽⁵⁾⁽⁶⁾ Commercial Industrial	IPD		4 0.25 5 0.3	12 4.0 14 5.0	μA μA μA μA	VDD = 15V, sleep timer enabled VDD = 15V, sleep timer disabled VDD = 15V, sleep timer enabled VDD = 15V, sleep timer disabled
Brown-Out Detector Threshold	V		3.1		V	5V Core
Brown-Out Detector Threshold	V		2.2		V	3V Core

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.
- 6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is exited or during initial power-up.

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7.2 DC Characteristics: PIC16HV540-04, 20 (Commercial) PIC16HV540-04I, 20I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature		0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)			
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
Input Low Voltage	V _{IL}						
I/O Ports PORTA		V _{SS}		0.15 V _{IO}	V	Pin at hi-impedance	
MCLR (Schmitt Trigger)		V _{SS}		0.15 V _{IO}	V		
T0CKI (Schmitt Trigger)		V _{SS}		0.15 V _{IO}	V		
OSC1 (Schmitt Trigger)		V _{SS}		0.15 V _{IO}	V		RC option only ⁽⁴⁾
OSC1		V _{SS}		0.3 V _{IO}	V		HS, XT and LP options
I/O Ports PORTB		V _{SS}		TBD	V		
Input High Voltage	V _{IH}						
I/O Ports PORTA		0.25 V _{IO} +0.8V		V _{IO}	V	For all V _{IO} ⁽⁵⁾	
MCLR (Schmitt Trigger)		0.85 V _{IO}		V _{DD}	V		
T0CKI (Schmitt Trigger)		0.85 V _{IO}		V _{DD}	V		
OSC1 (Schmitt Trigger)		0.85 V _{IO}		V _{DD}	V		RC option only ⁽⁴⁾
OSC1		0.7 V _{IO}		V _{IO}	V		XT and LP options
I/O Ports PORTB		TBD		TBD	V		HS, XT and LP options
Hysteresis of Schmitt Trigger inputs	V _{HYS}	0.15 V _{IO} *			V		
Input Leakage Current⁽³⁾	I _{IL}						
I/O Ports		-1.0	0.5	+1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at hi-impedance	
MCLR		-5.0		+5.0	μA	V _{PIN} = V _{SS} + 0.25V ⁽²⁾	
T0CKI		-3.0	0.5	+3.0	μA	V _{PIN} = V _{DD} ⁽²⁾	
OSC1		-3.0	0.5	+3.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}	
RB7			TBD		μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , HS, XT and LP options	
						Sleep mode, WPC enabled	
Output Low Voltage	V _{OL}						
I/O Ports PORTA				0.6	V	V _{DD} = 15V, V _{IO} = 5V, I _{OL} = 8.7 mA	
OSC2/CLKOUT				0.6	V	V _{DD} = 15V, V _{IO} = 5V, I _{OL} = 5 mA	
						V _{DD} = 15V, V _{IO} = 5V, I _{OL} = 2.8 mA	
						V _{DD} = 15V, V _{IO} = 5V, I _{OL} = 1.5 mA	
I/O ports PORT B				0.6	V	RC option only	
						V _{DD} = 15V, I _{OL} = 8.7 mA, V _{IO} = 5V	
Output High Voltage	V _{OH}						
I/O Ports ⁽³⁾ PORTA		V _{IO} -0.7			V	V _{DD} = 15V, V _{IO} = 3V, I _{OH} = -2 mA	
						V _{DD} = 15V, V _{IO} = 5V, I _{OH} = -5.4 mA	
OSC2/CLKOUT		V _{IO} -0.7			V	V _{DD} = 15V, V _{IO} = 3V, I _{OH} = -0.5 mA	
						V _{DD} = 15V, V _{IO} = 5V, I _{OH} = -1.0 mA	
I/O Ports PORTB		V _{DD} -0.7			V	RC option only	
						V _{DD} = 15V, I _{OH} = -8 mA, V _{IO} = 5V	
Threshold Voltage							
I/O Ports PORTB [7]	V _{LEV}	TBD	V _{DD} -1.0	TBD	V	Slowly rising input detect level	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16HV540 be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

7.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

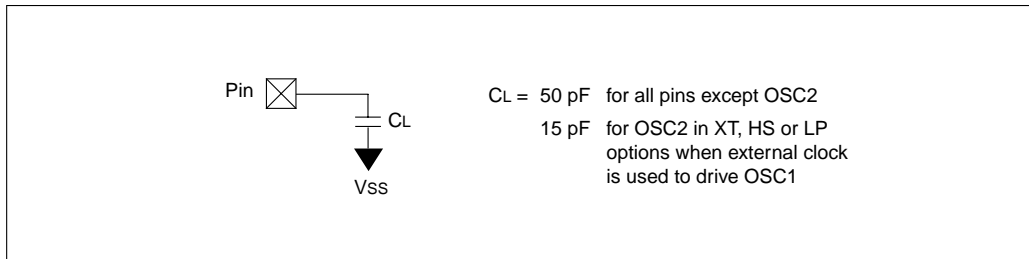
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 7-1: LOAD CONDITIONS - PIC16HV540



PIC16HV540

7.4 Timing Diagrams and Specifications

FIGURE 7-2: EXTERNAL CLOCK TIMING - PIC16HV540

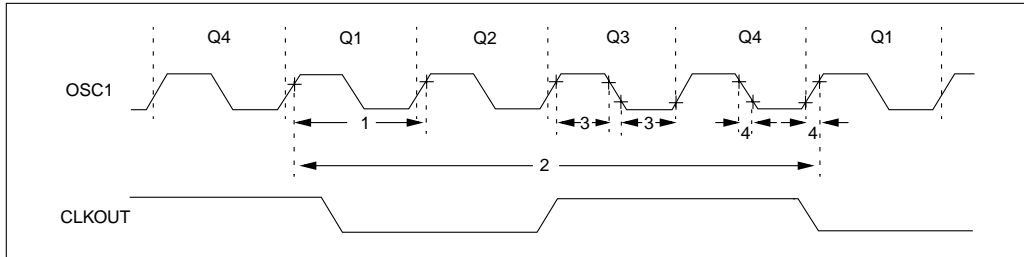


TABLE 7-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16HV540

AC Characteristics		Standard Operating Conditions (unless otherwise specified)						
		Operating Temperature						
		0°C ≤ TA ≤ +70°C (commercial),						
		-40°C ≤ TA ≤ +85°C (industrial)						
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
	Fosc	External CLKIN Frequency ⁽²⁾	DC	—	4.0	MHz	RC osc mode	
			DC	—	20	MHz	HS osc mode	
			DC	—	4.0	MHz	XT osc mode	
			DC	—	200	kHz	LP osc mode	
			Oscillator Frequency ⁽²⁾	DC	—	4.0	MHz	RC osc mode
				0.1	—	20	MHz	HS osc mode
				0.1	—	4.0	MHz	XT osc mode
				5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period ⁽²⁾	250	—	—	ns	RC osc mode	
			250	—	—	ns	HS osc mode	
			250	—	—	ns	XT osc mode	
			5.0	—	—	μs	LP osc mode	
		Oscillator Period ⁽²⁾	250	—	—	ns	RC osc mode	
			250	—	10,000	ns	HS osc mode	
			250	—	10,000	ns	XT osc mode	
			5.0	—	200	μs	LP osc mode	
2	Tcy	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—	—		
3	TosL, TosH	Clock in (OSC1) Low or High Time	50	—	—	ns	HS osc mode	
			50*	—	—	ns	XT oscillator	
			2.0*	—	—	μs	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	HS osc mode	
			—	—	25*	ns	XT oscillator	
			—	—	50*	ns	LP oscillator	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at VIO = 5V, VDD = 9V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

FIGURE 7-3: CLKOUT AND I/O TIMING - PIC16HV540

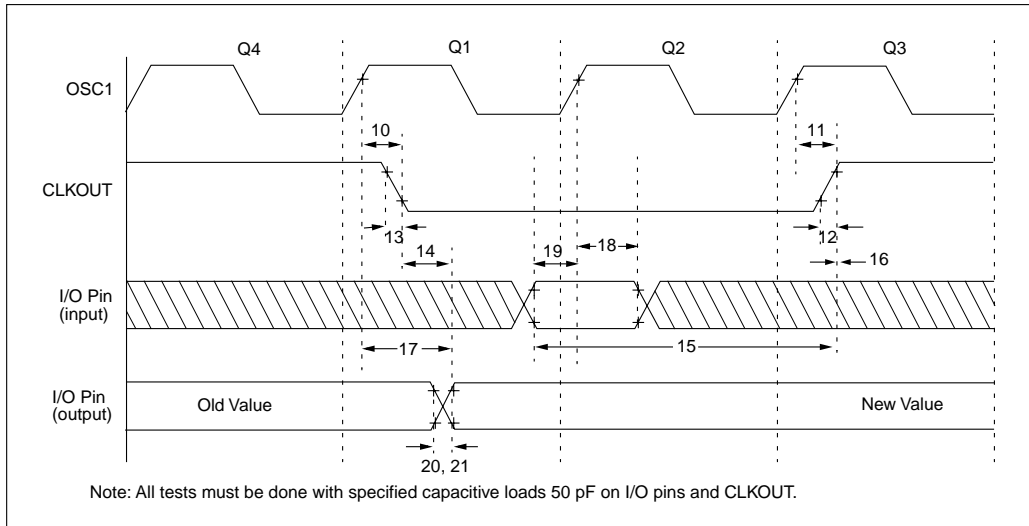


TABLE 7-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16HV540

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), -40°C ≤ TA ≤ +85°C (industrial).				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽²⁾	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽²⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽³⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at V_{IO} = 5V, V_{DD} = 9V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 7-1 for loading conditions.

PIC16HV540

FIGURE 7-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16HV540

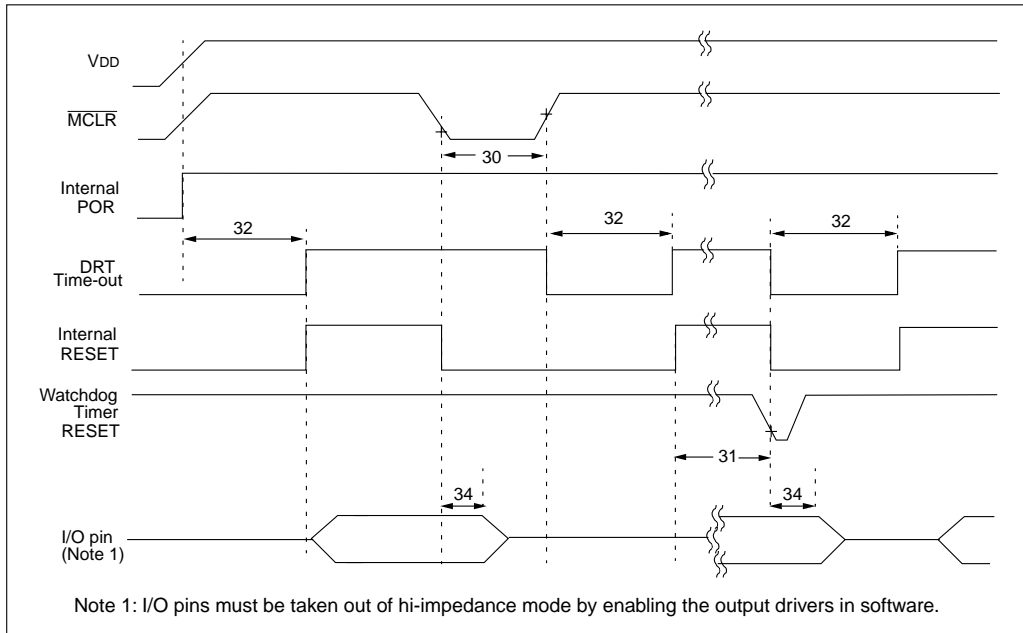


TABLE 7-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16HV540

AC Characteristics Standard Operating Conditions (unless otherwise specified)							
		Operating Temperature		0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)			
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	—	2	—	μs	VDD = 15V, VIO = 5V
31	Twdt	Watchdog Timer Time-out Period	9.0*	18*	40*	ms	VDD = 15V, VIO = 5V
32	TDRT	Device Reset Timer Period	9.0* 0.55*	18* 1.1*	30* 2.5	ms	VDD = 15V, VIO = 5V, RC mode
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	100*	ns	
—	Tpc	Pin Change Pulse Width	—	2	—	μs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at VIO = 5V, VDD = 9V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 7-5: TIMER0 CLOCK TIMINGS - PIC16HV540

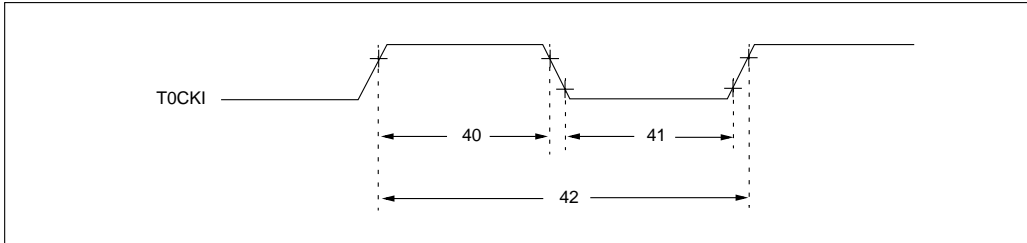


TABLE 7-4: TIMER0 CLOCK REQUIREMENTS - PIC16HV540

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 T _{CY} + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 T _{CY} + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16HV540

8.0 DC AND AC CHARACTERISTICS - PIC16HV540

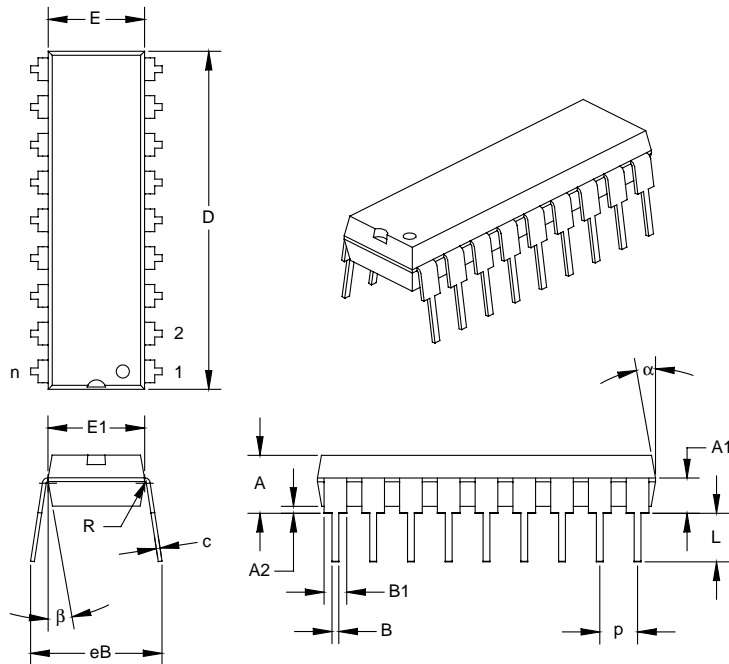
The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

Not available at this time.

9.0 PACKAGING INFORMATION

Package Type: K04-007 18-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits			0.300			7.62	
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.010	0.015	0.13	0.25	0.38
Top to Seating Plane	A	0.110	0.155	0.155	2.79	3.94	3.94
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41	2.92
Base to Seating Plane	A2	0.000	0.020	0.020	0.00	0.51	0.51
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.890	0.895	0.900	22.61	22.73	22.86
Molded Package Width	E‡	0.245	0.255	0.265	6.22	6.48	6.73
Radius to Radius Width	E1	0.230	0.250	0.270	5.84	6.35	6.86
Overall Row Spacing	eB	0.310	0.349	0.387	7.87	8.85	9.83
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

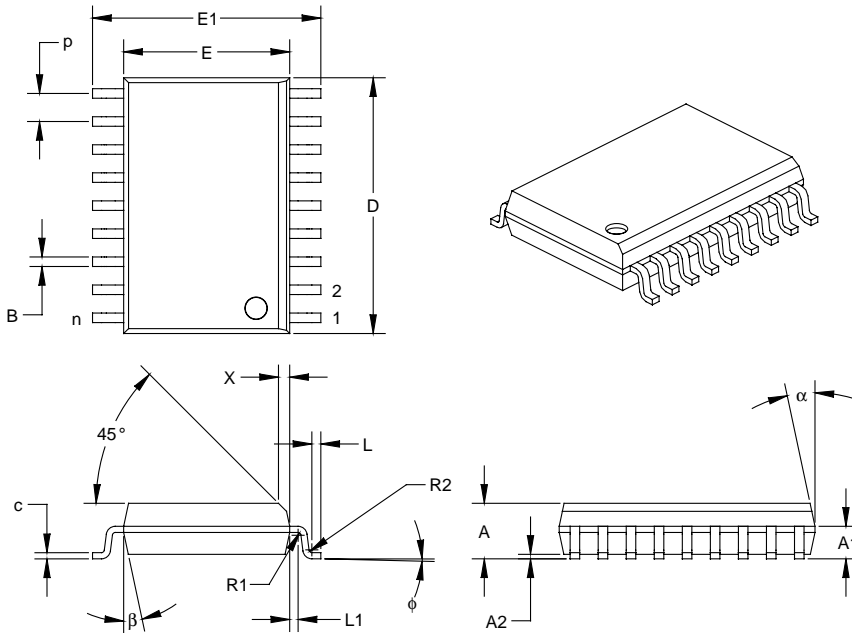
* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16HV540

Package Type: K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		18			18	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D [‡]	0.450	0.456	0.462	11.43	11.58	11.73
Molded Package Width	E [‡]	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B [†]	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

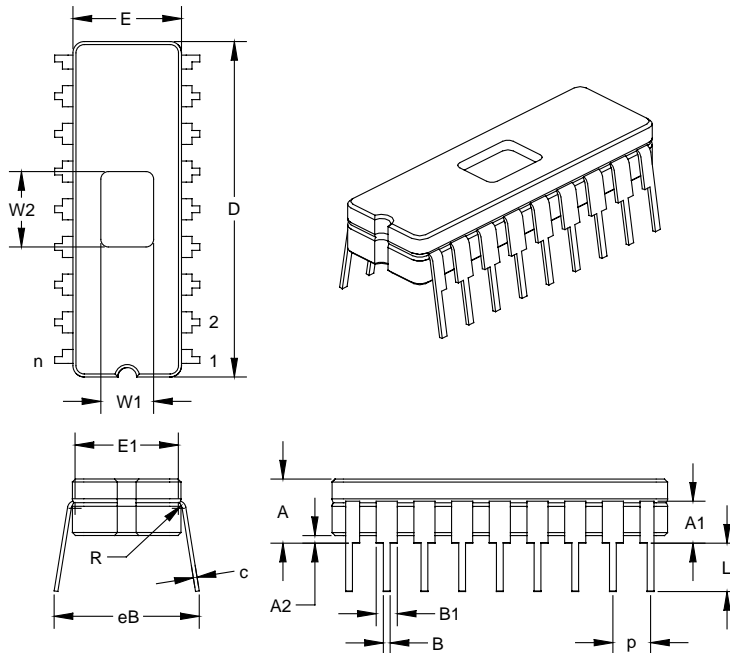
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16HV540

Package Type: K04-010 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil

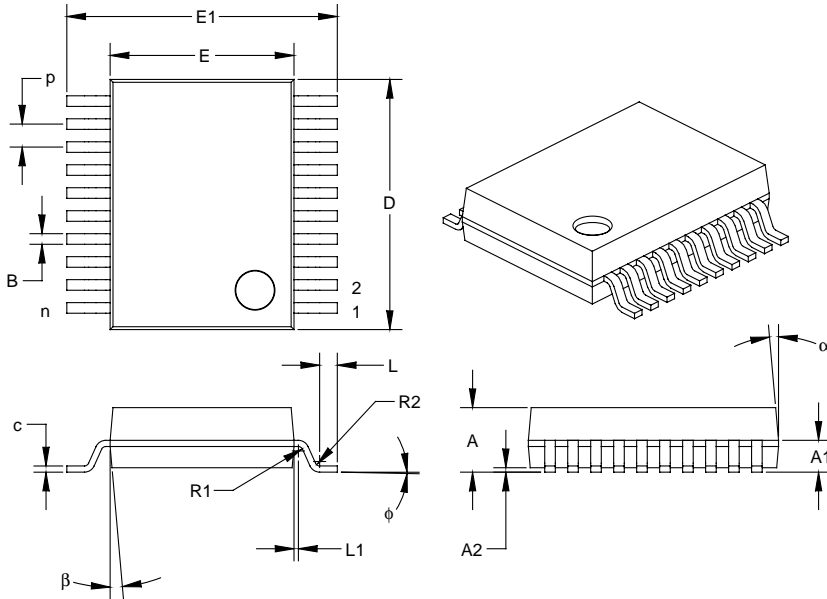


Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Shoulder Radius	R	0.010	0.013	0.015	0.25	0.32	0.38
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.175	0.183	0.190	4.45	4.64	4.83
Top of Lead to Seating Plane	A1	0.091	0.111	0.131	2.31	2.82	3.33
Base to Seating Plane	A2	0.015	0.023	0.030	0.00	0.57	0.76
Tip to Seating Plane	L	0.125	0.138	0.150	3.18	3.49	3.81
Package Length	D	0.880	0.900	0.920	22.35	22.86	23.37
Package Width	E	0.285	0.298	0.310	7.24	7.56	7.87
Radius to Radius Width	E1	0.255	0.270	0.285	6.48	6.86	7.24
Overall Row Spacing	eB	0.345	0.385	0.425	8.76	9.78	10.80
Window Width	W1	0.130	0.140	0.150	0.13	0.14	0.15
Window Length	W2	0.190	0.200	0.210	0.19	0.2	0.21

* Controlling Parameter.

PIC16HV540

Package Type: K04-072 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



Units		INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
Pitch	p		0.026			0.65	
Number of Pins	n		20			20	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D [†]	0.278	0.283	0.289	7.07	7.20	7.33
Molded Package Width	E [‡]	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	phi	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B [†]	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	alpha	0	5	10	0	5	10
Mold Draft Angle Bottom	beta	0	5	10	0	5	10

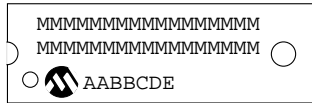
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

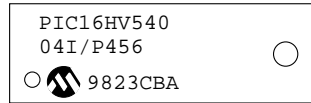
‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

9.1 Package Marking Information

18-Lead PDIP



Example



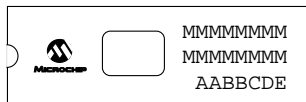
18-Lead SOIC



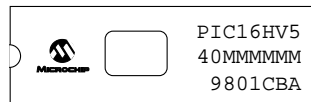
Example



18-Lead CERDIP Windowed



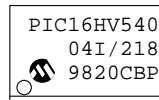
Example



20-Lead SSOP



Example



Legend: MM...M	Microchip part number information
XX...X	Customer specific information*
AA	Year code (last 2 digits of calendar year)
BB	Week code (week of January 1 is week '01')
C	Facility code of the plant at which wafer is manufactured
	O = Outside Vendor
	C = 5" Line
	S = 6" Line
	H = 8" Line
D	Mask revision number
E	Assembly code of the plant or country of origin in which part was assembled

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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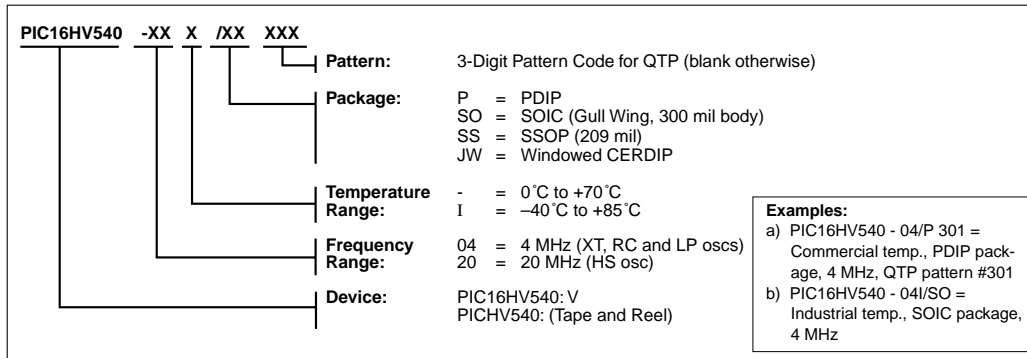
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