DS5026 ISSUE 2 August 1998

Features

- Parallel-to-serial and serial-to-parallel conversion of up to 1536 full duplex channels or 3072 time-slots
- Serial port data rates selectable between 2.048, 4.096 or 8.192 Mb/s
- Provides a mechanism for a double buffer function to be implemented in external memory
- 24 serial I/O lines programmable in different modes: 12 in/12 out at 8.192 Mb/s (1536 full duplex channels) or 24 bidirectional line modes for 2.048 and 4.096 Mb/s
- Provides a bidirectional 8-bit parallel port operating at 16.384 or 32.768 MByte/s for direct interface to external memory (dual port)
- Provides an external 13-bit output address bus for direct connection with an 8K-position dual port memory
- JTAG boundary scan

Applications

- Fast access to ST-BUS, SCSA, MVIP, and H-MVIP serial backplanes
- Voice processing cards for Computer Telephony Integration (CTI)
- Video and teleconferencing bridge cards
- Fast DSP access to serial TDM buses

Ordering Information

MT90210AL 100 Pin PQFP

-40 to +85°C

Description

The MT90210 is a 100-pin device used to interface a parallel bidirectional 8 bit bus to 24 time division multiplexed (TDM) serial streams. The device is configured to perform simultaneous parallel-to-serial and serial-to-parallel conversion with the capability of handling up to 3072 channels, 1536 on the transmit and 1536 on the receive direction. Depending on the operation mode selected at the mode pins, the individual 64 Kb/s channels on the serial links may be configured as inputs or outputs. The data on the parallel bus is in a format suitable for interfacing with a dual-port RAM. Depending on the data rate selected by the MD0-MD2 input pins, serial data is clocked in and out on the serial streams at either 2.048, 4.096 or 8.192 Mb/s.

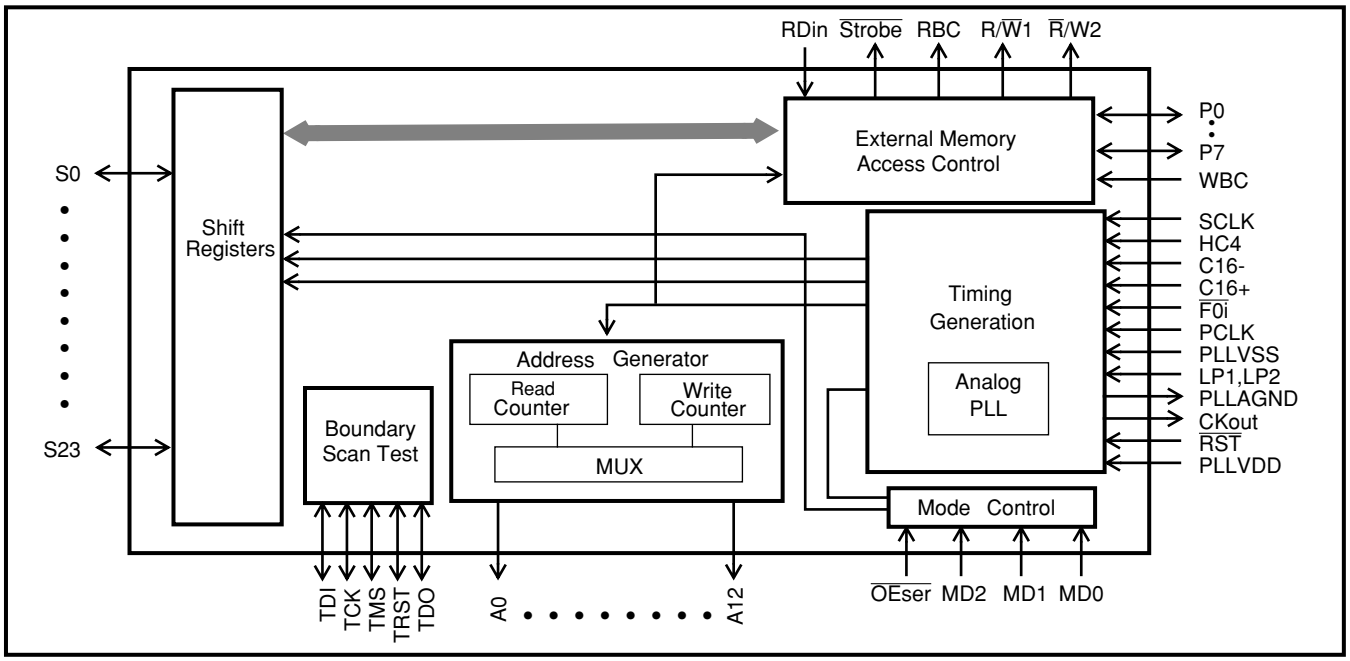
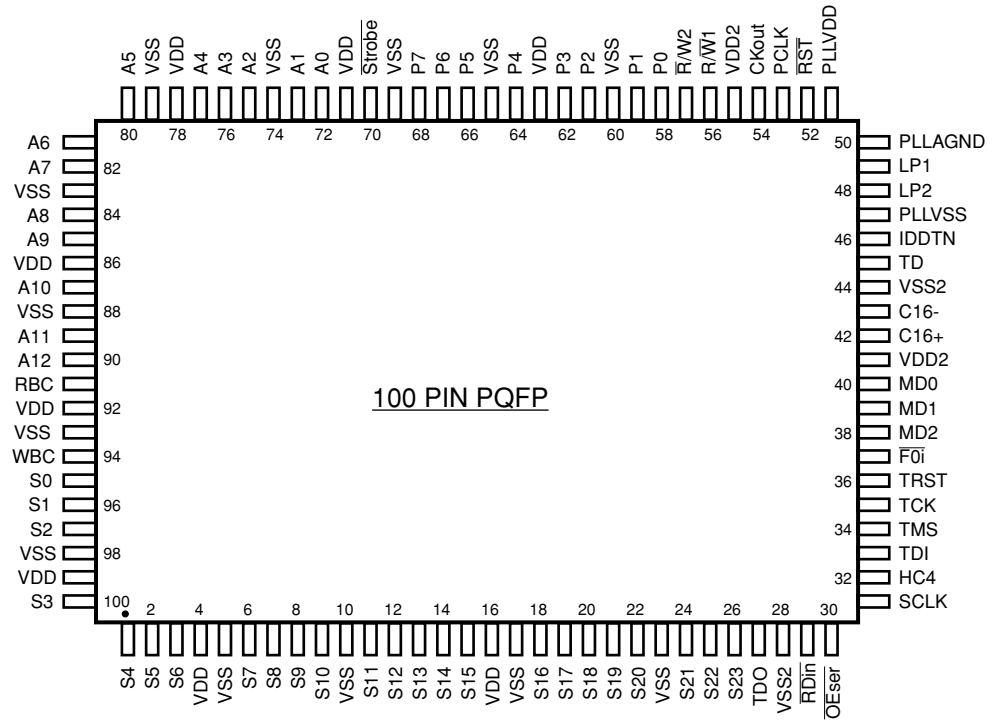


Figure 1 - Functional Block Diagram



Note: the PQFP package meets the JEDEC standard MO-108, CC1.
Critical dimensions:
Lead pitch = 0.65mm,
Body Size = 14mm x 20mm,
Package size = 17.9mm x 23.9mm.

Figure 2 - Pin Connections

Pin Description

Pin	Name	Description
95-97, 100, 1-3, 6	S0-S2, S3, S4-S6, S7	**Serial Lines 0-7** (TTL compatible with internal pullups in the range 25 - 125kΩ). Bidirectional, time division multiplexed serial streams. According to mode selected by MD0-2 inputs, distinct data rates can be selected at the serial port. In mode 3, these lines are configured as inputs only. In modes 1, 2, 4 and 5, these lines become bidirectional.
7-9, 11-15	S8-S10, S11-S15	**Serial Lines 8-15**. See description for S0-S7 above. In mode 3, S8-S11 are inputs and S12-S15 are outputs. In modes 1, 2, 4 and 5 these are bidirectional lines.
18-22, 24-26	S16-S20 S21-S23	**Serial Lines 16-23.** See descripton for S0 - S7 above. For mode 3, these lines are outputs and operate at 8.192 Mb/s rates. When operating in modes 1, 2, 4 and 5, these lines are bidirectional.
27	TDO	**Boundary Scan Test Data Output.**
29	$\overline{\text{RDin}}$	**Read P0-P7 input clock**. This input is used by the MT90210 to sample bytes coming in at the parallel port P0-P7 lines. Typically, the user should connect CKout to this input.
30	$\overline{\text{OEser}}$	**Serial Port Output Enable (Input).** On the parallel-to serial conversion direction, this input is used by the MT90210 to know which time-slots on the serial output streams will be placed in high-impedance. This input is sampled synchronously along with the parallel input data before the parallel-to-serial conversion takes place. When low, output serial channels are actively driven. When set high, the output bus drivers are disabled.

Pin Description (continued)

Pin	Name	Description
31	SCLK	**Serial Port Clock (input)**. The SCLK clock is used to control the serial port operation in modes 1,2,3 and 4. Depending on the operation mode selected at the MD0-MD2 inputs, this input can accept 4.096 (MD2-0=000), 8.192 (MD2-0=001) or 16.384 (MD2-0 =010 and 011) MHz clock. In mode 5, this input is ignored.
32	HC4	**H-MVIP C4.** This is a 4.096 MHz clock utilized in modes 4 and 5 to maintain compatibility with existing MVIP-90 systems. It is utilized to sample the frame pulse input (F0i). Not used in Modes 1 - 3.
33	TDI	**Boundary Scan Test Data Input.**
34	TMS	**Boundary Scan Test Mode Select.**
35	TCK	**Boundary Scan Test Clock.**
36	TRST	**Boundary Scan Test Reset.**
37	$\overline{F0i}$	**Frame Synchronization Signal (TTL compatible input).** This input signal establishes the frame boundary for the serial input/output streams.
38-40	MD2-MD0	**Operation Mode Bits 0-2 (Input).** Selects the data rate for the time division, multiplexed serial streams. 2.048 (mode 1, MD2-0=000), 4.096 (mode 2, MD2-0=001) or 8.192 (mode 3, MD2-0=010) Mb/s data rates are available. When MD2-0 are set to 011 (mode 4), the MT90210 operates in mixed data rates mode where S16-23 operate at 8.192 Mb/s and the remaining serial streams run at 2.048 Mb/s. In mode 5 (MD2-0=100), the MT90210 operates as per mode 4 but the device will accept a differential clock reference at 16.384 MHz at pins C16+ and C16-.
42	C16+	**Serial Port Clock Input.** In mode 5 (MD2-0= 100), this is a 16.384 MHz differential signal. Note used in Modes 1 - 3.
43	C16-	**Serial Port Clock Input**. The complement to C16+.
45	TD	**Reserved** - Do not connect.
46	IDDTN	Connect to Ground.
47	PLLVSS	**PLL Ground Input.**
48	LP2	**Loop Filter Input.** An external RC circuit is required at this input, refer to Figure 10.
49	LP1	**Loop Filter Input.** An external RC circuit is required at this input, refer to Figure 10.
50	PLLAGND	**PLL Analog Ground output.** Provides ground to PLL loop filter, refer to Figure 10.
51	PLLVDD	**PLL Power Input.** +5V
52	$\overline{RST}$	**RESET.** A low on this pin resets the device.
53	PCLK	**Parallel Port Clock Input**. CKout must be connected to this input.
54	CKout	**Internal VCO Output Signal.** Output of internal PLL frequency multiplier. In mode 1 the frequency is 16.384 MHz, for the other modes the frequency is 32.768 MHz. Must be connected to PCLK only.
56	R/$\overline{W}$1	**Read/Write Output 1.** This output signal toggles low for the last half of a memory write cycle indicating valid data.
57	$\overline{R}$/W2	**Read/Write Output 2.** This output is low for memory read operations and high for memory write operations.

Pin Description (continued)

Pin	Name	Description
58-59, 61-62, 64, 66-68	P0-P1, P2-P3, P4, P5-P7	**Parallel Input/Output Data Bus.** This 8 bit data bus is a bidirectional parallel port used to perform 8-bit transactions between the MT90210 and the external dual port RAM. Data is clocked in and out of the P0-P7 parallel port according to Figures 22 and 23.
70	$\overline{\text{Strobe}}$	**Strobe Output.** This output is typically connected to the Chip-enable input of the external dual port RAM. It is kept low during all read cycles, stays high during inactive periods and goes low for the last half of a memory write cycle.
72-73, 75- 77, 80-82, 84-85, 87, 89-90	A0-A1, A2-A4, A5-A7, A8-A9, A10, A11-A12	**External Memory Address Outputs A0-A12.** These 13 address output lines are provided by the MT90210 to allow a direct connection to an external dual port RAM.
91	RBC	**Read Data Block Complete (output)**. A transition on this output is used to notify the external CPU that the MT90210 has finished reading the contents of one entire 125µs frame from the external dual port memory (e.g.; from addresses 0000h to 0FFFh in modes 3, 4 or 5). Whenever RBC toggles, the MT90210 starts reading the next half of the memory (addresses 1000h to 1FFFh) while the local CPU updates the first half with more data to be sent. RBC toggles every 125µs. When this signal is low, the MT90210 is reading the lower memory block.
94	WBC	**Write Data Block Complete (Output).** A transition on this output is used to notify the external CPU that the MT90210 has finished writing the contents of one entire 125µs frame into the external dual port memory (e.g; from addresses 0000h to 0FFFh in modes 3,4 or 5). Once WBC toggles, the local CPU can access the Dual port memory to get the data while the MT90210 writes the contents of the next 125µs frame into the other half (addresses 1000h to 1FFFh) of the dual port memory. WBC toggles every 125µs. When this signal is low, the MT90210 is writing to the lower memory block.
4,16, 63, 71, 78, 86, 92, 99	V_{DD}	**Supply Input.** +5V.
41, 55	V_{DD2}	**Supply Input.** +5V.
5,10, 17, 23, 60, 65, 69, 74, 79,83, 88, 93, 98	V_{SS}	**Ground.**
28	V_{SS2}	**Ground.**

Functional Description

The MT90210 is a 100-pin device that converts incoming serial telecom streams of 2.048, 4.096 or 8.192 Mb/s on to an 8-bit parallel bus, and converts input data on this parallel bus to the outgoing serial telecom links. The device is configured to perform simultaneous parallel-to-serial and serial-to-parallel conversion.

MT90210 interfaces up to 24 bidirectional serial data streams to a byte oriented parallel port for access by a dual-port RAM. It contains an address generator for parallel port read and write operations directly to an external dual port memory. A single MT90210 device can handle up to 3072 channels, 1536 on the transmit and 1536 on the receive direction.

Depending on the operation mode selected at the mode pins (MD0-MD2), the 64 kb/s serial telecom channels may be configured as inputs or outputs. The data on the parallel bus is in a format suitable for interfacing with popular dual port memories. Depending on the data rate selected by the MD0-MD2 input pins, serial data is clocked in and out on the serial streams at either 2.048, 4.096 or 8.192 Mb/s, as shown in Figure 6. A mechanism for implementing external double buffering is provided by the Write Block Complete (WBC) and Read Block Complete (RBC) output pins. Double buffering the data allows the processor to independently access an entire frame of data in the external memory while the MT90210 reads or writes the complementary frame in the memory. For example, in mode 3 (Figure 4), during the first frame the MT90210 will read and write in to the first half of the memory space (Block 0) and during the second frame the MT90210 will read and write in to the second half of the memory space (Block 1). Within each block the transmit data and receive data are separated and located at fixed address locations. The operation of WBC and RBC is shown in Figures 7a and 7b.

On the external memory port side, the device performs 8-bit wide operations with a cycle time of 30 or 61 ns. The parallel port operates at 16.384 MByte/s (for mode 1) or 32.768 MByte/s (for modes 2,3,4 and 5). To create the high speed clock required to manage the byte operations at the parallel port, a built in PLL multiplies the serial port input clock (SCLK) by a factor of two or four depending on the mode. In all operation modes, the user should connect the PLL CKout to PCLK input.

A separate input pin, Output Enable serial ($\overline{\text{OEser}}$ pin 30), may be used to selectively tristate individual 64Kb/s serial links. By using a 9-bit external dual port RAM and connecting the ninth bit to $\overline{\text{OEser}}$ as shown in Figure 9, the processor may disable an individual channel by setting the ninth bit for that channel in the transmit (TX) portion of the current block. The remaining 8 bits for this channel may be any value since they are ignored by the MT90210 when the ninth bit is 1. To avoid contention on the serial bus, it is recommend that the user configure all serial streams as inputs at start-up. This may be done by setting all $\overline{\text{OEser}}$ bits to 1 in the TX portions of both memory blocks. In mode 3, the serial streams are permanently configured as 12 inputs and 12 outputs, and the state of $\overline{\text{OEser}}$ is ignored.

An Overview of CTI bus protocols

Multi-Vendor Integration Protocol (MVIP) provides a coherent approach to building solutions for worldwide markets by merging computing and communications technologies under one open architecture. MVIP ensures inter-operability among telephone-based resources (such as trunk interfaces, voice, video, fax, text-to-speech, speech recognition) for use within a computer chassis in an individual or networked configuration. H-MVIP addresses the need for higher telephony traffic capacity in individual computer chassis. H-MVIP defines three major items that together make a useful digital telephony transport and switching environment: the H-MVIP digital telephony bus with up to 3072 "time-slots" of 64 Kb/s each; a bus interface with digital switching that allows a group of H-MVIP interfaced circuit boards to provide complete, flexible, distributed telephony switching; and a logical device driver model and standard software interface to a logical model.

Operating Modes

The MT90210 device can operate in one of five modes appropriate for different application needs. Mode selection must be done while the device is in reset ($\overline{\text{RST}}$ low and a valid clock applied to the PCLK input). These modes are explained in the following paragraphs.

Mode 1: The serial input/output format conforms to the ST-BUS requirements when the data rate is 2.048 Mb/s (see Figure 6). Serial port clock (SCLK) is 4.096 MHz. The on-chip PLL produces a phase locked 16.384 MHz clock (CKout) from the SCLK input. In this data rate operation, the 24 serial lines (S0-23) become bidirectional links at 2.048 Mb/s. The ST-BUS is a time-division multiplexed serial bus with 32, 8-bit channels per frame. Frame boundaries are delineated by the frame pulse. Figure 3 depicts

how the data from the serial port is mapped into the external dual port memory.

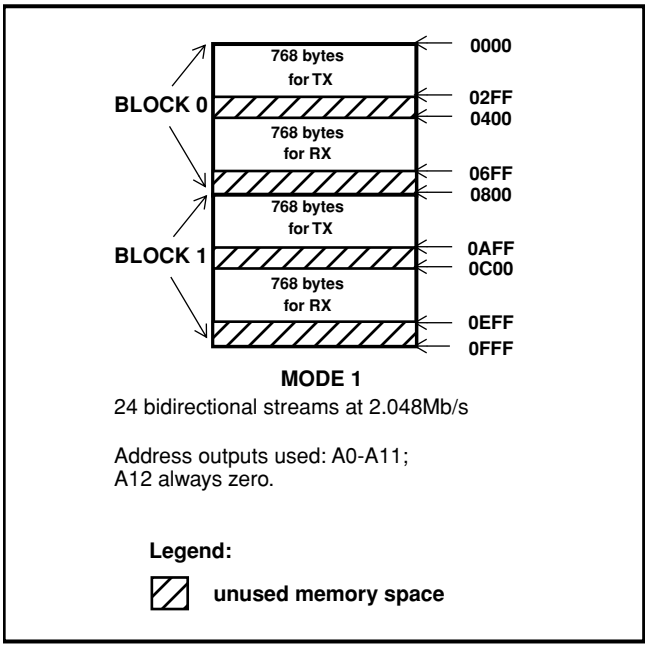


Figure 3 - Dual Port RAM Memory Map for Mode 1

Mode 2: When the device is configured for 4.096 Mb/s data rate operation, each of the 24 time-division multiplexed serial streams is made up of 64 channels. In this data rate operation, the 24 serial lines (S0-23) become bidirectional links at 4.096 Mb/s. Serial port clock (SCLK) is 8.192 MHz. The on-chip PLL produces a phase locked 32.768 MHz clock (CKout) from the SCLK input. Figure 4 depicts how the data from the serial port is mapped into the external dual port memory.

Mode 3: When the device is configured for 8.192 Mb/s data rate operation, each of the 24 time-division multiplexed serial streams is made up of 128 channels. In this mode, bidirectional operation on the serial port streams is not provided and the MT90210 is set in a 12 in / 12 out configuration and the $\overline{OE}$ser input is ignored. Streams S0-S11 are configured as inputs, and S12-S23 are configured as outputs. Serial port clock is 16.384 MHz. The on-chip PLL doubles this clock to produce a CKout clock of 32.768 MHz. Figure 4 depicts how the data from the serial port is mapped into the external dual port memory. Figure 12 and Table 3 show the write and read operations on the parallel port at the frame boundary.

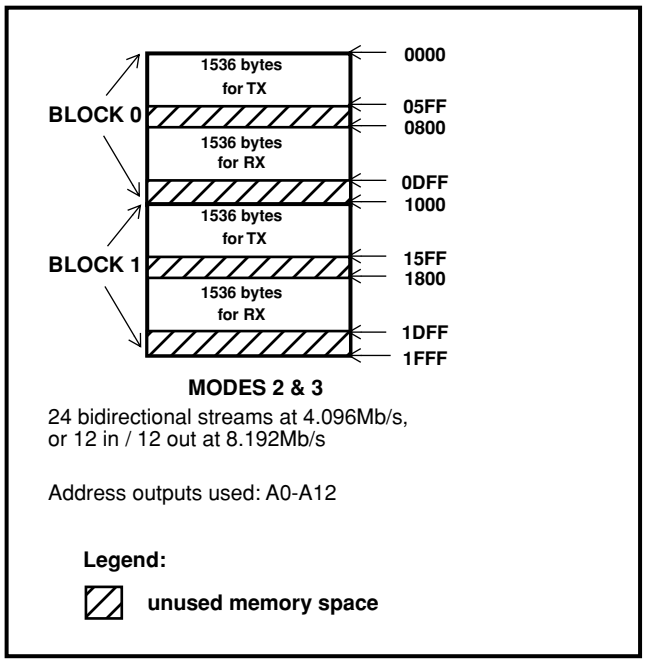


Figure 4 - Dual Port RAM Memory Map for Modes 2 and 3

Mode 4: The MT90210 is configured such that the 24 serial streams are bidirectional and split into two different functional groups: (i) streams S0-S15 operate at 2 Mb/s rate (512 timeslots), (ii) S16-S23 operate at 8.192 Mb/s rate (1024 timeslots). Memory mapping for mode 4 is described in Figure 5. For compatibility with legacy MVIP timing, mode 4 provides an additional clock input at 4.096 MHz (HC4 input pin) which allows the device to detect frame sync pulse ($\overline{F0i}$) with a typical width of 244 ns. In mode 4, the 16.384 (SCLK) and 4.096 (HC4) MHz clocks should be in sync according to H-MVIP specifications. The on-chip PLL doubles SCLK to produce a CKout signal of 32.768 MHz. Figure 13 and Table 4 show the write and read operations on the parallel port at the frame boundary.

Mode 5: Identical operation as per mode 4 with the difference that the 16.384 MHz clock is a differential signal received at the two input pins, C16+ and C16- of the MT90210 device. The differential clock is needed to eliminate distortion in the clock signal passing through a ribbon cable as per H-MVIP specification. The SCLK input is not used in this mode. Memory mapping for mode 5 is depicted in Figure 5.

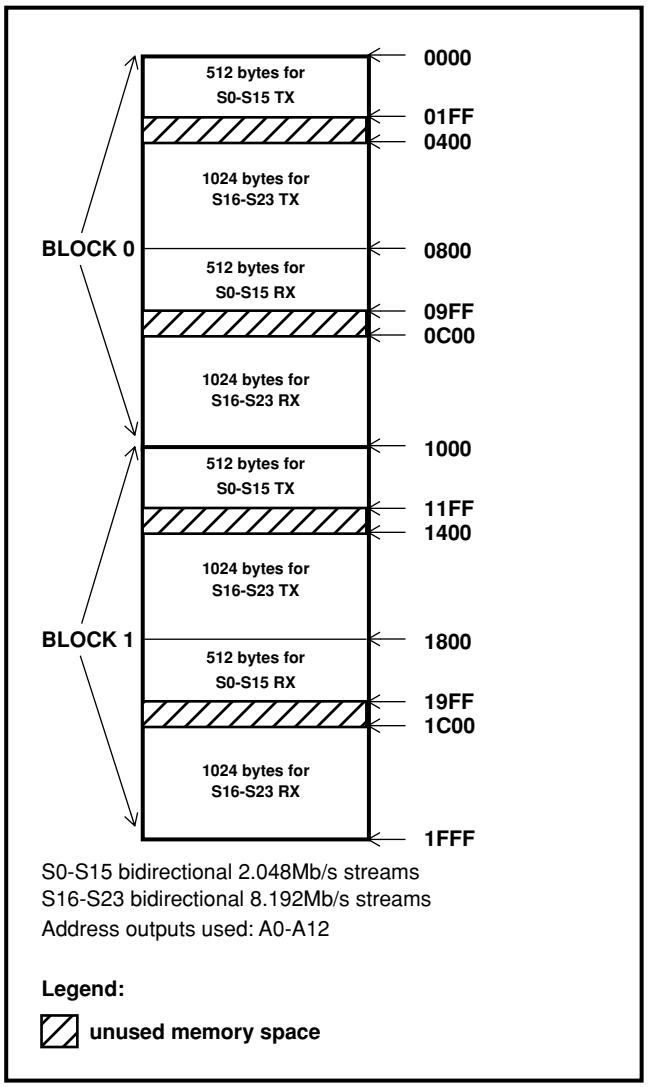


Figure 5- External Double Buffer Operation and Memory Arrangement in Modes 4 and 5.

Bidirectional Operation: Serial output channel timeslots can be tri-stated by setting the $\overline{\text{OEser}}$ input pin high during a specific parallel channel timeslot. Note that when operating in bidirectional mode, the MT90210's I/O buffers on the serial port are permanently at high impedance and the control of contention on the serial bus has to be done by the user through the $\overline{\text{OEser}}$ input pin. In modes 1, 2, 4 and 5 all of the transmit channels on the serial port side are copied back to the memory interface. This is true only in bidirectional modes (i.e., modes 1, 2, 4 and 5). Note that only the transmit (output) channels are copied back to the memory and that the input channels remain unaffected.

For a specific time-slot sampled at the external memory parallel interface, the respective $\overline{\text{OEser}}$ input pin must be in the desired state; i.e., the sampling of the $\overline{\text{OEser}}$ input is synchronized with the parallel byte read at the P0-P7 lines.

Functional operation of the MT90210 device at the parallel interface for modes 1, 2, and 3

Figures 8, 12, and 13 depict the parallel port READ and WRITE operation of the MT90210 device. The state of the signals R/$\overline{\text{W}}$1, $\overline{\text{R}}$/W2 and $\overline{\text{Strobe}}$ defines a valid Read or a valid Write operation. During a valid READ operation the signals $\overline{\text{Strobe}}$ and $\overline{\text{R}}$/W2 stay LOW while the signal R/$\overline{\text{W}}$1 is always HIGH. For the valid WRITE operation the signal $\overline{\text{R}}$/W2 always stays HIGH while the signals R/$\overline{\text{W}}$1 and $\overline{\text{Strobe}}$ toggle. Table 3 represents the sequence of events as depicted in Figure 12 during the last channel at the end of an ST-BUS frame. The MT90210 device repeats the same sequence of operation during the entire frame. For example, during channel 127 at the end of an ST-BUS frame the MT90210 will write channel 126 (streams 0 to 11) and read from channel 1 (streams 12 to 23) of the next frame as shown in Table 3. Note that there is a two channel difference between a write and a read sequence. In mode 1 and mode 2, the MT90210 device performs a group of writes and a group of reads separated by 8 PCLK periods, while for modes 3, 4 and 5 they are separated by 4 PCLK periods.

Functional operation of the MT90210 device at the parallel interface for mode 4 and mode 5

Table 4 represents the sequence of events when the MT90210 device is operating at a mixed rate of operation (mode 4 and mode 5) as depicted in Figure 13. The MT90210 device repeats the same sequence of operation as shown in Table 4 throughout the entire frame. In mode 4 and mode 5 the MT90210 device is configured with 24 bidirectional serial streams and split into two different rates: S0 to S15 operate at 2.048 Mb/s data rates (512 time-slots) and streams S16 to S23 run at 8 Mb/s data rates (1024 time-slots). In this mode, 12 writes are carried out during a parallel port write cycle and 12 reads during a read cycle. Of each group of 12, 8 are dedicated to the high-speed 8.192 Mb/s links, therefore four slots are available for the 2.048 Mb/s links. To process all the 16 streams devoted for 2.048 Mb/s, four separate write or read cycles are required (these slots are denoted with the suffix "a", "b", "c", "d" in Figure 13). Each write or read cycle will use four time-slots. For example, read or write cycle "a" uses streams S0 to S3, read or write cycle "b" uses streams S4 to S7, read or write cycle "c" uses streams S8 to S11 and read or write cycle "d" uses streams S12 to S15 (see Table 4). There is a two channel difference between a read and write sequence for 2 Mb/s data and an eight channel difference for 8 Mb/s data.

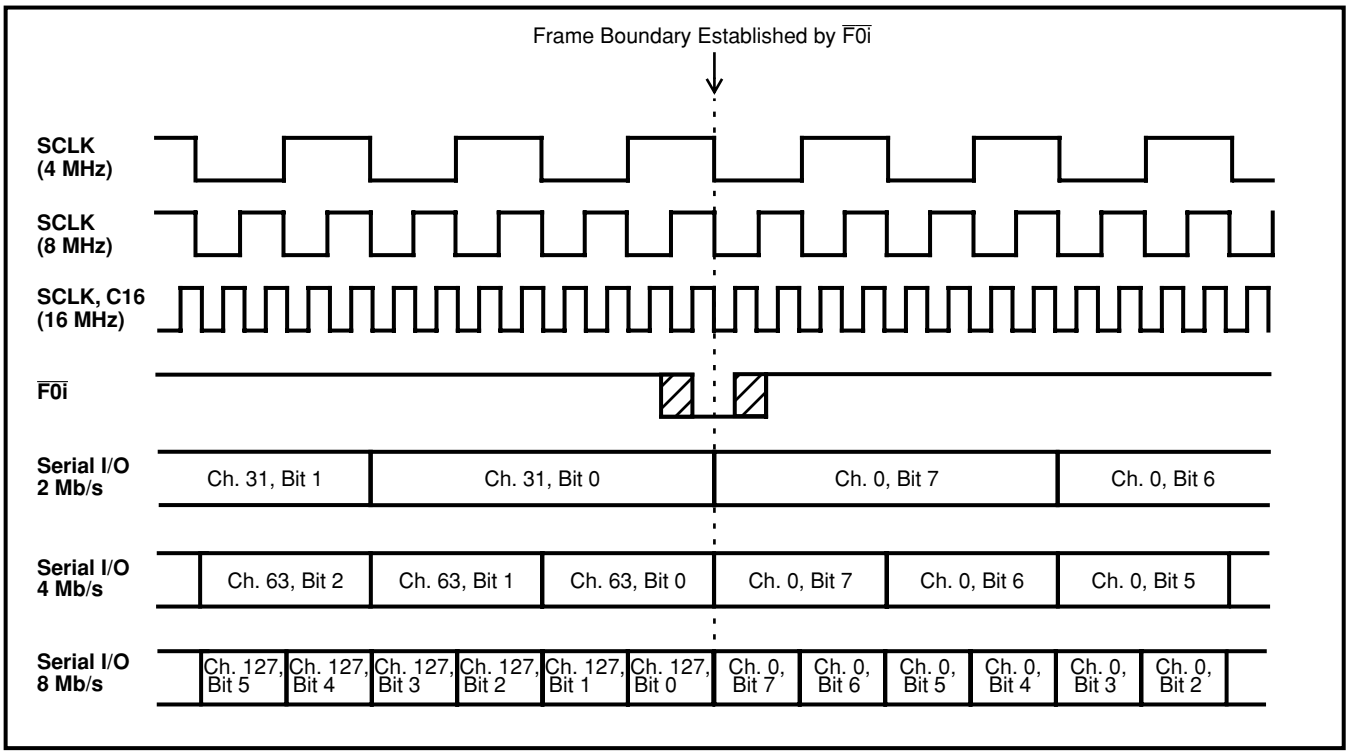


Figure 6 - Serial Port Functional Timing

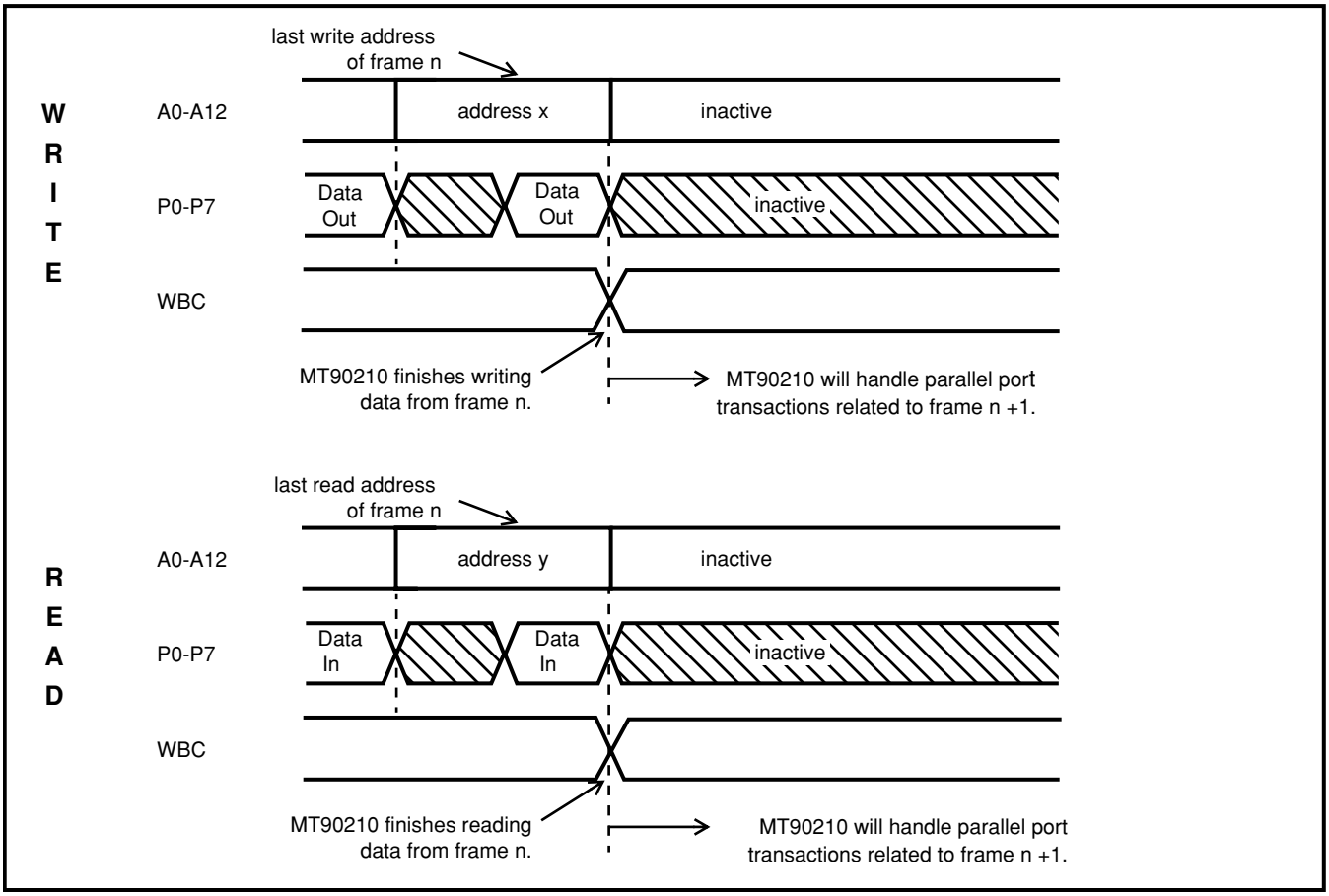


Figure 7a - WBC and RBC Output Transition

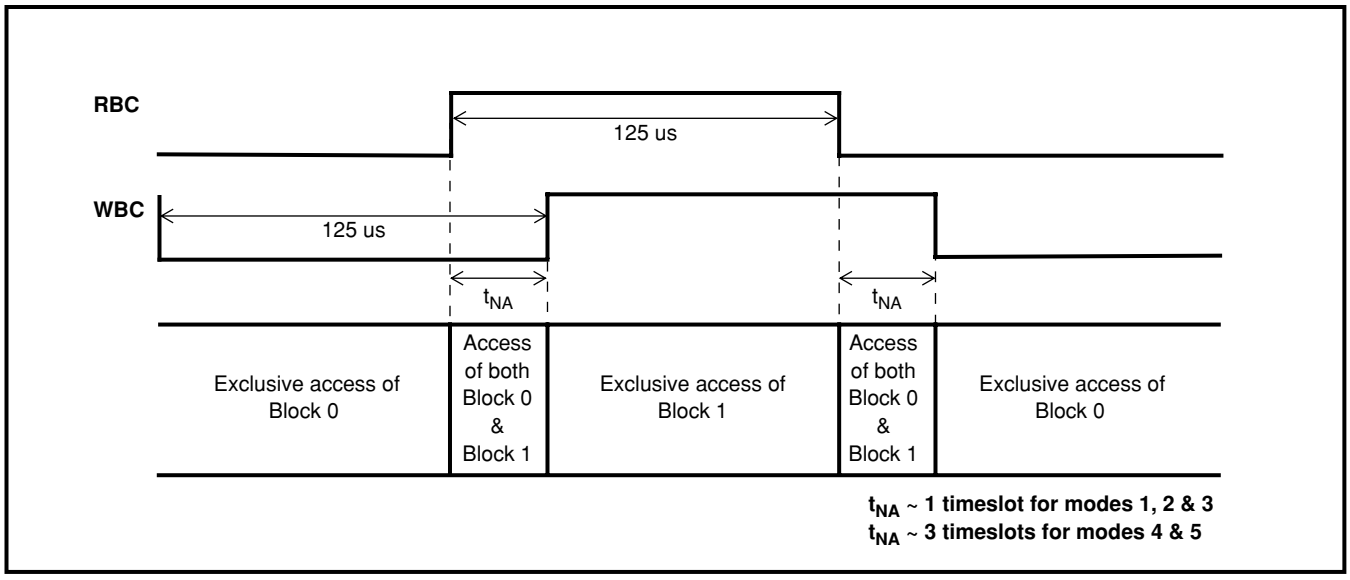
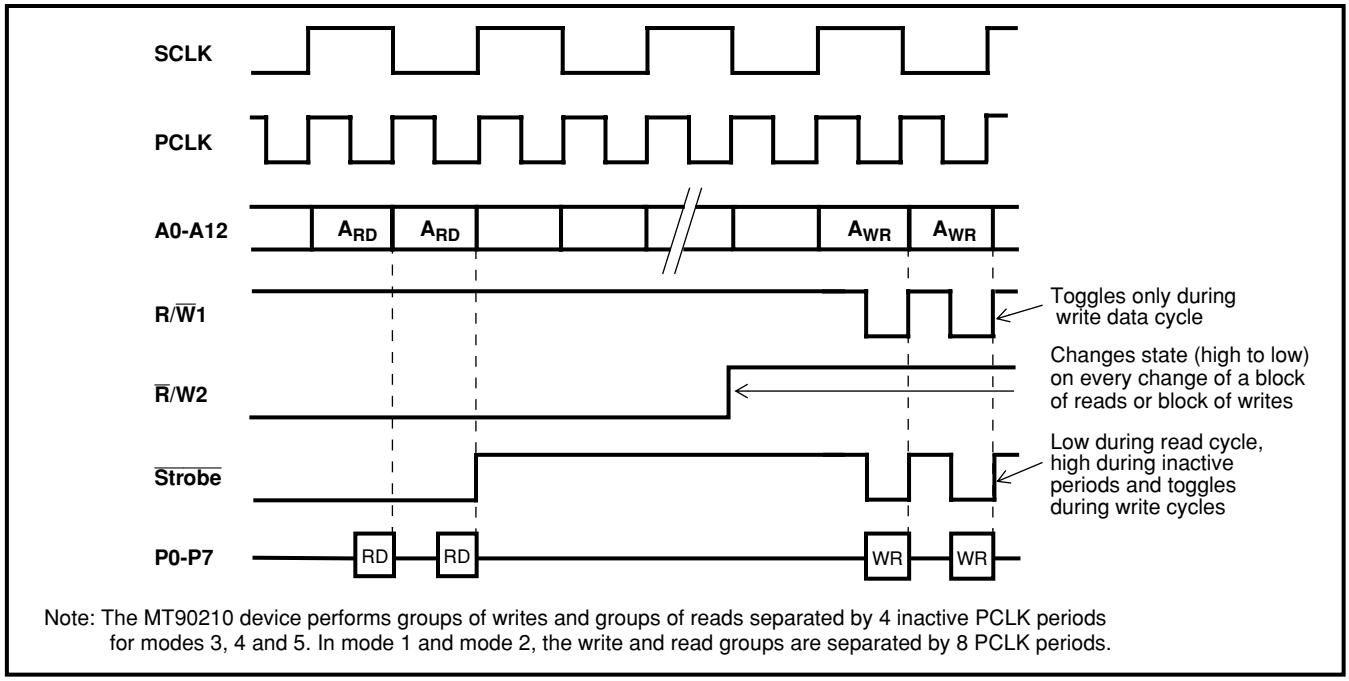


Figure 7b - WBC and RBC operation in relation to accessing data from Block 0 and Block 1



Note: The MT90210 device performs groups of writes and groups of reads separated by 4 inactive PCLK periods for modes 3, 4 and 5. In mode 1 and mode 2, the write and read groups are separated by 8 PCLK periods.

Figure 8 - Parallel Port Functional Read/Write Operation

JTAG Support

The MT90210 JTAG interface is designed according to the Boundary-Scan standard IEEE1149.1. The standard specifies a design-for-testability technique called Boundary-Scan Test (BST). A boundary-scan IC has a shift-register stage or 'Boundary-Scan Cell' (BSC) in between the core logic and the I/O buffers adjacent to each I/O pin. The BSCs can control and observe what happens at each I/O pin of the IC. The operation of the boundary-scan circuitry is controlled by a Test Access Port (TAP) Controller.

Test Access Port (TAP)

The Test Access Port (TAP) provides access to many test support functions built into the MT90210. It consists of three input connections and one output connection. The following connections form the TAP:

- Test Clock Input (TCK)
- Test Mode Select Input (TMS)
- Test Data Input (TDI)
- Test port Reset (TRST)
- Test Data Output (TDO)

I[0:1]	Instruction	Description	
[00]	EXTEST	Boundary-Scan register selected, Test Enabled	This instruction is specifically provided to allow board-level interconnect testing of opens, bridging errors etc. When the EXTEST instruction is selected, the on-chip logic is isolated from the MT90210's I/O pin such that the value of the I/O pins is determined by its boundary-scan register. Data for the execution of this instruction can be preloaded into the boundary-scan register with the SAMPLE/PRELOAD instruction.
[01], [10]	SAMPLE/ PRELOAD	Boundary-Scan register selected, Test Disabled	Two functions can be performed by the use of this instruction. It allows a SAMPLE ('snapshot') of the normal operation of the MT90210 to be taken for examination. And, prior to the selection of another test operation, a PRELOAD can place data values into the latched parallel outputs of the Boundary-Scan cells. During the execution of the instruction, the on-chip logic operation is not hampered in any way.
[11]	BYPASS/ NOTEST	Bypass register selected, Test Disabled	This instruction is used to BYPASS the MT90210 while performing boundary-scan testing on other devices with scan registers in the same serial register chain. The MT90210 is allowed to function normally. This instruction is automatically loaded upon reset of the MT90210, as specified in IEEE1149.1

Table1 - Instruction Register

Instruction Register

In accordance with the IEEE 1149.1 standard, the MT90210 uses public instructions listed in Table 1. The MT90210 JTAG Interface contains a two bit instruction register. Instructions are serially loaded into the Instruction Register from the TDI when the TAP Controller is in its Shift-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

Test Data Registers

As specified in the IEEE 1149.1 Standard, the MT90210 JTAG interface contains two test data registers:

- The Boundary Scan Register
- The Bypass Register

The MT90210 boundary-scan register contains 144 bits. Bit 144 in Table 2 is the first bit clocked out. All tristate enable bits are asserted high: a logic 1 enables the corresponding group of outputs/bidirectionals. Note that clocking all zeros into the scan path register will set all outputs to tristate.

Bits	Definition	BSC Type †
1:60	S4 - S23	B
61	RDIN	I
62	$\overline{\text{OEser}}$	I
63	SCLK	I
64	HC4	I
65	$\overline{\text{F0i}}$	I
66:68	MD2 - MD0	I
69	$\overline{\text{RST}}$	I
70	PCLK	I
71:72	CKO	O
73:76	R/$\overline{\text{W}}$1 - $\overline{\text{R}}$/W2	O
77:100	P0 - P7	B
101:102	$\overline{\text{Strobe}}$	O
103:128	A0 - A12	O
129:130	RBC	O
131:132	WBC	O
133:144	S0 - S3	B

Table 2 - Boundary Scan Register

† B - bidirectional: input cell, output cell followed by tristate cell.

I - input: input cell.

O - output: output cell, followed by tristate cell.

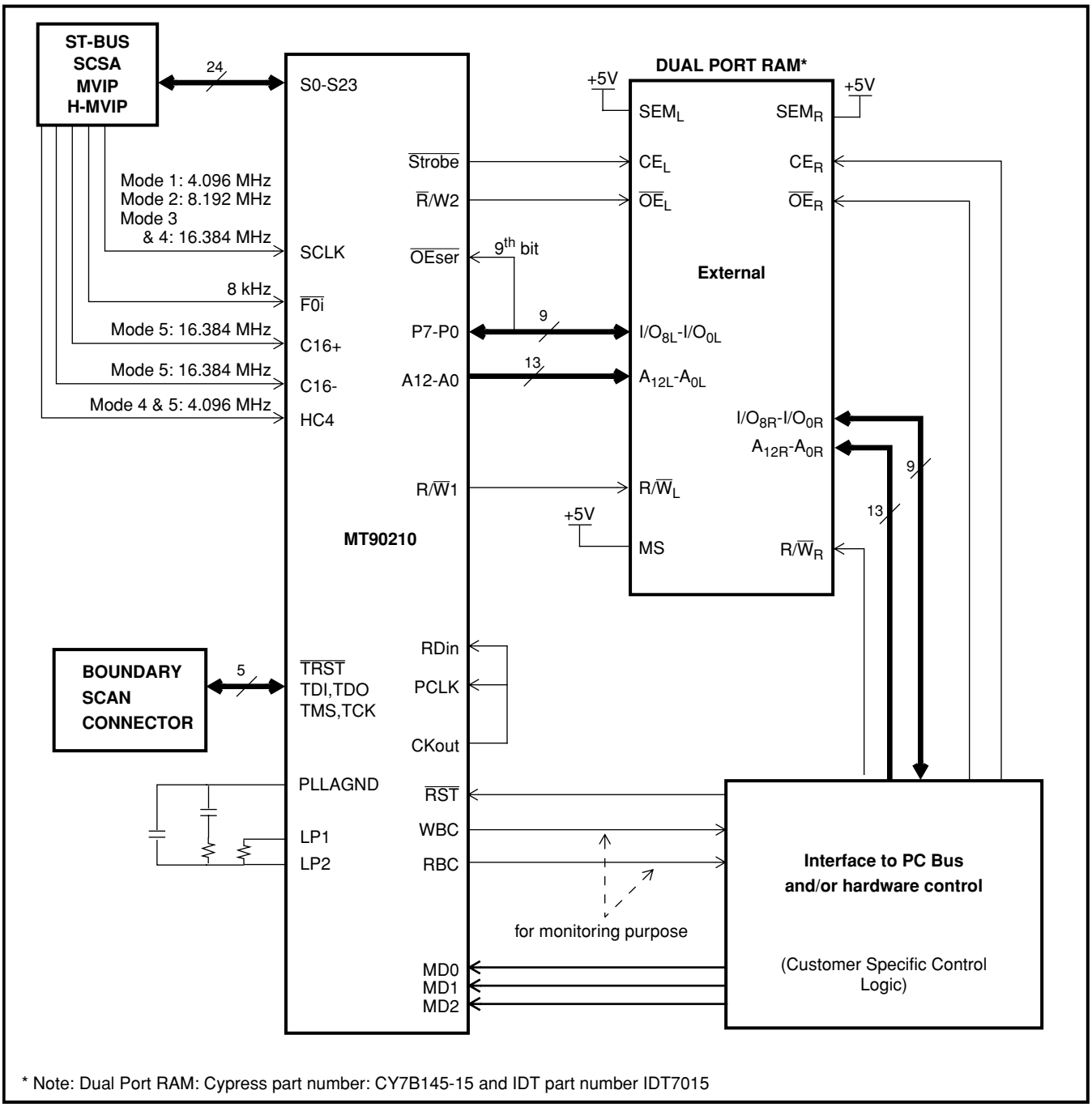


Figure 9 - Functional Example of the MT90210 Application Circuit

Applications

The MT90210 device may be used in applications such as video and teleconferencing bridge cards and voice processing cards for CTI (Computer Telephony Integration). MT90210 transfers all TDM channels of the ST-BUS interface into an external buffer. This eliminates long answer time and permits fast DSP access to ST-BUS, SCSA, MVIP or H-MVIP serial TDM buses. The MT90210 component can be set in H-MVIP mode with 24 fully bidirectional serial streams that are configured in different data rate combinations. Two data I/O subsets of H-MVIP are provided by the MT90210: (i) the 24/2 mode in which all 24 lines operate at 2.048 Mb/s and (ii) the mixed rate of operation in which 16 streams operate at 2.048 Mb/s and the remaining 8 streams operate at 8.192 Mb/s data rates. When operating at 8.192 Mb/s rates, the MT90210 automatically terminates the C16+ and C16- differential clocks specified by the H-MVIP specifications. Figure 9 shows a functional block diagram of the MT90210 in a typical application.

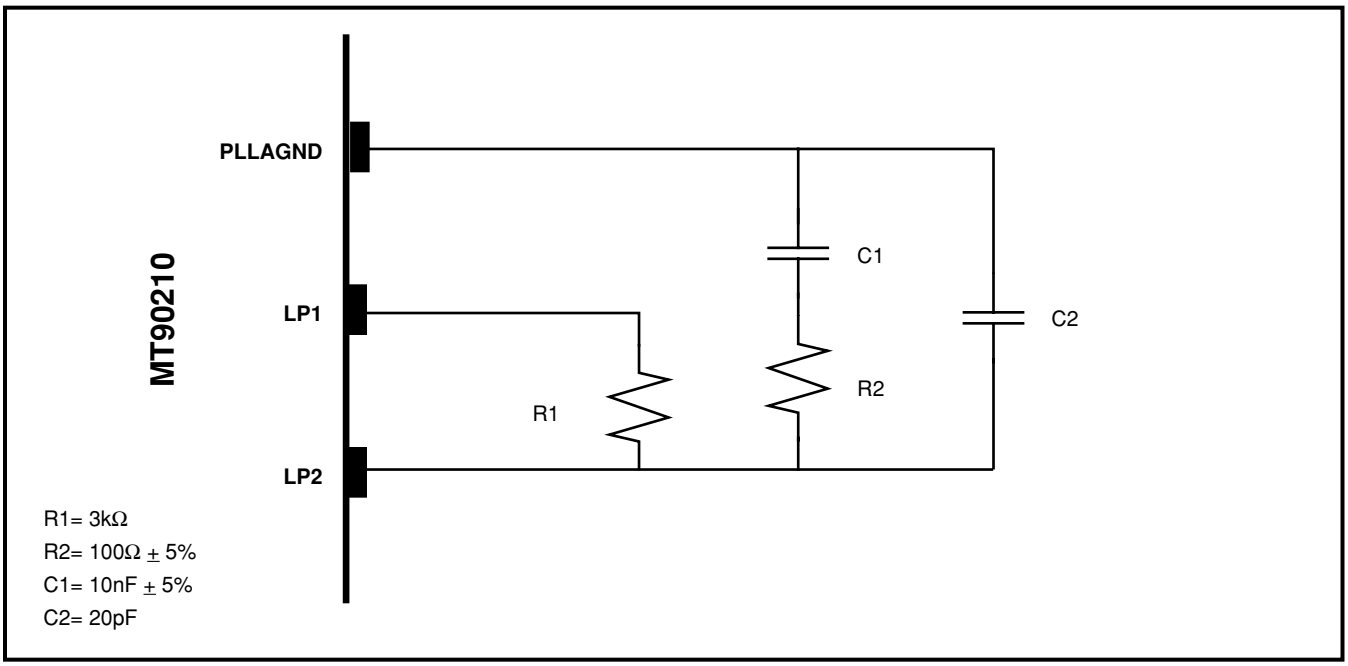


Figure 10 - Analog PLL Low Pass Filter Circuit

PLL Considerations

The MT90210 device contains an analog Phase-Locked Loop (PLL) which is used to create a higher speed clock for parallel port operation from the input SCLK. This analog PLL requires a loop filter circuit to be connected to the LP1 and LP2 pins, as shown in Figure 10. Additionally, the following design considerations are recommended for the PLL circuitry:

- Phase tolerance and jitter are independent of the PLL frequency.
- Jitter is affected by the noise on the PLLVDD and PLLVSS pins. It will increase if the noise level increases and is recommended to be kept less than 10 MHz on PLLVDD.
- Use of a C2 capacitor of 15-25pF (±10%) is recommended to reduce jitter.
- The components should be connected within one inch (1") of the package.
- Use a wide PCB trace for PLLVDD and PLLVSS separate from the device VDD/VSS connections.
- In some setups, an RC network (Figure 11) between PLLVDD and PLLVSS supplies helps to reduce jitter.

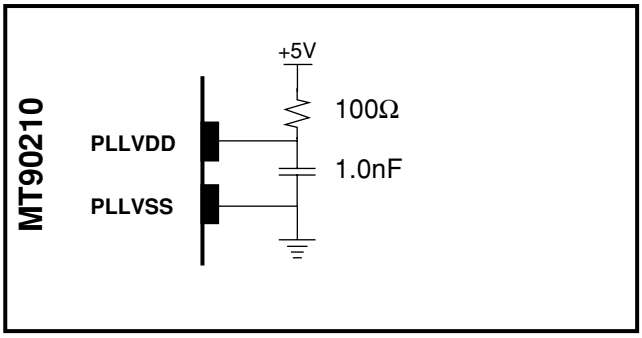


Figure 11 - PLLVDD/PLLVSS RC Circuit

PCLK Cycle	Read	Write	Channel	Stream	Memory Address
1	-	wr	126	0	0DE8h
2	-	wr	126	1	0DE9h
3	-	wr	126	2	0DEAh
4	-	wr	126	3	0DEBh
5	-	wr	126	4	0DECh
6	-	wr	126	5	0DEDh
7	-	wr	126	6	0DEEh
8	-	wr	126	7	0DEFh
9	-	wr	126	8	0DF0h
10	-	wr	126	9	0DF1h
11	-	wr	126	10	0DF2h
12	-	wr	126	11	0DF3h
13 to 16	**INACTIVE**				
17	rd	-	0	0	1000h
18	rd	-	0	1	1001h
19	rd	-	0	2	1002h
20	rd	-	0	3	1003h
21	rd	-	0	4	1004h
22	rd	-	0	5	1005h
23	rd	-	0	6	1006h
24	rd	-	0	7	1007h
25	rd	-	0	8	1008h
26	rd	-	0	9	1009h
27	rd	-	0	10	100Ah
28	rd	-	0	11	100Bh
29 to 32	**INACTIVE**				

Table 3 - Functional Example of the Read and Write Operation (Mode 3)

PCLK Cycle	Read	Write	8Mb/s Channel	8 Mb/s Stream	2 Mb/s Channel	2 Mb/s Stream	Memory Address
1	-	wr	124	16	-	-	0FE0h
. .							
8	-	wr	124	23	-	-	0FE7h
9	-	wr	-	-	31	0	09F0h
10	-	wr	-	-	31	1	09F1h
11	-	wr	-	-	31	2	09F2h
12	-	wr	-	-	31	3	09F3h
13	INACTIVE						
. .							
16							
17 to 24	rd	-	4	16 to 23	-	-	0420h to 0427h
25 to 28	rd	-	-	-	1	0 to 3	0010h to 0013h
29 to 32	INACTIVE						
33 to 40	-	wr	125	16 to 23	-	-	0FE8h to 0FEFh
41 to 44	-	wr	-	-	31	4 to 7	09F4h to 09F7h
45 to 48	INACTIVE						
49 to 56	rd	-	5	16 to 23	-	-	0428h to 042Fh
57 to 60	rd	-	-	-	1	4 to 7	0014h to 0017h
61 to 64	INACTIVE						
65 to 72	-	wr	126	16 -23	-	-	0FF0h to 0FF7h
73 to 76	-	wr	-	-	31	8 to 11	09F8h to 09FBh
77 to 80	INACTIVE						
81 to 88	rd	-	6	16 to 23	-	-	0430h to 0437h
89 to 92	rd	-	-	-	1	8 to 11	0018h to 001Bh
93 to 96	INACTIVE						
97 to 104	-	wr	127	16 to 23	-	-	0FF8h to 0FFFh
105 to 108	-	wr	-	-	31	12 to 15	09FCh to 09FFh
109 to 112	INACTIVE						
113 to 120	rd	-	7	16 to 23	-	-	0438h to 043Fh
121 to 124	rd	-	-	-	1	12 to 15	001Ch to 001Fh

Table 4 - Functional Example of the Parallel Interface for Mode 4 and 5

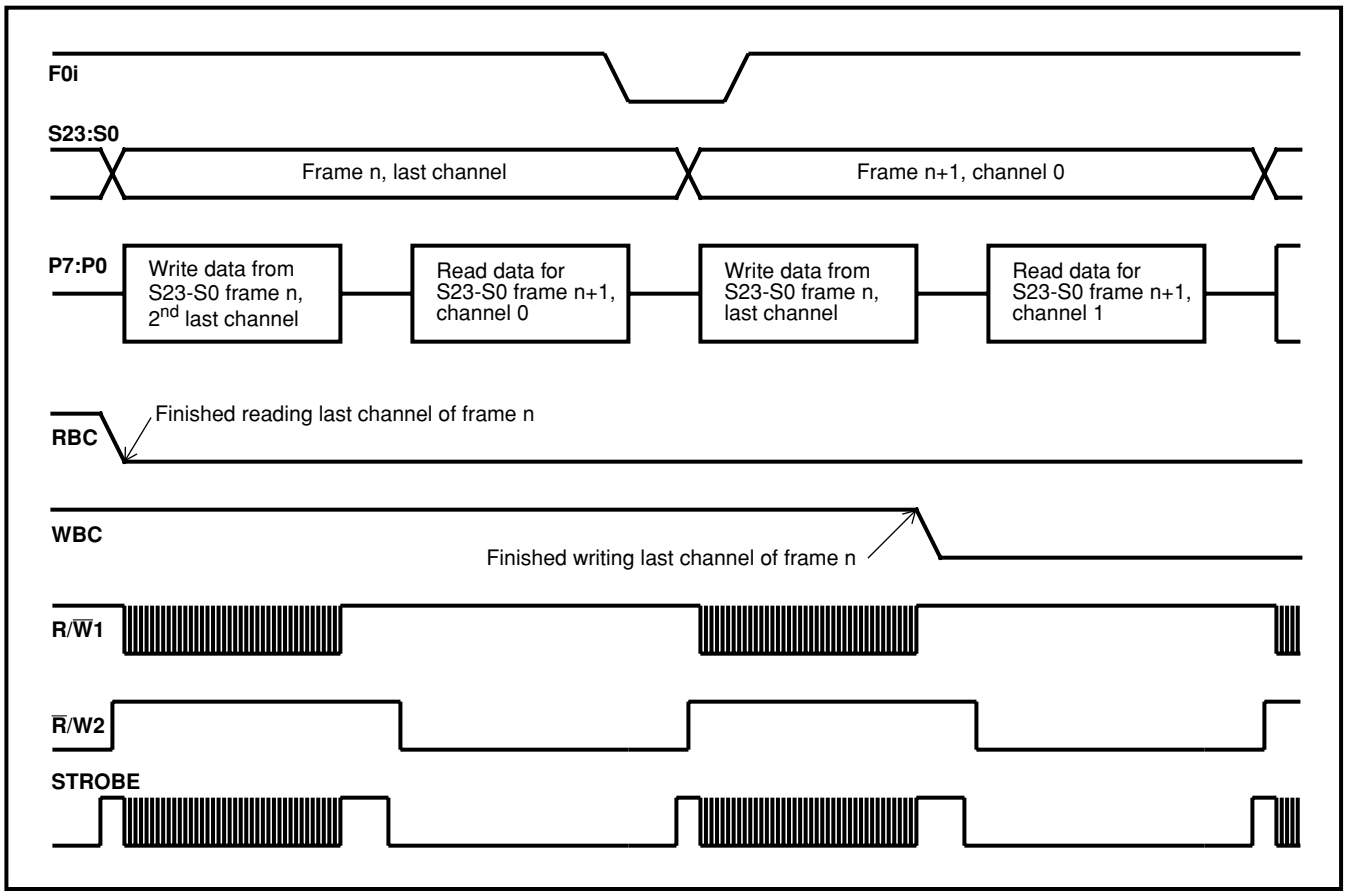


Figure 12 - Modes 1, 2, 3 Read/Write Timing

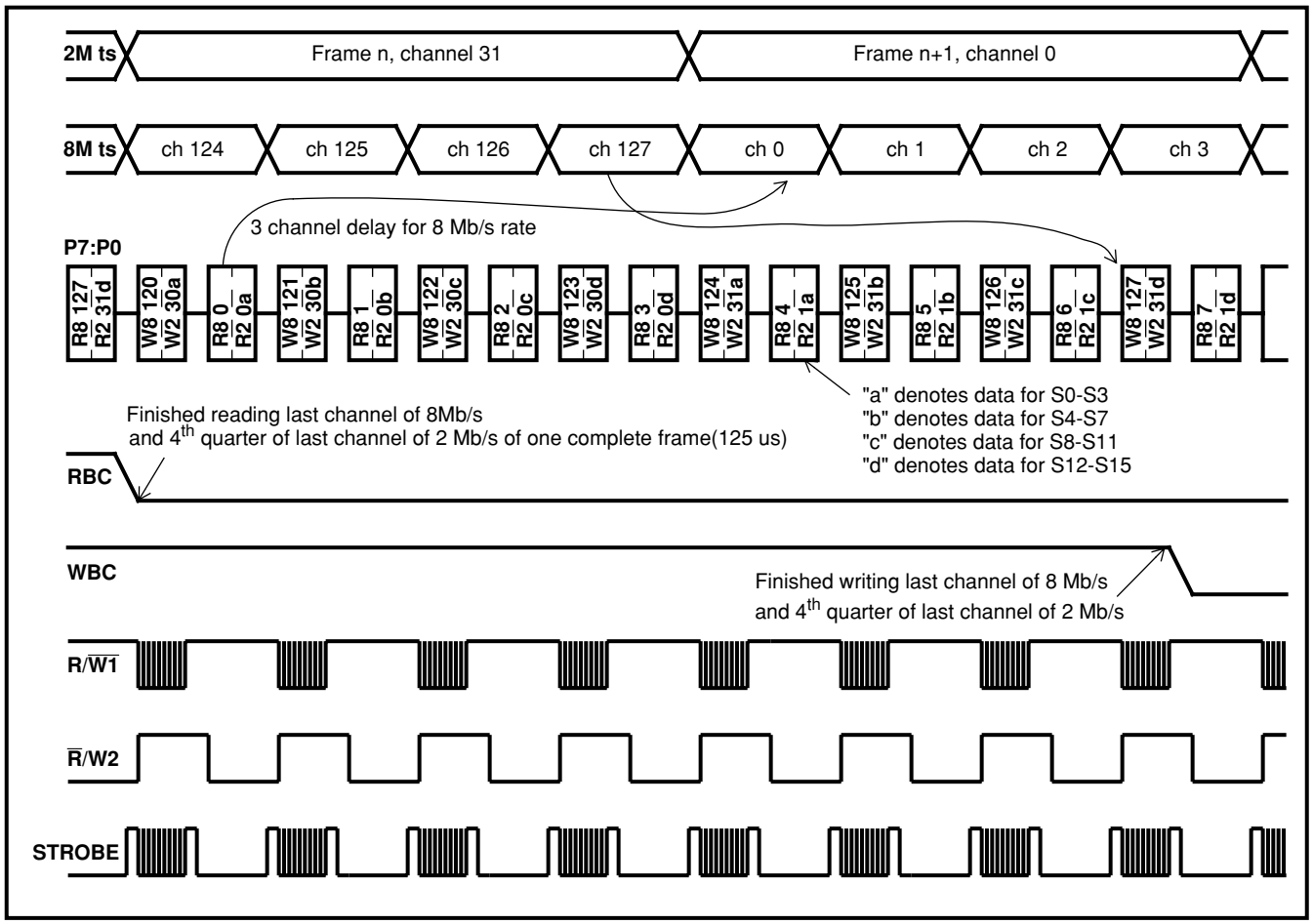


Figure 13 - Mode 4 and Mode 5 Read/Write Timing

Mode	TX/RX	Memory Address Location Formula for Block 0	Memory Address Location Formula for Block 1
1	TX	24C + S	24C + S + 800h
1	RX	24C + S + 0400h	24C + S + C00h
2	TX	24C + S	24C + S + 1000h
2	RX	24C + S + 0800h	24C + S + 1800h
3	TX	12C + S	12C + S + 1000h
3	RX	12C + S + 0800h	12C + S + 1800h
4 or 5 (@ 2M)	TX	16C + S	16C + S + 1000h
4 or 5 (@ 2M)	RX	16C + S + 0800h	16C + S + 1800h
4 or 5 (@ 8 M)	TX	8C + (S-16) + 0400h	8C + (S-16) + 1400h
4 or 5 (@ 8M)	RX	8C + (S-16) + 0C00h	8C + (S-16) + 1C00h

Table 5 - Memory Address Location Formulae for all modes of operation

C = channel number, S = stream number

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage V_{DD} to V_{SS}	V_{DD}		6	V
2	Voltage on any pin (other than supply pins)	V_i	V_{SS}+0.3	V_{DD}+0.3	V
3	Current at any pin (except V_{DD} and V_{SS})	I_O		40	mA
4	Package Power Dissipation	P_D		2	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40	25	+85	°C	
2	Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	

DC Electrical Characteristics†

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Supply Current	I_{DD}		15	100	mA	
2	Input High Voltage, all inputs	V_{IH}	2.0		V_{DD}	V	
3	Input Low Voltage, all inputs	V_{IL}	0		0.8	V	
4	Specific Output High Sourcing Current	I_{OH}	12			mA	V_{OH}=2.4V
5	Specific Output Low Sinking Current	I_{OL}	12			mA	V_{OL}=0.4V
6	Leakage Current S0-S23 All other pins	I_{LK}			 200 5	µA	
7	Pin Capacitance	C_P			10	pF	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25°C and are for design aid only.

AC Electrical Characteristics† - The following table specifies voltage reference levels used in both input timing and output timing specifications. The setup/hold and propagation delays are based on a single reference level which is 1.5V for TTL(V_{TT}) and 0.5*V_{DD} for CMOS (V_{CT}).

Voltage Reference	Voltage Value when Connected to TTL	Voltage Value when Connected to CMOS	Units
V_H	2.4	0.9*V_{DD}	V
V_{HM}	2.0	0.7*V_{DD}	V
V_{LM}	0.8	0.3*V_{DD}	V
V_L	0.4	0.1*V_{DD}	V
V_{TT}	1.5	not applicable	V
V_{CT}	not applicable	0.5*V_{DD}	V

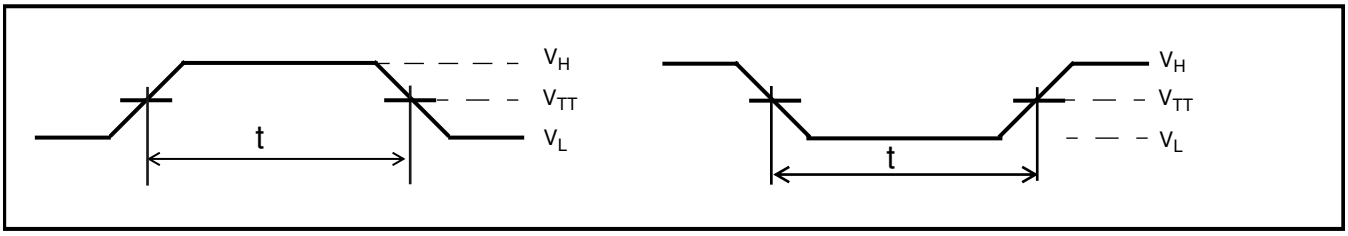


Figure 14 - Input Pulse Width

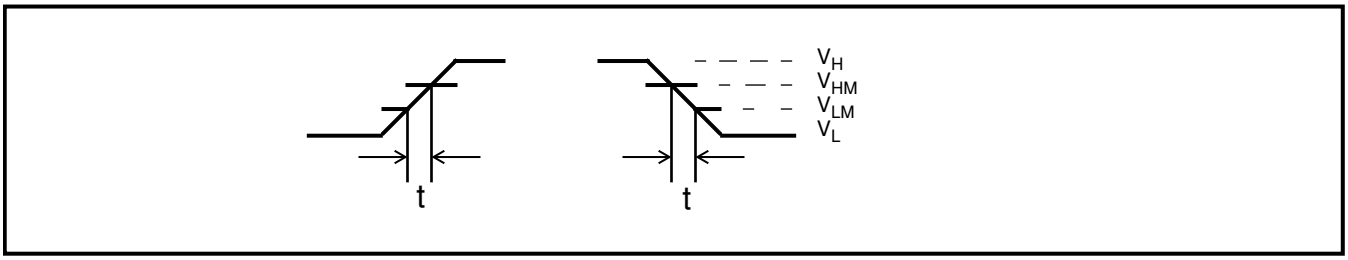


Figure 15 - Input Rise and Fall Times

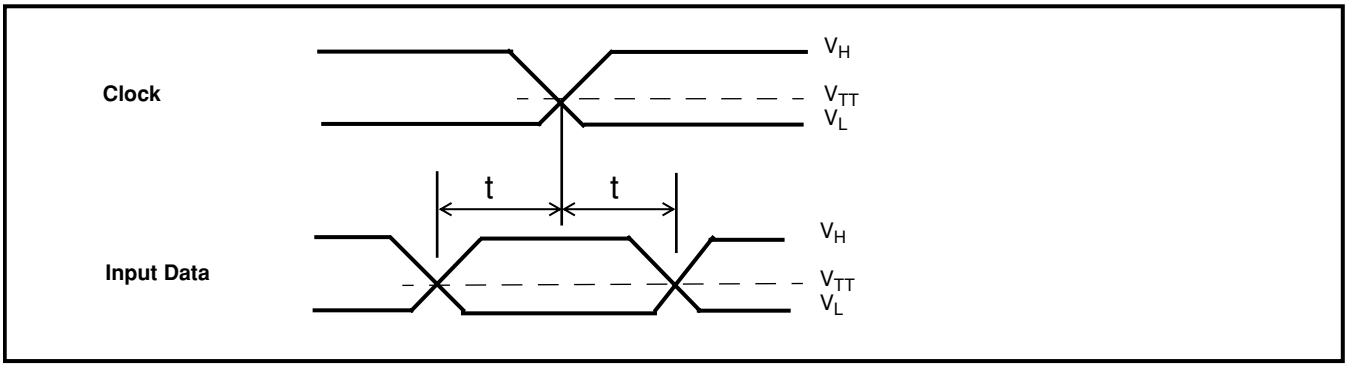


Figure 16 - Setup Time and Hold Time

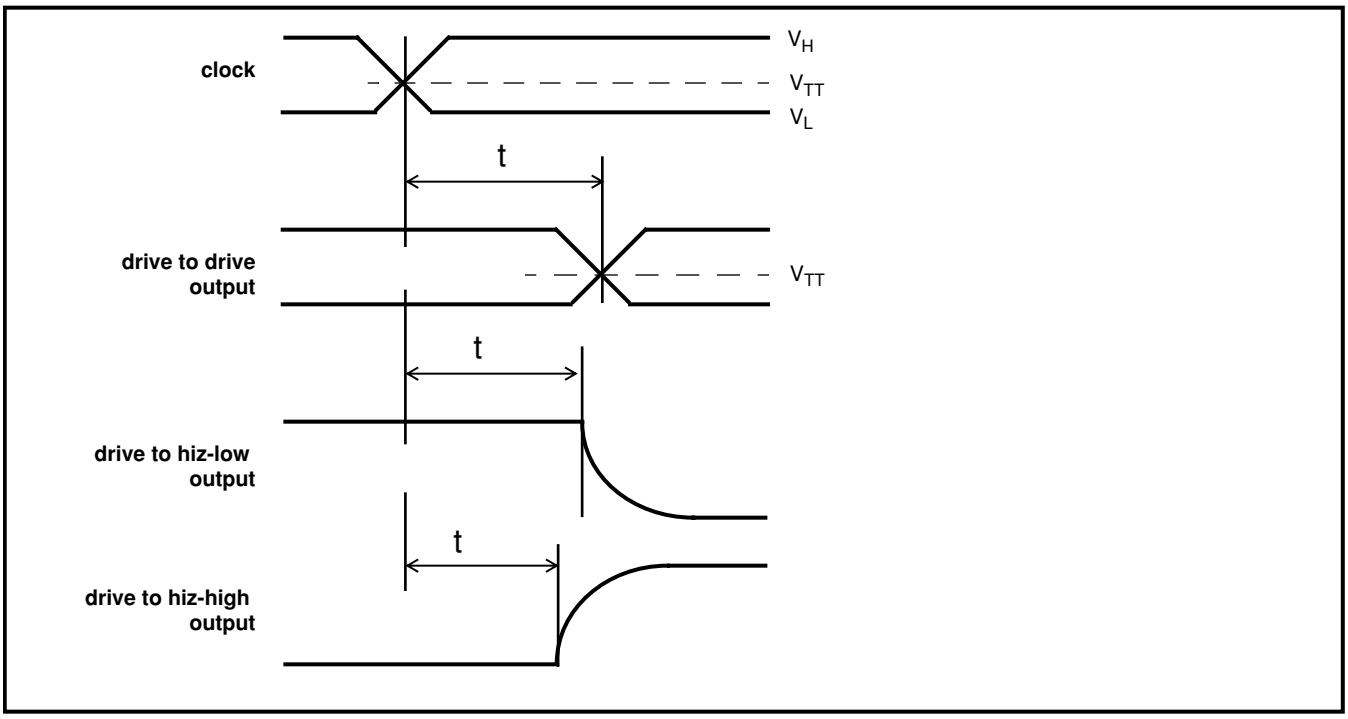
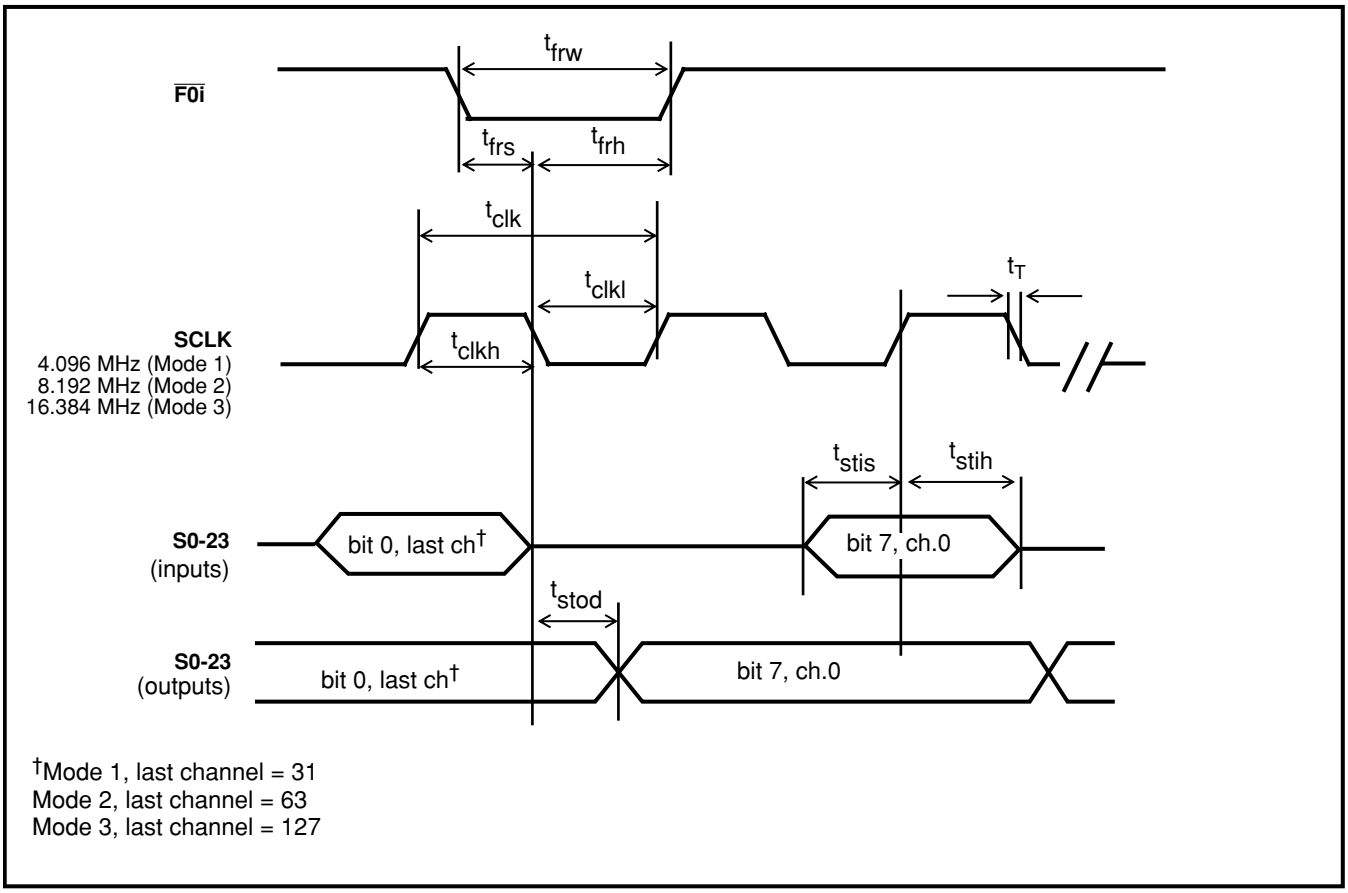


Figure 17 - Output Delays



†Mode 1, last channel = 31
Mode 2, last channel = 63
Mode 3, last channel = 127

Figure 18 - Serial Port Timing for Modes 1, 2, 3

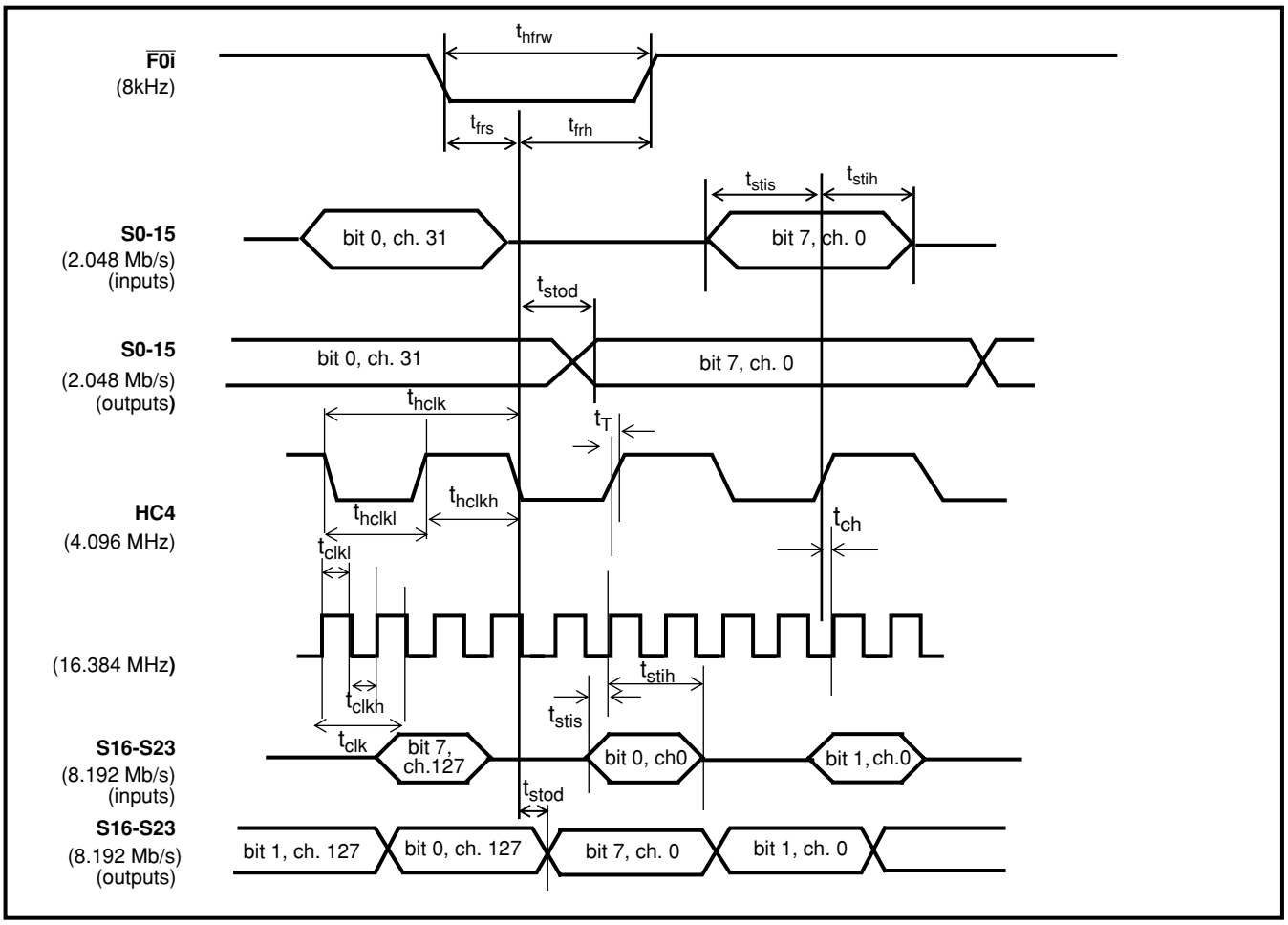


Figure 19 - Serial Port Timing for Modes 4 and 5

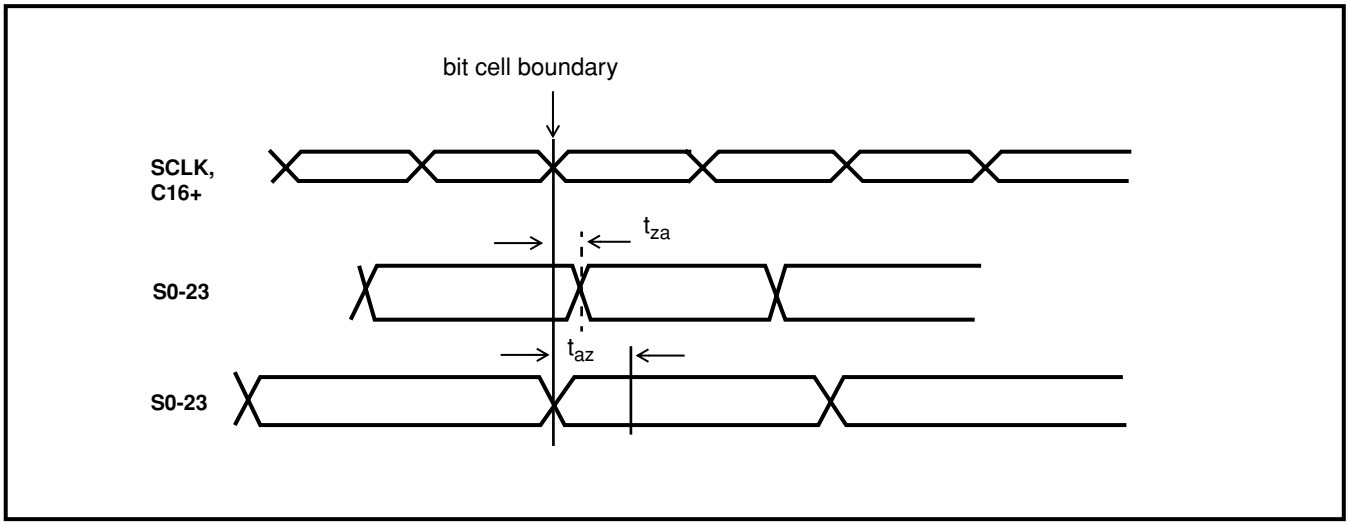


Figure 20 - Serial Port Tri-state Timing

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	SCLK, C16 Period	t_{clk}					
	2.048 Mb/s (4.096 MHz)			244		ns	
	4.096 Mb/s (8.192 MHz)			122		ns	
	8.192 Mb/s (16.384 MHz)			60		ns	
2	SCLK, C16 Pulse Width High	t_{clkh}					
	2.048 Mb/s			122		ns	
	4.096 Mb/s			60		ns	
	8.192 Mb/s			30		ns	
3	SCLK, C16 Pulse Width Low	t_{clkl}					
	2.048 Mb/s			122		ns	
	4.096 Mb/s			60		ns	
	8.192 Mb/s			30		ns	
4	SCLK rise/fall time	t_T			5	ns	
5	HC4 hold related to C16	t_{ch}		3		ns	
6	HC4 period	t_{hclk}		244		ns	
7	HC4 pulse low	t_{hclkl}		122		ns	
8	HC4 pulse high	t_{hclkh}		122		ns	
9	Frame Pulse Setup (ST-BUS)	t_{frs}	0			ns	
10	Frame Pulse Hold (ST-BUS)	t_{frh}	10			ns	
11	Frame pulse width in modes 1,2,3	t_{frw}					
	2.048 Mb/s			244		ns	
	4.096 Mb/s			122		ns	
	8.192 Mb/s			60		ns	
12	Frame pulse width in modes 4,5	t_{hfrw}		244		ns	
13	S0-23 delay from active to High-Z 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s	t_{az}			30	ns	R_L=1K, C_L=200pF
14	S0-23 delay from High-Z to active 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s	t_{za}			30	ns	R_L=1K, C_L=200pF
15	S0-23 Delay (high and low) from CLK falling (ST-BUS mode) 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s	t_{stod}			30	ns	R_L=1K, C_L=200pF
16	S0-23 Set-up Time before CLK rising (ST-BUS mode)	t_{stis}	0			ns	
17	S0-23 Hold Time from CLK rising (ST-BUS mode)	t_{stih}	10			ns	
18	CKout output delay from SCLK	t_{dpll}			5	ns	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25°C and are for design aid only.

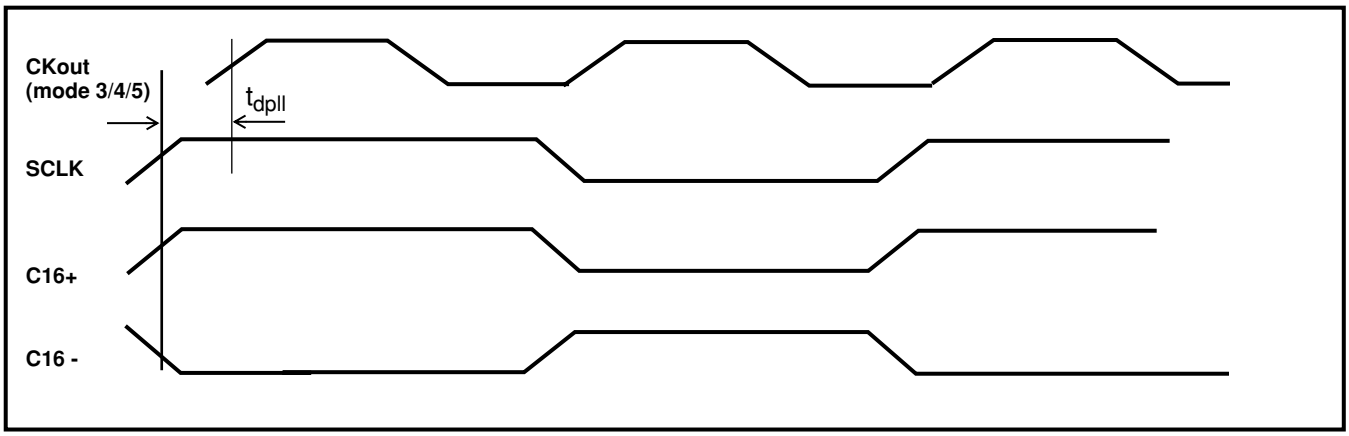
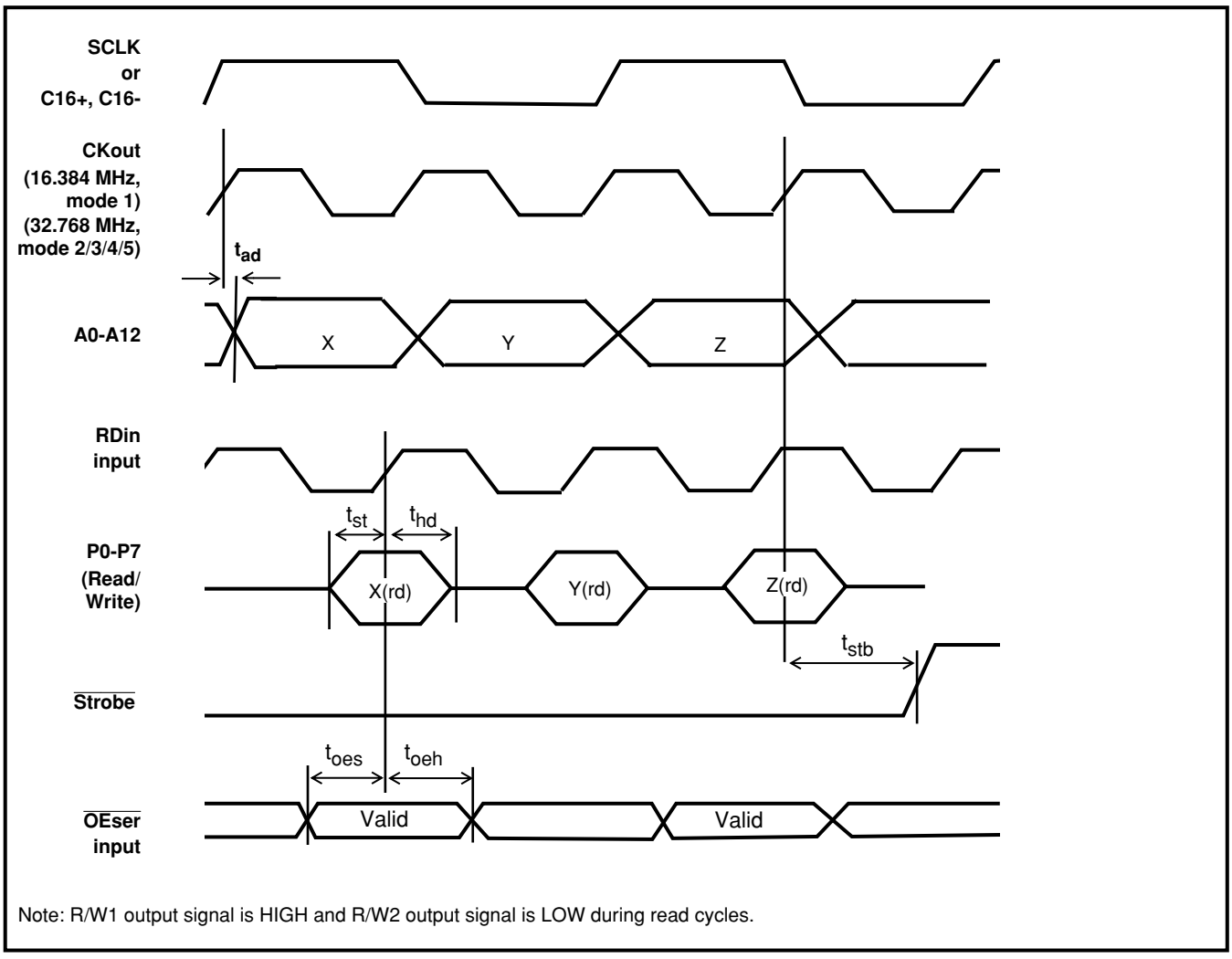
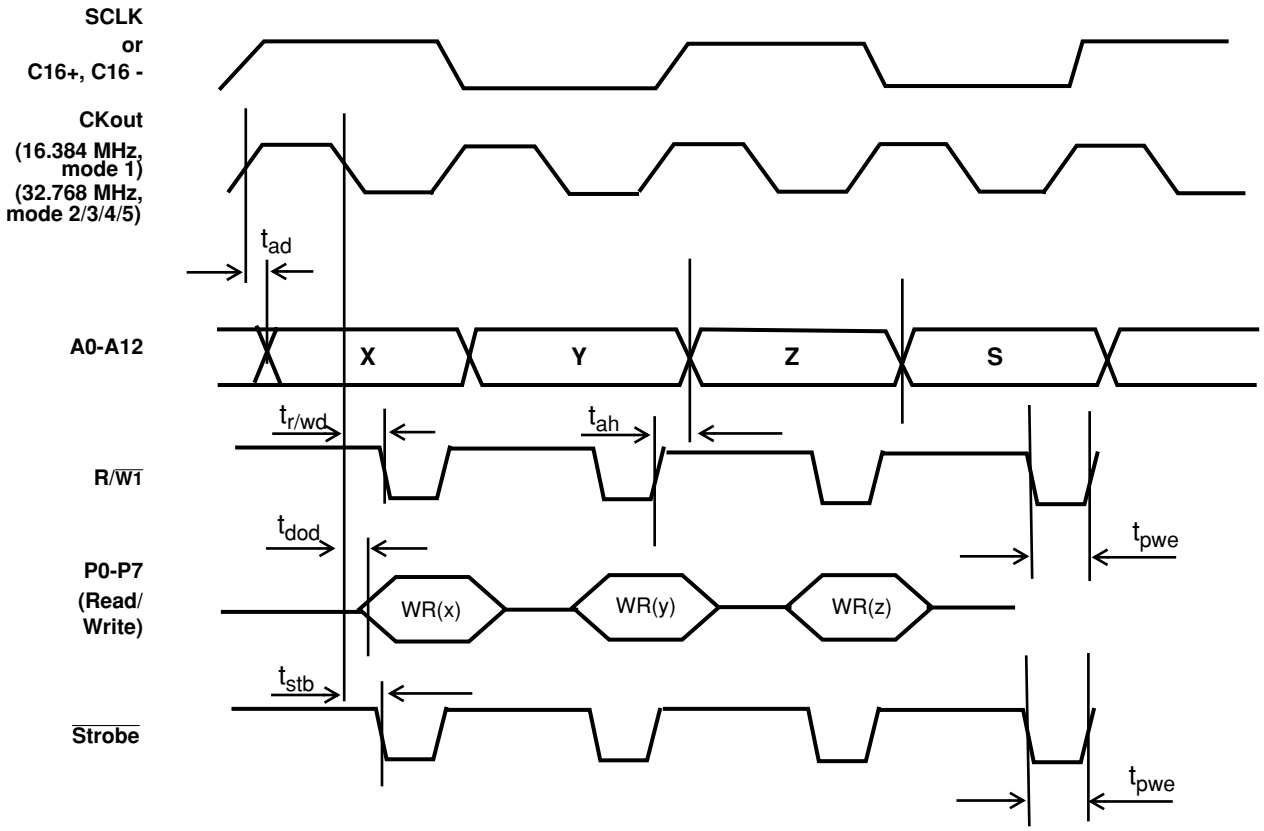


Figure 21 - PLL Timing



Note: R/W1 output signal is HIGH and R/W2 output signal is LOW during read cycles.

Figure 22 - Parallel Port Data Read Cycle



Note: R/W2 output signal is HIGH during write cycles.

Figure 23- Parallel Port Data Write Cycle

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Address Output Delay from Clock	t_{ad}			15	ns	output load 50pF
2	Output Delay on R/$\overline{W}$1 and $\overline{Strobe}$	$t_{r/wd}$, t_{stb}			9.5	ns	
3	Pulse Width Low - R/$\overline{W}$1 and $\overline{Strobe}$ modes 2, 3, 4 & 5 mode 1	t_{pwe}	 13.5 30			ns	pulse width low on PCLK for 30 ns
4	Internal Data Output Delay from Clock Falling	t_{dod}			10	ns	output load 50 pF
5	Address Hold from Write Inactive	t_{ah}	2.25			ns	
6	Input Data & $\overline{OE}$ setup times	t_{st}, t_{oes}	0			ns	
7	Input Data & $\overline{OE}$ hold times	t_{hd}, t_{oeh}	5			ns	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25°C and are for design aid only.

For more information about all Zarlink products visit our Web Site at

www.zarlink.com