

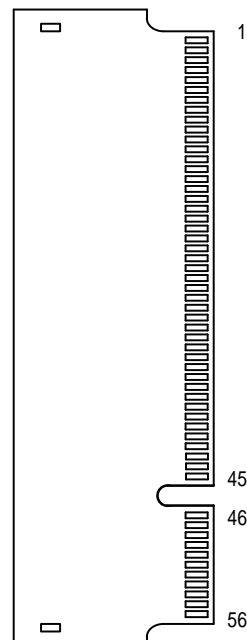
*Advance Information*  
**128KB/256KB Secondary Cache  
Module**  
**With Tag, Valid, and Dirty for i486  
Processor Systems**

This family of cache modules is well suited to provide the secondary cache for the Intel 82420 PCI chipset. This family provides the 128K Byte and 256K Byte cache sizes with valid, dirty and a choice of 7, 8, or 9 tag bits. The tag/valid bits have 12 ns access times for zero wait states at 33 MHz clock speeds. The PD pins map into the configuration register of the 82420 for auto-configuration of the cache controller during system startup.

- Low Profile Edge Connector: Burndy Part Number: CELP2X56SC3Z48
- Single 5 V  $\pm$  10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Cycle Time: Up to External Processor Bus Speed of 33 MHz
- Cache Byte Write, Bank Chip Enable, Bank Output Enable
- Decoupling Capacitors are Used for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Planes

**MCM32A732**  
**MCM32A832**  
**MCM32A932**  
**MCM32A764**  
**MCM32A864**  
**MCM32A964**

112-LEAD  
CARD EDGE  
CASE 1112-01  
TOP VIEW



BurstRAM is a registered trademark of Motorola.  
I486 is a registered trademark Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1  
6/95

**PIN ASSIGNMENT  
CACHE MODULE  
112-LEAD CARDEDGE  
TOP VIEW**

PD4	PD3	PD2	PD1	PD0	Cache Size	Main Memory Max	Module
NC	NC	NC	NC	NC	—	—	No Module
V <sub>CC</sub>	V <sub>CC</sub>	NC	NC	V <sub>CC</sub>	128KB	16MB	32A732
V <sub>CC</sub>	NC	NC	NC	V <sub>CC</sub>	128KB	32MB	32A832
V <sub>CC</sub>	NC	V <sub>CC</sub>	NC	V <sub>CC</sub>	128KB	64MB	32A932
V <sub>CC</sub>	V <sub>CC</sub>	NC	V <sub>CC</sub>	NC	256KB	32MB	32A764
V <sub>CC</sub>	NC	NC	V <sub>CC</sub>	NC	256KB	64MB	32A864
V <sub>CC</sub>	NC	V <sub>CC</sub>	V <sub>CC</sub>	NC	256KB	128MB	32A964

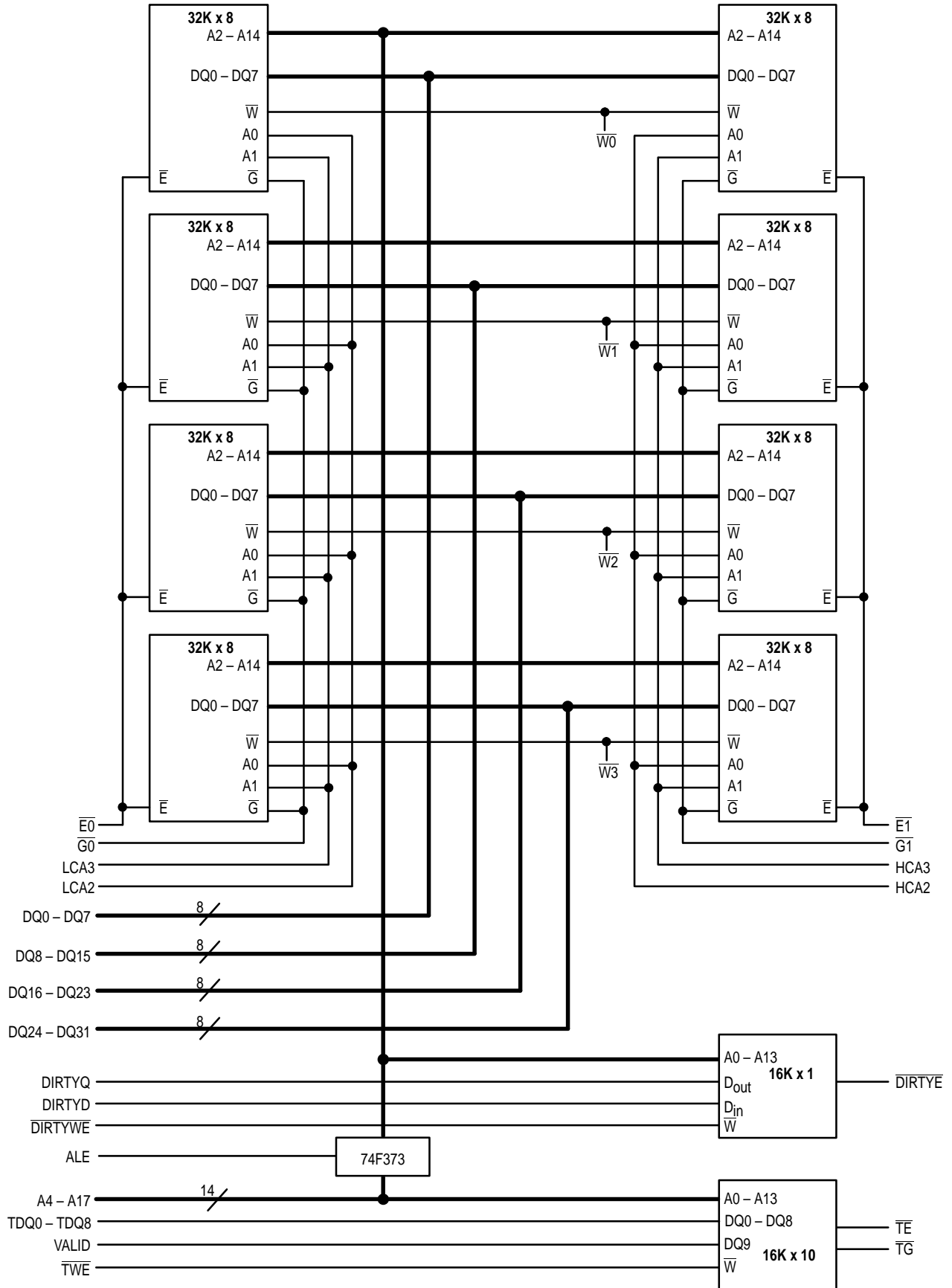
PIN NAMES	
A4 – A19	Address Inputs
HCA2, HCA3	Upper Bank Address Inputs
LCA2, LCA3	Lower Bank Address Inputs
ALE	Address Latch Enable
$\overline{Wx}$	Byte Write Enable
$\overline{E0}, \overline{E1}$	Bank Chip Enable
$\overline{G0}, \overline{G1}$	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TDQ0 – TDQ8	Tag Data Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{TG}$	Tag Output Enable
$\overline{TE}$	Tag Chip Enable
VALID	Valid Bit
$\overline{DIRTYWE}$	Dirty Write Enable
$\overline{DIRTYE}$	Dirty Chip Enable
DIRTYD	Dirty Data Input
DIRTYQ	Dirty Data Output
PD0 – PD4	Presence Detect
NC	No Connect
V <sub>CC</sub>	+5 V Power Supply
V <sub>SS</sub>	Ground

V <sub>SS</sub>	57	1	V <sub>SS</sub>
DQ0	58	2	DQ1
DQ2	59	3	DQ3
DQ4	60	4	DQ5
DQ6	61	5	DQ7
V <sub>CC</sub>	62	6	V <sub>CC</sub>
NC	63	7	NC
DQ8	64	8	DQ9
DQ10	65	9	DQ11
DQ12	66	10	DQ13
V <sub>SS</sub>	67	11	V <sub>SS</sub>
DQ14	68	12	DQ15
DQ16	69	13	DQ17
DQ18	70	14	DQ19
DQ20	71	15	DQ21
V <sub>CC</sub>	72	16	V <sub>CC</sub>
DQ22	73	17	DQ23
NC	74	18	NC
DQ24	75	19	DQ25
DQ26	76	20	DQ27
V <sub>SS</sub>	77	21	V <sub>SS</sub>
DQ28	78	22	DQ29
DQ30	79	23	DQ31
LA2	80	24	HA2
LA3	81	25	HA3
V <sub>CC</sub>	82	26	V <sub>CC</sub>
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	NC
NC	90	34	NC
V <sub>SS</sub>	91	35	V <sub>SS</sub>
DIRTYD	92	36	DIRTYQ
TDQ0	93	37	TDQ1
TDQ2	94	38	TDQ3
TDQ4	95	39	TDQ5
V <sub>SS</sub>	96	40	V <sub>SS</sub>
TDQ6	97	41	TDQ7*
VALID	98	42	TDQ8**
$\overline{TE}$	99	43	ALE
$\overline{TWE}$	100	44	$\overline{WE0}$
V <sub>CC</sub>	101	45	V <sub>CC</sub>
V <sub>SS</sub>	102	46	V <sub>SS</sub>
$\overline{TG}$	103	47	$\overline{WE1}$
DIRTYWE	104	48	$\overline{WE2}$
DIRTYE	105	49	$\overline{WE3}$
V <sub>CC</sub>	106	50	V <sub>CC</sub>
$\overline{G0}$	107	51	$\overline{G1}$
$\overline{E0}$	108	52	$\overline{E1}$
PD0	109	53	PD1
PD2	110	54	PD3
PD4	111	55	NC
V <sub>SS</sub>	112	56	V <sub>SS</sub>

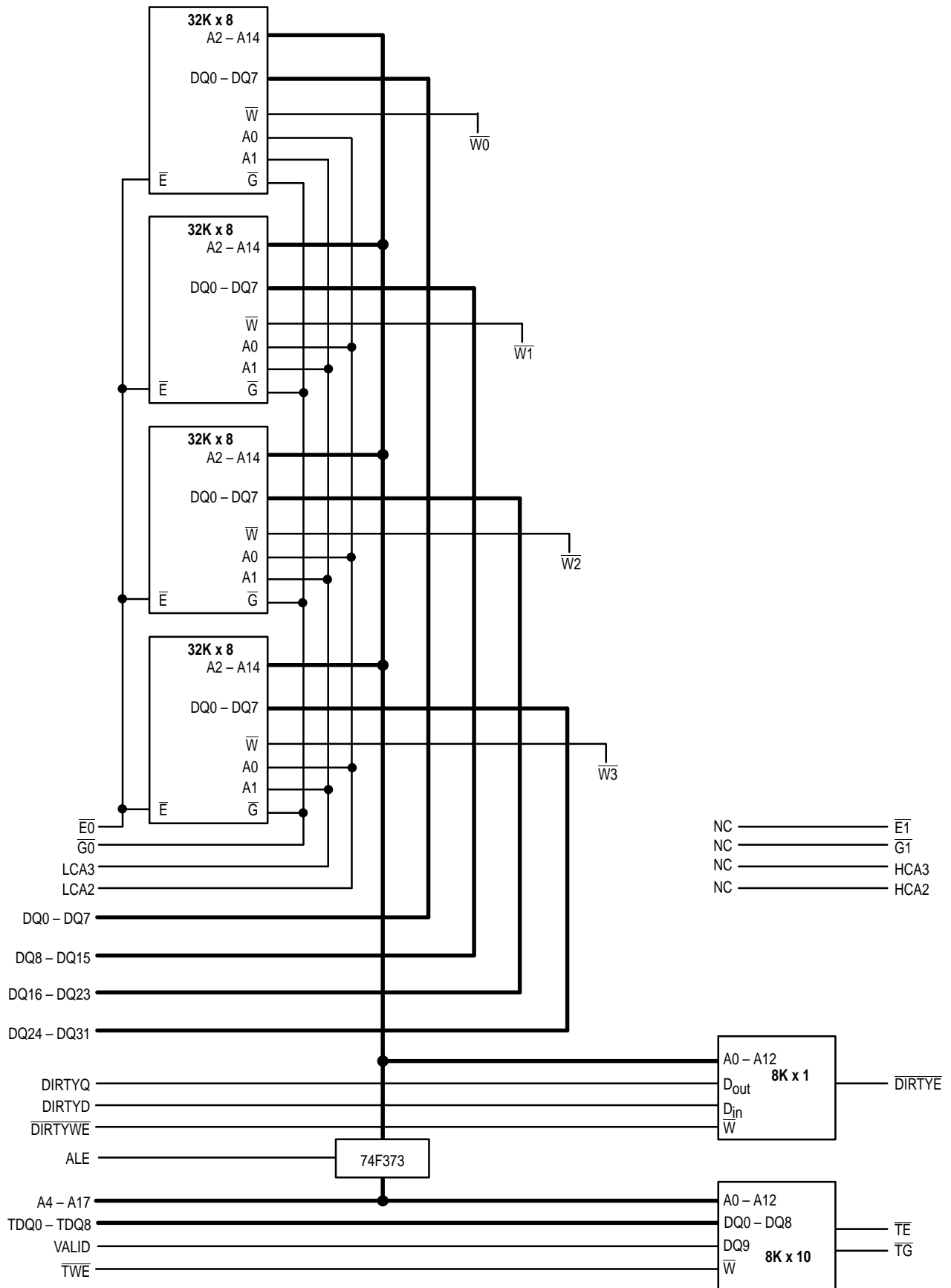
\* No Connect for 32A864, 32A832

\*\* No Connect for 32A764, 32A864, 32A732, 32A832

**486 256KB CACHE MODULE BLOCK DIAGRAM  
WITH 9 TAG BITS**



**486 128KB CACHE MODULE BLOCK DIAGRAM  
WITH 9 TAG BITS**



**TRUTH TABLE** (X = Don't Care)

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	V <sub>CC</sub> Current	Output	Cycle
H	X	X	Not Selected	I <sub>SB1</sub> , I <sub>SB2</sub>	High-Z	–
L	H	H	Output Disabled	I <sub>CCA</sub>	High-Z	–
L	L	H	Read	I <sub>CCA</sub>	D <sub>out</sub>	Read Cycle
L	X	L	Write	I <sub>CCA</sub>	High-Z	Write Cycle

NOTE:  $\bar{E}$  = Exx, ET;  $\bar{W}$  = Wxx, WT, WA;  $\bar{G}$  = GA, GB

**ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	– 0.5 to + 7.0	V
Voltage Relative to V <sub>SS</sub> For Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	– 0.5 to V <sub>CC</sub> + 0.5	V
Output Current	I <sub>out</sub>	± 20	mA
Power Dissipation	P <sub>D</sub>	11.0	W
Temperature Under Bias	T <sub>bias</sub>	– 10 to + 85	°C
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Storage Temperature — Plastic	T <sub>stg</sub>	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3**	V
Input Low Voltage	V <sub>IL</sub>	– 0.5*	—	0.8	V

\* V<sub>IL</sub> (min) = – 0.5 V dc; V<sub>IL</sub> (min) = – 2.0 V ac (pulse width ≤ 20 ns)

\*\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0 V ac (pulse width ≤ 20 ns)

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(I)</sub>	—	± 10	μA
Output Leakage Current ( $\bar{E}$ = V <sub>IH</sub> or $\bar{G}$ = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(O)</sub>	—	± 10	μA
Output High Voltage (I <sub>OH</sub> = – 4.0 mA)	V <sub>OH</sub>	2.4	—	V
Output Low Voltage (I <sub>OL</sub> = 8.0 mA)	V <sub>OL</sub>	—	0.4	V

**POWER SUPPLY CURRENTS**

Parameter	Symbol	32Ax32 33 MHz	32Ax64 33 MHz	Unit
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>CC</sub> = Max, f = f <sub>max</sub> )	I <sub>CCA</sub>	750	1250	mA
AC Standby Current ( $\bar{E}$ = V <sub>IH</sub> , V <sub>CC</sub> = Max, f = f <sub>max</sub> )	I <sub>SB1</sub>	180	300	mA
CMOS Standby Current (V <sub>CC</sub> = Max, f = 0 MHz, $\bar{E}$ ≥ V <sub>CC</sub> – 0.2 V, V <sub>in</sub> ≤ V <sub>SS</sub> + 0.2 V, or ≥ V <sub>CC</sub> – 0.2 V)	I <sub>SB2</sub>	120	200	mA

**CAPACITANCE** (f = 1 MHz, dV = 3 V, T<sub>A</sub> = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Cache Address Input Capacitance	C <sub>in</sub>	48	pF
Control Pin Input Capacitance	( $\bar{E}$ , $\bar{W}$ ) C <sub>in</sub>	8	pF
I/O Capacitance	C <sub>I/O</sub>	8	pF
Tag Address Input Capacitance	C <sub>in</sub>	18	pF

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 5 ns  
 Output Timing Measurement Reference Level ..... 1.5 V  
 Output Load ..... Figure 1A Unless Otherwise Noted

**READ CYCLE** (See Notes 1 and 2)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t <sub>AVAV</sub>	30	—	30	—	30	—	ns	3
Address Access Time xCA2-3 (Transparent Mode) A4 - A19	t <sub>AVQV</sub>	—	20	—	12	—	—	ns	9
	t <sub>AVQV</sub>	—	25	—	12	—	25	ns	
Chip Select Access Time	t <sub>ELQV</sub>	—	20	—	12	—	20	ns	4
Output Enable to Output Valid	t <sub>GLQV</sub>	—	10	—	6	—	—	ns	
Output Hold from Address Change	t <sub>AXQX</sub>	4	—	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t <sub>ELQX</sub>	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High-Z	t <sub>EHQZ</sub>	—	9	—	7	—	9	ns	5,6,7
Output Enable Low to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High-Z	t <sub>GHQZ</sub>	—	8	—	6	—	—	ns	5,6,7

NOTES:

- $\bar{W}$  is high for read cycle.
- $\bar{E} = \bar{E}xx, \bar{E}T; \bar{W} = \bar{W}xx, \bar{W}T, \bar{W}A; \bar{G} = \bar{G}A, \bar{G}B$
- All timings are referenced from the last valid address to the first transitioning address.
- Addresses valid prior to or coincident with  $\bar{E}$  going low.
- At any given voltage and temperature, t<sub>EHQZ</sub> (max) is less than t<sub>ELQX</sub> (min), and t<sub>GHQZ</sub> (max) is less than t<sub>GLQX</sub> (min), both for a given device and from device to device.
- Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ( $\bar{E} = V_{IL}, \bar{G} = V_{IL}$ ).
- TAG Address Access Time t<sub>AVTV</sub>.

**AC TEST LOADS**

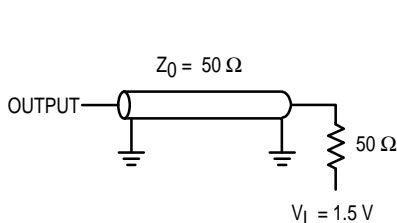


Figure 1A

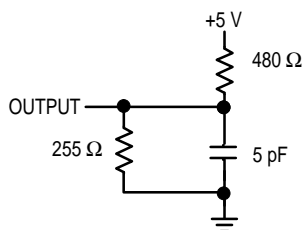
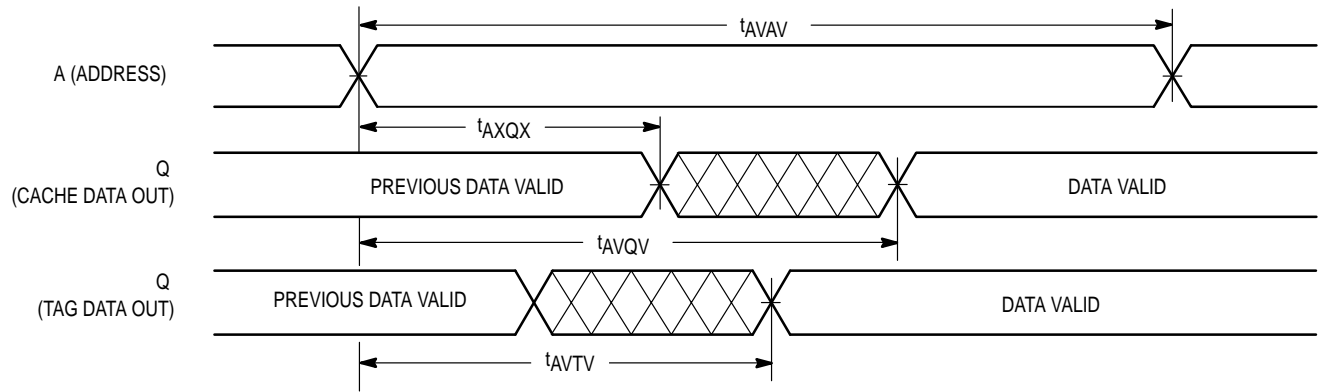


Figure 1B

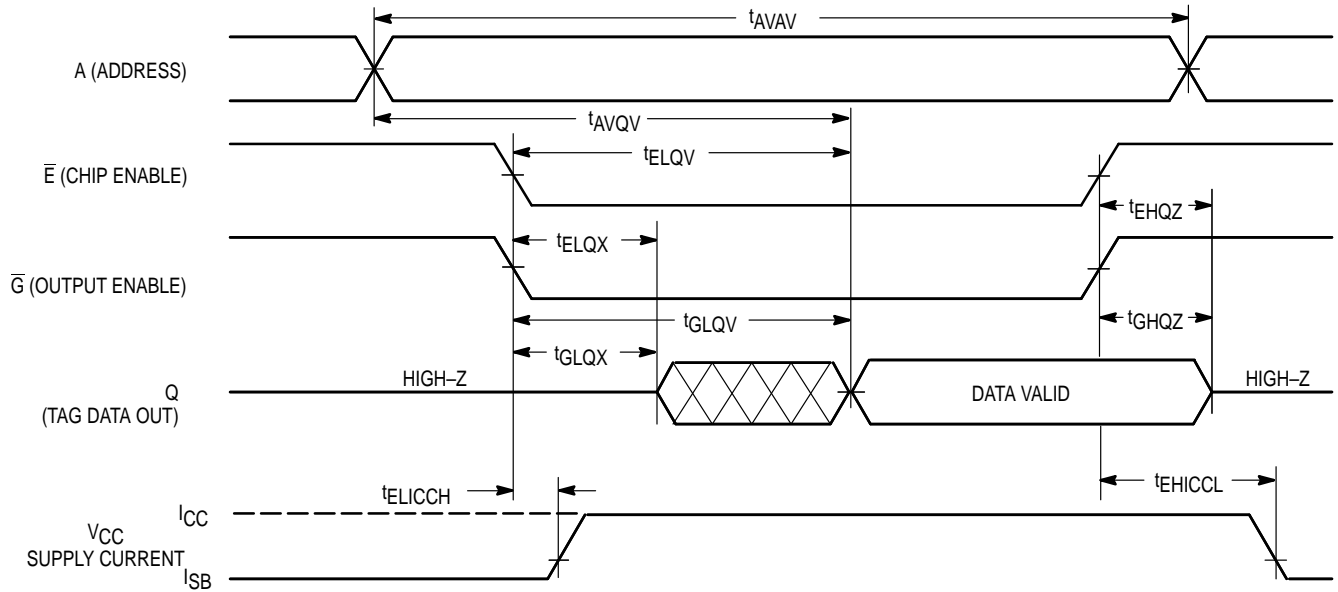
**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1 (See Note 7)**



**READ CYCLE 2 (See Note 3)**



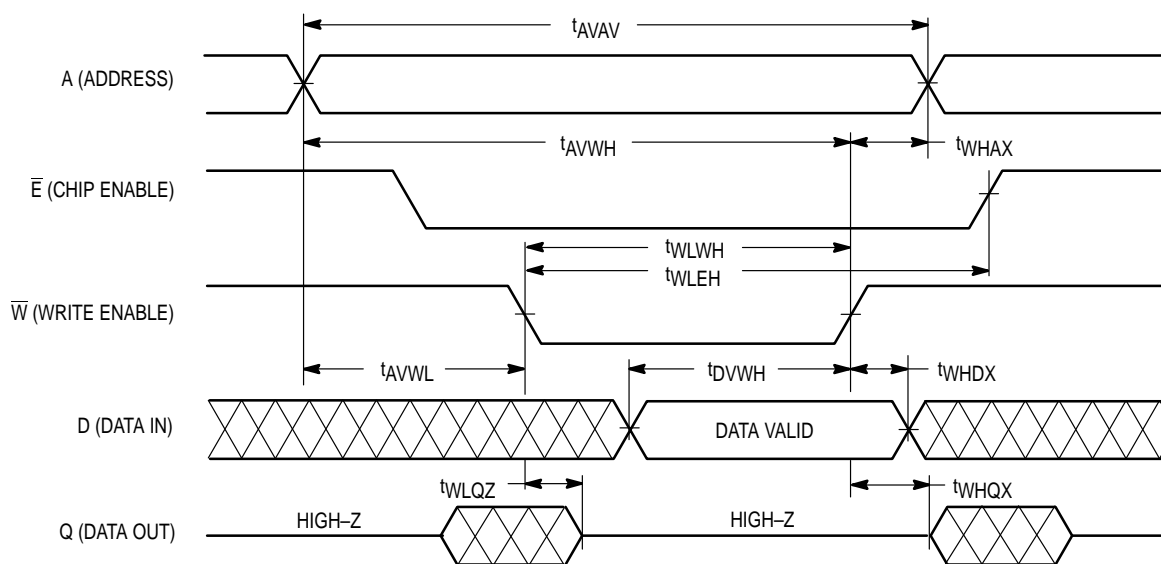
**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	30	—	30	—	30	—	ns	4
Address Setup Time (A4 – A5) (A6 – A19)	$t_{AVWL}$	2 10	— —	— 2	— —	— 10	— —	ns	
Address Valid to End of Write	$t_{AVWH}$	20	—	10	—	20	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	12	—	12	—	12	—	ns	
Data Setup to Write Time	$t_{DVWH}$	8	—	6	—	8	—	ns	
Data Hold from Write Time	$t_{WHDX}$	0	—	0	—	0	—	ns	
Write Low to Output High-Z	$t_{WLQZ}$	0	8	0	6	0	8	ns	6,7,8
Write High to Output Active	$t_{WHQX}$	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
2.  $\overline{E} = \overline{E}x, \overline{E}T; \overline{W} = \overline{W}x, \overline{W}T, \overline{W}A; \overline{G} = \overline{G}A, \overline{G}B$
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If  $\overline{G} \geq V_{IH}$ , the output will remain in a high impedance state.
6. At any given voltage and temperature,  $t_{WLQZ}$  (max) is less than  $t_{WHQX}$  (min), both for a given device and from device to device.
7. Transition is measured  $\pm 500$  mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

**WRITE CYCLE 1** ( $\overline{W}$  Controlled, See Notes 1 and 2)



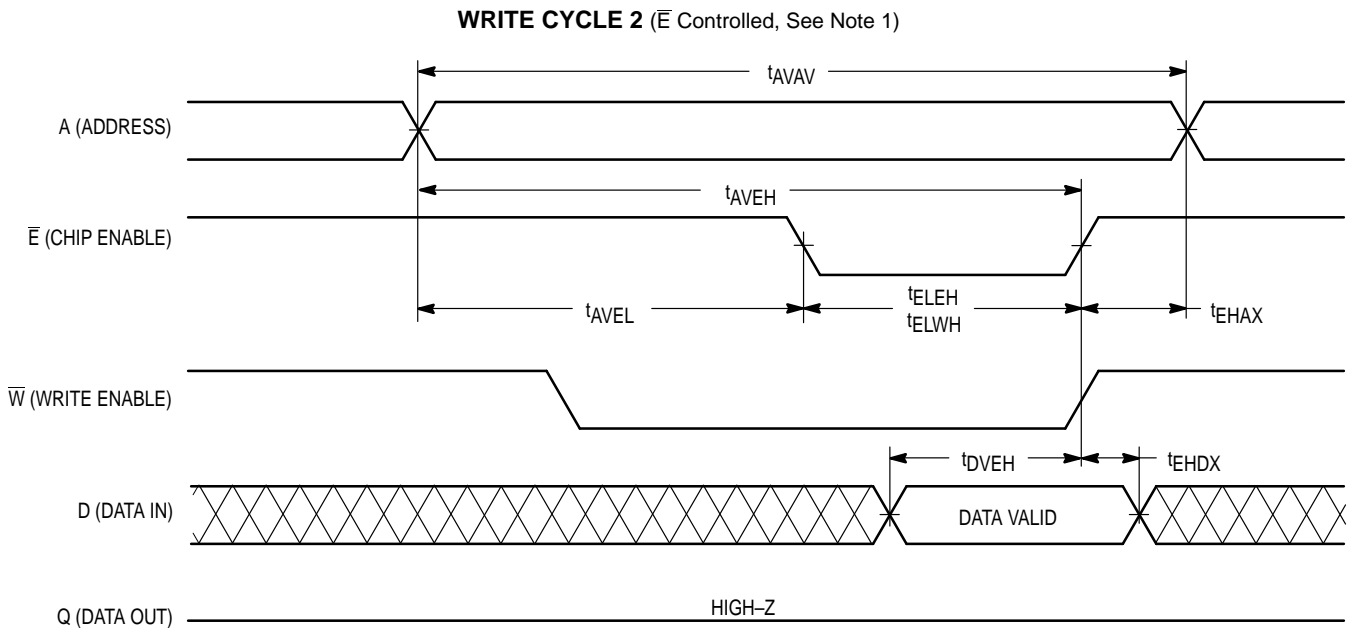


**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	30	—	30	—	30	—	ns	4
Address Setup Time (A4 – A5) (A6 – A19)	$t_{AVEL}$	2 10	— —	— 2	— —	— 10	— —	ns	
Address Valid to End of Write	$t_{AVEH}$	20	—	10	—	20	—	ns	
Write Pulse Width	$t_{ELEH}$ , $t_{ELWH}$	15	—	10	—	15	—	ns	
Data Setup to Write Time	$t_{DVEH}$	8	—	6	—	8	—	ns	
Data Hold from Write Time	$t_{EHDX}$	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	ns	

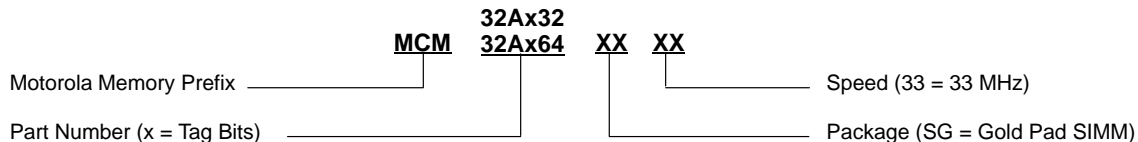
**NOTES:**

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2.  $\bar{E}$  =  $\bar{E}x$ ,  $\bar{E}T$ ;  $\bar{W}$  =  $\bar{W}x$ ,  $\bar{W}T$ ,  $\bar{W}A$ ;  $\bar{G}$  =  $\bar{G}A$ ,  $\bar{G}B$
3. All timings are referenced from the last valid address to the first transitioning address.
4. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high impedance state.
5. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high impedance state.




## ORDERING INFORMATION

(Order by Full Part Number)

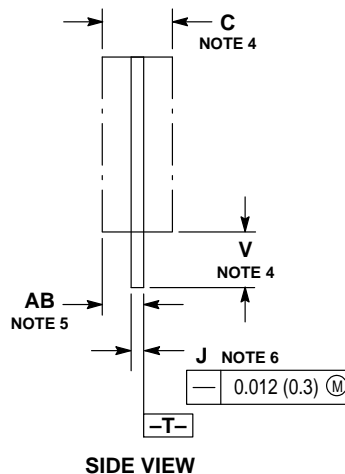
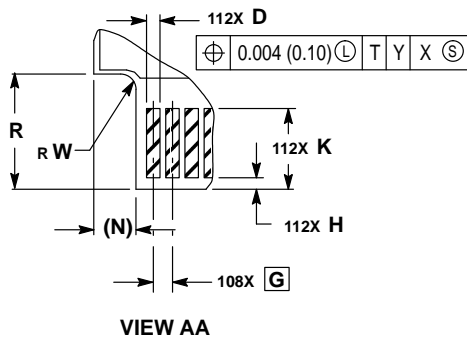
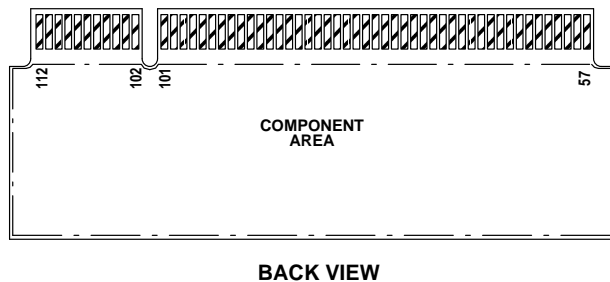
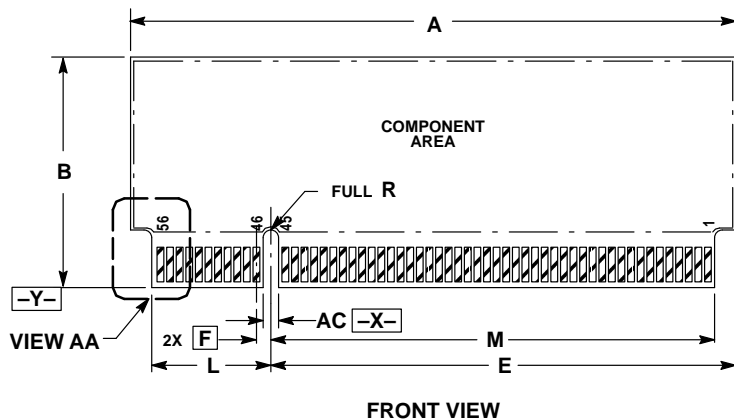


Full Part Numbers — MCM32A732SG33 MCM32A764SG33  
MCM32A832SG33 MCM32A864SG33  
MCM32A932SG33 MCM32A964SG33

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# PACKAGE DIMENSIONS

## 112-LEAD CARD EDGE MODULE CASE 1112-01



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
  4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
  5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
  6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	3.130	3.150	79.50	80.01
B	1.190	1.210	30.23	30.73
C	—	0.365	—	9.27
D	0.033	0.037	0.84	0.94
E	2.415	2.425	61.34	61.60
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.030	—	0.76
J	0.055	0.069	1.40	1.75
K	0.210	—	5.33	—
L	0.605	0.615	15.37	15.62
M	2.305	2.315	58.55	58.80
N	0.110 REF		2.79 REF	
R	0.285	0.305	7.24	7.75
V	0.285	—	7.24	—
W	0.040	0.060	1.02	1.52
AB	—	0.220	—	5.59
AC	0.072	0.076	1.83	1.93

**Literature Distribution Centers:**

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.



**MOTOROLA**



MCM32A732/D

