NVE CORPORATION

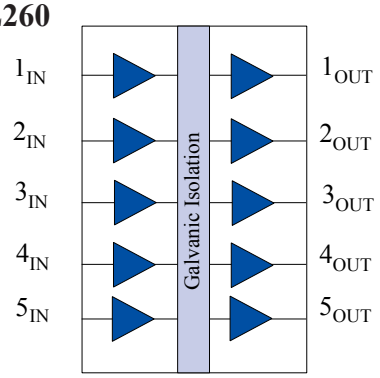
Preliminary

IL26X IsoLoop®

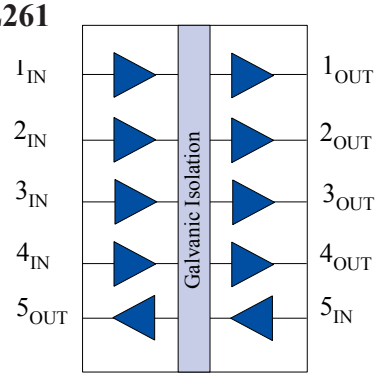
High Speed Five Channel Digital Coupler

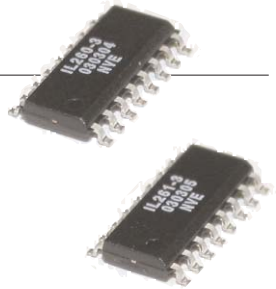
Functional Diagram

IL260



IL261





Features

- 5V CMOS/TTL Compatible
- High Speed: 110 MBaud
- 2500 V_{RMS} Isolation (1 min)
- 2 ns Typical Pulse Width Distortion
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- 30 kV/µs Typical Transient Immunity
- 2 ns Channel to Channel Skew
- 0.3" and 0.15" 16–Pin SOIC Packages
- Extended Temperature Range (-40°C to +85°C)
- UL1577 Approval Pending
- IEC 61010-1 Approval Pending

Isolation Applications

- ADCs and DACs
- Multiplexed Data Transmission
- Data Interfaces
- Board-To-Board Communication
- Digital Noise Reduction
- Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting
- Plasma Displays

Description

NVE's family of high-speed digital isolators are CMOS devices created by integrating active circuitry and our GMR-based and patented* IsoLoop® technology. The IL260 and IL261 are five channel versions of the world's fastest digital isolator with a 110 Mbaud data rate. These devices provide the designer with the most compact isolated logic devices yet available. All transmit and receive channels operate at 110 Mbd over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns achieving the best specifications of any isolator device. Typical transient immunity of 30 kV/µs is unsurpassed. The IL260 has five transmit channels, while the IL261 has four transmit channels and one receive channel. Their high channel density make them ideally suited to isolating multiple ADCs and DACs, parallel buses and peripheral interfaces.

Performance is specified over the temperature range of -40°C to +85°C without any derating.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	175	°C
Ambient Operating Temperature[1]	T_A	-55	125	°C
Supply Voltage	V_{DD1}, V_{DD2}	-0.5	7	Volts
Input Voltage	V_I	-0.5	V_{DD}+0.5	Volts
Output Voltage	V_O	-0.5	V_{DD}+0.5	Volts
Output Current Drive Channel	I_O		10	mA
Lead Solder Temperature (10s)			280	°C
ESD	2kV Human Body Model			

Recommended Operating Conditions

Parameters	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	85	°C
Supply Voltage (5.0 V operation)	V_{DD1},V_{DD2}	4.5	5.5	Volts
Logic High Input Voltage	V_{IH}	2.4	V_{DD}	Volts
Logic Low Input Voltage	V_{IL}	0	0.8	Volts
Minimum Signal Rise and Fall Times	t_{IR},t_{IF}		1	µsec

Insulation Specifications

Parameter	Symbol	Min	Typ.	Max.	Units	Test Condition
Barrier Impedance				$>10^{14}$ ||7		Ω || pF
Creepage Distance (External)		8.077 (0.3" SOIC) 4.026 (0.15" SOIC)			mm	
Leakage Current			0.2		µA	240 V_{RMS}

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input-Output)[5]	C_{I-O}		4.0		pF	f= 1MHz
Thermal Resistance	θ_{JCT}				°C/W	Thermocouple located at
0.15" 16-Pin SOIC			40			center underside of package
0.30" 16-Pin SOIC			28			
Package Power Dissipation	P_{PD}		65		mW	f= 1MHz ,V_{DD}=5V

IEC61010-1*

TUV Certificate Numbers: Pending
Classification as Table 1.

Model	Pollution Degree	Material Group	Max Working Voltage	Package Type *16–SOIC (0.3")*	Package Type *16–SOIC (0.15")*
IL260, IL261	II	III	300 V_{RMS}	✓	
IL260-3, IL261-3	II	III	150 V_{RMS}		✓

UL 1577*

Component Recognition program. File # Pending
Rated 2500Vrms for 1min.

* UL & IEC approval is pending for the these parts.

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Electrical Specifications

Electrical Specifications are T_{min} to T_{max}

Parameter	Symbol	5.0 Volt Specifications			Units	Test Conditions
DC Specifications		**Min.**	**Typ.**	**Max.**		
Input Quiescent Supply Current						
IL260	I_{DD1}		30	40		µA
IL261	I_{DD1}		2.5	3.0		mA
Output Quiescent Supply Current						
IL260	I_{DD2}		10	15		mA
IL261	I_{DD2}		8	12		mA
Logic Input Current	I_I	-10		10		µA
Logic High Output Voltage	V_{OH}	V_{DD}-0.1	V_{DD}		V	I_O =-20 µA, V_I =V_{IH}
	0.8*V_{DD}	V_{DD}-0.5				I_O = -4 mA, V_I =V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I =V_{IL}
		0.5	0.8			I_O = 4 mA, V_I =V_{IL}
Switching Parameters						
Maximum Data Rate			100	110	MBd	C_L = 15 pF
Minimum Pulse Width	PW		10		ns	50% points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion[2] | tPHL- tPLH |	PWD		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10-90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10-90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	|CMH| |CML|	20	30		kV/µs	Vcm = 300V
Channel to Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption[6]			170	210	µA/mHz	per Channel

Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $| t_{PHL} - t_{PLH} |$. %PWD is equal to the PWD divided by the pulse width.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1-8 shorted and pins 9-16 shorted.
6. Dynamic power consumption numbers are calculated per channel.

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Application Notes:

Dynamic Power Consumption

Isoloop® devices achieve their low power consumption from the manner by which they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on-state and frequency.

The approximate power supply current per channel for Isoloop® is:

$$I(\text{input}) = 40\left(\frac{f}{fmax}\right)\left(\frac{1}{4}\right)\text{ mA}$$

where f = operating frequency
fmax = 50 MHz

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 100 nF ceramic capacitors. For data rates in excess of 10MBd, use of ground planes for both GND1 and GND2 is highly recommended. Capacitors should be located as close as possible to the device.

Signal Status on Start-up and Shut Down

To minimize power dissipation, the input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start-up circuit. Initialization consists of toggling each channel either high then low or low then high, depending on the desired state.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are *pulse width distortion* and *propagation delay skew*.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in ns. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \text{ x } 100\%$$

For example: For data rates of 12.5 Mb

$$\text{PWD\%} = \frac{3\text{ ns}}{80\text{ ns}} \text{ x } 100\% = \textbf{3.75\%}$$

This figure is almost ***three times*** better than for any available optocoupler with the same temperature range, and ***two times*** better than any optocoupler regardless of published temperature range. The *IsoLoop*® range of isolators will run at almost 35 Mb before reaching the 10% limit.

Propagation delay skew is the difference in time taken for two or more channels to propagate their signals. This becomes significant when clocking is involved since it is undesirable for the clock pulse to arrive before the data has settled. A short propagation delay skew is therefore critical, especially in high data rate parallel systems, to establish and maintain accuracy and repeatability. The *IsoLoop*® range of isolators all have a maximum propagation delay skew of 6 ns, which is ***five times*** better than any optocoupler. The maximum channel to channel skew in the IsoLoop® coupler is only 3 ns which is ***ten times*** better than any optocoupler.

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Applications:

Figure 1 Single Channel ΔΣ

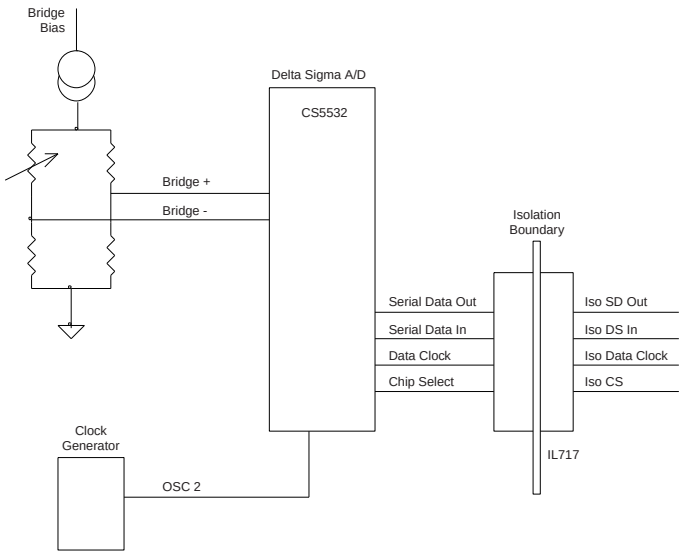
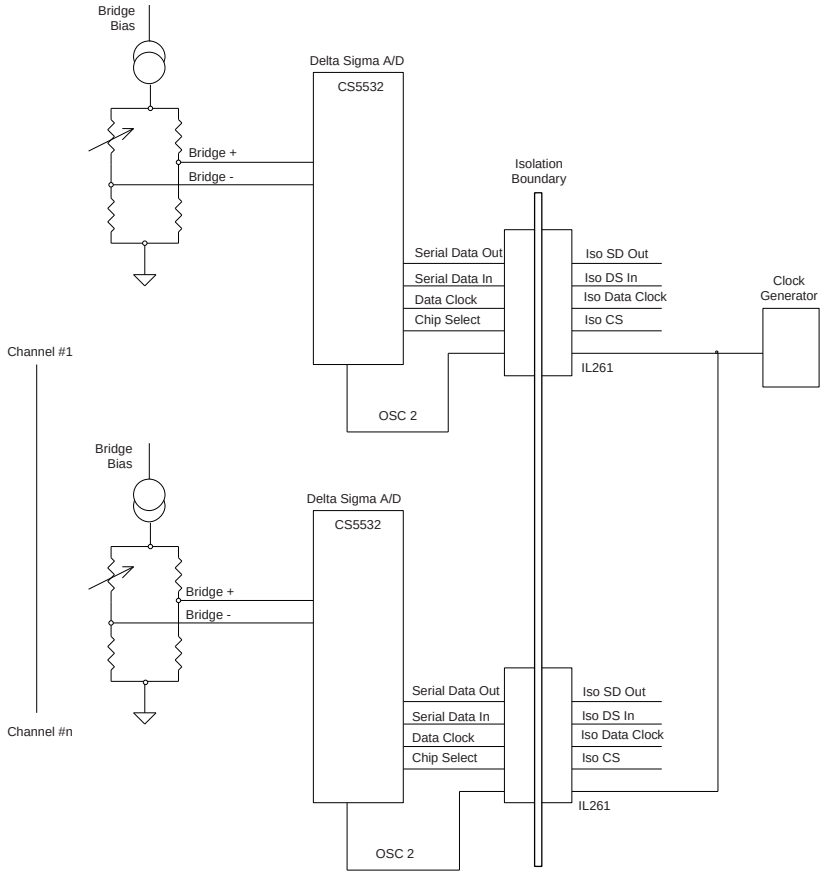


Figure 1 shows a typical single channel ΔΣ ADC application. The A/D is located on the bridge with no signal conditioning electronics between the bridge sensor and the ADC. In this application, the IL717 is the best choice for isolation. It isolates the control bus from the microcontroller. The system clock is located on the isolated side of the system.

Figure 2 Multi Channel ΔΣ

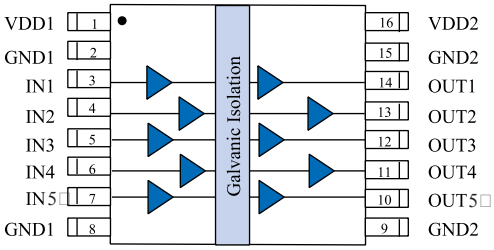


The second ΔΣ application is where multiple ADC's are configured in a channel-to-channel isolation configuration. The problem for designers is how to control clock jitter and edge placement accuracy of the system clock for each ADC. The best solution is to use a single clock on the system side and distribute this to each ADC. The IL261 adds a 5th channel to the IL717. This 5th channel is used to distribute a single, isolated clock to multiple ADC's as shown in Figure 2.

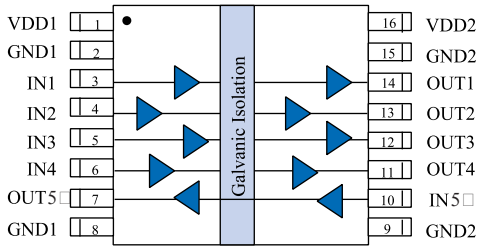
Pin Configurations IL260, IL261

Note: Connected Internally
Pins 2 & 8
Pins 9 & 15

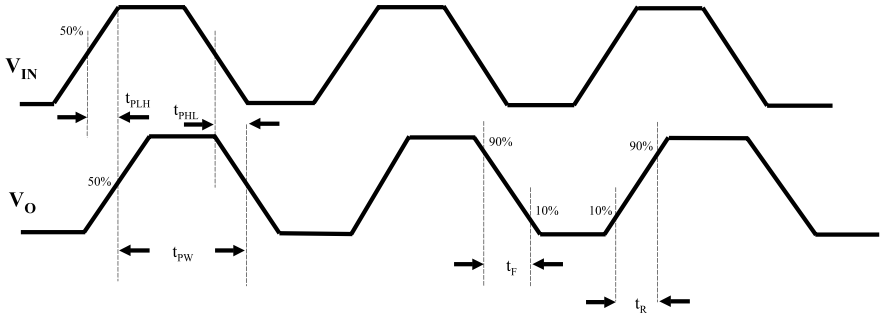
IL260□



IL261



Timing Diagram

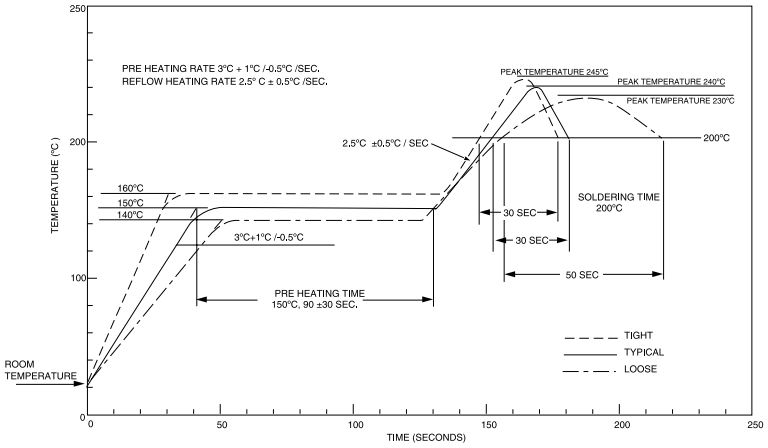


Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

IR Soldering Profile

Recommended profile shown. Maximum temperature allowed on any profile is 260° C.



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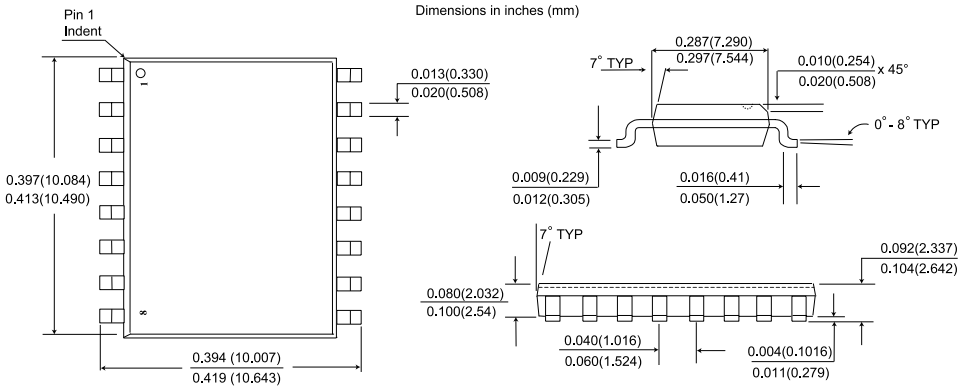
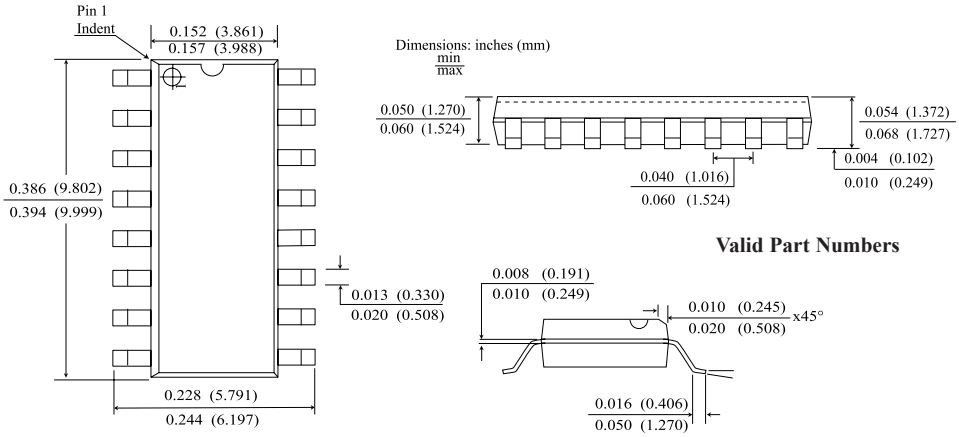
0.3" SOIC-16 Package



0.15" SOIC-16 Package



Ordering Information: use the following format to order these devices

IL 260 -3 B TR13

Bulk Package
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Supply Voltage
B = 5.0 VDC

Package
Blank = SOIC (0.3")
-3 = SOIC (0.15")

Base Part Number
260 = 5 drive channels
261 = 4 drive and 1 receive channels

Product Family
IL = Isolators

Valid Part Numbers

IL 260B	IL 261B
IL 260-3B	IL 261-3B
IL 260BTR13	IL 261BTR13
IL 260-3BTR13	IL 261-3BTR13
IL 260-3BTR7	IL 261-3BTR7