HD66787

528-channel, One-chip Driver with 262,144-color Display RAM and Power Supply Circuit for Low-temperature Poli-Si TFT (LTPS-TFT) Panels with Incorporated Gate Drivers

REJxxxxxxx-xxxx
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10 June, 2003

Description

The HD66787 handles 262,144 TFT colors and can drive a TFT color liquid crystal display of 176RGB x 240 dots with an incorporated RAM compliant to a graphics display of 176 RGB x 240 dots at maximum, a 528-channel source driver, and a power supply circuit. The HD66787 generates signals to control panel-integrated gate circuit to drive a TFT panel with incorporated gate driver with a single chip.

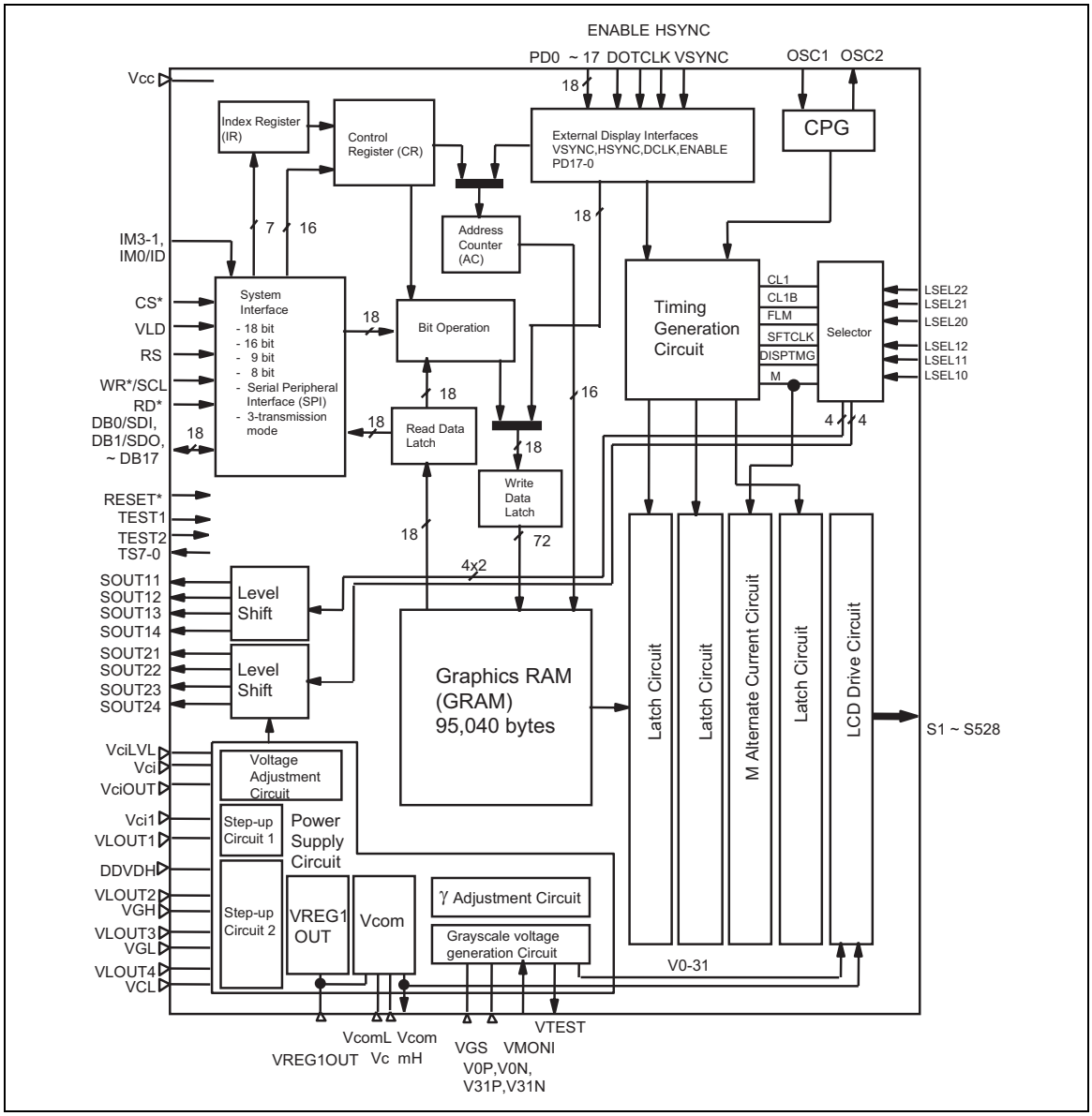
The HD66787's bit-operation functions, 8/9/16/18-bit high-speed bus interface, and high-speed RAM-write functions enable efficient transfer of data and high-speed data update on a graphics RAM. The HD66787 incorporates 6/16/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0) and VSYNC interface (system interface + VSYNC) as an interface for moving picture display. With a window address function that facilitates the moving picture display in an arbitrary area and simultaneous display of moving pictures and the contents of the internal RAM, the HD66787 enables moving picture display not constrained by the still picture area. Accordingly, the data transmission is reduced to minimum, thereby saving power consumed by a system as a whole when displaying moving pictures.

The HD66787 supports power-saving operation up to the power supply voltage of 2.4V with a voltage follower circuit that generate voltage to drive liquid crystal. The HD66787 also incorporates 8-color display and standby functions that allow precise power control by software. These features make this LSI the ideal solution for any medium or small sized portable battery-driven products such as digital cellular phones supporting WWW browsers or small PDA, where long battery life and board size are major concern.

Features

- Liquid crystal controller/driver for 262,144 TFT-color 176RGB x 240-dot graphics display
- Control signal for a low-temperature poly-Si TFT (LTPS-TFT) panel with incorporated gate circuit
- Single chip solution for gate-less display panels
- System interface
  - 8-/9-/16-/18-bit high-speed bus interface
  - Serial Peripheral Interface (SPI)
  - 8-bit transmission x 3 times (262k/65k color modes)
- Interface for moving picture display
  - 6-/16-/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0)
  - VSYNC interface (System interface + VSYNC)
- High-speed burst RAM write function
- Window address function to write data to the rectangular area of RAM specified by the window address
  - Interface to facilitate moving picture display in an arbitrary area
  - Reduce data transmission by transmitting only the data for the moving picture display area
  - Simultaneous display of moving pictures and the contents of the internal RAM
- Bit unit operations for processing graphics
  - Write data mask function by bit
  - Logical operation and conditional rewrite by pixel
- Functions for controlling abundant color displays
  - Simultaneous availability of 262,144 colors with γ-correction function
  - Line-unit vertical scrolling
- Low-power architecture: features for low-power operation
  - Vcc = 2.4 ~ 3.3 V (internal logic power supply)
  - IOVcc = 1.8 ~ 3.3 V (interface I/O power supply)
  - Vci = 2.5 ~ 3.3 V (analogue power supply)
  - DDVDH = 4.5 ~ 5.5 V (liquid-crystal drive voltage)
  - Power-saving drive function (standby mode etc.)
  - Partial liquid crystal drive to display two screens at arbitrary positions
  - Voltage followers for liquid crystal drive power circuit to fend off the direct current from bleeder-resistors
- Step-up circuit generating liquid crystal drive voltage boosted up to 6-time scale
- 95,040-byte internal RAM
- Incorporated liquid crystal display driver with 582 source outputs
- n-raster-row liquid crystal AC drive, enabling polarity inversion by every arbitrary number of raster-rows
- Internal oscillation, and hardware reset
- Reversible direction of signals between RAM and source driver
- Exclusive for Cst structure

Block Diagram



Pin Functions

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM3~1, IM0/ID</td><td>4</td><td>I</td><td>GND or IOVcc</td><td>Pins to select MPU-interface mode.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU-Interface Mode</th><th>DB Pin</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>IOVcc</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>GND</td><td>GND</td><td>IOVcc</td><td>GND</td><td>80-system 16-bit interface</td><td>DB17~10, DB8~1</td></tr>
<tr><td>GND</td><td>GND</td><td>IOVcc</td><td>IOVcc</td><td>80-system 8-bit interface</td><td>DB17 ~10</td></tr>
<tr><td>GND</td><td>IOVcc</td><td>GND</td><td>ID</td><td>Serial Peripheral Interface (SPI)</td><td>DB1~ 0</td></tr>
<tr><td>GND</td><td>IOVcc</td><td>IOVcc</td><td>*</td><td>Setting disabled</td><td></td></tr>
<tr><td>IOVcc</td><td>GND</td><td>GND</td><td>GND</td><td>Setting disabled</td><td></td></tr>
<tr><td>IOVcc</td><td>GND</td><td>GND</td><td>IOVcc</td><td>Setting disabled</td><td></td></tr>
<tr><td>IOVcc</td><td>GND</td><td>IOVcc</td><td>GND</td><td>80-system 18-bit interface</td><td>DB17~0</td></tr>
<tr><td>IOVcc</td><td>GND</td><td>IOVcc</td><td>IOVcc</td><td>80-system 9-bit interface</td><td>DB17~9</td></tr>
<tr><td>IOVcc</td><td>IOVcc</td><td>*</td><td>*</td><td>Setting disabled</td><td></td></tr>
</table>
When Serial Peripheral Interface is selected, IM0 pin is used for the device code ID setting.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Select the HD66787.
Low: the HD6678 is selected and accessible
High: the HD66787 is not selected and not accessible
Must be fixed to the GND level while not used.</td></tr>
<tr><td>VLD</td><td>1</td><td>I</td><td>MPU</td><td>Indicate whether data is valid or not during RAM write.
Low: Valid (Write data to RAM).
High: Invalid (Not write data to RAM).
RAM address is updated irrespective of VLD.
Must be fixed to the GND level while not used.
This signal is available when external display interface is used.
<table>
<tr><th>CS</th><th>VLD</th><th>RAM Write</th><th>RAM Address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>1</td><td>*</td><td>Invalid</td><td>Hold</td></tr>
</table></td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions
RS	1	I	MPU	Select register. Low: Index/status, High: Control Fix to the “IOVcc” or “GND” level while using SPI.
WR*/SCL	1	I	MPU	In 80-system bus interface mode, serves as a write strobe signal. Data are written at “Low” level. In Serial Peripheral Interface mode, serves as synchronizing clock signal.
RD*	1	I	MPU	In 80-system bus interface mode, serves as read-strobe signal. Data are read at the low level of the signal. Fix to the “IOVcc” or “GND” level while using SPI.
DB0/SDI	1	I/O	MPU	18-bit parallel bi-directional data bus. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0 Unused pins must be fixed to the IOVcc or GND level. Serves as serial data input pin (SDI) in Serial Peripheral Interface mode, where data are input on the rising edge of SCL signal.
DB1/SDO	1	I/O	MPU	18-bit parallel bi-directional data bus. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0 Unused pins must be fixed to the IOVcc or GND level. Serves as serial data output pin (SDO) in Serial Peripheral Interface mode, where data are output on the falling edge of the SCL signal.
DB2~DB17	16	I/O	MPU	18-bit parallel bi-directional data bus. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0 Unused pins must be fixed to the IOVcc or GND level.
ENABLE	1	I	MPU	Indicate whether RAM data are valid or not when RGB interface is used. Low: Selected (access enabled) High: Not selected (access disabled) Must be fixed to the IOVcc or GND level while not used. ENABLE signal invert the polarity according to the setting of EPL resister.

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>
<table>
<tr><th>EPL</th><th>ENABLE</th><th>VLD</th><th>RAM Write</th><th>RAM Address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
</table>
</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Frame synchronizing signal.
This signal is active low.
Must be fixed at the IOVcc level while not used.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Line synchronizing signal.
This signal is active low.
Must be fixed at the IOVcc level while not used.</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>Dot-clock signal
This signal is active low
The timing of data input is determined at the falling edge of the signal. Must be fixed at the IOVcc level while not used</td></tr>
<tr><td>PD0~PD17</td><td>18</td><td>I</td><td>MPU</td><td>18-bit bus for RGB data.
6-bit bus: PD17-PD12
16-bit bus: PD17-PD13 and PD11-PD1
18-bit bus: PD17-PD0
Unused pins must be fixed to the IOVcc or GND level.</td></tr>
<tr><td>RESET*</td><td>1</td><td>I</td><td>MPU or reset circuit</td><td>Reset pin.
Initializes the LSI at the “Low” level.
Power-on reset required after turning on the power.</td></tr>
<tr><td>S1~S528</td><td>528</td><td>O</td><td>LCD</td><td>Output voltage applied to liquid crystal.
The shift direction of segment signals is changeable with SS bit. For example, if SS = 0, RAM address “0000” is output from S1. If SS = 1, it is output from S528.
S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).</td></tr>
<tr><td>LSEL22,21,20</td><td>3</td><td>I</td><td>GND or IOVcc</td><td>Output level shift output signals, SOUT24, 23, 22,21.</td></tr>
<tr><td>LSEL12,11,10</td><td>3</td><td>I</td><td>GND or IOVcc</td><td>Output level shift output signals, SOUT14, 13, 12,11.</td></tr>
</table>

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>SOUT14,13, 12,11
SOUT24,23, 22,21</td><td>8</td><td>O</td><td>LCD</td><td>Level-shift and then output display clocks.
Output pins for SOUT14-11 are arranged on either left or right side of the chip and pins for SOUT24-21 are arranged on the other side of the chip. The kinds of output signals can be selected as shown in the following table with LSEL22-20 and LSEL12-10 bits and output from both or either one side of SOUT14-11 and SOUT 24-21 pins. If signals are output from either one side, halt the operation of unused circuits.
When signals are output from SOUT14-11, SOUT 24-21 pins, 6 different kind of 8 level-shift signals are output at maximum. The amplitude of level-shift signal is between VGH and VGL.
Pin settings / Level shift signal
<table>
<tr><th colspan="3">Pin settings</th><th colspan="4">Level shift signal</th></tr>
<tr><th>LSEL 12</th><th>LSEL 11</th><th>LSEL 10</th><th>SOUT 11</th><th>SOUT 12</th><th>SOUT 13</th><th>SOUT 14</th></tr>
<tr><th>LSEL 22</th><th>LSEL 21</th><th>LSEL 20</th><th>SOUT 21</th><th>SOUT 22</th><th>SOUT 23</th><th>SOUT 24</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>FLM</td><td>SFTCLK</td><td>CL1</td><td>CL1B</td></tr>
<tr><td>GND</td><td>GND</td><td>IOVcc</td><td>FLM</td><td>SFTCLK</td><td>CL1</td><td>DISPTMG</td></tr>
<tr><td>GND</td><td>IOVcc</td><td>GND</td><td>FLM</td><td>SFTCLK</td><td>M</td><td>CL1B</td></tr>
<tr><td>GND</td><td>IOVcc</td><td>IOVcc</td><td>FLM</td><td>SFTCLK</td><td>M</td><td>DISPTMG</td></tr>
<tr><td>IOVcc</td><td>GND</td><td>GND</td><td>FLM</td><td>DISPTMG</td><td>CL1</td><td>CL1B</td></tr>
<tr><td>IOVcc</td><td>GND</td><td>IOVcc</td><td colspan="4">Setting disabled</td></tr>
<tr><td>IOVcc</td><td>IOVcc</td><td>GND</td><td colspan="4">Setting disabled</td></tr>
<tr><td>IOVcc</td><td>IOVcc</td><td>IOVcc</td><td>Halt (VGL)</td><td>Halt (VGL)</td><td>Halt (VGL)</td><td>Halt (VGL)</td></tr>
</table>
</td></tr>
<tr><td>Vcom1, Vcom2</td><td>2</td><td>O</td><td>TFT common electrode</td><td>Power supply for TFT common electrode.
When Vcom AC drive is not selected, output the same level of voltage as VcomL level. When Vcom AC drive is selected, output the voltage with the amplitude between VcomH and VcomL. The AC cycle can be set with M signal.
Connect to the TFT common electrode.</td></tr>
<tr><td>VcomR</td><td>1</td><td>I</td><td>Variable resistor or open</td><td>Reference voltage for VcomH.
When adjusting VcomH externally, VcomH internal adjusting circuit must be halted by register setting and place a variable resistor between VREG1OUT and GND to make an adjustment. Otherwise, leave open and adjust VcomH by internal-register setting.</td></tr>
<tr><td>VcomH</td><td>1</td><td>O</td><td>Stabilizing capacitor</td><td>High level of Vcom during Vcom AC drive. Connect to a stabilizing capacitor.</td></tr>
<tr><td>VcomL</td><td>1</td><td>O</td><td>Stabilizing capacitor or open</td><td>Vcom voltage when Vcom AC drive is not selected.
Low level of Vcom during Vcom AC drive. Voltage can be adjusted with internal registers. Connect to a stabilizing capacitor. When VCOMG bit is set to LOW, a stabilizing capacitor is not necessary because VcomL output is halted.</td></tr>
<tr><td>C11+, C11-</td><td>2</td><td>-</td><td>Step-up capacitor</td><td>Step-up capacitor connection pins for step-up circuit 1. When the internal step-up circuit is not used, leave open.</td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions
C12+, C12- C21+, C21- C22+, C22-	6	-	Step-up capacitor	Step-up capacitor connection pins for step-up circuit 2. Capacitor connection will be necessary depending on the step-up scale. When the internal step-up circuit is not used, leave open.
OSC1, OSC2	2	I or O	Resistor for the oscillator	Connect to an external resistor for R-C oscillation. When supplying clock signals externally, it must be supplied through OSC1 and leave OSC2 open.
FLM	1	O	MPU or open	Frame head pulse with amplitude between GND and Vcc. Use when writing data to RAM in synchronization with FLM. When FLM is not used, leave open.
Vci	1	I	Power supply	Power supply for analogue circuits. In this case, power supply for the VciOUT amplifier. Connect to an external power supply of 2.5~3.3V.
VciLVL	1	I	Power supply	Generates a reference voltage (VciOUT, REGP) in accordance to the ratio set with VC2~0 registers. Connect to the same power supply as the Vci, which has separate wiring from the VciLVL on the FPC.
REGP	1	I/O	Test pin	Test pin for VREG1OUT. Leave open.
VciOUT	1	I	Stabilizing capacitor, Vci1	Internal reference voltage with amplitude between Vci and GND. Set with VC bit.
Vci1	1	I	VciOUT	A reference voltage for the step-up circuit 1. Connect to an external power supply of 2.75V or less when the internal reference voltage is not used.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output twice stepped-up Vci1 voltage from the step-up circuit 1. Connect to a stabilizing capacitor. VLOUT1 = 4.0~5.5V
DDVDH	1	I	VLOUT1	Power supply for source driver liquid crystal output portion. A reference voltage for the step-up circuit 2.
VLOUT2	1	O	Stabilizing capacitor, VGH	Output stepped-up DDVDH voltage, which is stepped up to the level Vci1 x 4~6 from the step-up circuit 2. The step-up scale is determined with BT bits. Connect to a stabilizing capacitor. VLOUT2 = max 16.5V
VGH	1	I	VLOUT2	Power supply for TFT gate drive. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	Output stepped-up DDVDH voltage, which is stepped up to the level Vci1 x (- 3) ~ (-5) from the step-up circuit 2. The step-up scale is determined with BT bits. Connect to a stabilizing capacitor. VLOUT2 = min -16.5V
VGL	1	I	VLOUT3	A power supply for TFT gate drive. Connect to VLOUT3.
VLOUT4	1	O	Stabilizing capacitor, VCL	Output the Vci1 x (-1) voltage from the step-up circuit 2. Connect to a stabilizing capacitor. VLOUT4 = 0 ~ -3.3V
VCL	1	I	VLOUT4	Power supply for VcomL drive. Connect to VLOUT4.

Signals	Number of Pins	I/O	Connected to	Functions
VREG1OUT	1	I/O	Stabilizing capacitor or power supply	Reference voltage with amplitude between DDVDH and GND, which is generated from the reference voltage internally generated with amplitude between Vci and GND. The scale of output voltage can be set with VRH bits. VREG1OUT becomes (1) a source driver grayscale reference voltage VDH, (2) a VcomH level reference voltage, or (3) a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V
Vcc	1	-	Power supply	Power supply for a logic circuit. Vcc = 2.4 ~ 3.3V
IOVcc	1	-	Power supply	Power supply for interface pins. IOVcc = 1.8 ~ 3.3V. IOVcc must be turned on with the same voltage as the internal logic voltage Vcc. When it is assembled on COG, connect to Vcc on the FPC to avoid effects from the noise when IOVcc is used.
RVcc	1	-	Power supply	Vcc power supply for RAM. Supply with the same potential as the Vcc.
GND	1	-	Power supply	Ground for the logic side. GND = 0V
AGND	1	-	Power supply	Ground for the analog side. AGND = 0V. When assembled on COG, connect to GND on the FPC to avoid effects from the noise.
RGND	1	-	Power supply	Ground for internal RAM. RGND = 0V. When assembled on COG, connect to GND on the FPC to avoid effects from the noise.
TEST1	1	I	GND	Test pin. Fix it to the GND level.
TEST2	1	I	GND	Test pin. Fix it to the GND level.
V0P, V31P	2	I or O	Stabilizing capacitor	Output from internal positive polarity operational amplifier when the operational amplifier is ON (SAP2-0 = “001”, “010”, “011”, “100”, and “101”). Stabilize by connecting to a capacitor.
V0N, V31N	2	I or O	Stabilizing capacitor	Output from internal negative polarity operational amplifier when the operational amplifier is ON (SAP2-0 = “001”, “010”, “011”, “100”, and “101”). Stabilize by connecting to a capacitor.
VGS	1	I	GND or external resistor	Reference level for grayscale voltage generation circuit. Connect to an external resistor when source driver is used to adjust grayscale levels for each panel.
VTESTS	1	I/O	open	Test pin. Leave open.
TS0~TS7	8	O	open	Test pin. Leave open.
TESTA1	1	I/O	open	Test pin for VcomH. Leave open.
TESTA2	1	I/O	open	Test pin for VcomL. Leave open.
TESTA4	1	I/O	open	Test pin for VcomL. Leave open or connect to a stabilizing capacitor depending on the display quality.
VMONI	1	O	open	Test pin. Leave open.
IOVccDUM1~4	4	O	Input pin	Internal IOVcc level. When neighboring input pins are fixed to the IOVcc side, short-circuit them.

Signals	Number of Pins	I/O	Connected to	Functions
IOGNDDUM1~7	7	O	Input pin	Internal GND level. When neighboring input pins are fixed to the IOVcc side, short-circuit them.
TESTO1~2	2	-	-	Dummy pads. Leave open.
DUMMY		-	-	Dummy pad. Leave open.
DUMMYR		-	-	Dummy pad. Leave open.

PAD Arrangement

- Chip Size : 20.50mm×2.80mm
- Chip Thickness : 550μm (typ.)
- Pad Coordinate: PAD Center
- Coordinate Origin : Chip center

- Au bump size :

(1) 80μm x 80μm
Corner dummy
No.1, No211, No.229, No.768

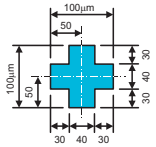
(2)54μm×100μm
Input :
No.2 ~ No.210 ,
No.230 ~ No.234 , No.763 ~ No.767

(3)100μm×54μm
Input :
No.212 ~ No.228 , No.769 ~ No.791

(4)33μm×77μm
Laced LCD output side:
No.235 ~ No.762

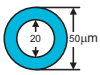
- Au bump pitch : see PAD coordinate
- Au bump height :15μm (typ.)
- Numbers in the figure indecates numbers of PAD coordinate
- Alignment mark

(1) Arrangement : 2 places
Coordinate(X,Y)= (-9394.4, 1214.7)
Coordinate(X,Y)= (9394.4, 1214.7)

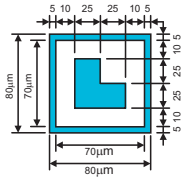


(2-a) Coordinate(X,Y) =(-10024.0,1264.6)

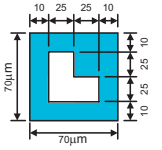
(2-b) Coordinate(X,Y) =(10024.0,1264.6)

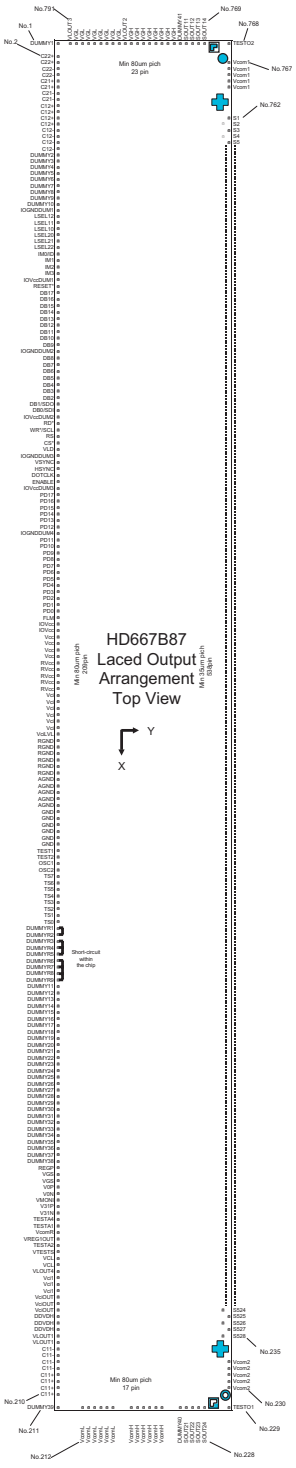


(3-a)Coordinate (X,Y) = (-10114.6, 1160.7)



(3-b)Coordinate (X,Y) = (10114.6, 1160.7)





PAD Coordinate

pad No	pad name	X	Y
1	DUMMY1	-10114.0	-1264.0
2	C22+	-9885.5	-1254.0
3	C22+	-9805.3	-1254.0
4	C22-	-9725.2	-1254.0
5	C22-	-9645.0	-1254.0
6	C21+	-9564.9	-1254.0
7	C21+	-9484.7	-1254.0
8	C21-	-9404.6	-1254.0
9	C21-	-9324.4	-1254.0
10	C12+	-9186.0	-1254.0
11	C12+	-9105.9	-1254.0
12	C12+	-9025.7	-1254.0
13	C12+	-8945.6	-1254.0
14	C12-	-8807.1	-1254.0
15	C12-	-8727.0	-1254.0
16	C12-	-8646.8	-1254.0
17	C12-	-8566.7	-1254.0
18	DUMMY2	-8433.7	-1254.0
19	DUMMY3	-8353.5	-1254.0
20	DUMMY4	-8273.4	-1254.0
21	DUMMY5	-8193.2	-1254.0
22	DUMMY6	-8113.1	-1254.0
23	DUMMY7	-8032.9	-1254.0
24	DUMMY8	-7952.8	-1254.0
25	DUMMY9	-7872.6	-1254.0
26	DUMMY10	-7792.5	-1254.0
27	IOGNDDUM1	-7618.5	-1254.0
28	LSEL12	-7501.1	-1254.0
29	LSEL11	-7421.0	-1254.0
30	LSEL10	-7340.8	-1254.0
31	LSEL20	-7260.7	-1254.0
32	LSEL21	-7180.5	-1254.0
33	LSEL22	-7100.4	-1254.0
34	IM0/ID	-7020.2	-1254.0
35	IM1	-6940.1	-1254.0
36	IM2	-6859.9	-1254.0
37	IM3	-6779.8	-1254.0
38	IOVccDUM1	-6635.3	-1254.0
39	RESET*	-6512.5	-1254.0
40	DB17	-6372.9	-1254.0
41	DB16	-6292.7	-1254.0
42	DB15	-6212.6	-1254.0
43	DB14	-6132.4	-1254.0
44	DB13	-6052.3	-1254.0
45	DB12	-5972.1	-1254.0
46	DB11	-5892.0	-1254.0
47	DB10	-5811.8	-1254.0
48	DB9	-5731.7	-1254.0
49	IOGNDDUM2	-5587.2	-1254.0
50	DB8	-5469.9	-1254.0
51	DB7	-5389.7	-1254.0
52	DB6	-5309.6	-1254.0
53	DB5	-5229.4	-1254.0
54	DB4	-5149.3	-1254.0
55	DB3	-5069.1	-1254.0
56	DB2	-4989.0	-1254.0
57	DB1/SDO	-4908.8	-1254.0
58	DB0/SDI	-4828.7	-1254.0
59	IOVccDUM2	-4684.2	-1254.0
60	RD*	-4566.9	-1254.0
61	WR*/SCL	-4486.7	-1254.0
62	RS	-4406.6	-1254.0
63	CS*	-4326.4	-1254.0
64	VLD	-4246.3	-1254.0
65	IOGNDDUM3	-4101.8	-1254.0
66	VSYNC	-3984.5	-1254.0
67	HSYNC	-3904.3	-1254.0
68	DOTCLK	-3824.2	-1254.0
69	ENABLE	-3744.0	-1254.0
70	IOVccDUM3	-3599.6	-1254.0
71	PD17	-3482.2	-1254.0
72	PD16	-3402.1	-1254.0
73	PD15	-3321.9	-1254.0
74	PD14	-3241.8	-1254.0
75	PD13	-3161.6	-1254.0
76	PD12	-3081.5	-1254.0
77	IOGNDDUM4	-2937.0	-1254.0
78	PD11	-2819.7	-1254.0
79	PD10	-2739.5	-1254.0
80	PD9	-2659.4	-1254.0
81	PD8	-2579.2	-1254.0
82	PD7	-2499.1	-1254.0
83	PD6	-2418.9	-1254.0
84	PD5	-2338.8	-1254.0
85	PD4	-2258.6	-1254.0
86	PD3	-2178.5	-1254.0
87	PD2	-2098.3	-1254.0
88	PD1	-2018.2	-1254.0
89	PD0	-1938.0	-1254.0
90	FLM	-1857.9	-1254.0
91	IOVcc	-1702.6	-1254.0
92	IOVcc	-1622.4	-1254.0
93	Vcc	-1478.6	-1254.0
94	Vcc	-1398.4	-1254.0
95	Vcc	-1307.4	-1254.0
96	Vcc	-1227.3	-1254.0
97	RVcc	-1083.4	-1254.0
98	RVcc	-1003.3	-1254.0
99	RVcc	-912.3	-1254.0
100	RVcc	-832.1	-1254.0
101	RVcc	-752.0	-1254.0
102	Vci	-608.1	-1254.0
103	Vci	-528.0	-1254.0
104	Vci	-447.8	-1254.0
105	Vci	-367.7	-1254.0
106	Vci	-287.5	-1254.0
107	Vci	-207.4	-1254.0
108	VciLVL	-57.7	-1254.0
109	RGND	86.6	-1254.0
110	RGND	166.8	-1254.0
111	RGND	246.9	-1254.0
112	RGND	327.1	-1254.0
113	RGND	407.2	-1254.0
114	RGND	487.4	-1254.0
115	AGND	620.4	-1254.0
116	AGND	700.5	-1254.0
117	AGND	780.7	-1254.0
118	AGND	860.8	-1254.0
119	AGND	941.0	-1254.0
120	GND	1074.0	-1254.0
121	GND	1154.1	-1254.0
122	GND	1287.1	-1254.0
123	GND	1367.3	-1254.0
124	GND	1447.4	-1254.0
125	GND	1527.6	-1254.0
126	TEST1	1679.2	-1254.0
127	TEST2	1759.4	-1254.0
128	OSC1	1899.0	-1254.0
129	OSC2	1979.2	-1254.0
130	TS7	2118.8	-1254.0
131	TS6	2199.0	-1254.0
132	TS5	2279.1	-1254.0
133	TS4	2359.3	-1254.0
134	TS3	2439.4	-1254.0
135	TS2	2519.6	-1254.0
136	TS1	2599.7	-1254.0
137	TS0	2679.9	-1254.0
138	DUMMYR1	2824.3	-1254.0
139	DUMMYR2	2904.5	-1254.0
140	DUMMYR3	2984.6	-1254.0
141	DUMMYR4	3064.8	-1254.0
142	DUMMYR5	3144.9	-1254.0
143	DUMMYR6	3225.1	-1254.0
144	DUMMYR7	3305.2	-1254.0
145	DUMMYR8	3385.4	-1254.0
146	DUMMYR9	3465.5	-1254.0
147	DUMMY11	3598.5	-1254.0
148	DUMMY12	3678.7	-1254.0
149	DUMMY13	3758.8	-1254.0
150	DUMMY14	3839.0	-1254.0
151	DUMMY15	3919.1	-1254.0
152	DUMMY16	3999.3	-1254.0
153	DUMMY17	4079.4	-1254.0
154	DUMMY18	4159.6	-1254.0
155	DUMMY19	4239.7	-1254.0
156	DUMMY20	4319.9	-1254.0
157	DUMMY21	4400.0	-1254.0
158	DUMMY22	4480.2	-1254.0
159	DUMMY23	4560.3	-1254.0
160	DUMMY24	4640.5	-1254.0
161	DUMMY25	4720.6	-1254.0
162	DUMMY26	4800.8	-1254.0
163	DUMMY27	4880.9	-1254.0
164	DUMMY28	4961.1	-1254.0
165	DUMMY29	5041.2	-1254.0
166	DUMMY30	5121.4	-1254.0
167	DUMMY31	5201.5	-1254.0
168	DUMMY32	5281.7	-1254.0
169	DUMMY33	5361.8	-1254.0
170	DUMMY34	5442.0	-1254.0
171	DUMMY35	5522.1	-1254.0
172	DUMMY36	5602.3	-1254.0
173	DUMMY37	5682.4	-1254.0
174	DUMMY38	5762.6	-1254.0
175	REGP	5969.8	-1254.0
176	VGS	6115.4	-1254.0
177	VGS	6241.2	-1254.0
178	V0P	6367.0	-1254.0
179	V0N	6492.9	-1254.0
180	VMONI	6618.7	-1254.0
181	V31P	6744.5	-1254.0
182	V31N	6870.3	-1254.0
183	TESTA4	7020.0	-1254.0
184	TESTA1	7302.8	-1254.0
185	VcomR	7428.6	-1254.0
186	VREG1OUT	7554.4	-1254.0
187	TESTA2	7680.2	-1254.0
188	VTESTS	7806.1	-1254.0
189	VCL	7950.3	-1254.0
190	VCL	8033.1	-1254.0
191	VLOUT4	8113.3	-1254.0
192	Vci1	8251.7	-1254.0
193	Vci1	8331.8	-1254.0
194	Vci1	8412.0	-1254.0
195	VciOUT	8492.1	-1254.0
196	VciOUT	8572.3	-1254.0
197	VciOUT	8652.4	-1254.0
198	DDVDH	8796.3	-1254.0
199	DDVDH	8876.4	-1254.0
200	DDVDH	8956.6	-1254.0
201	VLOUT1	9100.4	-1254.0
202	VLOUT1	9180.6	-1254.0
203	C11-	9324.4	-1254.0
204	C11-	9404.6	-1254.0
205	C11-	9484.7	-1254.0
206	C11-	9564.9	-1254.0
207	C11+	9645.0	-1254.0
208	C11+	9725.2	-1254.0
209	C11+	9805.3	-1254.0
210	C11+	9885.5	-1254.0
211	DUMMY39	10114.0	-1264.0
212	VcomL	10104.0	-1035.5
213	VcomL	10104.0	-897.1
214	VcomL	10104.0	-758.6
215	VcomL	10104.0	-620.2
216	VcomL	10104.0	-481.8
217	VcomL	10104.0	-343.4
218	VcomH	10104.0	-204.9
219	VcomH	10104.0	-66.5
220	VcomH	10104.0	71.9
221	VcomH	10104.0	210.4
222	VcomH	10104.0	348.8
223	VcomH	10104.0	487.2
224	DUMMY40	10104.0	655.3
225	SOUT21	10104.0	788.3
226	SOUT22	10104.0	868.4
227	SOUT23	10104.0	948.6
228	SOUT24	10104.0	1028.7
229	TESTO1	10114.0	1264.0
230	Vcom2	9892.1	1254.0
231	Vcom2	9811.9	1254.0
232	Vcom2	9731.8	1254.0
233	Vcom2	9651.6	1254.0
234	Vcom2	9571.5	1254.0
235	S528	9240.0	1148.5
236	S527	9205.0	1265.5
237	S526	9170.0	1148.5
238	S525	9135.0	1265.5
239	S524	9100.0	1148.5
240	S523	9065.0	1265.5
241	S522	9030.0	1148.5
242	S521	8995.0	1265.5
243	S520	8960.0	1148.5
244	S519	8925.0	1265.5
245	S518	8890.0	1148.5
246	S517	8855.0	1265.5
247	S516	8820.0	1148.5
248	S515	8785.0	1265.5
249	S514	8750.0	1148.5
250	S513	8715.0	1265.5
251	S512	8680.0	1148.5
252	S511	8645.0	1265.5
253	S510	8610.0	1148.5
254	S509	8575.0	1265.5
255	S508	8540.0	1148.5
256	S507	8505.0	1265.5
257	S506	8470.0	1148.5
258	S505	8435.0	1265.5
259	S504	8400.0	1148.5
260	S503	8365.0	1265.5
261	S502	8330.0	1148.5
262	S501	8295.0	1265.5
263	S500	8260.0	1148.5
264	S499	8225.0	1265.5
265	S498	8190.0	1148.5
266	S497	8155.0	1265.5
267	S496	8120.0	1148.5
268	S495	8085.0	1265.5
269	S494	8050.0	1148.5
270	S493	8015.0	1265.5
271	S492	7980.0	1148.5
272	S491	7945.0	1265.5
273	S490	7910.0	1148.5
274	S489	7875.0	1265.5
275	S488	7840.0	1148.5
276	S487	7805.0	1265.5
277	S486	7770.0	1148.5
278	S485	7735.0	1265.5
279	S484	7700.0	1148.5
280	S483	7665.0	1265.5
281	S482	7630.0	1148.5
282	S481	7595.0	1265.5
283	S480	7560.0	1148.5
284	S479	7525.0	1265.5
285	S478	7490.0	1148.5
286	S477	7455.0	1265.5
287	S476	7420.0	1148.5
288	S475	7385.0	1265.5
289	S474	7350.0	1148.5
290	S473	7315.0	1265.5
291	S472	7280.0	1148.5
292	S471	7245.0	1265.5
293	S470	7210.0	1148.5
294	S469	7175.0	1265.5
295	S468	7140.0	1148.5
296	S467	7105.0	1265.5
297	S466	7070.0	1148.5
298	S465	7035.0	1265.5
299	S464	7000.0	1148.5
300	S463	6965.0	1265.5
301	S462	6930.0	1148.5
302	S461	6895.0	1265.5
303	S460	6860.0	1148.5
304	S459	6825.0	1265.5
305	S458	6790.0	1148.5
306	S457	6755.0	1265.5
307	S456	6720.0	1148.5
308	S455	6685.0	1265.5
309	S454	6650.0	1148.5
310	S453	6615.0	1265.5
311	S452	6580.0	1148.5
312	S451	6545.0	1265.5
313	S450	6510.0	1148.5
314	S449	6475.0	1265.5
315	S448	6440.0	1148.5
316	S447	6405.0	1265.5
317	S446	6370.0	1148.5
318	S445	6335.0	1265.5
319	S444	6300.0	1148.5
320	S443	6265.0	1265.5
321	S442	6230.0	1148.5
322	S441	6195.0	1265.5
323	S440	6160.0	1148.5
324	S439	6125.0	1265.5
325	S438	6090.0	1148.5
326	S437	6055.0	1265.5
327	S436	6020.0	1148.5
328	S435	5985.0	1265.5
329	S434	5950.0	1148.5
330	S433	5915.0	1265.5
331	S432	5880.0	1148.5
332	S431	5845.0	1265.5
333	S430	5810.0	1148.5
334	S429	5775.0	1265.5
335	S428	5740.0	1148.5
336	S427	5705.0	1265.5
337	S426	5670.0	1148.5
338	S425	5635.0	1265.5
339	S424	5600.0	1148.5
340	S423	5565.0	1265.5
341	S422	5530.0	1148.5
342	S421	5495.0	1265.5
343	S420	5460.0	1148.5
344	S419	5425.0	1265.5
345	S418	5390.0	1148.5
346	S417	5355.0	1265.5
347	S416	5320.0	1148.5
348	S415	5285.0	1265.5
349	S414	5250.0	1148.5
350	S413	5215.0	1265.5
351	S412	5180.0	1148.5
352	S411	5145.0	1265.5
353	S410	5110.0	1148.5
354	S409	5075.0	1265.5
355	S408	5040.0	1148.5
356	S407	5005.0	1265.5
357	S406	4970.0	1148.5
358	S405	4935.0	1265.5
359	S404	4900.0	1148.5
360	S403	4865.0	1265.5
361	S402	4830.0	1148.5
362	S401	4795.0	1265.5
363	S400	4760.0	1148.5
364	S399	4725.0	1265.5
365	S398	4690.0	1148.5
366	S397	4655.0	1265.5
367	S396	4620.0	1148.5
368	S395	4585.0	1265.5
369	S394	4550.0	1148.5
370	S393	4515.0	1265.5
371	S392	4480.0	1148.5
372	S391	4445.0	1265.5
373	S390	4410.0	1148.5
374	S389	4375.0	1265.5
375	S388	4340.0	1148.5
376	S387	4305.0	1265.5
377	S386	4270.0	1148.5
378	S385	4235.0	1265.5
379	S384	4200.0	1148.5
380	S383	4165.0	1265.5
381	S382	4130.0	1148.5
382	S381	4095.0	1265.5
383	S380	4060.0	1148.5
384	S379	4025.0	1265.5
385	S378	3990.0	1148.5
386	S377	3955.0	1265.5
387	S376	3920.0	1148.5
388	S375	3885.0	1265.5
389	S374	3850.0	1148.5
390	S373	3815.0	1265.5
391	S372	3780.0	1148.5
392	S371	3745.0	1265.5
393	S370	3710.0	1148.5
394	S369	3675.0	1265.5
395	S368	3640.0	1148.5
396	S367	3605.0	1265.5
397	S366	3570.0	1148.5
398	S365	3535.0	1265.5
399	S364	3500.0	1148.5
400	S363	3465.0	1265.5

pad No	pad name	X	Y
401	S362	3430.0	1148.5
402	S361	3395.0	1265.5
403	S360	3360.0	1148.5
404	S359	3325.0	1265.5
405	S358	3290.0	1148.5
406	S357	3255.0	1265.5
407	S356	3220.0	1148.5
408	S355	3185.0	1265.5
409	S354	3150.0	1148.5
410	S353	3115.0	1265.5
411	S352	3080.0	1148.5
412	S351	3045.0	1265.5
413	S350	3010.0	1148.5
414	S349	2975.0	1265.5
415	S348	2940.0	1148.5
416	S347	2905.0	1265.5
417	S346	2870.0	1148.5
418	S345	2835.0	1265.5
419	S344	2800.0	1148.5
420	S343	2765.0	1265.5
421	S342	2730.0	1148.5
422	S341	2695.0	1265.5
423	S340	2660.0	1148.5
424	S339	2625.0	1265.5
425	S338	2590.0	1148.5
426	S337	2555.0	1265.5
427	S336	2520.0	1148.5
428	S335	2485.0	1265.5
429	S334	2450.0	1148.5
430	S333	2415.0	1265.5
431	S332	2380.0	1148.5
432	S331	2345.0	1265.5
433	S330	2310.0	1148.5
434	S329	2275.0	1265.5
435	S328	2240.0	1148.5
436	S327	2205.0	1265.5
437	S326	2170.0	1148.5
438	S325	2135.0	1265.5
439	S324	2100.0	1148.5
440	S323	2065.0	1265.5
441	S322	2030.0	1148.5
442	S321	1995.0	1265.5
443	S320	1960.0	1148.5
444	S319	1925.0	1265.5
445	S318	1890.0	1148.5
446	S317	1855.0	1265.5
447	S316	1820.0	1148.5
448	S315	1785.0	1265.5
449	S314	1750.0	1148.5
450	S313	1715.0	1265.5
451	S312	1680.0	1148.5
452	S311	1645.0	1265.5
453	S310	1610.0	1148.5
454	S309	1575.0	1265.5
455	S308	1540.0	1148.5
456	S307	1505.0	1265.5
457	S306	1470.0	1148.5
458	S305	1435.0	1265.5
459	S304	1400.0	1148.5
460	S303	1365.0	1265.5
461	S302	1330.0	1148.5
462	S301	1295.0	1265.5
463	S300	1260.0	1148.5
464	S299	1225.0	1265.5
465	S298	1190.0	1148.5
466	S297	1155.0	1265.5
467	S296	1120.0	1148.5
468	S295	1085.0	1265.5
469	S294	1050.0	1148.5
470	S293	1015.0	1265.5
471	S292	980.0	1148.5
472	S291	945.0	1265.5
473	S290	910.0	1148.5
474	S289	875.0	1265.5
475	S288	840.0	1148.5
476	S287	805.0	1265.5
477	S286	770.0	1148.5
478	S285	735.0	1265.5
479	S284	700.0	1148.5
480	S283	665.0	1265.5
481	S282	630.0	1148.5
482	S281	595.0	1265.5
483	S280	560.0	1148.5
484	S279	525.0	1265.5
485	S278	490.0	1148.5
486	S277	455.0	1265.5
487	S276	420.0	1148.5
488	S275	385.0	1265.5
489	S274	350.0	1148.5
490	S273	315.0	1265.5
491	S272	280.0	1148.5
492	S271	245.0	1265.5
493	S270	210.0	1148.5
494	S269	175.0	1265.5
495	S268	140.0	1148.5
496	S267	105.0	1265.5
497	S266	70.0	1148.5
498	S265	35.0	1265.5
499	S264	-35.0	1148.5
500	S263	-70.0	1265.5

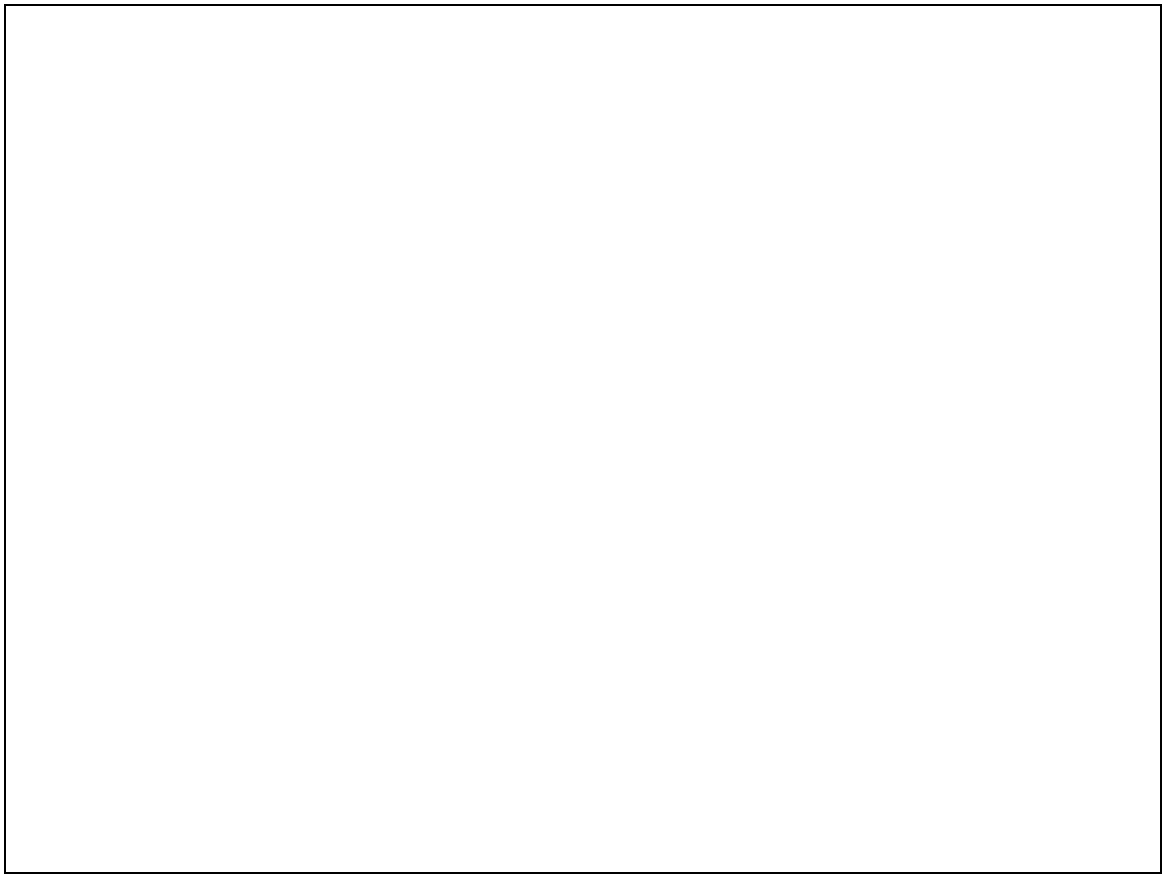
pad No	pad name	X	Y
501	S262	-105.0	1148.5
502	S261	-140.0	1265.5
503	S260	-175.0	1148.5
504	S259	-210.0	1265.5
505	S258	-245.0	1148.5
506	S257	-280.0	1265.5
507	S256	-315.0	1148.5
508	S255	-350.0	1265.5
509	S254	-385.0	1148.5
510	S253	-420.0	1265.5
511	S252	-455.0	1148.5
512	S251	-490.0	1265.5
513	S250	-525.0	1148.5
514	S249	-560.0	1265.5
515	S248	-595.0	1148.5
516	S247	-630.0	1265.5
517	S246	-665.0	1148.5
518	S245	-700.0	1265.5
519	S244	-735.0	1148.5
520	S243	-770.0	1265.5
521	S242	-805.0	1148.5
522	S241	-840.0	1265.5
523	S240	-875.0	1148.5
524	S239	-910.0	1265.5
525	S238	-945.0	1148.5
526	S237	-980.0	1265.5
527	S236	-1015.0	1148.5
528	S235	-1050.0	1265.5
529	S234	-1085.0	1148.5
530	S233	-1120.0	1265.5
531	S232	-1155.0	1148.5
532	S231	-1190.0	1265.5
533	S230	-1225.0	1148.5
534	S229	-1260.0	1265.5
535	S228	-1295.0	1148.5
536	S227	-1330.0	1265.5
537	S226	-1365.0	1148.5
538	S225	-1400.0	1265.5
539	S224	-1435.0	1148.5
540	S223	-1470.0	1265.5
541	S222	-1505.0	1148.5
542	S221	-1540.0	1265.5
543	S220	-1575.0	1148.5
544	S219	-1610.0	1265.5
545	S218	-1645.0	1148.5
546	S217	-1680.0	1265.5
547	S216	-1715.0	1148.5
548	S215	-1750.0	1265.5
549	S214	-1785.0	1148.5
550	S213	-1820.0	1265.5
551	S212	-1855.0	1148.5
552	S211	-1890.0	1265.5
553	S210	-1925.0	1148.5
554	S209	-1960.0	1265.5
555	S208	-1995.0	1148.5
556	S207	-2030.0	1265.5
557	S206	-2065.0	1148.5
558	S205	-2100.0	1265.5
559	S204	-2135.0	1148.5
560	S203	-2170.0	1265.5
561	S202	-2205.0	1148.5
562	S201	-2240.0	1265.5
563	S200	-2275.0	1148.5
564	S199	-2310.0	1265.5
565	S198	-2345.0	1148.5
566	S197	-2380.0	1265.5
567	S196	-2415.0	1148.5
568	S195	-2450.0	1265.5
569	S194	-2485.0	1148.5
570	S193	-2520.0	1265.5
571	S192	-2555.0	1148.5
572	S191	-2590.0	1265.5
573	S190	-2625.0	1148.5
574	S189	-2660.0	1265.5
575	S188	-2695.0	1148.5
576	S187	-2730.0	1265.5
577	S186	-2765.0	1148.5
578	S185	-2800.0	1265.5
579	S184	-2835.0	1148.5
580	S183	-2870.0	1265.5
581	S182	-2905.0	1148.5
582	S181	-2940.0	1265.5
583	S180	-2975.0	1148.5
584	S179	-3010.0	1265.5
585	S178	-3045.0	1148.5
586	S177	-3080.0	1265.5
587	S176	-3115.0	1148.5
588	S175	-3150.0	1265.5
589	S174	-3185.0	1148.5
590	S173	-3220.0	1265.5
591	S172	-3255.0	1148.5
592	S171	-3290.0	1265.5
593	S170	-3325.0	1148.5
594	S169	-3360.0	1265.5
595	S168	-3395.0	1148.5
596	S167	-3430.0	1265.5
597	S166	-3465.0	1148.5
598	S165	-3500.0	1265.5
599	S164	-3535.0	1148.5
600	S163	-3570.0	1265.5

pad No	pad name	X	Y
601	S162	-3605.0	1148.5
602	S161	-3640.0	1265.5
603	S160	-3675.0	1148.5
604	S159	-3710.0	1265.5
605	S158	-3745.0	1148.5
606	S157	-3780.0	1265.5
607	S156	-3815.0	1148.5
608	S155	-3850.0	1265.5
609	S154	-3885.0	1148.5
610	S153	-3920.0	1265.5
611	S152	-3955.0	1148.5
612	S151	-3990.0	1265.5
613	S150	-4025.0	1148.5
614	S149	-4060.0	1265.5
615	S148	-4095.0	1148.5
616	S147	-4130.0	1265.5
617	S146	-4165.0	1148.5
618	S145	-4200.0	1265.5
619	S144	-4235.0	1148.5
620	S143	-4270.0	1265.5
621	S142	-4305.0	1148.5
622	S141	-4340.0	1265.5
623	S140	-4375.0	1148.5
624	S139	-4410.0	1265.5
625	S138	-4445.0	1148.5
626	S137	-4480.0	1265.5
627	S136	-4515.0	1148.5
628	S135	-4550.0	1265.5
629	S134	-4585.0	1148.5
630	S133	-4620.0	1265.5
631	S132	-4655.0	1148.5
632	S131	-4690.0	1265.5
633	S130	-4725.0	1148.5
634	S129	-4760.0	1265.5
635	S128	-4795.0	1148.5
636	S127	-4830.0	1265.5
637	S126	-4865.0	1148.5
638	S125	-4900.0	1265.5
639	S124	-4935.0	1148.5
640	S123	-4970.0	1265.5
641	S122	-5005.0	1148.5
642	S121	-5040.0	1265.5
643	S120	-5075.0	1148.5
644	S119	-5110.0	1265.5
645	S118	-5145.0	1148.5
646	S117	-5180.0	1265.5
647	S116	-5215.0	1148.5
648	S115	-5250.0	1265.5
649	S114	-5285.0	1148.5
650	S113	-5320.0	1265.5
651	S112	-5355.0	1148.5
652	S111	-5390.0	1265.5
653	S110	-5425.0	1148.5
654	S109	-5460.0	1265.5
655	S108	-5495.0	1148.5
656	S107	-5530.0	1265.5
657	S106	-5565.0	1148.5
658	S105	-5600.0	1265.5
659	S104	-5635.0	1148.5
660	S103	-5670.0	1265.5
661	S102	-5705.0	1148.5
662	S101	-5740.0	1265.5
663	S100	-5775.0	1148.5
664	S99	-5810.0	1265.5
665	S98	-5845.0	1148.5
666	S97	-5880.0	1265.5
667	S96	-5915.0	1148.5
668	S95	-5950.0	1265.5
669	S94	-5985.0	1148.5
670	S93	-6020.0	1265.5
671	S92	-6055.0	1148.5
672	S91	-6090.0	1265.5
673	S90	-6125.0	1148.5
674	S89	-6160.0	1265.5
675	S88	-6195.0	1148.5
676	S87	-6230.0	1265.5
677	S86	-6265.0	1148.5
678	S85	-6300.0	1265.5
679	S84	-6335.0	1148.5
680	S83	-6370.0	1265.5
681	S82	-6405.0	1148.5
682	S81	-6440.0	1265.5
683	S80	-6475.0	1148.5
684	S79	-6510.0	1265.5
685	S78	-6545.0	1148.5
686	S77	-6580.0	1265.5
687	S76	-6615.0	1148.5
688	S75	-6650.0	1265.5
689	S74	-6685.0	1148.5
690	S73	-6720.0	1265.5
691	S72	-6755.0	1148.5
692	S71	-6790.0	1265.5
693	S70	-6825.0	1148.5
694	S69	-6860.0	1265.5
695	S68	-6895.0	1148.5
696	S67	-6930.0	1265.5
697	S66	-6965.0	1148.5
698	S65	-7000.0	1265.5
699	S64	-7035.0	1148.5
700	S63	-7070.0	1265.5

pad No	pad name	X	Y
701	S62	-7105.0	1148.5
702	S61	-7140.0	1265.5
703	S60	-7175.0	1148.5
704	S59	-7210.0	1265.5
705	S58	-7245.0	1148.5
706	S57	-7280.0	1265.5
707	S56	-7315.0	1148.5
708	S55	-7350.0	1265.5
709	S54	-7385.0	1148.5
710	S53	-7420.0	1265.5
711	S52	-7455.0	1148.5
712	S51	-7490.0	1265.5
713	S50	-7525.0	1148.5
714	S49	-7560.0	1265.5
715	S48	-7595.0	1148.5
716	S47	-7630.0	1265.5
717	S46	-7665.0	1148.5
718	S45	-7700.0	1265.5
719	S44	-7735.0	1148.5
720	S43	-7770.0	1265.5
721	S42	-7805.0	1148.5
722	S41	-7840.0	1265.5
723	S40	-7875.0	1148.5
724	S39	-7910.0	1265.5
725	S38	-7945.0	1148.5
726	S37	-7980.0	1265.5
727	S36	-8015.0	1148.5
728	S35	-8050.0	1265.5
729	S34	-8085.0	1148.5
730	S33	-8120.0	1265.5
731	S32	-8155.0	1148.5
732	S31	-8190.0	1265.5
733	S30	-8225.0	1148.5
734	S29	-8260.0	1265.5
735	S28	-8295.0	1148.5
736	S27	-8330.0	1265.5
737	S26	-8365.0	1148.5
738	S25	-8400.0	1265.5
739	S24	-8435.0	1148.5
740	S23	-8470.0	1265.5
741	S22	-8505.0	1148.5
742	S21	-8540.0	1265.5
743	S20	-8575.0	1148.5
744	S19	-8610.0	1265.5
745	S18	-8645.0	1148.5
746	S17	-8680.0	1265.5
747	S16	-8715.0	1148.5
748	S15	-8750.0	1265.5
749	S14	-8785.0	1148.5
750	S13	-8820.0	1265.5
751	S12	-8855.0	1148.5
752	S11	-8890.0	1265.5
753	S10	-8925.0	1148.5
754	S9	-8960.0	1265.5
755	S8	-8995.0	1148.5
756	S7	-9030.0	1265.5
757	S6	-9065.0	1148.5
758	S5	-9100.0	1265.5
759	S4	-9135.0	1148.5
760	S3	-9170.0	1265.5
761	S2	-9205.0	1148.5
762	S1	-9240.0	1265.5
763	Vcom1	-9571.5	1254.0
764	Vcom1	-9651.6	1254.0
765	Vcom1	-9731.8	1254.0
766	Vcom1	-9811.9	1254.0
767	Vcom1	-9892.1	1254.0
768	TESTO2	-10114.0	1264.0
769	SOUT14	-10104.0	1028.7
770	SOUT13	-10104.0	948.6
771	SOUT12	-10104.0	868.4
772	SOUT11	-10104.0	788.3
773	DUMMY41	-10104.0	655.3
774	VGH	-10104.0	512.8
775	VGH	-10104.0	432.6
776	VGH	-10104.0	352.5
777	VGH	-10104.0	272.3
778	VGH	-10104.0	192.2
779	VGH	-10104.0	112.0
780	VGH	-10104.0	31.9
781	VGH	-10104.0	-48.3
782	VLOUT2	-10104.0	-181.3
783	VGL	-10104.0	-341.4
784	VGL	-10104.0	-421.6
785	VGL	-10104.0	-501.7
786	VGL	-10104.0	-581.9
787	VGL	-10104.0	-662.0
788	VGL	-10104.0	-742.2
789	VGL	-10104.0	-822.3
790	VGL	-10104.0	-902.5
791	VLOUT3	-10104.0	-1035.5

Alignment Mark	X	Y
L-type (Positive)	-10114.6	1160.7
L-type (Negative)	10114.6	1160.7
Circle (Positive)	-10024.0	1264.6
Circle (Negative)	10024.0	1264.6
Cross	-9394.4	1214.7
	9394.4	1214.7

BUMP Arrangements (T.B.D.)



Block Function

1. System Interface

The HD66787 has five high-speed system interfaces: 80-system 18-/16-/9-/8-bit bus and Serial Peripheral Interface (SPI) port. The interface mode is selected with IM3-0 pins.

The HD66787 has three registers: 16-bit index register (IR), 18-bit write-data register (WDR), and 18-bit read-data register (RDR). The IR stores index information from control registers and GRAM. The WDR temporarily stores data to write into the control registers and GRAM, and the RDR temporarily stores data read from GRAM. Data written into GRAM from the MPU is first written into the WDR and then automatically written into GRAM by internal operation. Since data are read through the RDR from GRAM, the data read out first are invalid data and the ensuing data are read out normally.

The execution time for instructions other than oscillation start is 0-clock cycle, which enables writing instructions consecutively.

Register Selection (8/9/16/18 Parallel Interfaces)

80-system Bus

WR*	RD*	RS	Operation
0	1	0	Write index to IR
1	0	0	Read internal status
0	1	1	Write to the control registers or GRAM through WDR
1	0	1	Read from GRAM through RDR

Values of CS and VLD during RAM Write

CS*	VLD	Operations
0	0	Write data to GRAM. RAM address is updated.
1	0	Not write data to GRAM. RAM address is not updated.
0	1	Not write data to GRAM. RAM address is updated.
1	1	Not write data to GRAM. RAM address is not updated.

Note 1) The VLD setting is only effective with RAM write instructions.

Register Selection (Serial Peripheral Interface)

Start bytes

R/W	RS	Operations
0	0	Write index to IR
1	0	Read internal status
0	1	Write into the control register and GRAM through WDR
1	1	Read from GRAM through RDR

2. External Display Interface

The HD66787 incorporates RGB and VSYNC interfaces as an external interface for displaying moving pictures. When RGB-I/F is selected, the display operation is executed in synchronization with the externally supplied signals, VSYNC, HSYNC, and DOTCLK. The display data (PD17-0) are written according to the values of data enable signal (ENABLE) and data valid signal (VLD) in synchronization with VSYNC, HSYNC, and DOTCLK signals. This data write method allows flicker-free screen update. When VSYNC-I/F is selected, operations other than the frame synchronization by VSYNC signal are synchronized with internal clocks. The display data are written to GRAM through a system interface. In this case, there are constraints on the timing and methods of RAM update. See the "External Display Interface" section for more details.

Switching between conventional system interfaces and external display interfaces is made through instructions. An optimum interface is selected whether the screen is displaying moving or still pictures. All data written through RGB-I/F are written to GRAM. Therefore, data is transmitted only when the screen is being updated, which reduces the amount of data transmission, thereby saving power when moving pictures are being displayed.

3. Bit Operations

The HD66787 supports a write data mask function that selects and writes data into GRAM by bit, and performs logical operation or conditional rewrite on the contents of compare registers and the data to write to GRAM. For details, see the "Graphics Operation Functions" section.

4. Address Counter (AC)

Address counter (AC) assigns address to GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing data to GRAM, the AC is automatically updated plus or minus 1. The AC is not updated when the data are read from GRAM. Window address function enables data write only in the rectangular area of GRAM specified by the window address.

5. Graphics RAM (GRAM)

GRAM is a graphics RAM that stores bit-pattern data of 176 x 240 bytes with 18 bits per pixel.

6. Grayscale Power Supply Voltage Generating Circuit

Grayscale voltage generation circuit generates liquid crystal drive voltage according to the grayscale data set in the γ-correction register, enabling 262,144-color display. For details, see the "γ-Correction Register" section.

7. Timing Generator

Timing generator generates timing signals for the operation of internal circuits such as GRAM. The timing for display operation such as RAM read and the internal operation timing such as access from MPU are generated in a way to avoid mutual interfere. The interface signals (M, FLM, CL1, EQ, DCCLK,

DISPTMG, and SFTCLK) are generated internally, and a part of the signals is output through a level transforming circuit.

8. Oscillation Circuit (OSC)

The HD66787 can provide R-C oscillation simply by placing an external oscillation-resistor between OSC1 and OSC2 pins. An appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can be supplied externally. Since R-C oscillation is halted during the standby mode, current consumption will be reduced. For details, see the "Oscillation Circuit" section.

9. LCD Driver Circuit

The LCD driver circuit of HD66787 consists of a 528-output source driver (S1 ~ S528). Display pattern data are latched when 528-bit data arrive. The latched data controls the source driver and generates drive waveforms. The shift direction of outputting 528 bits from source driver is changeable with the SS bit. Select an appropriate shift direction for an assembly.

10. LCD Drive Power Supply Circuit

The LCD drive power supply circuit of HD66787 generates voltages V0, V31P, V31N, VGH, and Vcom required for driving LCD.

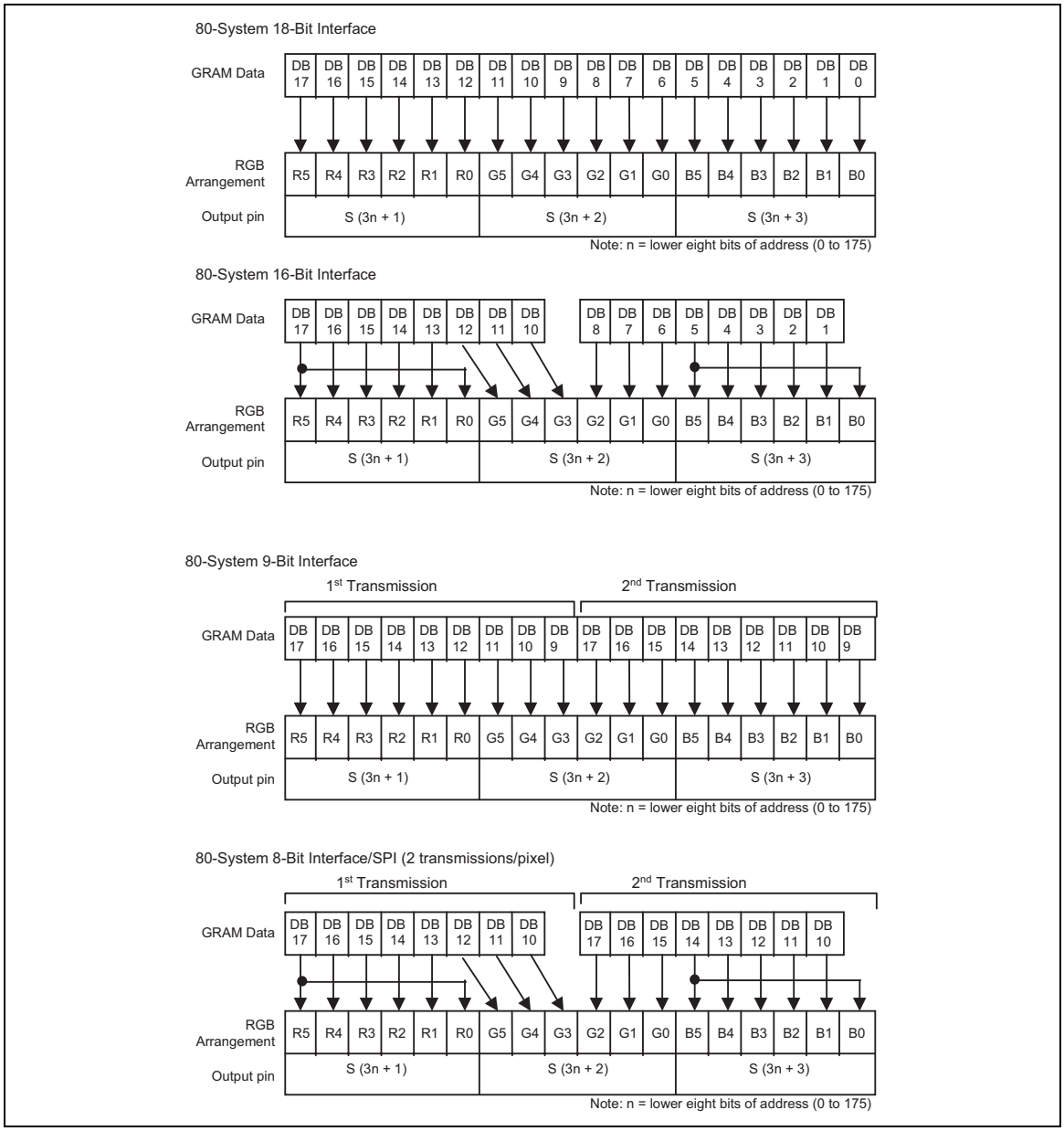
11. LTPS Panel Interface Circuit

LTPS Panel Interface Circuit level-shifts and outputs display clock signal to control LTPS (gate-less) panel. Output pins arranged on both sides of the LSI allow flexible panel design. The LSEL22-20 pins allows a combination of display clocks from SOUT24-21 and the LSEL12-10 pins allows a combination of display clocks from SOUT14-11.

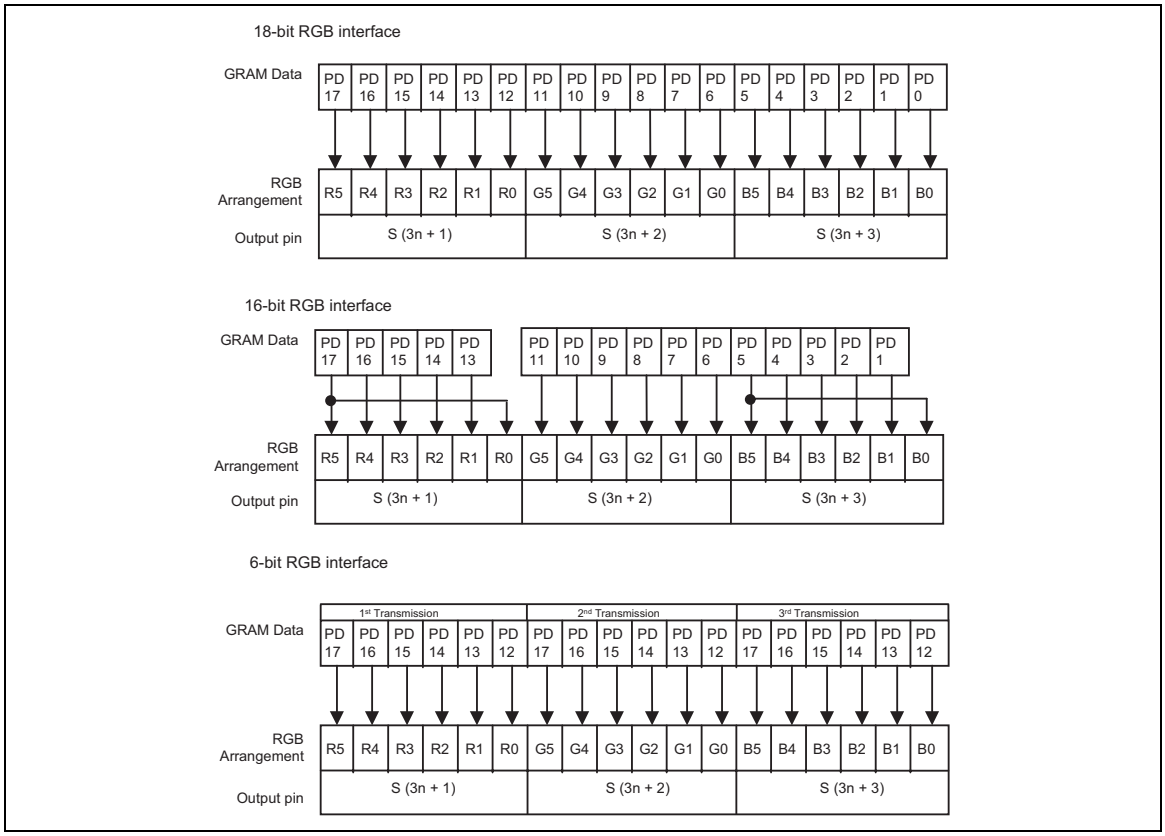
GRAM Address MAP

SG pin	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
	PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0			PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0		PD 17 ... 0	
G1	"0000"H		"0001"H		"0002"H		"0003"H		.....	"00AC"H		"00AD"H		"00AE"H		"00AF"H									
G2	"0100"H		"0101"H		"0102"H		"0103"H		.....	"01AC"H		"01AD"H		"01AE"H		"01AF"H									
G3	"0200"H		"0201"H		"0202"H		"0203"H		.....	"02AC"H		"02AD"H		"02AE"H		"02AF"H									
G4	"0300"H		"0301"H		"0302"H		"0303"H		.....	"03AC"H		"03AD"H		"03AE"H		"03AF"H									
G5	"0400"H		"0401"H		"0402"H		"0403"H		.....	"04AC"H		"04AD"H		"04AE"H		"04AF"H									
G6	"0500"H		"0501"H		"0502"H		"0503"H		.....	"05AC"H		"05AD"H		"05AE"H		"05AF"H									
G7	"0600"H		"0601"H		"0602"H		"0603"H		.....	"06AC"H		"06AD"H		"06AE"H		"06AF"H									
G8	"0700"H		"0701"H		"0702"H		"0703"H		.....	"07AC"H		"07AD"H		"07AE"H		"07AF"H									
G9	"0800"H		"0801"H		"0802"H		"0803"H		.....	"08AC"H		"08AD"H		"08AE"H		"08AF"H									
G10	"0900"H		"0901"H		"0902"H		"0903"H		.....	"09AC"H		"09AD"H		"09AE"H		"09AF"H									
G11	"0A00"H		"0A01"H		"0A02"H		"0A03"H		.....	"0AAC"H		"0AAD"H		"0AAE"H		"0AAF"H									
G12	"0B00"H		"0B01"H		"0B02"H		"0B03"H		.....	"0BAC"H		"0BAD"H		"0BAE"H		"0BAF"H									
G13	"0C00"H		"0C01"H		"0C02"H		"0C03"H		.....	"0CAC"H		"0CAD"H		"0CAE"H		"0CAF"H									
G14	"0D00"H		"0D01"H		"0D02"H		"0D03"H		.....	"0DAC"H		"0DAD"H		"0DAE"H		"0DAF"H									
G15	"0E00"H		"0E01"H		"0E02"H		"0E03"H		.....	"0EAC"H		"0EAD"H		"0EAE"H		"0EAF"H									
G16	"0F00"H		"0F01"H		"0F02"H		"0F03"H		.....	"0FAC"H		"0FAD"H		"0FAE"H		"0FAF"H									
G17	"1000"H		"1001"H		"1002"H		"1003"H		.....	"10AC"H		"10AD"H		"10AE"H		"10AF"H									
G18	"1100"H		"1101"H		"1102"H		"1103"H		.....	"11AC"H		"11AD"H		"11AE"H		"11AF"H									
G19	"1200"H		"1201"H		"1202"H		"1203"H		.....	"12AC"H		"12AD"H		"12AE"H		"12AF"H									
G20	"1300"H		"1301"H		"1302"H		"1303"H		.....	"13AC"H		"13AD"H		"13AE"H		"13AF"H									
⋮	⋮		⋮		⋮		⋮			⋮		⋮		⋮		⋮									
G233	"0800"H		"0801"H		"0802"H		"0803"H		.....	"E8AC"H		"E8AD"H		"E8AE"H		"E8AF"H									
G234	"0900"H		"0901"H		"0902"H		"0903"H		.....	"E9AC"H		"E9AD"H		"E9AE"H		"E9AF"H									
G235	"EA00"H		"EA01"H		"EA02"H		"EA03"H		.....	"EAAC"H		"EAAD"H		"EAAE"H		"EAAF"H									
G236	"EB00"H		"EB01"H		"EB02"H		"EB03"H		.....	"EBAC"H		"EBAD"H		"EBAE"H		"EBAF"H									
G237	"EC00"H		"EC01"H		"EC02"H		"EC03"H		.....	"ECAC"H		"ECAD"H		"ECAE"H		"ECAF"H									
G238	"ED00"H		"ED01"H		"ED02"H		"ED03"H		.....	"EDAC"H		"EDAD"H		"EDAE"H		"EDAF"H									
G239	"EE00"H		"EE01"H		"EE02"H		"EE03"H		.....	"EEAC"H		"EEAD"H		"EEAE"H		"EEAF"H									
G240	"EF00"H		"EF01"H		"EF02"H		"EF03"H		.....	"EFAC"H		"EFAD"H		"EFAE"H		"EFAF"H									

GRAM address and display panel position (SS =”0”)



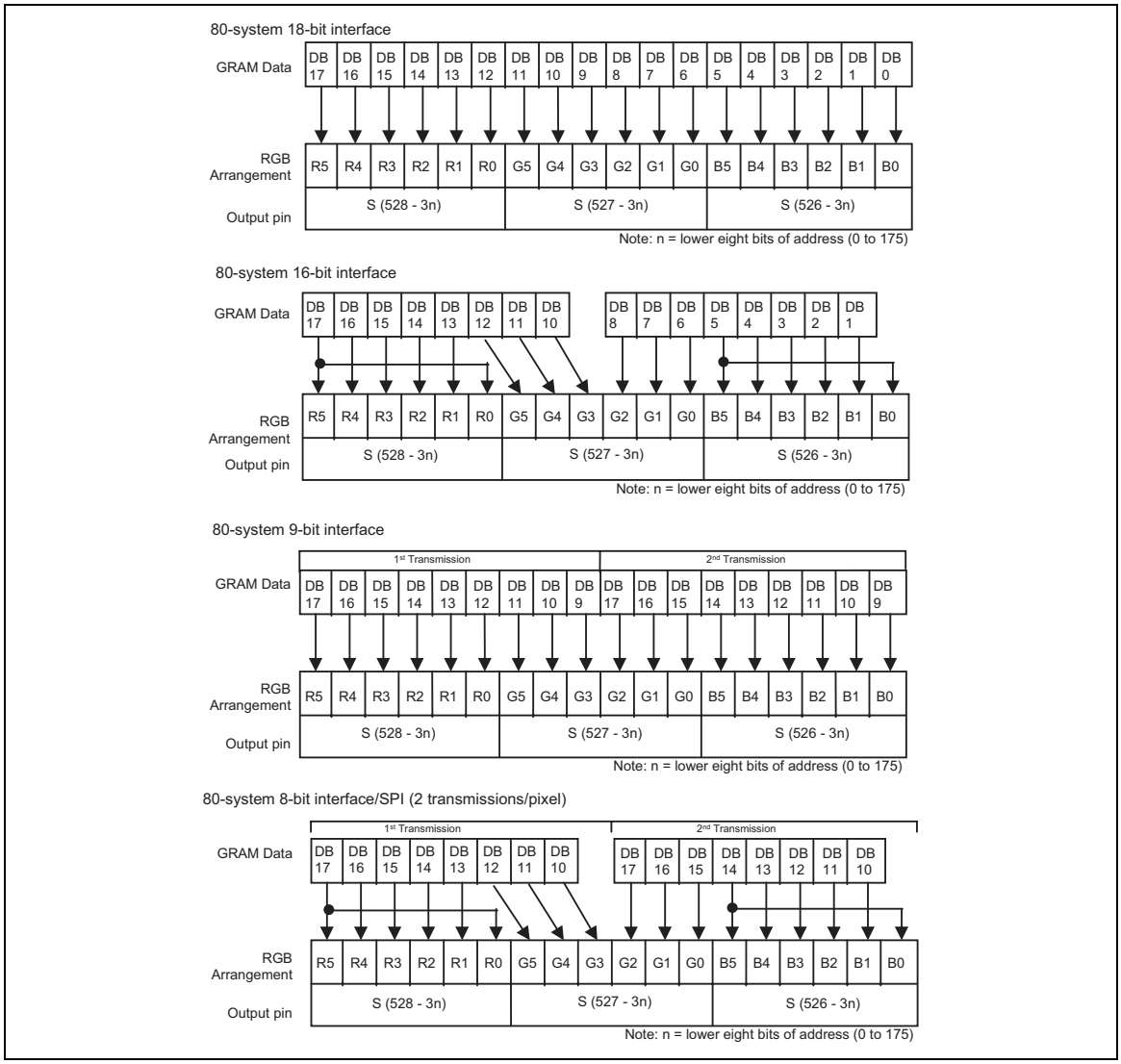
GRAM data and RGB assignment (SS = “0”, BGR = “0”)



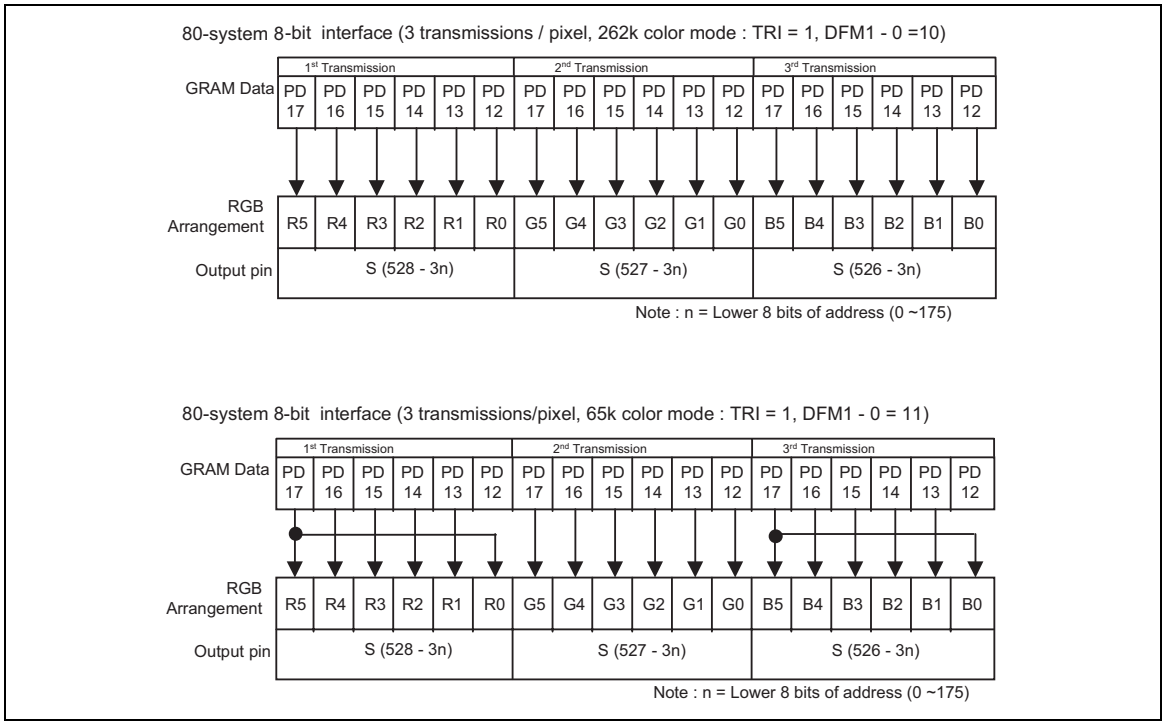
GRAM data and RGB assignment (SS = "0", BGR = "0")

SG pin	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
	PD 17 ... 0			PD 17 ... 0			PD 17 ... 0			PD 17 ... 0				PD 17 ... 0			PD 17 ... 0			PD 17 ... 0			PD 17 ... 0		
G1	"00AF"H			"00AE"H			"00AD"H			"00AC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	"01AF"H			"01AE"H			"01AD"H			"01AC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	"02AF"H			"02AE"H			"02AD"H			"02AC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	"03AF"H			"03AE"H			"03AD"H			"03AC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	"04AF"H			"04AE"H			"04AD"H			"04AC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	"05AF"H			"05AE"H			"05AD"H			"05AC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	"06AF"H			"06AE"H			"06AD"H			"06AC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	"07AF"H			"07AE"H			"07AD"H			"07AC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	"08AF"H			"08AE"H			"08AD"H			"08AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	"09AF"H			"09AE"H			"09AD"H			"09AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	"0AAF"H			"0AAE"H			"0AAD"H			"0AAC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	"0BAF"H			"0BAE"H			"0BAD"H			"0BAC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	"0CAF"H			"0CAE"H			"0CAD"H			"0CAC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	"0DAF"H			"0DAE"H			"0DAD"H			"0DAC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	"0EAF"H			"0EAE"H			"0EAD"H			"0EAC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	"0FAF"H			"0FAE"H			"0FAD"H			"0FAC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	"10AF"H			"10AE"H			"10AD"H			"10AC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	"11AF"H			"11AE"H			"11AD"H			"11AC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	"12AF"H			"12AE"H			"12AD"H			"12AC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	"13AF"H			"13AE"H			"13AD"H			"13AC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G233	"E8AF"H			"E8AE"H			"E8AD"H			"E8AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G234	"E9AF"H			"E9AE"H			"E9AD"H			"E9AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G235	"EAAF"H			"EAAE"H			"EAAD"H			"EAAC"H			.....	"EA03"H			"EA02"H			"EA01"H			"EA00"H		
G236	"EBAF"H			"EBAE"H			"EBAD"H			"EBAC"H			.....	"EB03"H			"EB02"H			"EB01"H			"EB00"H		
G237	"ECAF"H			"ECAE"H			"ECAD"H			"ECAC"H			.....	"EC03"H			"EC02"H			"EC01"H			"EC00"H		
G238	"EDAF"H			"EDAE"H			"EDAD"H			"EDAC"H			.....	"ED03"H			"ED02"H			"ED01"H			"ED00"H		
G239	"EEAF"H			"EEAE"H			"EEAD"H			"EEAC"H			.....	"EE03"H			"EE02"H			"EE01"H			"EE00"H		
G240	"EFAF"H			"EFAE"H			"EFAD"H			"EFAC"H			.....	"EF03"H			"EF02"H			"EF01"H			"EF00"H		

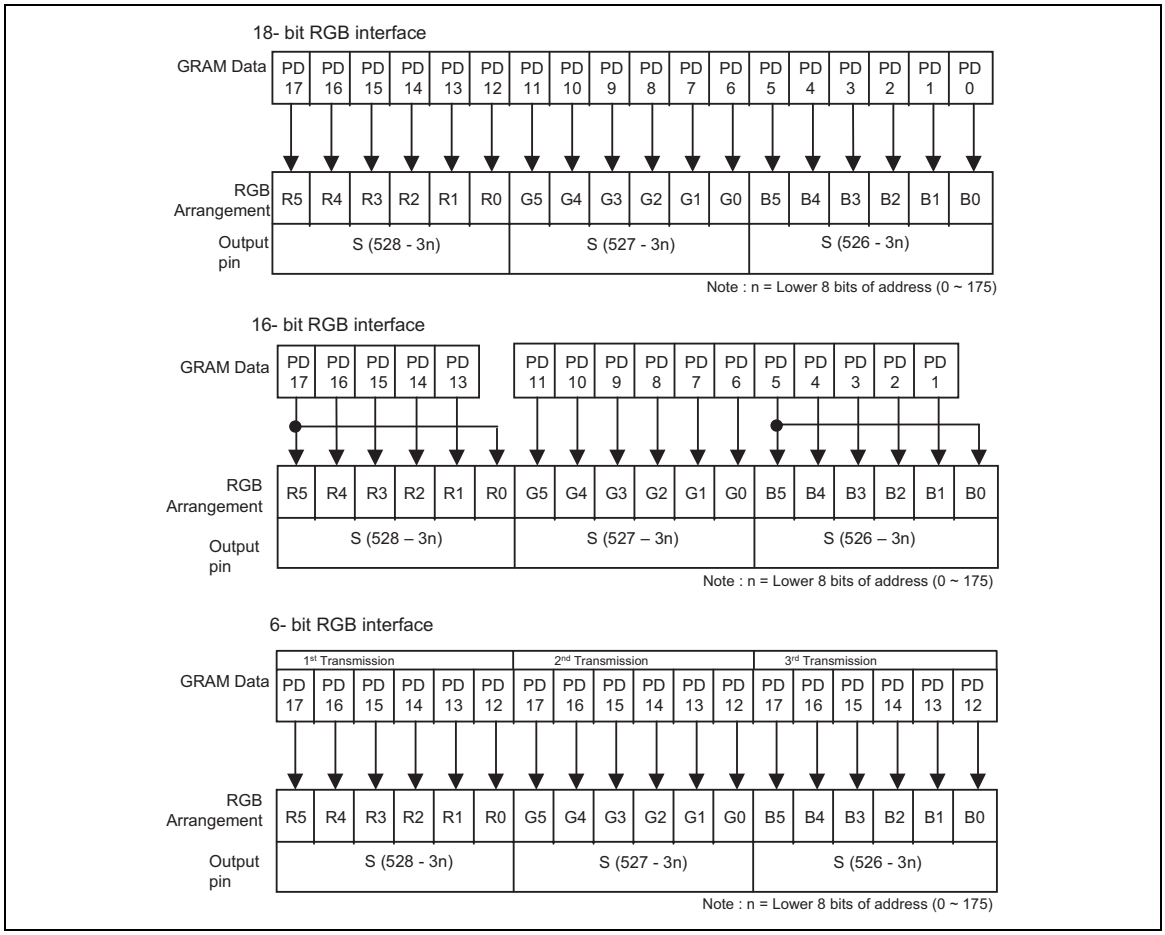
GRAM address and display panel position (SS =”1”, BGR “1”)



GRAM data and RGB assignment (SS = “1”, BGR = “1”)



GRAM data and RGB assignment (SS = “1”, BGR = “1”)



GRAM data and RGB assignment (SS = “1”, BGR = “1”)

Instructions

Outline

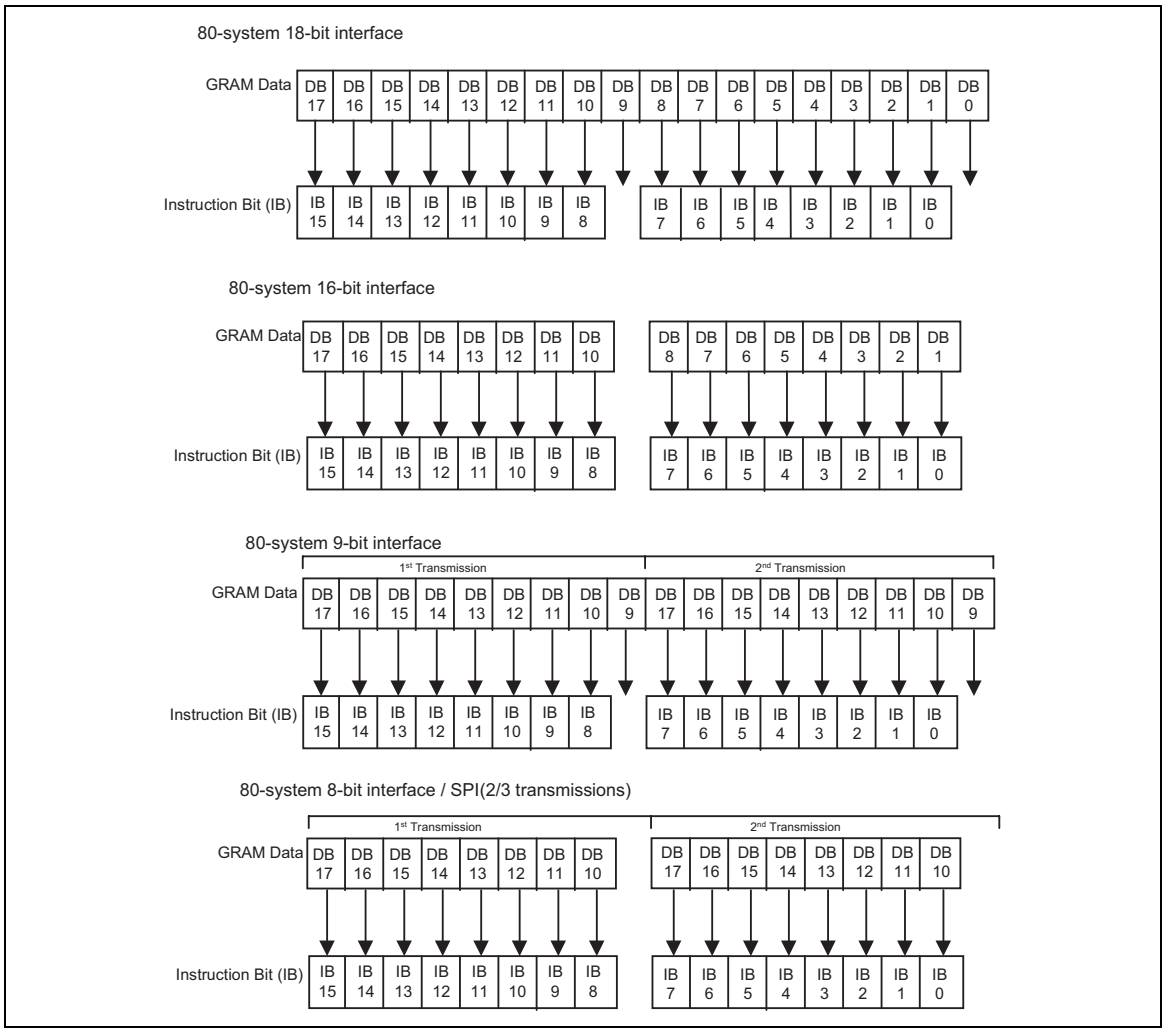
The HD66787 adapts 18-bit bus architecture that enables high-speed interfacing with a high-performance microcomputer. Data sent from external (18/16/9/8 bits) are stored temporarily in the instruction register (IR) and the data register (DR) to store control information before internal operation starts. Since internal operation is decided according to the signal sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signal (DB15 to DB0) are called instruction. GRAM is accessed through internal 18-bit data bus. There are eight categories of instructions:

1. Specify index
2. Read status
3. Control display
4. Control power management
5. Process graphics data
6. Set internal GRAM address
7. Transfer data to and from internal GRAM
8. Set grayscale level for internal grayscale γ-adjustment

Normally, the 7th instruction to write display data is executed the most frequently. The address of internal GRAM is updated automatically after data are written to the internal GRAM. With the window address function, this reduces the amount of data transmission to minimum and thereby lightens the load on the program in the microcomputer. Since instructions are executed in 0 cycle, it is possible to write instructions consecutively.

As the following figure shows, the assignment to the 16 instruction bits (IB15-0) varies according to the interface in use. An instruction must adopt the data format for each interface.

.



Instruction bits

Instruction Descriptions

The following are detail explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index

The index instruction specifies the index (R00h to R4Fh) of control register and RAM control. It sets the register number from 0000000 to 1111111 in binary form. Do not try to access to the register to which the index is not assigned.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction reads the internal status of the HD66787.

L7–0: Indicate the position of raster-row driving liquid crystal.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator in a halt state during the standby mode. After executing this instruction, wait at least 10 ms for stabilizing oscillation before issuing a next instruction. For details, see the "Standby Mode" section.

"0787"H is read out, if this register is forced to read out.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	0	0	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

SS: Select the shift direction of outputs from the source driver. When SS = 0, the shift direction of outputs is from S1 to S528. When SS = 1, the shift direction of output is from S528 to S1. In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins. To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0. To assign R, G, B dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = "0" : ENABLE = "Low" / Write data to PD17-0.
: ENABLE = "High" / Data write invalid.
EPL ="1" : ENABLE = "High" / Write data to PD17-0.
: ENABLE = "Low" / Data write invalid.

The following table shows the relationship between EPL, ENABLE, VLD and RAM access.

EPL	ENABLE	VLD	RAM write	RAM address
0	0	0	Valid	Updated
0	0	1	Invalid	Updated
0	1	*	Invalid	Hold
1	0	*	Invalid	Hold
1	1	0	Valid	Updated
1	1	1	Invalid	Updated

VSPL: Invert the polarity of signal for VSYNC pin.

VSPL = ”0” : Low active.
VSPL = ”1” : High active.

HSPL: Invert the polarity of signal for HSYNC pin.

HSPL = ”0” : Low active.
HSPL = ”1” : High active.

DPL: Invert the polarity of signal for DOTCLK pin.

DPL = ”0” : Data are read in synchronization with the rising edge of the DOTCLK.
DPL = ”1” : Data are read in synchronization with the falling edge of the DOTCLK.

NL4-0: Specify the number of LCD drive raster-rows. The number of drive raster-rows is changeable by 8 multiples. The GRAM address mapping is independent of this setting. Select a number of raster-rows that the display size covers the size of a panel.

NL bits

NL4	NL3	NL2	NL1	NL0	Display Size	Liquid crystal drive raster-rows	Gate Driver Lines Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	528 x 16 dots	16	G1–G16
0	0	0	1	0	528 x 24 dots	24	G1–G24
0	0	0	1	1	528 x 32 dots	32	G1–G32
0	0	1	0	0	528 x 40 dots	40	G1–G40
0	0	1	0	1	528 x 48 dots	48	G1–G48
0	0	1	1	0	528 x 56 dots	56	G1–G56
0	0	1	1	1	528 x 64 dots	64	G1–G64
0	1	0	0	0	528 x 72 dots	72	G1–G72
		.			.	.	.
		.			.	.	.
		.			.	.	.
		.			.	.	.
		.			.	.	.
1	1	0	0	0	528 x 200 dots	200	G1–G200
1	1	0	0	1	528 x 208 dots	208	G1–G208
1	1	0	1	0	528 x 216 dots	216	G1–G216
1	1	0	1	1	528 x 224 dots	224	G1–G224
1	1	1	0	0	528 x 232 dots	232	G1–G232
1	1	1	0	1	528 x 240 dots	240	G1–G240

Note 1) A front porch period (set in the FP register) and a back porch period (set in the BP register) will be inserted as a blank period before and after driving all gate lines.

LCD Driving Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

NW5-0: Specify n, the number of raster-rows from 1 to 64 to alternate every n+1 raster-rows when C-pattern waveform is generated (B/C = 1).

EOR: When EOR = 1 and a C-pattern waveform is generated (B/C =1), an odd/even frame select signal and an n-raster-row inversion signal are AC-driven. This instruction is available when liquid crystal AC drive is not made depending on the combination of numbers of LCD drive raster-rows and the value of "n" of n-raster-row inversion AC drive. For details, see "n-raster-row inversion AC drive".

B/C: When B/C =0, a field AC waveform is generated. Alternation occurs every frame when driving liquid crystal. When B/C=1, alternation occurs every n raster-row. For details, see the "n-raster-row Inversion AC Drive" section.

Entry Mode (R03h)

Compare Register 1 (R04h)

Compare Register 2 (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM1	DFM0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

The HD66787 modifies write data sent from the microcomputer before writing to GRAM. This enables high-speed GRAM data update, and reduces the load on the microcomputer software. For details, see the "Graphics Operation Function" section.

TRI: RAM write data are transmitted in 3 times through 8-bit interface when TRI = 1. When 8-bit interface mode is not selected, set TRI to 0.

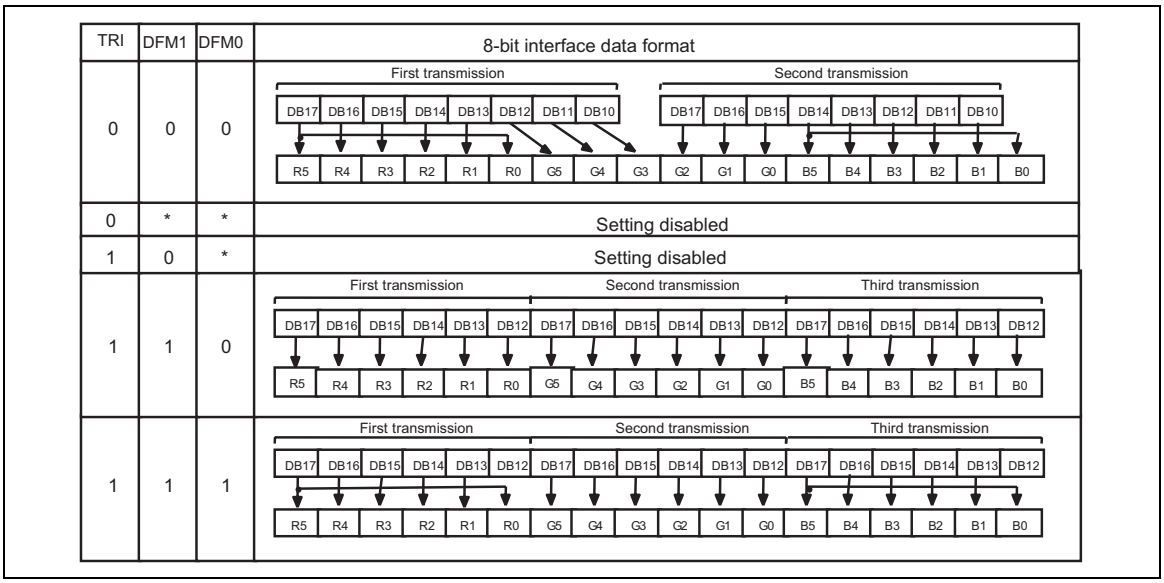
DFM1-0: Specify the data format for RAM write data transmission when TRI = 1 (8-bit interface mode only).

DFM1-0 = "10": 262k mode (6bit x 3 transmissions)
DFM1-0 = "11": 65k mode (5,6,5 bits transmissions)

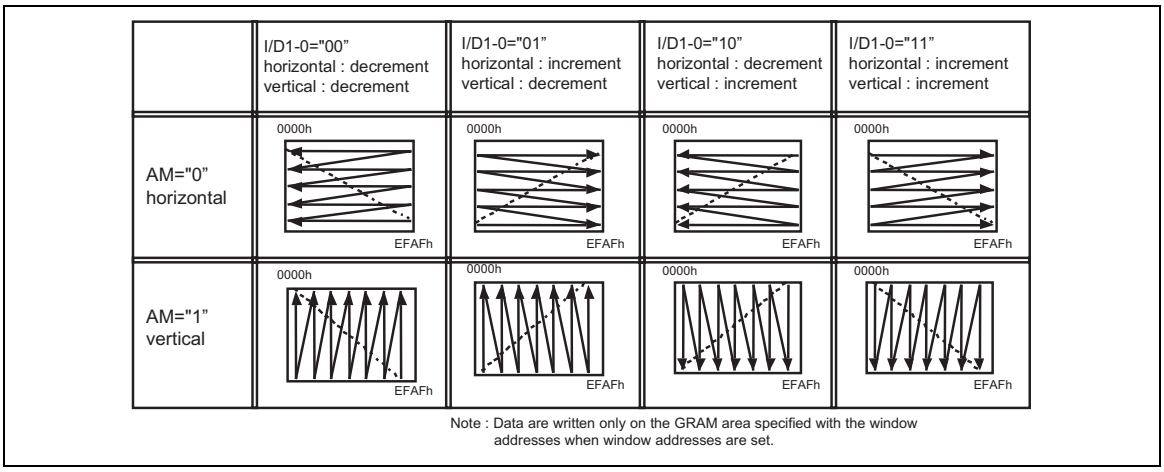
HWM: When HWM=1, data are written to GRAM in high speed. In high-speed write mode, 4 words are written to GRAM in a single operation after executing 4 RAM write operations. If RAM write is terminated before it is executed 4 times, the last data will not be written. Make sure that RAM write is executed 4 times. For this reason, the lower 2 bits must be set to "0" when setting the RAM address. For details, see "High-Speed RAM Write Mode" section.

I/D1-0: The address counter is automatically incremented by 1, after data are written to GRAM when I/D1-0 = "1". The address counter is automatically decremented by 1, after data are written to GRAM when I/D1-0 = "0". An independent setting for the increment or decrement of the address counter can be made to the upper (AD15-8) and the lower (AD7-0) bits of the address. The address transition direction when data are written to GRAM is set with AM bits.

AM: Set the direction of updating address counter automatically after data are written to GRAM. When AM = "0", the address counter is updated in the horizontal direction. When AM = "1", the address counter is updated in the vertical direction. When the window address is specified, data are written to the GRAM area specified by the window address in the manner specified with I/D1-0, AM bits.



8-bit interface data format

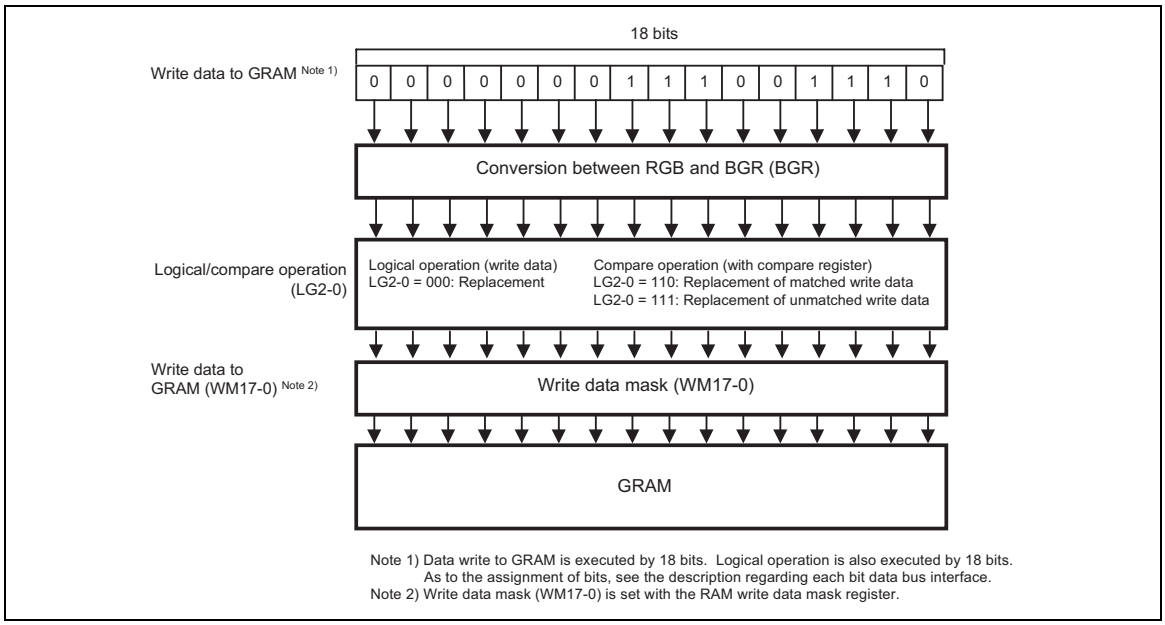


Address transition direction

LG2–0: Rewrite data to GRAM after comparing the data that are written by the microcomputer to GRAM with the values in the compare registers (CP17–0) and performing logical operation. For details, see the "Graphics Operation Function"

CP17–0: Set the value for the compare register, with which the data read out from GRAM or data written to GRAM by the microcomputer are compared. This function is not available with the external display interface mode. In the external display interface mode, make sure LG2-0 = "000".

BGR: Reverse the order from R, G, B to B, G, R to the 18-bit data to write to GRAM. When setting BGR = 1, CP17-0 and WM17-0 bits will be automatically changed to the same effect.



Logic/Compare Operation

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	DTE	CL	REV	D1	D0

PT1-0: Determine the kind of source output in a non-display area in the partial display mode. For details, see the "Screen-split Drive function" section.

PT1-0 bits

		Source Output for Non-display Area	
PT1	**PT0**	**Positive Polarity**	**Negative Polarity**
0	0	V31	V0
0	1	V31	V0
1	0	GND	GND
1	1	High impedance	High impedance

VLE2–1: When VLE1 = 1, the first screen is scrolled in the vertical direction. When VLE2 = 1, the second screen is scrolled in the vertical direction. The first and second screens cannot be scrolled simultaneously. This function is not available with the external display interface mode. In this case, make sure VLE2-1 = 0.

VLE Bits

VLE2	VLE1	Image on 2nd Screen	Image on 1st Screen
0	0	Stationary	Stationary
0	1	Stationary	Scrolled
1	0	Scrolled	Stationary
1	1	Setting disabled	Setting disabled

CL: When CL = 1, 8-color display mode is selected. For details, see the "8-Color Display Mode" section.

CL Bit

CL	Colors
0	262,144
1	8

SPT: When SPT = 1, liquid crystal is driven with 2 split screens. For details, see the "Screen Split Drive Function" section. This function is not available in the external display interface mode. In this case, make sure SPT = 0.

REV: When REV = 1, a reverse display is shown. Inverting the grayscale levels allows the display of same data on both normally white and normally black panels. The source output during front, back porch periods and blank periods during the 2-split-screen display is made in accordance with settings with PT1-0 bits.

Source Output in the Display Area

		Source Output in the Display Area*	
REV	GRAM Data	Positive Polarity	Negative Polarity
0	18'h00000	V31	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V31
1	18'h00000	V0	V31
	⋮	⋮	⋮
	18'h3FFFF	V31	V0

Note: The output on the source lines during the front and back porch periods and blanking of the partial display is determined with PT1-0 bits.

DTE: When DTE = 0, the DISPTMG output is fixed to GND.

DTE Bit

DTE	DISPTMG Output
0	Halt (GND)
1	Operation (Vcc/GND)

D1–0: The graphics display is on when D1 = 1, and off when D1 = 0. When setting D1 = 0, the data are retained in GRAM. This means the graphics is instantly redisplayed when setting D1 to 1. When D1 is 0 (i.e., the display is off) all the source outputs are set to the GND level. This reduces the charged/discharged current on LCD, accompanied by the liquid crystal AC drive.

When D1-0 = 01, the HD66787 continues the internal display operation, even while the external display is off. When D1-0 = 00, both the internal display operations and the external display operation are halted.

In combination with GON and DTE bits, D1-0 bits control ON/OFF of display. For details, see the "Instruction Setting Flow" section.

D1-0

D1	D0	Source Output	HD67789 Internal Operations	Gate-Driver Control Signals (CL1, FLM, and M)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Note 1) Data are written to GRAM from the microcomputer irrespective of the setting of D1-0 bits.

Note 2) In the standby mode, D1-0 = "00". However, the D1-0 register setting before entering standby modes is retained.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0/BP3-0: Make settings for blank periods (the front and back porches), which are placed at the beginning and end of the display. FP3-0 and BP3-0 bits specify the number of raster-rows for the front and back porch respectively. When making this setting, make sure:

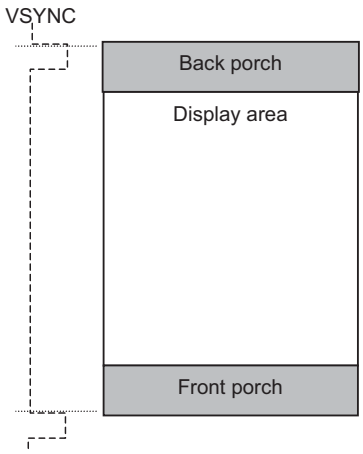
BP + FP = <16 raster-rows
FP >= 2 raster-rows
BP >= 2 raster-rows

In the external display interface mode, the back porch (BP) starts on the falling edge of VSYNC signal,

followed by display operation. After displaying the number of raster-rows set with NL bits, the front porch starts. After the front porch, a blank period ensues until an input of next VSYNC signal.

FP and BP

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
	. .			. .
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting disabled



Note: The output timing to the LCD panels is delayed two raster-rows from the input of synchronization signal.

External display interface

BP3-0, FP3-0 Setting

Set BP3-0, FP3-0 bits as follows each in the following operation modes.

Operation of internal clock	**FLD1-0 = 01**	BP>= 2 lines	FP >= 2 lines	FP +BP <= 16 lines
	FLD1-0 = 11	BP= 3 lines	FP = 5 lines	
RGB interface		BP >= 2 lines	FP >= 2 lines	FP +BP <= 16 lines
VSYNC interface		BP >= 2 lines	FP >= 2 lines	FP +BP = 16 lines

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the 1H (1 raster-row) period.

RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Raster-row
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
		:		:
1	1	1	0	30
1	1	1	1	31

DIV1-0: Set the division ratio of clocks for internal operations (DIV1-0). Internal operations are in synchronization with the clock, the frequency of which is divided according to the DIV1-0 setting. When changing the number of drive raster-rows, adjust the frame frequency too. For details, see "Frame Frequency Adjustment Function".

DIV Bits and Division Ratio

DIV1	DIV0	Division Ratio	Internal Operating Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency
Line: number of drive raster-rows (NL bit)
Division ratio: DIV bit
Clock cycles per raster-row: RTN bit
FP : the number of raster-rows in the front porch
BP : the number of raster-rows in the back porch

EQ1-0: Equalizing period is prolonged as the number of clocks specified with EQ1-0 bits. The equalization signal is output only with the alternating current.

EQ Bits

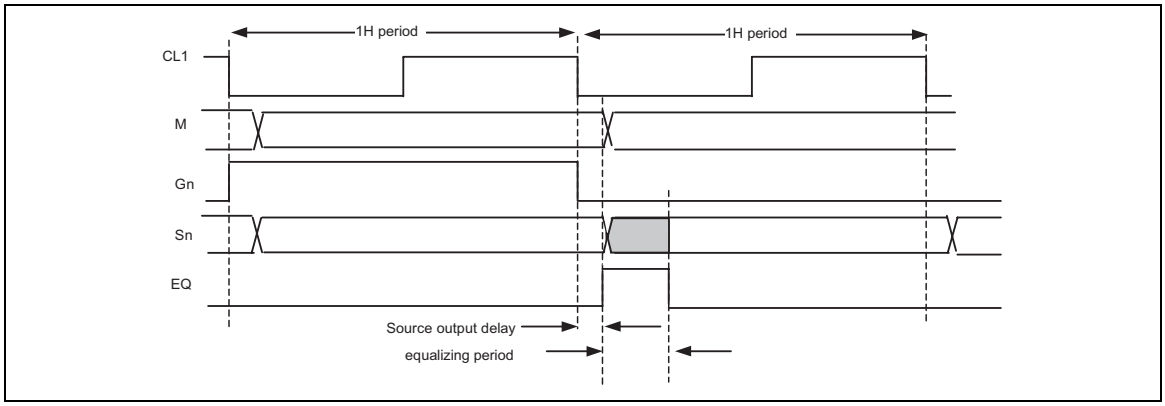
		Equalizing period	
EQ1	EQ0	Internal Operation (synchronized with the internal operating clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	Not equalized	Not equalized
0	1	1 clock	8 clocks
1	0	2 clocks	16 clocks
1	1	3 clocks	24 clocks

SDT1-0: Determine the amount of delay for the source output from the falling edge of the gate output.

SDT Bits

		Delay Time for Source Signal	
SDT1	**SDT0**	**Internal Operation (synchronized with the internal operating clock)**	**RGB I/F Operation (synchronized with DOTCLK)**
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Note 1) The amount of delay for the source output is measured from the falling edge of the CL1.



Source output delay and equalize period

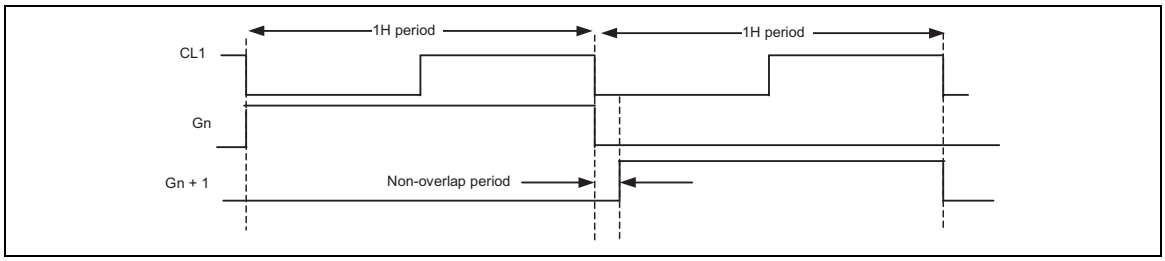
Note 1) In internal operation and VSYNC interface modes, the reference clock is the internal operating clock. In RGB interface modes, the reference clock is DOTCLK.

NO1-0: Specify the amount of non-overlap time for the gate output.

NO Bits

		Non-overlap time	
NO1	**NO0**	**Internal Operation (synchronized with the internal operating clock)**	**RGB I/F Operation (synchronized with DOTCLK)**
0	0	0 clock	0 clock
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks

Note 1) The amount of non-overlap time is defined from the falling edge of the CL1.



Non-overlap period

External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1–0: Specify the RGB I/F mode when RGB interface is selected. Specifically, this setting specifies the RGB interface mode when it is selected by the setting DM and RM bits. The setting must be made before the display operation through external display interface. Do not make a setting during display.

RIM Bits

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one-time transfer/pixel)
0	1	16-bit RGB interface (one-time transfer/pixel)
1	0	6-bit RGB interface (three-time transfers/pixel)
1	1	Setting disabled

Note 1) The instruction register setting is possible only through a system interface.

Note 2) Data transmission and input of DOTCLK in the 6-bit RGB interface mode should be executed by RGB.

DM1–0: Specify the display operation mode. The interface through which display operation is executed is selected with DM1-0 bits. This setting enables switching between internal clock operation and external display interface. Switching within the external display interface modes (between RGB-I/F and VSYNC-I/F) cannot be made.

DM Bits

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Specify the interface for RAM accesses. RAM is accessible only through the interface specified with RM bit. When the display data is written through RGB-I/F, set RM = 1. The RM-bit setting can be made irrespective of the display operation mode. This means the display data can be updated through a system interface even during the display period through RGB interface by setting RM = 0.

RM Bit

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Setting for external display interface control allows selecting an optimum interface for the kind of display as follows. When displaying a moving picture (RGB-I/F/VSYNC-I/F), the display data must be written in the high-speed mode (HWM = 1) which enables high-speed RAM access with low power consumption.

Display state and interfaces

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1) The instruction register setting is made only through system interface.

Note 2) Switching between RGB-I/F and VSYNC-I/F cannot be made.

Note 3) The RGB-I/F mode settings is not changeable during RGB I/F operation.

Note 4) For details on the transition flow between operation modes, see the “External Display Interface” section.

Note 5) Use the high-speed write mode (HWM = 1) during the write operation in RGB-I/F and VSYNC-I/F modes.

Internal clock operation mode

All display operations are controlled by signals generated by the internal clock in internal clock operation mode. All inputs through the external display interface are invalid. The internal RAM is accessible only through a system interface.

RGB interface mode (1)

Display operation is controlled by the frame synchronization clock (VSYNC), line synchronizing signal (VSYNC), and dot clock (DOTCLK) in the RGB interface mode. These signals must be supplied throughout the display operation in this mode.

All display data are stored in the internal RAM, transmitted with PD17-0 bits by pixel. The combination with the high-speed write mode and window address function enables simultaneous display of both moving picture areas and the internal RAM area. The data are transmitted only when the screen is being updated, thereby reducing the overall data transmission to minimum.

The periods of the front (FP) and back (BP) porches and the display period (NL) are automatically generated in the HD66782 by counting the clock of line synchronizing signal (HSYNC) in accordance to the frame synchronizing signal (VSYNC). Transmit pixel data with PD 17-0 bits in accordance with the setting specified above.

RGB interface mode (2)

When RGB-I/F is selected, RAM data are changeable through the system interface. This write operation must be performed while display data are not being transmitted through the RGB-I/F (ENABLE = High). When reverting from the system interface mode to the data transmission through the RGB interface, make a new setting for the address set and index (R22h) after changing the aforementioned settings.

VSYNC interface mode

The internal display operation is synchronized with the frame-synchronizing signal (VSYNC) in the VSYNC interface mode. By writing data to RAM at a fixed speed on the falling edge of VSYNC, it enables moving pictures display with a system interface. In this case, there are some constraints in the RAM write speed and methods. For details, see the "External Display Interface" section.

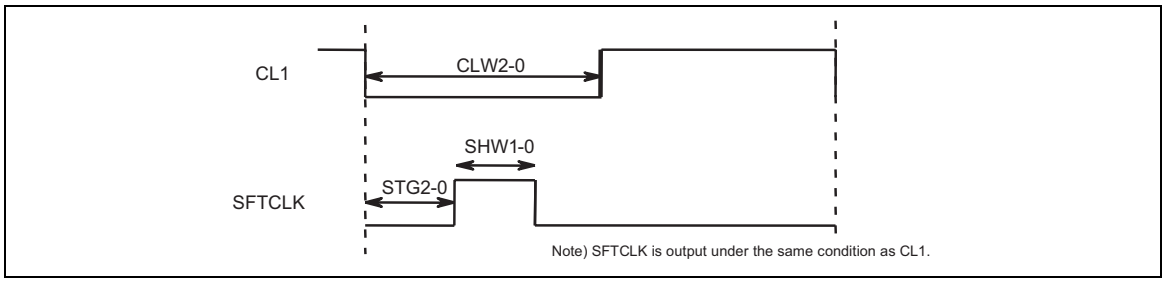
In the VSYNC-I/F mode, only VSYNC input is valid. Other input signals for the external display interface are invalid.

The front porch (FP), back porch (BP) periods and display period (NL) are automatically generated in accordance to the frame synchronizing signal (VSYNC) according to the register setting of HD66787.

LTPS Interface Control (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	TG0	0	CLW 2	CLW 1	CLW 0	0	0	SHW 1	SHW 0	0	STG 2	STG 1	STG 0

The HD66787 enables connection to LTPS-TFT panels by outputting timing signals (CL1, SFTCLK) for controlling low-temperature poli-Si TFT (LTPS-TFT) panels with incorporated gates. For details, see the "Low-temperature Poli-Si TFT Control" section.



Timing signals for LTPS-TFT panels

STG2-0: Set the output position of the pulse of SFTCLK signal.

STG2-0

STG 2	STG 1	STG 0	SFTCLK signal : pulse output position	
			internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	0	0 clock	0 clock
0	0	1	1 clock	8 clocks
0	1	0	2 clocks	16 clocks
0	1	1	3 clocks	24 clocks
1	0	0	4 clocks	32 clocks
1	0	1	5 clocks	40 clocks
1	1	0	6 clocks	48 clocks
1	1	1	7 clocks	56 clocks

Note 1) The number of clocks is counted from the falling edge of the CL1 signal.

SHW1-0: Set the width of the pulse of SFTCLK signal during "High".

SHW1-0

SHW 1	SHW 0	SFTCLK signal : purse width during "High"	
		internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

In making settings for SFTCLK signal, the following condition must be observed.

STG2-0 + SHW1-0 ≤ 8 clocks (Internal operation)

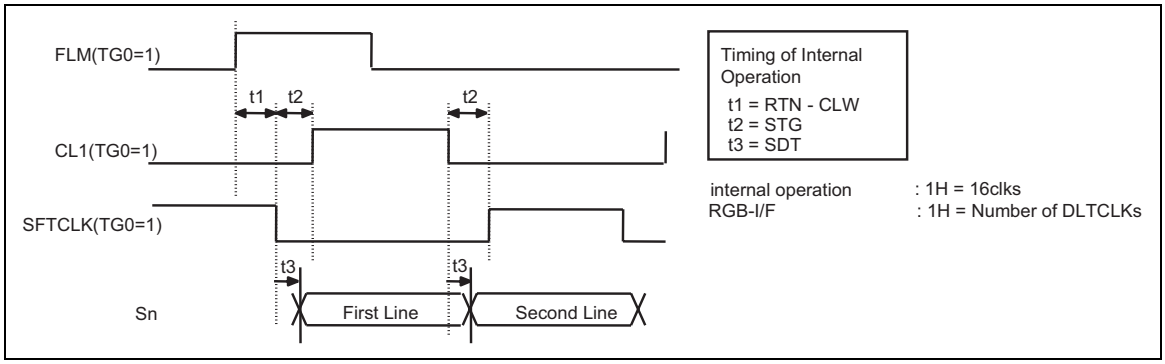
≤ 64 clocks (RGB interface operation)

CLW2-0: Set the width of the pulse of CL1 signal during "Low".

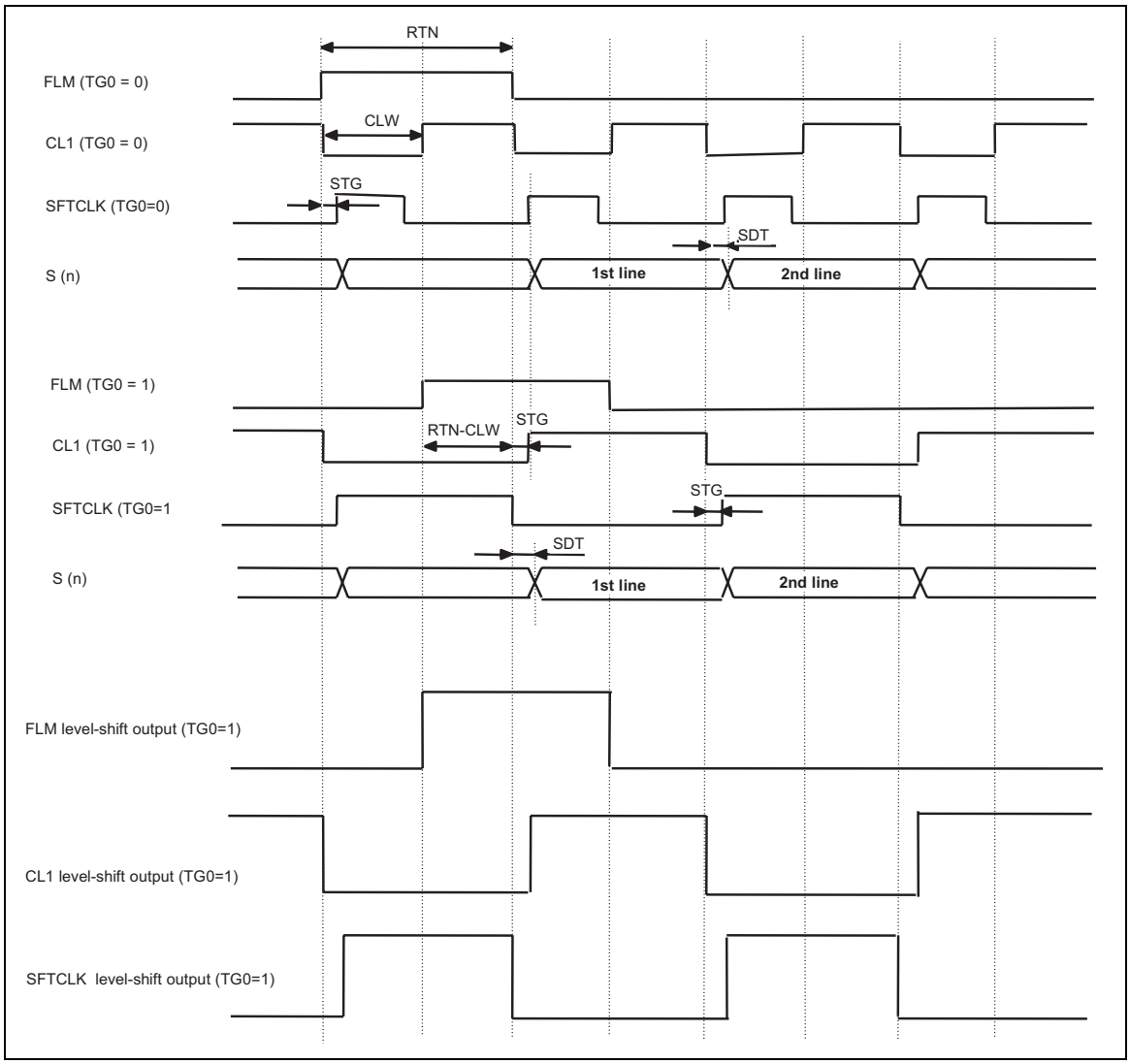
CLW 2	CLW 1	CLW 0	CL1 signal : pulse width during "Low"	
			internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	0	1 clock	8 clocks
0	0	1	2 clocks	16 clocks
0	1	0	3 clocks	24 clocks
0	1	1	4 clocks	32 clocks
1	0	0	5 clocks	40 clocks
1	0	1	6 clocks	48 clocks
1	1	0	7 clocks	56 clocks
1	1	1	8 clocks	64 clocks

Note 1) The number of clocks is counted from the falling edge of the CL1 signal.

TG0: Change the output timing of CL1 and SFTCLK signals. If TG0 =1, the setting in SHW is nullified and the frequencies of CL1 and SFTCLK become the frequency of normal mode divided by 2. The output timing of each signal is illustrated as follows.



CL1 and SFTCLK (TG0 = 1)



CL1 and SFTCLK timing chart

Power Control 1 (R10h)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP2	SAP1	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

SAP2-0: Adjust the amount of fixed current from the fixed current source of operational amplifier for the source driver. When the amount of fixed current is set large, the operational amplifier will stabilize, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. During non-display operation, set SAP2-0 = "000" to halt the operation of operational amplifier, to reduce the current consumption.

SAP Bits and the amount of current for the Op-amp

SAP2	SAP1	SAP0	Op-amp Current
0	0	0	Halt
0	0	1	Setting disabled
0	1	0	0.62 (fixed)
0	1	1	0.71 (fixed)

SAP2	SAP1	SAP0	Op-amp Current
1	0	0	1 (fixed)
1	0	1	1.25 (fixed)
1	1	0	1.43 (fixed)
1	1	1	Setting disabled

BT2–0: Change the step-up scale of the step-up circuit. Adjust the scale according to the voltage. Smaller scale consumes lesser current.

DC02–00: Select the operating frequency for the step-up circuit 1. The higher frequency enhances the drive capacity of step-up circuit as well as the display quality, while the current consumption will increase. Adjust the frequency taking both the display quality and the current consumption into consideration.

DC12–10: Select the operating frequency for the step-up circuit 2. The higher frequency enhances the drive capacity of step-up circuit as well as the display quality, while the current consumption will increase. Adjust the frequency taking both the display quality and the current consumption into consideration.

AP2–0: Adjust the amount of fixed current from the fixed current source of operational amplifier for the liquid crystal drive power supply. When the amount of fixed current is set large, the liquid crystal drive capacity will be enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. During non-display operation, set AP2-0 = "000" to halt the operation of operational amplifier to reduce current consumption.

DK: Control the operation of the step-up circuit 1. When turning on the power supply, stop the start up of VLOUT1 for a moment, and wait for an enough time until VLOUT2 is stabilized before starting up VLOUT1. For details, see the "Power Supply Setting Flow" section.

SLP: When SLP = 1, the HD66789 enters into the sleep mode. In the sleep mode, internal display operation is halted except the R-C oscillator to reduce current consumption. Only power control instructions
(BT2–0, DC2–0, AP2–0, SLP, STB, VC2-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits) are executed during the sleep mode. No change is made to the GRAM data or instructions during the sleep mode, although it is retained.

STB: When STB = 1, the HD66789 enters into the standby mode. In the standby mode, display operation is completely halted, and all internal operation including the internal R-C oscillator and reception of external clock pulse, is halted. For details, see the "Standby Mode" section. Only instructions to release the standby mode (STB = 0) and to start oscillation are accepted during the standby mode. Changes in the GRAM data or instructions during the standby mode are susceptible to destruction. These changes should be made after releasing the standby mode.

VC2-0: Adjust the reference voltage for VREG1OUT, VciOUT voltages to the optimum ratio of Vci.

AP2	AP1	AP0	Amount of current in operational amplifier
0	0	0	halt
0	0	1	setting disabled
0	1	0	0.5 (fixed)
0	1	1	0.75 (fixed)
1	0	0	1 (fixed)
1	0	1	1.25 (fixed)
1	1	0	1.5 (fixed)
1	1	1	setting disabled

DC02	DC01	DC00	Step-up circuit 1 step-up frequency
0	0	0	oscillation clock / 8
0	0	1	oscillation clock / 16
0	1	0	oscillation clock / 32
0	1	1	oscillation clock / 64
1	0	0	oscillation clock / 128
1	0	1	setting disabled
1	1	0	setting disabled
1	1	1	setting disabled

DC12	DC11	DC10	Step-up circuit 2 step-up frequency
0	0	0	oscillation clock / 16
0	0	1	oscillation clock / 32
0	1	0	oscillation clock / 64
0	1	1	oscillation clock / 128
1	0	0	oscillation clock / 256
1	0	1	setting disabled
1	1	0	setting disabled
1	1	1	setting disabled

BT2	BT1	BT0	VLOUT1 output (DDVDH)	VLOUT4 output (VCL)	VLOUT2 output (VGH)	VLOUT3 output (VGL)	Capacitor connection pins
0	0	0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x 6]	- (Vci1+DDVDH x 2) [x –5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	0	1	↑	↑	DDVDH x 3 [x 6]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	1	0	↑	↑	DDVDH x 3 [x 6]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	1	1	↑	↑	Vci1 +DDVDH x 2 [x 5]	- (Vci1+DDVDH x 2) [x –5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	0	0	↑	↑	Vci1 +DDVDH x 2 [x 5]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	0	1	↑	↑	Vci1 +DDVDH x 2 [x 5]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	1	0	↑	↑	DDVDH x 2 [x 4]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	1	1	↑	↑	DDVDH x 2 [x 4]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±

Note 1) The numerals in the bracket [ ] show the step-up scale from Vci1.

Note 2) The capacitor connection pins are step-up capacitors which are necessary for DDVDH, VCL, VGH, VGL voltages.

Note 3) Set the voltage within the following range: DDVDH = 5.5 V (Max.), VCL = - 3.3 V (Min.), VGH = 16.5 V (Max.), VGL = -16.5 V (Min.)

VC2	VC1	VC0	VciOUT output voltage (REGP)
0	0	0	Vci
0	0	1	0.92 x Vci
0	1	0	0.87 x Vci
0	1	1	0.83 x Vci
1	0	0	0.76 x Vci
1	0	1	0.73 x Vci
1	1	0	setting disabled
1	1	1	setting disabled

DK	Operation of step-up circuit 1
0	Operation
1	Halt

Power Control 3 (R12h)

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

PON: Start operation of VLOUT3. To stop operation, set PON = 0. To start operation, set PON = 1.

VRH3-0: Set the scale for amplifying VLOUT1 voltage (the reference voltage for VCOM and grayscale voltage). REGP voltage is amplified by 1.33 ~ 2.775 times.

VCOMG: When VCOMG = 1, VcomL outputs a negative voltage (1.0V ~ -Vci+0.5V Max.). When VCOMG = 0, the amplifiers for the negative voltage is halted, thereby saving power consumption. When VCOMG = 0, settings with VDV4-0 bits are invalid. In this case, to adjust AC amplitude of Vcom, make settings with VCM4-0 bits (VcomH setting). VCOMG = 1 is valid when PON = 1.

VDV4-0: Set the AC amplitude of Vcom during Vcom AC drive. The amplitude can be specified within the range of 0.6 ~ 1.23 times of VREG1OUT. When VCOMG = 0, this setting is invalid.

VCM4-0: Set the VcomH voltage (The higher voltage during Vcom AC drive). The voltage can be specified within the range of 0.4 ~ 0.98 times of VREG1OUT. When VCM4-0 = “11111”, the internal volume adjustment operation is halted, and the VcomH voltage can be adjust by placing an external resistor from VcomR.

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage
0	0	0	0	REGP x 1.33
0	0	0	1	REGP x 1.45
0	0	1	0	REGP x 1.55
0	0	1	1	REGP x 1.65
0	1	0	0	REGP x 1.75
0	1	0	1	REGP x 1.80
0	1	1	0	REGP x 1.85
0	1	1	1	halt
1	0	0	0	REGP x 1.90
1	0	0	1	REGP x 2.175
1	0	1	0	REGP x 2.325
1	0	1	1	REGP x 2.475
1	1	0	0	REGP x 2.625
1	1	0	1	REGP x 2.700
1	1	1	0	REGP x 2.775
1	1	1	1	halt

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH	VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.40	0	0	0	0	0	VREG1OUT x 0.60
0	0	0	0	1	VREG1OUT x 0.42	0	0	0	0	1	VREG1OUT x 0.63
0	0	0	1	0	VREG1OUT x 0.44	0	0	0	1	0	VREG1OUT x 0.66
:	:	:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	VREG1OUT x 0.64	0	1	1	0	0	VREG1OUT x 0.96
0	1	1	0	1	VREG1OUT x 0.66	0	1	1	0	1	VREG1OUT x 0.99
0	1	1	1	0	VREG1OUT x 0.68	0	1	1	1	0	VREG1OUT x 1.02
0	1	1	1	1	Halt internal volume. Adjust with a variable external resistor from VcomR.	0	1	1	1	1	Setting disabled
1	0	0	0	0	VREG1OUT x 0.70	1	0	0	0	0	VREG1OUT x 1.05
1	0	0	0	1	VREG1OUT x 0.72	1	0	0	0	1	VREG1OUT x 1.08
1	0	0	1	0	VREG1OUT x 0.74	1	0	0	1	0	VREG1OUT x 1.11
:	:	:	:	:	:	1	0	0	1	1	VREG1OUT x 1.14
1	1	1	0	0	VREG1OUT x 0.94	1	0	1	0	0	VREG1OUT x 1.17
1	1	1	0	1	VREG1OUT x 0.96	1	0	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 0.98	1	0	1	1	0	VREG1OUT x 1.23
1	1	1	1	1	Halt internal volume. Adjust with a variable external resistor from VcomR.	1	0	1	1		Setting disabled
						1	1	*	*	*	Setting disabled

Note 1) Adjust VREG1OUT and VCM0-4 to set VcomH the same level as VDH or less.
Note 2) Adjust VREG1OUT and VDV0-4 to set the amplitude of Vcom 6.0V or less.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

AD15–0: Make the initial setting for the GRAM address in the address counter (AC). After GRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and the setting for a new GRAM address is not required in the address counter. Therefore, data are written consecutively without resetting the address. The address counter is not automatically updated when data are read out from GRAM.

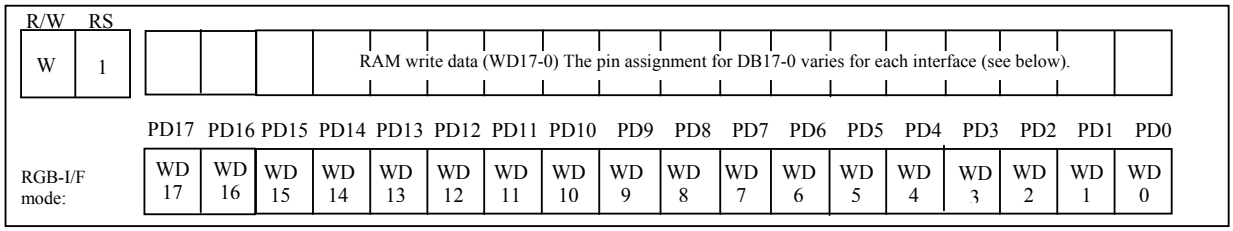
GRAM address setting can not be made during the standby mode. An address set should be made within the area specified with the window address.

When the RGB interface is selected (RM = 1), the setting of the address for AD15-0 is made every frame at the falling edge of VSYNC. When the internal clock operation or VSYNC interface is selected (RM = 0), the setting of the address is made when the instruction is executed.

GRAM Address Range

AD15–AD0	GRAM Setting
“0000”H – “00AF”H	Bitmap data for G1
“0100”H – “01AF”H	Bitmap data for G2
“0200”H – “02AF”H	Bitmap data for G3
“0300”H – “03AF”H	Bitmap data for G4
:	:
“EC00”H – “ECAF”H	Bitmap data for G237
“ED00”H – “EDAF”H	Bitmap data for G238
“EE00”H – “EEAF”H	Bitmap data for G239
“EF00”H – “EFAF”H	Bitmap data for G240

Write Data to GRAM (R22h)

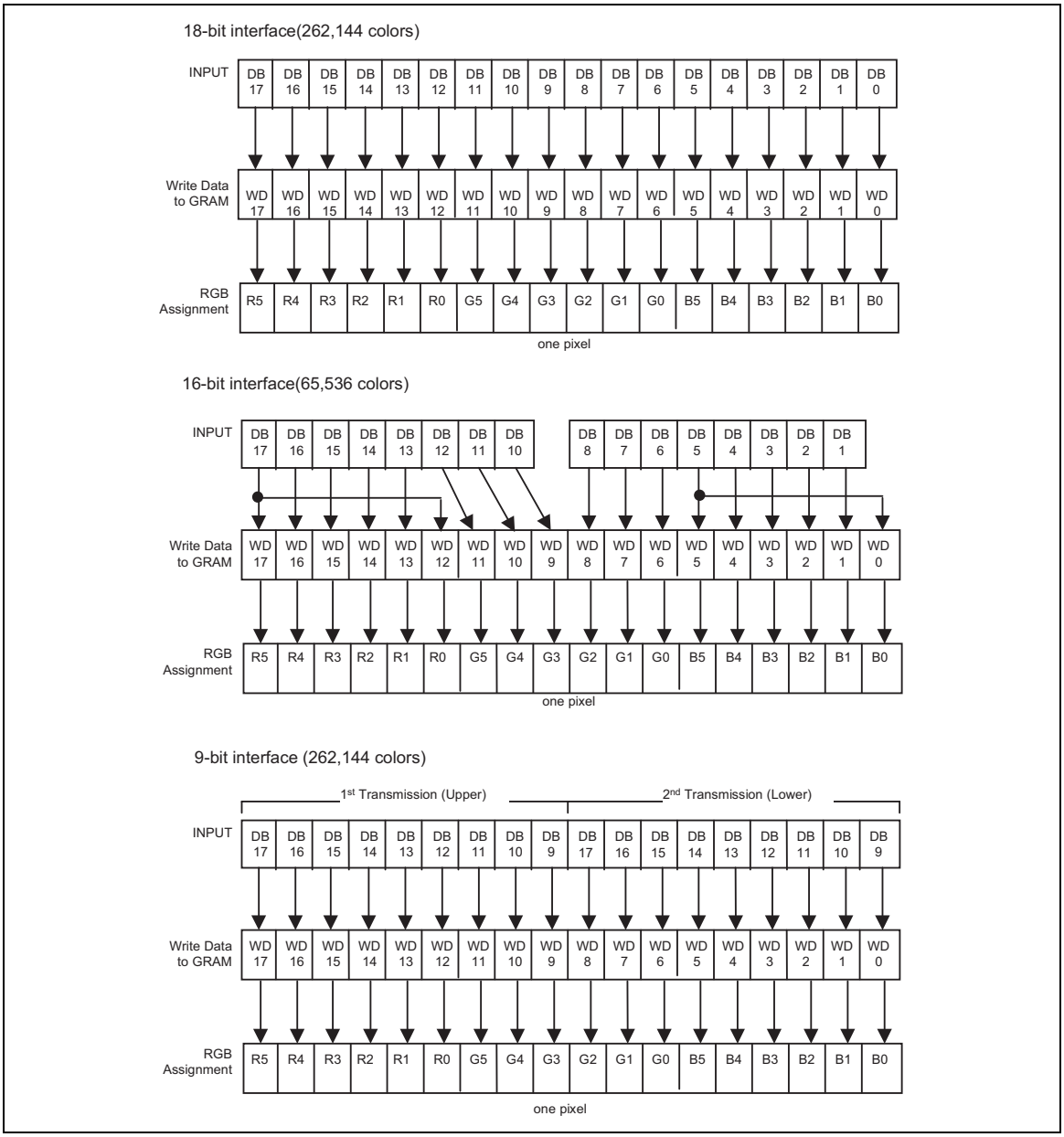


WD17–0: All data are expanded into 18 bits internally before written to GRAM. Each interface has its own way of expanding data to 18 bits.

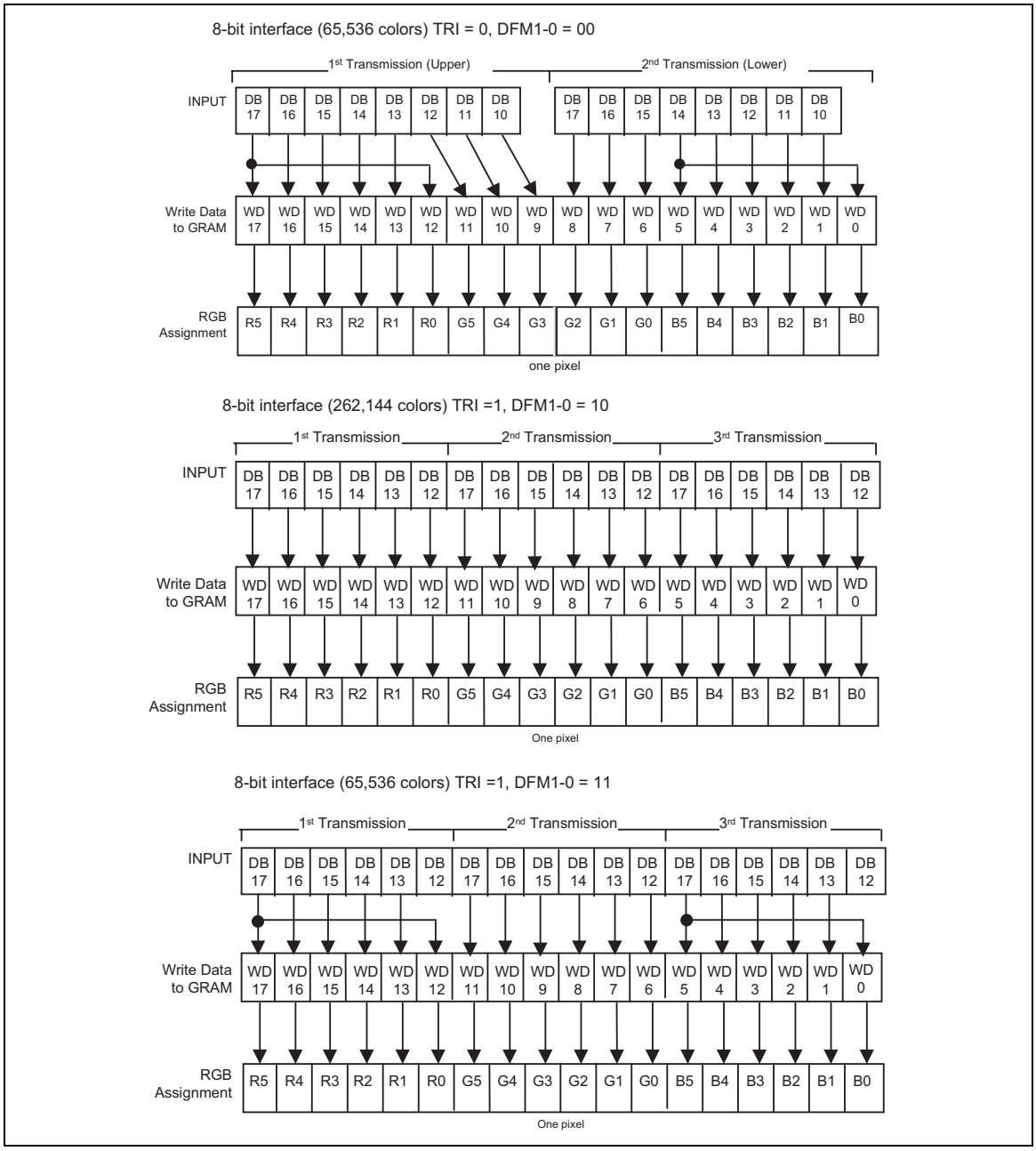
The grayscale level is selected according to the GRAM data. The address is automatically updated according to the setting with the AM and I/D bits after data are written to GRAM. During the standby mode, no access is allowed to GRAM. When 8 or 16 bit interface modes is selected, the data in the MSB of R and B pixels are also written to the LSB of R and B pixels respectively to expand the 8/16- bit data into the 18bit data internally.

During the RGB interface mode, when writing data to RAM through a system interface, make sure to avoid conflicts between writing through the RGB interface and writing through the system interface.

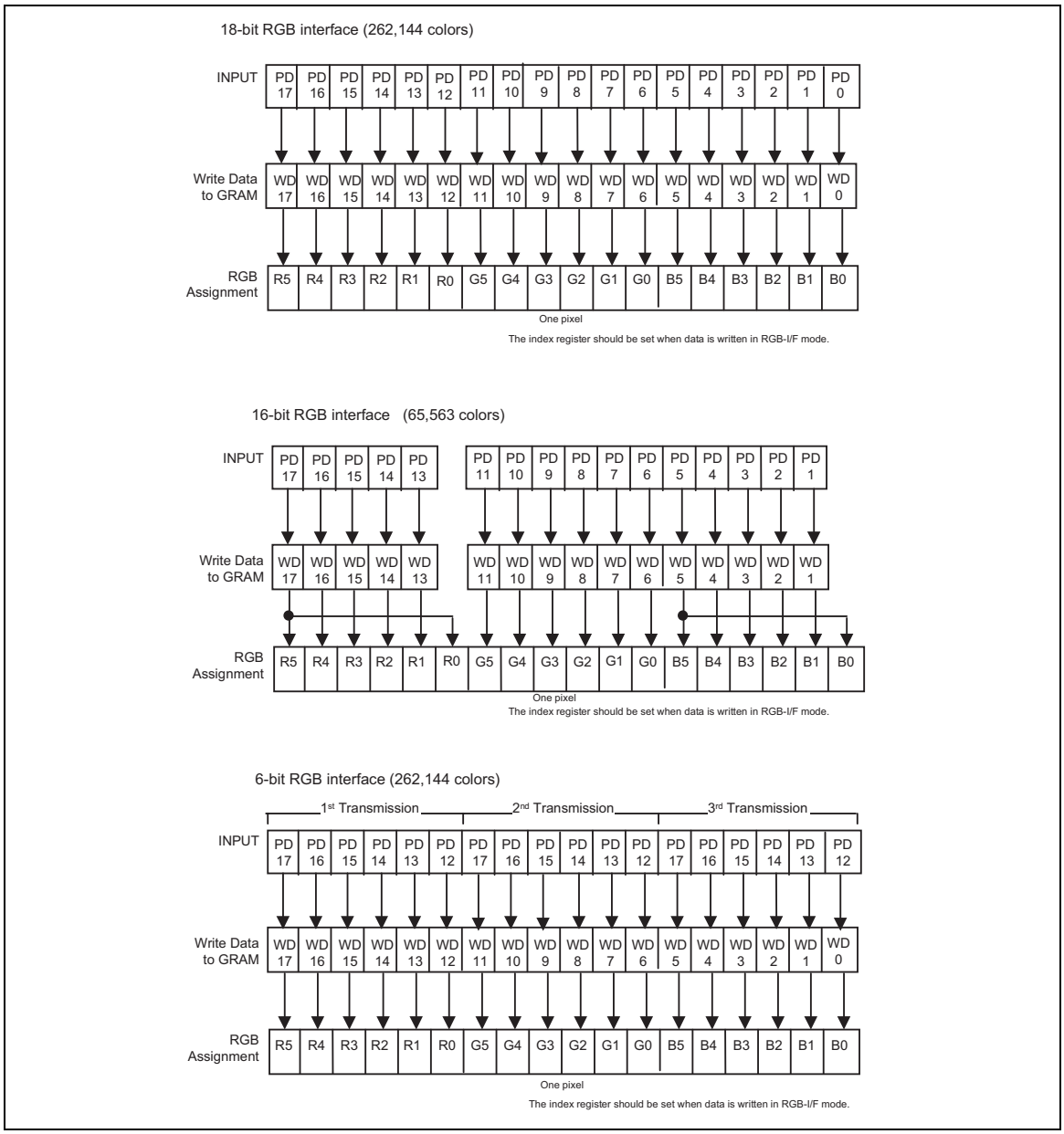
When the 18-bit RGB interface is selected, the18-bit data in PD17-0 bits are written, and 262,144 colors are available. When the 16-bit RGB interface is selected, the data in the MSB of R and B pixels are also written to the LSB of R and B pixels respectively, and 65,536 colors are available.



Write data to GRAM: Bit assignment



Write data to GRAM: Bit assignment



Write data to GRAM (RGB interface): Bit assignment

GRAM data settings RGB	Grayscale	
	Negative	Positive
000000	V0	V31
000001	(V0-V1)/2	(V30-V31)/2
000010	V1	V30
000011	(V1-V2)/2	(V29-V30)/2
000100	V2	V29
000101	(V2-V3)/2	(V28-V29)/2
000110	V3	V28
000111	(V3-V4)/2	(V27-V28)/2
001000	V4	V27
001001	(V4-V5)/2	(V26-V27)/2
001010	V5	V26
001011	(V5-V6)/2	(V25-V26)/2
001100	V6	V25
001101	(V6-V7)/2	(V24-V25)/2
001110	V7	V24
001111	(V7-V8)/2	(V23-V24)/2
010000	V8	V23
010001	(V8-V9)/2	(V22-V23)/2
010010	V9	V22
010011	(V9-V10)/2	(V21-V22)/2
010100	V10	V21
010101	(V10-V11)/2	(V20-V21)/2
010110	V11	V20
010111	(V11-V12)/2	(V19-V20)/2
011000	V12	V19
011001	(V12-V13)/2	(V18-V19)/2
011010	V13	V18
011011	(V13-V14)/2	(V17-V18)/2
011100	V14	V17
011101	(V14-V15)/2	(V16-V17)/2
011110	V15	V16
011111	(V15-V16)/2	(V15-V16)/2

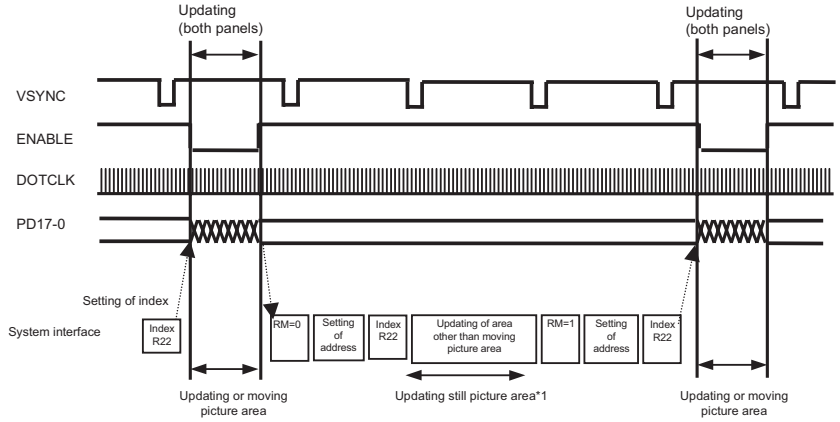
GRAM data settings RGB	Grayscale	
	Negative	Positive
100000	V16	V15
100001	(V16-V17)/2	(V14-V15)/2
100010	V17	V14
100011	(V17-V18)/2	(V13-V14)/2
100100	V18	V13
100101	(V18-V19)/2	(V12-V13)/2
100110	V19	V12
100111	(V19-V20)/2	(V11-V12)/2
101000	V20	V11
101001	(V20-V21)/2	(V10-V11)/2
101010	V21	V10
101011	(V21-V22)/2	(V9-V10)/2
101100	V22	V9
101101	(V22-V23)/2	(V8-V9)/2
101110	V23	V8
101111	(V23-V24)/2	(V7-V8)/2
110000	V24	V7
110001	(V24-V25)/2	(V6-V7)/2
110010	V25	V6
110011	(V25-V26)/2	(V5-V6)/2
110100	V26	V5
110101	(V26-V27)/2	(V4-V5)/2
110110	V27	V4
110111	(V27-V28)/2	(V3-V4)/2
111000	V28	V3
111001	(V28-V29)/2	(V2-V3)/2
111010	V29	V2
111011	(V29-V30)/2	(V1-V2)/2
111100	V30	V1
111101	(V30-V31)/2	(V0-V1)/2
111110	(V30-V31)/3	(V0-V1)/3
111111	V31	V0

GRAM data and LCD output level

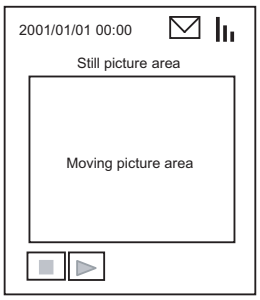
RAM Access through RGB-I/F and System I/F

The HD66787 writes all display data on the panels to the internal RAM. This enables the transfer of only the data for the moving picture area as well as for the frames for updating screens through the RGB interface. By writing data in the high speed write mode (HWM = 1) and with the window address function, the HD66787 enables the high-speed access to RAM with low power consumption while displaying moving pictures. In the frames other than the moving picture screen update, the display data in the area other than the moving picture area can be updated through a system interface.

The RAM access is also possible through a system interface even in the RGB-I/F mode. In the RGB interface mode, data are written to RAM in synchronization with the DOTCLK during ENABLE = "Low". When writing data in the RGB-I/F mode through the system interface, it is necessary to set the ENABLE "High" to stop writing through the RGB interface. After accessing to RAM through the system interface, wait an enough time for the write/read bus cycle before starting accessing to RAM through the RGB interface. When RAM accesses through the RGB and system interfaces conflict, there will be no guarantee that data are properly written to RAM.



Note 1) When RGB-I/F is selected, the address setting is made at every falling edge of VSYNC.
Note 2) The address set and the index set must be made before the RAM access throught the RGB interface.
Note 3) The high-speed write mode should be used in RGB-I/F and VSYNC-I/F modes.



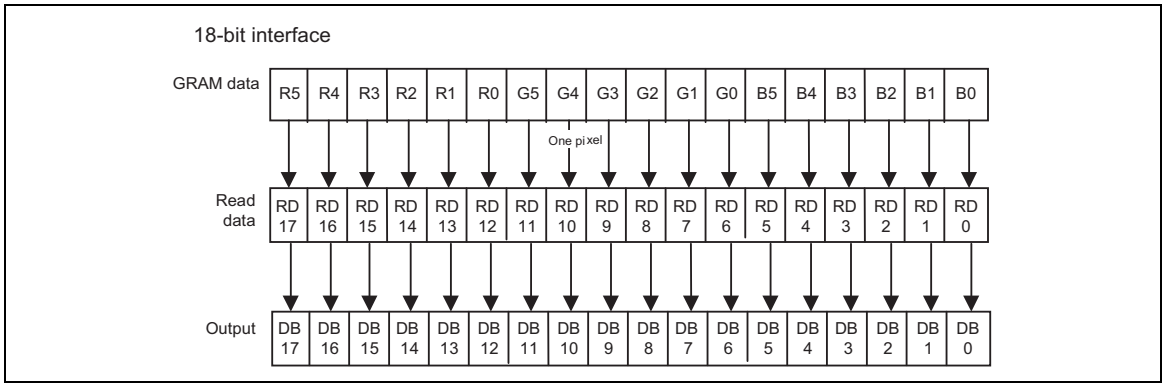
Updating Still Picture Area during Displaying a Moving Picture

Read Data Read from GRAM (R22h)

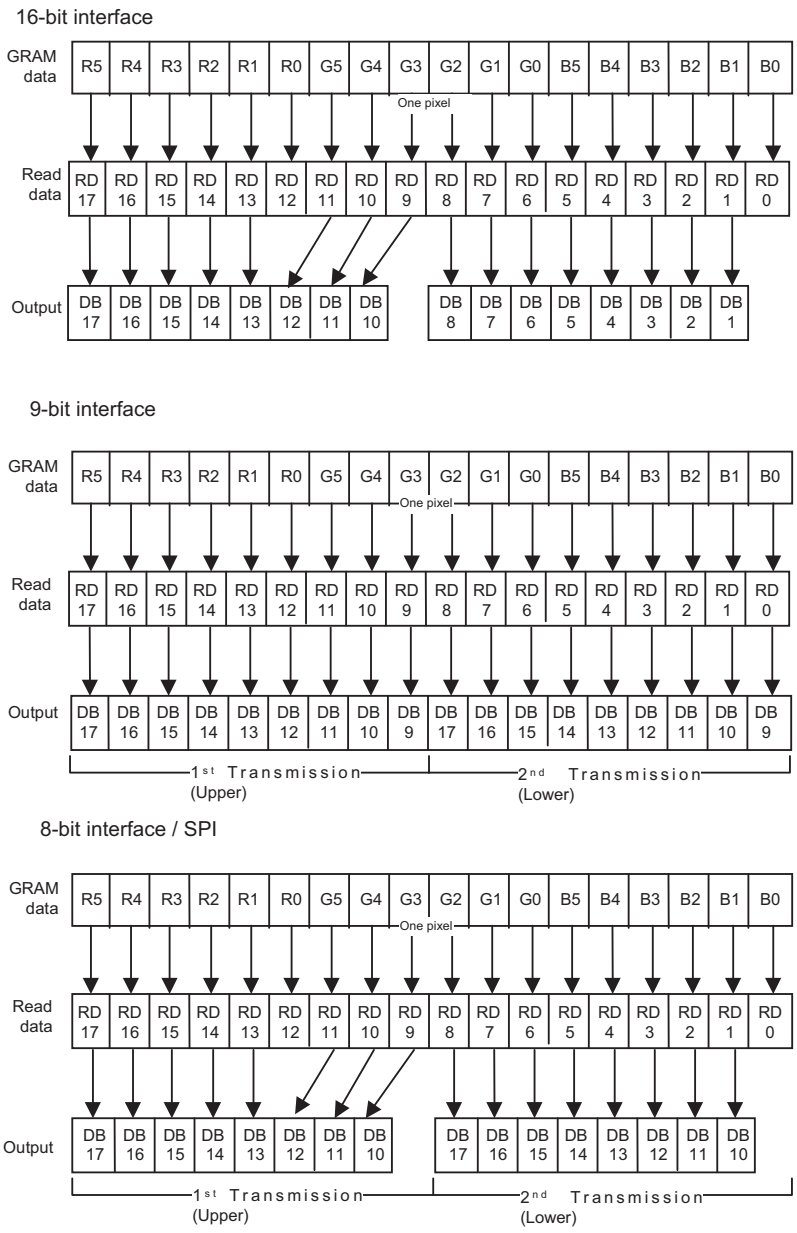
R/W	RS																							
R	1				RAM Read data (RD17-0) The pin assignment for DB17-0 varies for each interface (see below).																			

RD17–0: Read 18-bit data from GRAM. The bit assignment for the data that are read out from GRAM is different according to the interface.

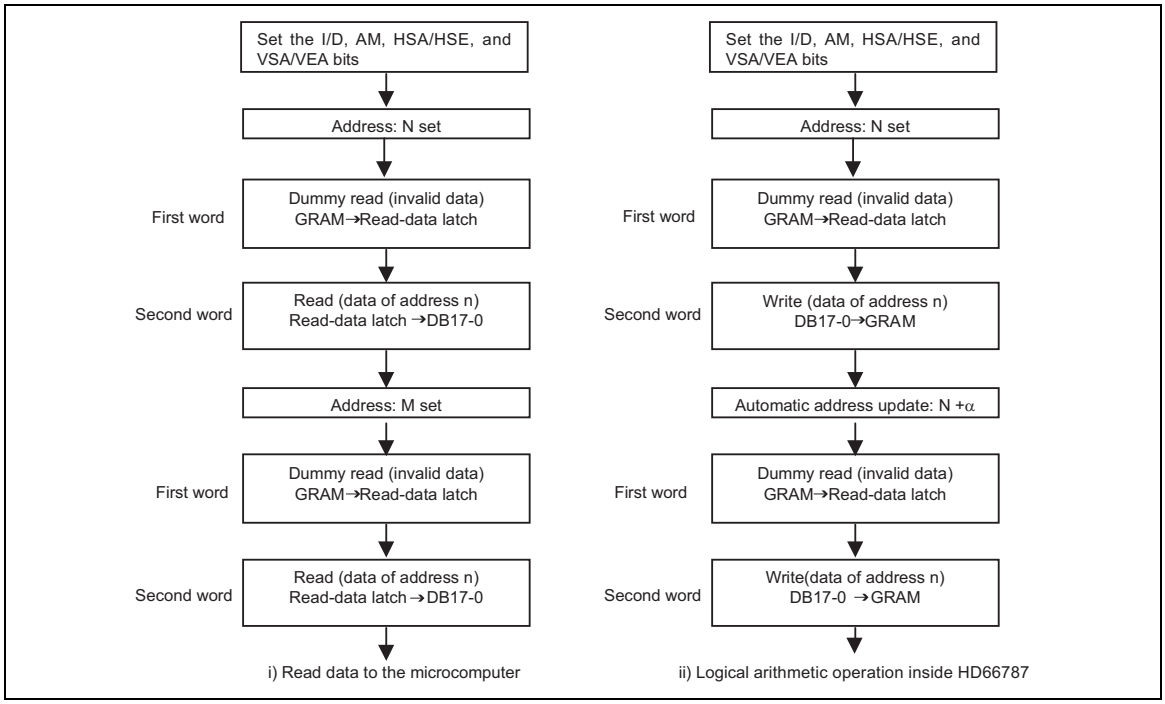
When data are read out from GRAM to the microcomputer, the first word read immediately after GRAM address set are latched in the internal read-data latch, and thereby nullify the data in the data bus (DB17–0). The second word is read as valid data. When the HD66787 performs an internal bit processing, such as logical operation, it uses the data latched in the read-data latch. Therefore the processing is completed by single read out operation. The data are expanded internally into 18 bits before going through the logical operation. When the 8-/16-bit interfaces are selected, the GRAM data in the LSBs of R and B pixels are not read out. This function is not available in RGB interface mode.



Read data from GRAM: Bit assignment



Read data from GRAM: Bit assignment



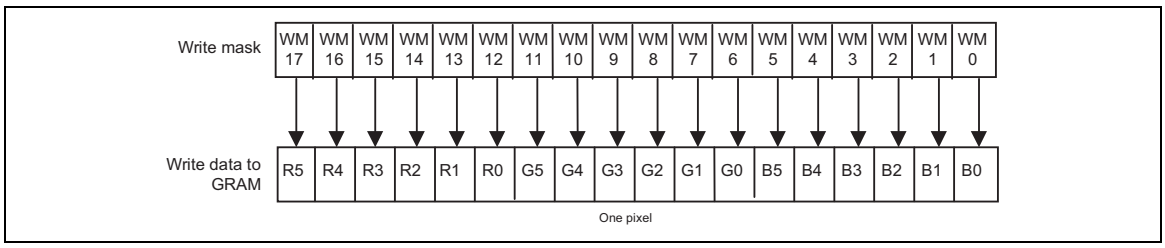
GRAM read sequence

RAM Write Data Mask (R23h)
RAM Write Data Mask (R24h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	0	0	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0
W	1	0	0	0	0	0	1	1	1	0	1	WM 17	WM 16	WM 15	WM 14	WM 13	WM 12

WM17–0: Write-mask the data when these data are written to GRAM by bit. For example, if WM17 = 1, the WM17 write-mask the MSB of the data to write to GRAM so that the data in the MSB are not written to GRAM. The rest of WM16-0 bits also write-mask the data in the corresponding bits when these bits are set to "1". For details, see the "Graphics Operation Function" section.

The WM17-0 bits write-mask the data to write to GRAM, which are expanded, if necessary, into 18 bits. This function is not available in the RGB-I/F mode.



RAM write data mask

γ Control (R30h to R39h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R31	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35	W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R38	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R39	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

γ Control Instructions

PKP52-00 : The γ fine adjustment registers for positive polarity.
PRP12-00 : The γ gradient adjustment registers for positive polarity.
PKN52-00 : The γ fine adjustment registers for negative polarity.
PRN12-00 : The γ gradient adjustment registers for negative polarity.
VRP14-00 : The amplitude adjustment registers for positive polarity.
VRN14-00 : The amplitude adjustment registers for negative polarity.

For details, see the "γ adjustment" section.

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7–0: Specify the number of raster-rows that are scrolled and control smooth scrolling in the vertical direction. The number of raster-rows is specified between 0 to 240. The raster-rows of the specified number are being scrolled during display. When the 240th raster-row is displayed, the scrolling display starts afresh from the 1st raster-row. The number of raster-rows that are scrolled (VL7–0) can be specified when the first panel vertical scroll enable bit VLE1 = 1 or the second panel vertical scroll enable bit VLE2 = 1. The number of raster-rows is fixed (not changeable) when VLE2-1 = 00. This function is not available in the external display interface mode.

VL Bits and Display-start Raster-row

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Amount of Scrolling (Number of raster-row)
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-rows
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	0	1	1	1	0	238 raster-rows
1	1	1	0	1	1	1	1	239 raster-rows

Note: When setting the number of raster-rows for scrolling, it must be 239 or less.

1st-Screen Drive Position (R42h)

2nd-Screen Drive Position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS17–10: Specify the start position for driving the first screen by line. The liquid crystal is driven by from the gate driver of "the set value + 1".

SE17–10: Specify the end position for driving the first screen by line. The liquid crystal is driven by to the gate driver of "the set value + 1". For instance, when SS17–10 = "07"H and SE17–10 = "10"H, the liquid crystal is driven from G8 to G17, and black display is driven from G1 to G7, and G18 thereafter. Make sure that SS17–10 ≤ SE17–10 ≤ "EF"H. For details, see the "Screen Split Drive Function" section.

SS27–20: Specify the start position for driving the second screen by line. The liquid crystal is driven by from the gate driver of "the set value + 1". The second screen is driven when SPT = 1.

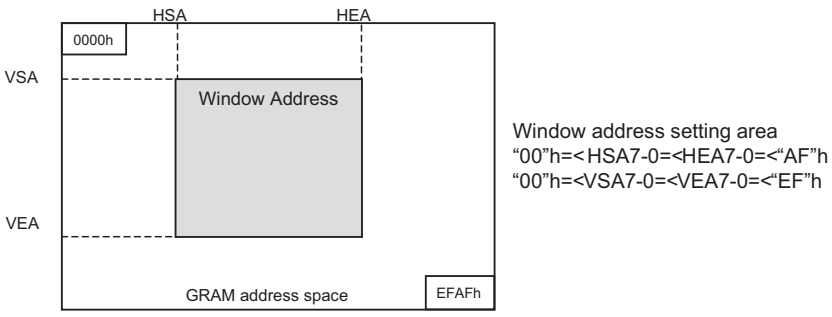
SE27–20: Specify the end position for driving the second screen by line. The liquid crystal is driven by to the gate driver of "the set value + 1". For instance, when SPT = 1, and SS27–20 = "20"H, SE27–20 = "4F"H, the liquid crystal is driven from G33 to G80. Make sure that SS17–10 ≤ SE17–10 < SS27–20 ≤ SE27–20 ≤ "EF"H. For details, see the "Screen Split Drive Function" section.

Horizontal RAM Address Position (R44h)
Vertical RAM Address Position (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA7-0/HEA7-0: Specify the start/end positions of the window-address range in the horizontal direction by address. Data are written to GRAM within the area determined by the addresses specified by HEA7-0 and HSA7-0. These addresses must be set before RAM write. In setting these bits, make sure that "00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "AF"h.

VSA7-0/VEA7-0: Specify the start/end positions of the window-address range in the vertical direction by address. Data are written to GRAM within the area determined by the addresses specified by VEA7-0 and VSA7-0. These addresses must be set before RAM write. In setting these bits, make sure that "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "EF"h.



Note 1) The window address area is set within the GRAM address space.

Note 2) In the high-speed write mode, data are written to the GRAM every four words. Therefore, depending on the window address setting, dummy write operations are required. For details, see the "High-Speed Burst RAM Write Function" section.

Note 3) The address set must be within the window address area. In the high-speed write mode, dummy write area must also be within the window address area.

GRAM address area and window-address range

Instruction List

Main Category		Sub Category		Upper Code								Lower Code								Note
Upper Index	Upper Index		Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index		Index	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
SR	Status Read		Status Read	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
0*	Display Control	00h	Oscillation Start	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
			Device Code Read	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	787
		01h	Driver Output Control	0	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	0	0	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (1)	
		02h	LCD AC driving Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
		03h	Entry Mode	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	HWM (0)	0	0	0	ID1 (1)	ID0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
		04h	Compare Register (1)	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
		05h	Compare Register (2)	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	
		06h	Setting Disabled																	
		07h	Display Control (1)	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	0	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
		08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
		09h	Setting Disabled																	
		0Ah	Setting Disabled																	
		0Bh	Frame Cycle Adjustment Control	NO1 (0)	NO0 (0)	SDT1 (0)	SDT0 (0)	EQ1 (0)	EQ0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
		0Ch	External Display Interface Control	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	0
		0Dh	LTPS Interface Control	0	0	0	TG0 (1)	0	CLW2 (0)	CLW1 (0)	CLW0 (0)	0	0	SHW1 (0)	SHW0 (0)	0	STG2 (0)	STG1 (0)	STG0 (0)	
		0Eh	Setting Disabled																	
		0Fh	Setting Disabled																	0
1*	Power Control	10h	Power Control (1)	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	AP2 (0)	AP1 (0)	AP0 (0)	0	DK (1)	SLP (0)	STB (0)	
		11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)	
		12h	Power Control (3)	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	0
		13h	Power Control (4)	0	0	VCOM G	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
		14h	Setting Disabled																	
		15h	Setting Disabled																	
		16h	Setting Disabled																	0
		17h	Setting Disabled																	0
		18h	Setting Disabled																	0
		19h	Setting Disabled																	0
		1Ah	Setting Disabled																	0
		1Bh	Setting Disabled																	0
		1Ch	Setting Disabled																	0
		1Dh	Setting Disabled																	0
		1Eh	Setting Disabled																	0
		1Fh	Setting Disabled																	0
2*	RAM Access	20h	Setting Disabled																	0
		21h	RAM Address Set	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	0
		22h	RAM data Write/Read	RAM Write Data (WD17-0 /RAM Read Data (RD17-0) *Bit assignment changes depending on the interface to be selected.																
		23h	RAM Write Data Mask (1)	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
		24h	RAM Write Data Mask (2)	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	0
		25h	Setting Disabled																	0
		26h	Setting Disabled																	0
		27h	Setting Disabled																	0
		28h	Setting Disabled																	0
		29h	Setting Disabled																	0
		2Ah	Setting Disabled																	0
		2Bh	Setting Disabled																	0
		2Ch	Setting Disabled																	0
		2Dh	Setting Disabled																	0
		2Eh	Setting Disabled																	0
		2Fh	Setting Disabled																	0
3*	γ Control	30h	γ Control (1)	0	0	0	0	0	PKP12 (0)	PKP11 (0)	PKP10 (0)	0	0	0	0	0	PKP02 (0)	PKP01 (0)	PKP00 (0)	0
		31h	γ Control (2)	0	0	0	0	0	PKP32 (0)	PKP31 (0)	PKP30 (0)	0	0	0	0	0	PKP22 (0)	PKP21 (0)	PKP20 (0)	0
		32h	γ Control (3)	0	0	0	0	0	PKP52 (0)	PKP51 (0)	PKP50 (0)	0	0	0	0	0	PKP42 (0)	PKP41 (0)	PKP40 (0)	0
		33h	γ Control (4)	0	0	0	0	0	PRP12 (0)	PRP11 (0)	PRP10 (0)	0	0	0	0	0	PRP02 (0)	PRP01 (0)	PRP00 (0)	0
		34h	γ Control (5)	0	0	0	0	0	PKN12 (0)	PKN11 (0)	PKN10 (0)	0	0	0	0	0	PKN02 (0)	PKN01 (0)	PKN00 (0)	0
		35h	γ Control (6)	0	0	0	0	0	PKN32 (0)	PKN31 (0)	PKN30 (0)	0	0	0	0	0	PKN22 (0)	PKN21 (0)	PKN20 (0)	0
		36h	γ Control (7)	0	0	0	0	0	PKN52 (0)	PKN51 (0)	PKN50 (0)	0	0	0	0	0	PKN42 (0)	PKN41 (0)	PKN40 (0)	0
		37h	γ Control (8)	0	0	0	0	0	PRN12 (0)	PRN11 (0)	PRN10 (0)	0	0	0	0	0	PRN02 (0)	PRN01 (0)	PRN00 (0)	0
		38h	γ Control (9)				VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)					VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)	
		39h	γ Control (10)				VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)					VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)	
		3Ah	Setting Disabled																	
		3Bh	Setting Disabled																	
		3Ch	Setting Disabled																	
		3Dh	Setting Disabled																	
		3Eh	Setting Disabled																	
		3Fh	Setting Disabled																	
4*	Coordination Control	40h	Setting Disabled																	0
		41h	Vertical Scroll Control	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	0
		42h	First Screen Driving Position	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	0
		43h	Second Screen Driving Position	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	0
		44h	Horizontal RAM Address Position	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	0
		45h	Vertical RAM Address Position	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (0)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	0
		46h	Setting Disabled																	0
		47h	Setting Disabled																	0
		48h	Setting Disabled																	0
		49h	Setting Disabled																	0
		4Ah	Setting Disabled																	0
		4Bh	Setting Disabled																	0
		4Ch	Setting Disabled																	0
		4Dh	Setting Disabled																	0
		4Eh	Setting Disabled																	0
		4Fh	Setting Disabled																	0
5*		*	Setting Disabled																	0
6*		*	Setting Disabled																	0
7*		*	Setting Disabled																	

Note 1) The numerals in parenthesis in the bit cells are initialized value.
Note 2) Do not access to the"Setting Disabled" indexes.

Reset Function

The HD66787 makes internal initialization with RESET input. During RESET, the HD66787 is in a busy state, and no instruction from the MPU and access to GRAM are accepted. The time required for the RESET input is at least 1ms. In case of power-on reset, wait at least 10ms after the power is turned on until the R-C oscillation frequency becomes stabilized. While waiting, do not make an initial setting for the instruction set or an access to GRAM.

Initial State of Instructions

a. Start oscillation
b. Driver output control (NL4–0 = "11101", SS = "0", SM = "0", EPL = "0", DPL = "0", HSPL = "0", VSPL = "0")
c. Liquid crystal AC drive control (B/C = "0", EOR = "0", NW5–0 = "00000")
d. Entry mode set (HWM = "0", I/D1-0 = "11": Increment by 1, AM = "0" : Horizontal direction, LG2–0 = "000" : Replace mode, BGR = "0", TRI = "0", DFM1-0 = "00")
e. Compare register (CP17–0 : "00 0000 0000 0000 0000")
f. Display control 1 (PT1-0 = "00", VLE2-1 = "00" : No vertical scroll, SPT = "0", DTE = "0", CL = "0" : 65,536-color mode, REV = "0", D1-0 = "00" : Display OFF)
g. Display control 2 (BP3-0 = "1000", FP3-0 = "1000")
h. Frame cycle control (NO1-0 = "00", SDT1-0 = "00", EQ1-0 = "00" : No equalization, DIV1-0 = "00": clock/1, RTN3-0 = "0000" : 16 clocks in 1H period)
i. External display interface (RIM1-0 = "00" : 18-bit RGB interface, DM1-0 = "00" : internal clock operation, RM = "0" : System interface)
j. LTPS interface control (TG0 = "1", STG2-0 = "000", SHW1-0 = "00", CLW2-0 = "000")
k. Power control 1 (SAP2-0 = "000", BT2-0 = "000", AP2–0 = "000": liquid crystal power off, DK = "1" : DCDC1 off, SLP = "0", STB = "0" : Standby mode off)
l. Power control 2 (DC12-0 = "000", DC02-00 = "000", VC2-0 = "000")
m. Power control 3 (PON = "0", VRH3-0 = "00000")
n. Power control 4 (VCOMG = "0", VDV4-0 = "00000", VCM4-0 = "00000")
o. RAM address set (AD15–0 = "0000"H)
p. RAM write data mask (WM17–0 = "18'h00000": No mask)
q. γ control
(PKP02-00 = "000", PKP12-10 = "000", PKP22-20 = "000", PKP32-30 = "000", PKP42-40 = "000", PKP52-50 = "000", PRP02-00 = "000", PRP12-10 = "000")
(PKN02-00 = "000", PKN12-10 = "000", PKN22-20 = "000", PKN32-30 = "000", PKN42-40 = "000", PKN52-50 = "000", PRN02-00 = "000", PRN12-10 = "000")
(VRP14-10 = "00000", VRP03-00 = "0000", VRN14-10 = "00000", VRN12-10 = "000")
r. Vertical scroll (VL7–0 = "00000000")
s. 1st split screen (SE17-10 = "11111111", SS17-10 = "00000000")
t. 2nd split screen (SE27-20 = "11111111", SS27-20 = "00000000")
u. Horizontal RAM address position (HEA7-0 = "10000011", HSA7-0 = "00000000")
v. Vertical RAM address position (VEA7-0 = "10101111", VSA7-0 = "00000000")

GRAM Data Initialization

The data in GRAM are not initialized by the RESET input. Initialize through software during the display OFF (D1–0 = “00”).

Initial state of Output Pins

a. Liquid crystal driver output pins (source outputs): Output GND level
b. Oscillator output pin (OSC2): Outputs oscillation signal

Interface Specifications

The HD66787 incorporates a system interface to make settings for instructions, and an external display interface to display moving pictures. By selecting an optimum interface for display (moving or still picture, or both), data are transmitted efficiently.

The external display interfaces are RGB-I/F and VSYNC-I/F. Through these interfaces, the data can be updated without flickering the moving picture on the display.

In the RGB-I/F mode, the display operation is performed in synchronization with the signals (VSYNC, HSYNC, and DOTCLK). The display data are written according to the values of the data enable signal (ENABLE), data valid signal (VLD) and PD17-0 bits in synchronization with VSYNC, HSYNC, and DOTCLK signals. The display data are written to GRAM to reduce the data transmission to minimum, i.e. only when the displays are being updated. With the window address function, only the RAM area used for moving picture display is overwritten, and therefore the simultaneous display of moving picture area, which is overwritten, and the RAM data in the area other than the moving picture area, which is not overwritten, is possible. In the RGB and VSYNC interface modes, write data to GRAM in the high speed write mode (HWM = 1) while displaying moving pictures to make an access to GRAM in high speed with low power consumption.

In the VSYNC interface mode, internal display operations are synchronized with the frame-synchronizing signal (VSYNC). By writing data in synchronization with the falling edge of VSYNC at a fixed speed to GRAM through a system interface, it enables moving pictures display with a system interface. In this case, there are some constraints in the RAM writing speed and method.

The HD66787 handles the following 4 operational modes for the type of display. The setting can be made through an external display interface. A transition between the modes must follow the transition flow.

Operation modes and interfaces

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

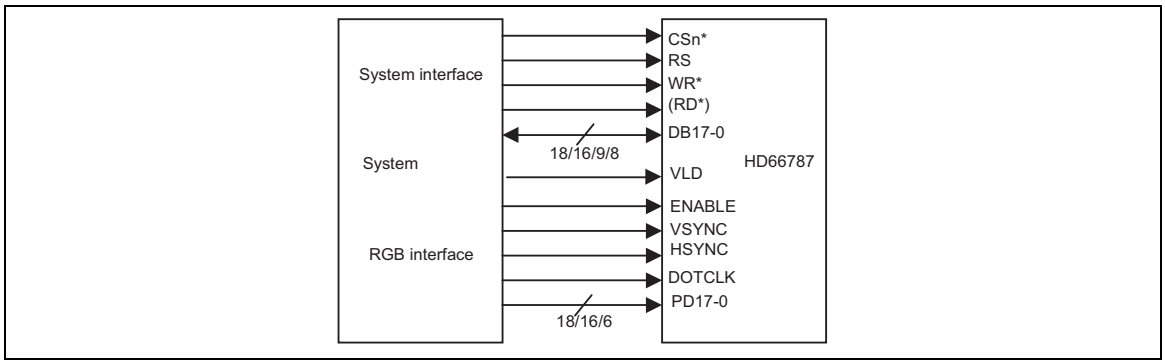
Note 1) the instruction register setting can be made only through a system interface.

Note 2) The RGB-I/F and VSYNC-I/F are not compatible with each other.

Note 3) Do not change the setting for RGB-I/F mode (RIM-0) while RGB I/F is in operation.

Note 4) See the “External Display Interface” section for the transition flow of each operation mode.

Note 5) In the RGB-I/F and VSYNC-I/F modes, write data in the high speed write mode (HWM = 1).



Interfaces and HD66787

System Interface

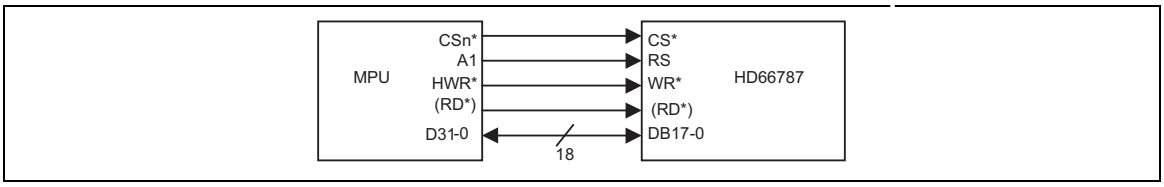
The following shows the kinds of system interfaces and the IM pins setting for selecting an interface. The instruction setting and RAM access are made through a system interface.

IM bits setting and the type of system interface

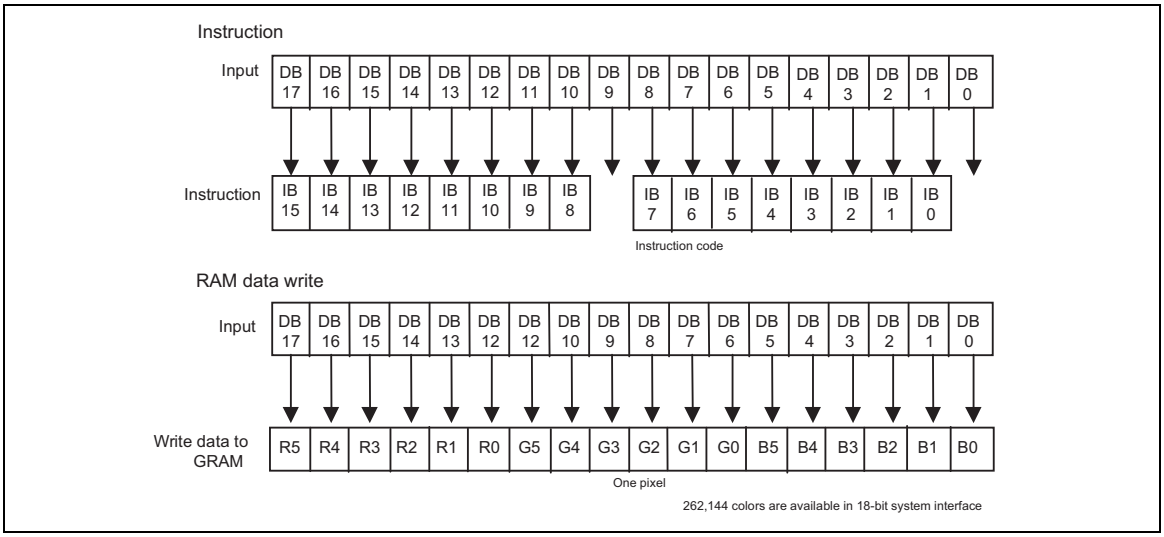
IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin
0	0	0	0	Setting disabled	
0	0	0	1	Setting disabled	
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8-to-1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Serial peripheral interface (SPI)	SDI, SDO
0	1	1	*	Setting disabled	
1	0	0	0	Setting disabled	
1	0	0	1	Setting disabled	
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled	

80-system 18-bit interface

80-system 18-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to IOVcc/GND/IOVcc/GND levels respectively.



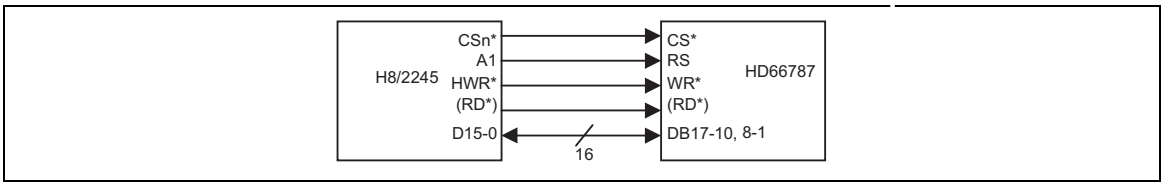
18-bit microcomputer and HD66787



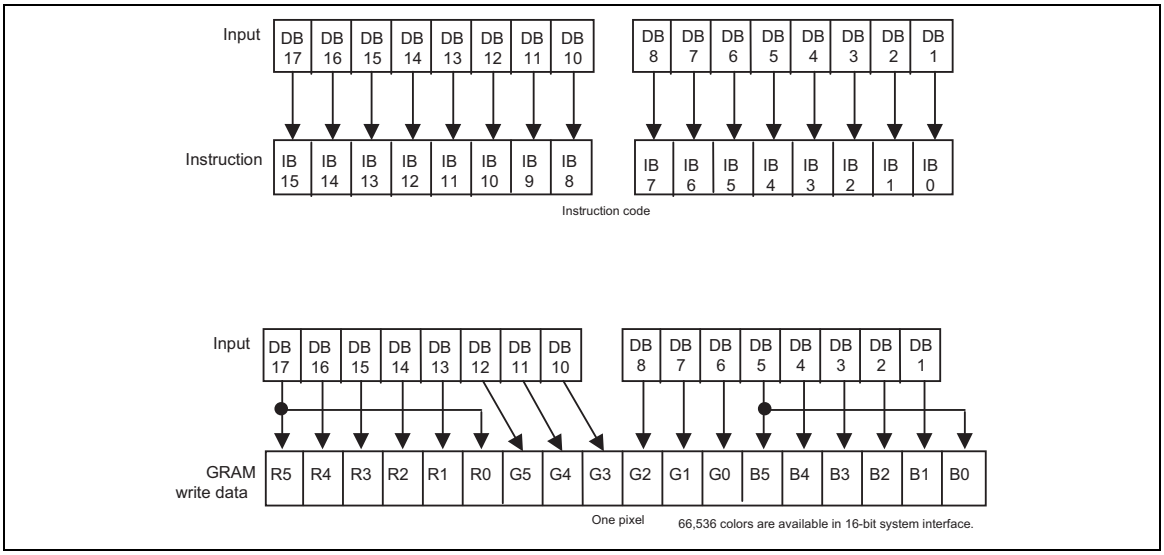
Data format for 18-bit interface

80-system 16-bit interface

The 80-system 16-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/IOVcc/GND levels respectively.



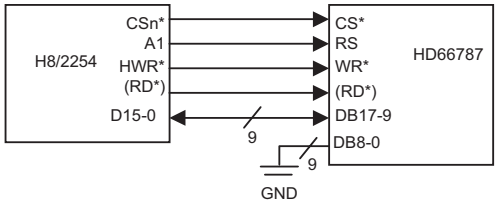
16-bit microcomputer and HD66787



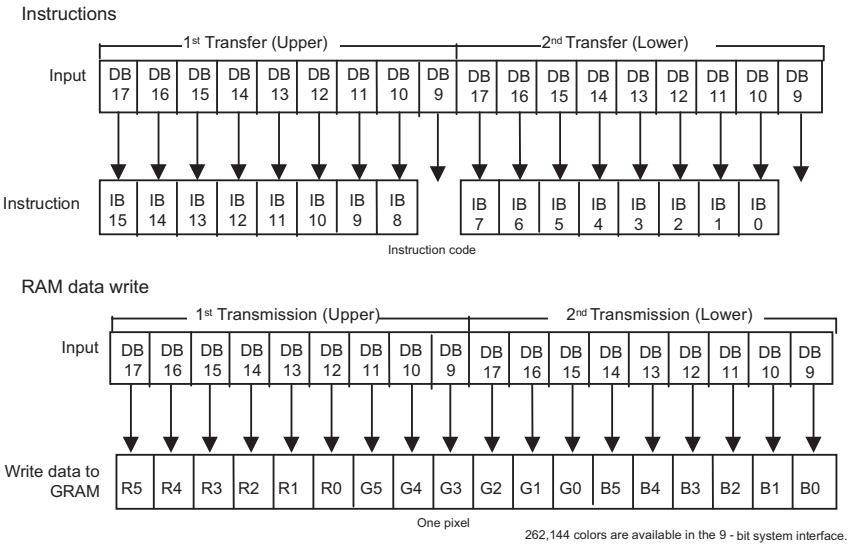
Data format for 16-bit interface

80-system 9-bit interface

The 80-system 9-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to IOVcc/GND/IOVcc/IOVcc levels respectively. When transmitting a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used) and the upper 8 bits are transmitted first. The RAM data is also divided into the upper and lower 9 bits, and the upper bits are transmitted first. The unused pins DB8-0 pins must be fixed to either IOVcc or GND level. When writing into the index register, the upper byte (8 bits) must be written.



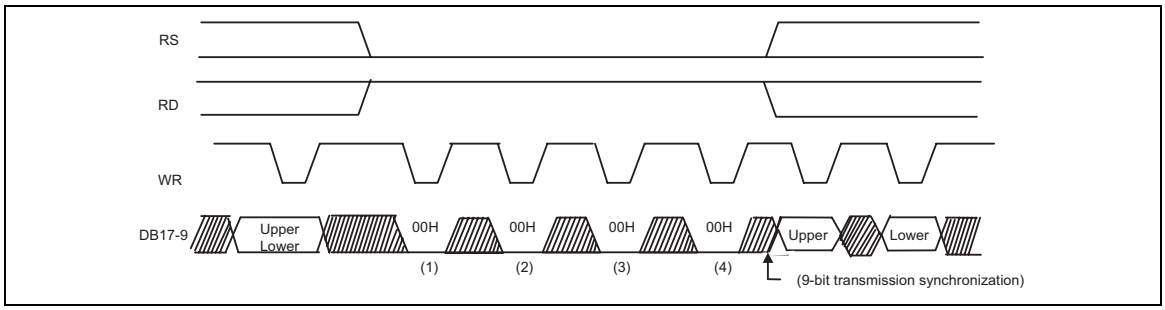
9-bit microcomputer and HD66787



Data format for 9-bit interface

Data transmission synchronizing in 9-bit bus interface mode

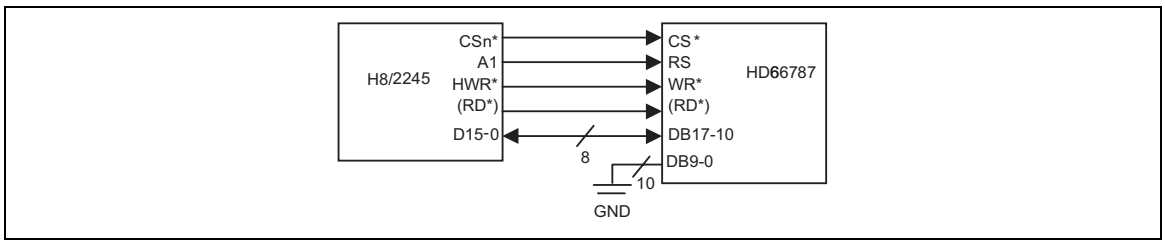
The HD66787 supports a data transmission synchronizing function, which resets the upper/lower counter that counts the number of transmission of upper/lower 9-bit data in the 9-bit bus interface mode. When a discrepancy occurs in the upper/lower 9-bit data transmission due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to forcibly reset the upper/lower counter so that data transmission restarts with an upper 9-bit data transmission. The excursion can be recovered by executing the synchronizing function periodically.



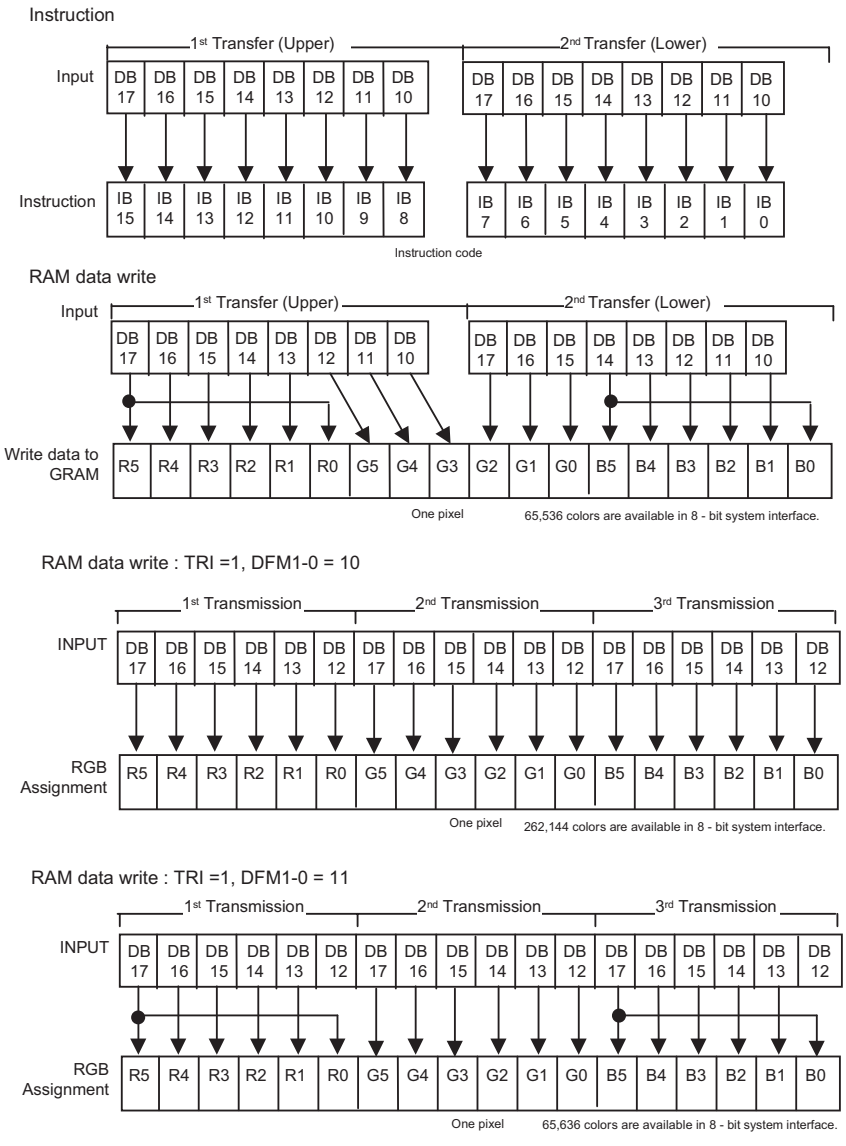
9-bit data transmission synchronization

80-system 8-bit interface

The 80-system 8-bit parallel data transmission becomes operable by setting IM3/2/1/0 pins to GND/GND/IOVcc/IOVcc levels respectively. When transmitting a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transmitted first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transmitted first. The data to write to RAM are expanded into 18 bits internally. The unused pins DB9-0 must be fixed to either IOVcc or GND level. When writing into the index register, the upper byte (8 bits) must be written.



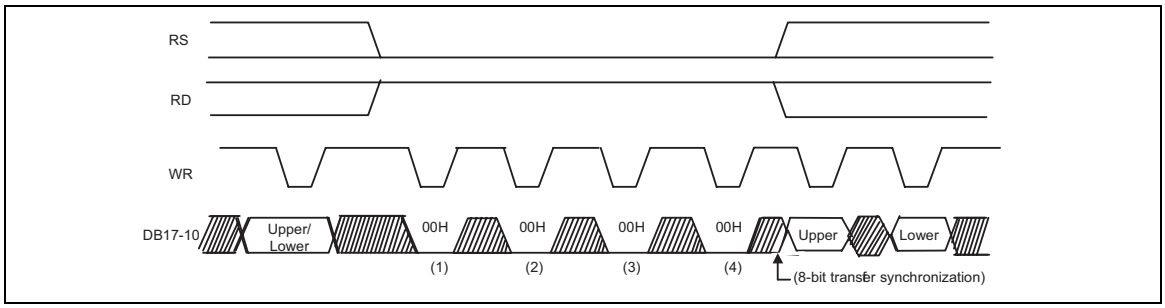
8-bit microcomputer and HD66787



Data format for 8-bit interface

Data transmission synchronization in 8-bit bus interface mode

The HD66787 supports a data transmission synchronizing function, which resets the upper/lower counter that counts the number of transmission of upper/lower 8-bit data in the 8-bit bus interface mode. When a discrepancy occurs in the transmission of upper/lower 8-bit data due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to forcibly reset the upper/lower counter so that data transmission restarts with the upper 8-bit transmission. The excursion can be recovered by executing the synchronizing function periodically.



8-bit data transmission synchronization

Serial Peripheral interface (SPI)

The Serial Peripheral Interface (SPI) becomes operable by setting IM3/2/1 pins to GND/IOVcc/GND levels respectively. The SPI is available through the chip select line (CS*), serial transfer clock line (SCL), serial data input (SDI), and serial data output (SDO). In the SPI mode, the IM0/ID pin functions as ID pin. In the SPI mode, the unused DB15-2 pins must be fixed at either IOVcc or GND level.

The HD66787 recognizes the start of data transfer at the falling edge of CS* input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CS* input. The HD66787 is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the HD66787 are compared and the both 6-bit data correspond. When selected, the HD66787starts taking in the subsequent data string. The setting for the least significant bit of the identification code is made with the ID pin. The five upper bits of the identification code must be 01110. Two different chip addresses must be assigned to the HD66787 because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When RS = 1, instruction write or RAM read/write is executed. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

In the SPI mode, the data are written to GRAM after two-byte data transmission. The data are expanded into 18 bits by adding one bit (the same data as the MSB of RB) next to the LSB of RB data.

After receiving the start byte, the HD66787 starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted. All HD66787 instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (DB15 to 0). The data to write to RAM are expanded into 18-bit data. After the start byte is received, the first byte is always fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction. The 4-byte data that are read from RAM right after the start byte are made invalid. The HD66789 reads as valid data from the 5th-byte data.

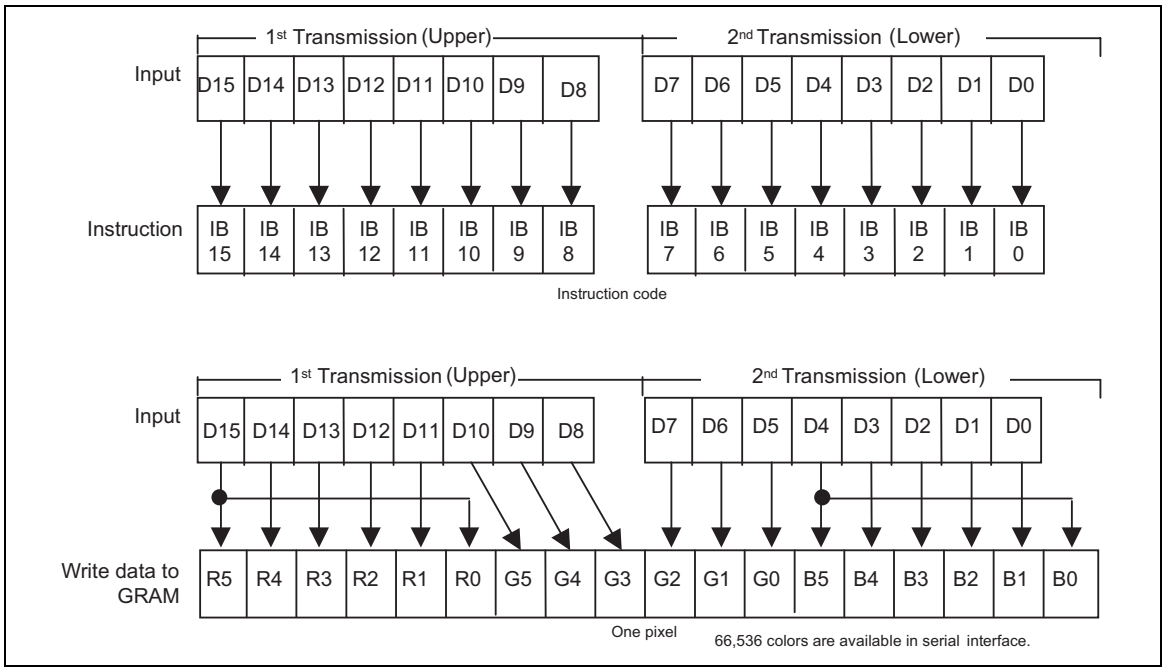
Start Byte Format

Transmitted bits	S	1	2	3	4	5	6	7	8
Start byte format	Transmission start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected with the IM0/ID pin.

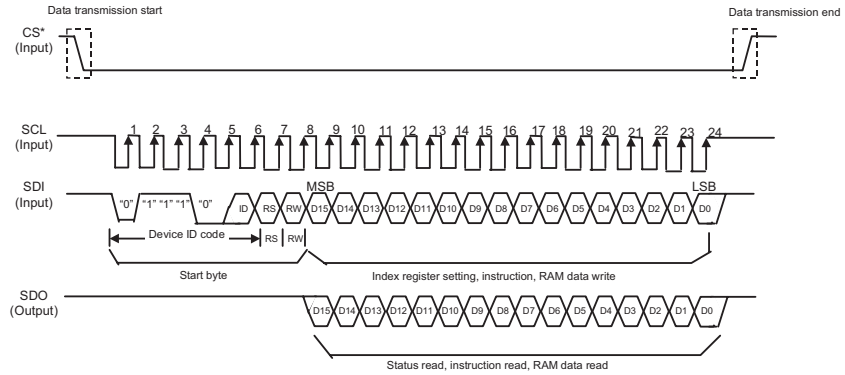
RS and R/W Bit Function

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

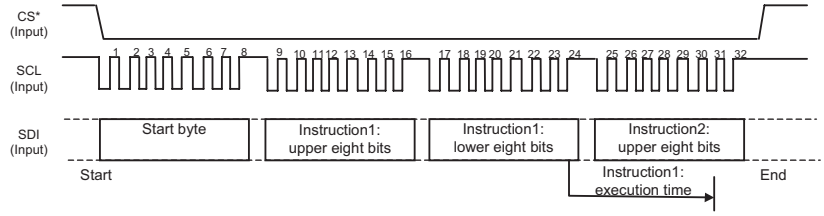


Data format for SPI

A)Basic data transmission through SPI

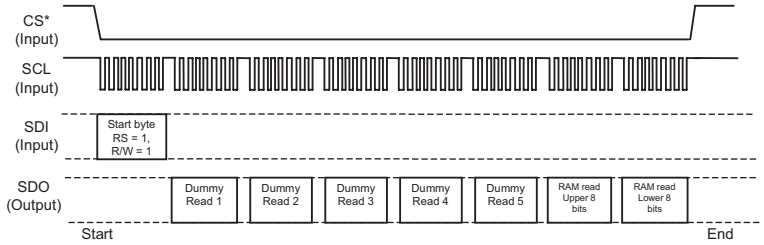


B)Consecutive data transmission through SPI



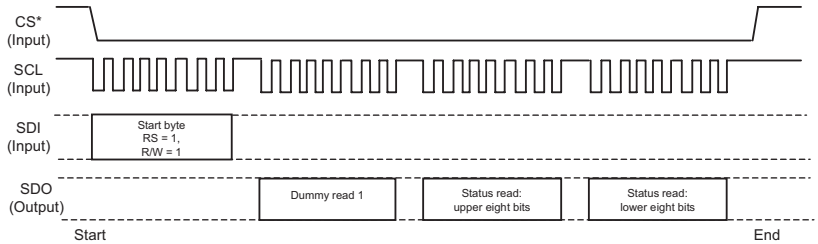
Note: The first byte after the start byte is always the upper eight bits.

C) RAM data read transmission



Note: Five bytes of invalid dummy data are read after the start byte.
The valid data are read from the 6th byte.

D) Status read / instruction read

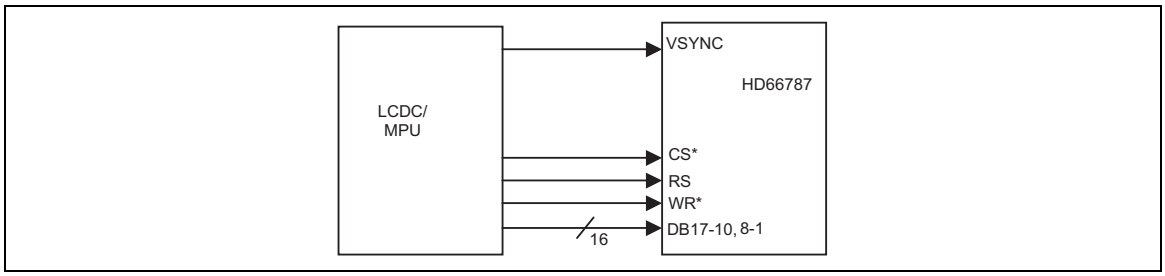


Note: One byte of invalid dummy data are read after the start byte.
The valid data are read from the second byte.

Data transmission through SPI

VSYNC Interface

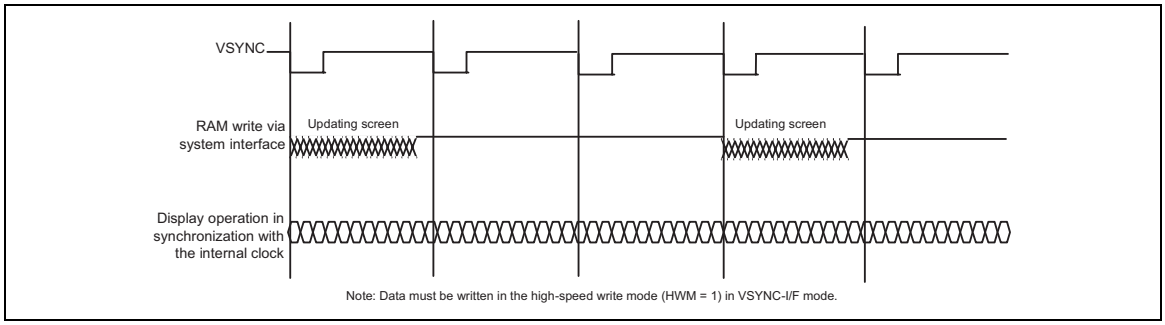
The HD66787 incorporates a VSYNC-I/F, which enables moving picture display with only a system interface and the frame-synchronizing signal (VSYNC). This interface enables moving picture display with minimum modification to a conventional system.



VYSNC interface

The VSYNC-I/F becomes operable by setting DM1-0 = 10 and RM = 0. In the VSYNC I/F mode, the internal display operations are synchronized with VSYNC. By writing data to RAM through a system interface in a speed that is higher for more than a fixed speed than the internal display operation speed, it enables moving picture display through a system interface, while preventing flickers while the screens are being updated.

Display operations are executed by the internal clock generated by the internal oscillator and VSYNC input. All display data are stored in RAM. This enables moving picture display only by transmitting data that are written over, thereby minimizing the number of data transmission while displaying moving picture. The high-speed write mode (HWM = 1) enables RAM access in high speed with low power consumption.



Moving picture data transmission through VSYNC interface

The VSYNC-I/F has limits on the minimum speed and the frequency of the internal clock for the RAM write through system interface. It requires a RAM write speed more than the result that is calculated from the following formula.

- Internal clock frequency (fosc) [Hz] = Frame frequency × (Display line (NL) + Front porch (FP) + Back porch (BP)) × 16 clocks × Fluctuation
- Minimum speed for RAM write (min.)[Hz] > 176 × Display line (NL) / {((Back porch (BP) + Display raster-row (NL) - Margin) × 16 clock) / fosc}

Note 1) When RAM write does not start right after the falling edge of VSYNC, the time between the falling edge of VSYNC and the start of RAM write must also be taken into account.

An example of RAM write speed and the frequency of the internal clock in the VSYNC interface mode is as follows.

[Example]

Display size	176 RGB × 240 lines
Display line	240 lines (NL = 11110)
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz] = 60 Hz × (240 + 2 + 14) × 16 Clock × 1.1 / 0.9 = 300 kHz

When calculating the internal clock frequency, possible causes of fluctuations must also be taken into consideration. The allowance for this fluctuation is ± 10 % from the center value, and the range of the frequency must be within VSYNC period.

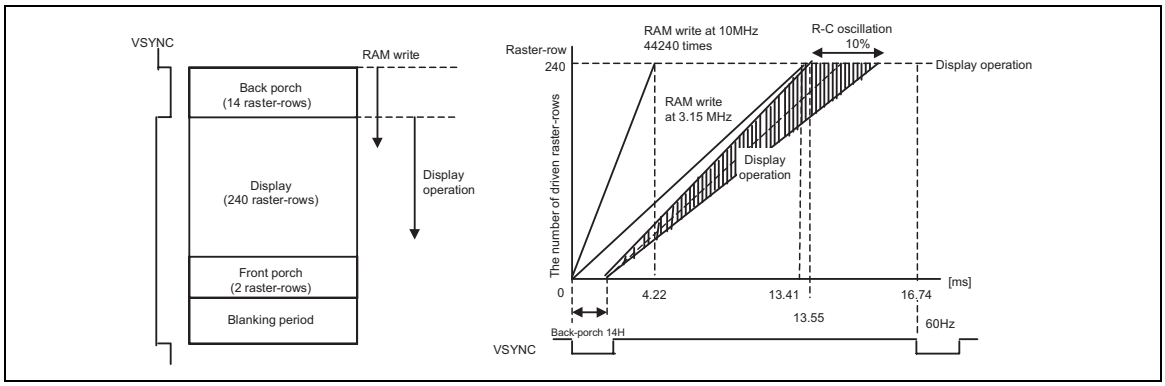
As the causes of fluctuations, the above example takes the variation in the LSI fabrication and the room temperature into account. Other possible causes of fluctuations, such as variation in the external resistors or the voltage change are not considered in the above example. It is necessary to make a setting with enough margins to include the allowances for these factors.

Minimum speed for RAM writing [Hz]
> 176 × 240 / {((14 + 240 - 2) raster-rows × 16 clock) / 300 kHz} = 3.14 MHz

In this case, RAM write is performed in synchronization with the falling edge of VSYNC.

When the data for one frame are written to RAM completely, there must be more than 2 raster-rows of margin before the raster-row starts to drive for the next frame.

By writing data to RAM on the falling edge of VSYNC at the speed of 3.14 MHz or more, the data for the whole screen on RAM are overwritten before the display operation starts. Accordingly, the flicker due to updating moving picture data can be avoided while displaying a moving picture.

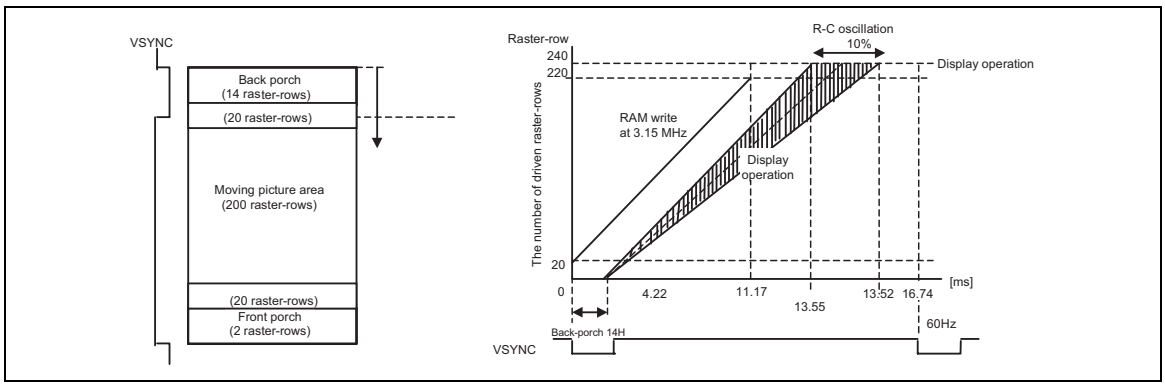


Operation through VSYNC interface

Notes to the VSYNC interface

1. The aforementioned example of calculation is just a result of calculation. In the actual settings, causes for the fluctuations such as internal clocks should be taken into consideration. It is necessary to make a setting for RAM write speed with enough margins.

2. The aforementioned example of calculation is the value in case of writing over the entire screen. Limiting the area for the moving picture display will create more margins for the RAM write speed.



Limiting moving picture display area

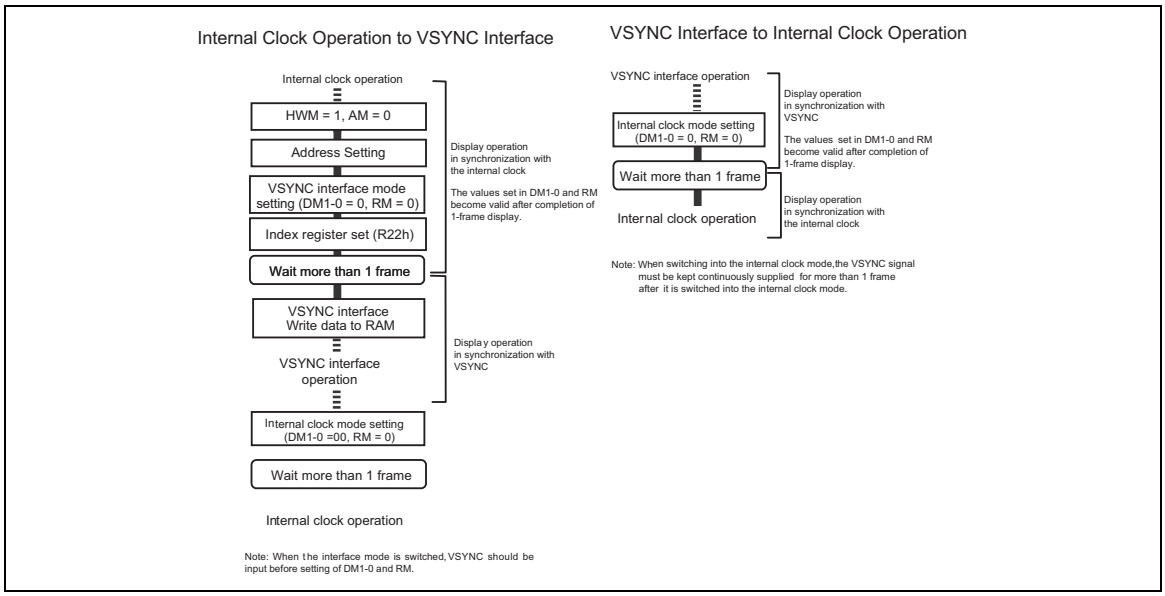
3. A front porch period continues after the completion of 1 frame display and until the next input of VSYNC.

4. The transition between the internal clock operation mode (DM1-0 = 00) and the VSYNC interface mode becomes effective after displaying one frame made during instruction setting.

5. In the VSYNC interface mode, the partial display, vertical scroll, and interlaced drive functions are not available.

6. In the VSYNC interface mode, set AM to 0 to transmit display data in the aforementioned method.

7. In the VSYNC interface mode, write display data to RAM in the high speed write mode (HWM = 1)



Transition flow between VSYNC and internal clock operation modes

External Display Interface

The following interfaces are available as the external display interface (RGB interface). The interface is selected by setting RIM1-0 bits. RAM is accessible through the RGB interface.

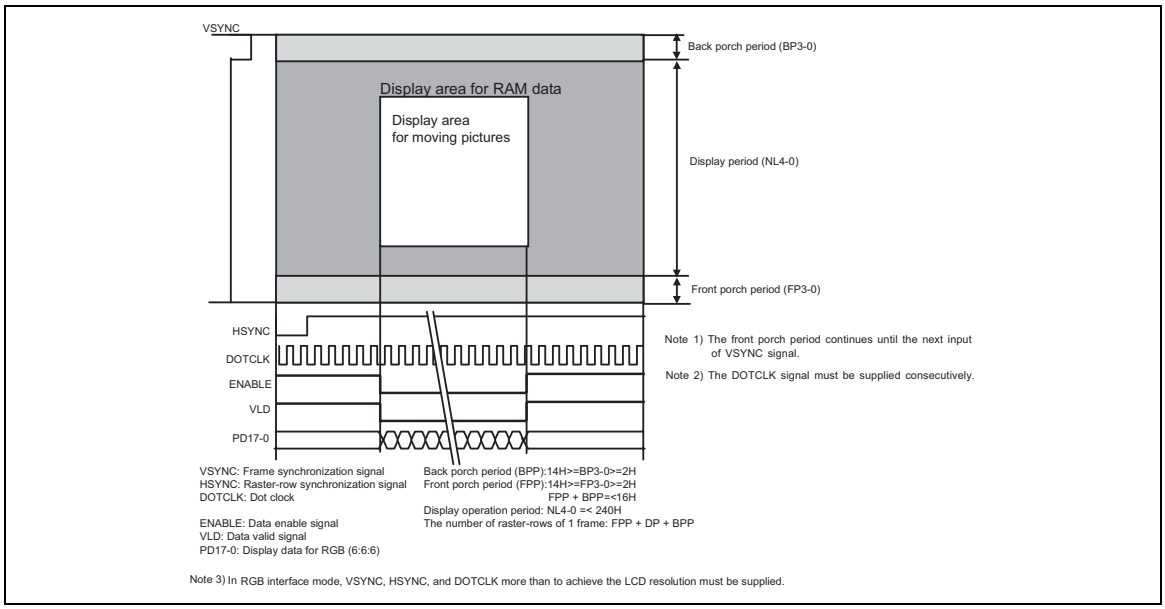
RIM bits setting and RGB interface

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface	PD17-12
1	1	Setting disabled	

Note 1) The use of multiple interfaces simultaneously is not possible.

RGB interface

Through the RGB-I/F, the display operation is performed in synchronization with VSYNC, HSYNC, and DOTCLK. The RGB interface enables data transmission with low power consumption by overwriting the area that needs update in high-speed write mode in combination with the window address function. The front and back porches must be set before and after the display period.



RGB interface

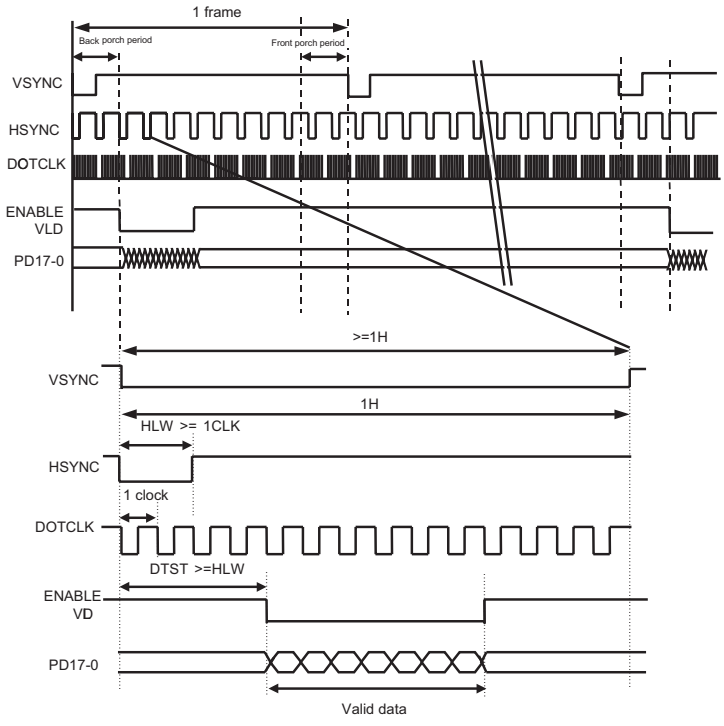
VLD and ENABLE signals

The relationship with the VLD and ENABLE signals is as follows. With the ENABLE signal, the addresses are not updated during data write, while with the VLD signal, the addresses are updated during data write when the ENABLE is "Low". The polarity of the ENABLE signal is inverted by the setting of EPL bit.

EPL	ENABLE	VLD	RAM Write	RAM Address
0	0	0	Valid	Updated
0	0	1	Invalid	Updated
0	1	*	Invalid	Unchanged
1	0	*	Invalid	Unchanged
1	1	0	Valid	Updated
1	1	1	Invalid	Updated

RGB interface timing

The timing chart of 16/18-bit RGB interfaces is as follows.

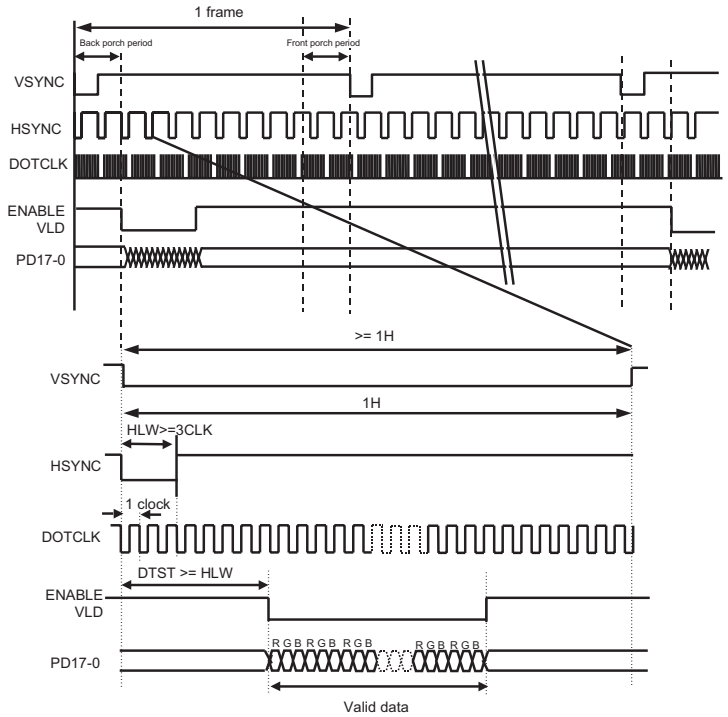


VLW: the period in which VSYNC is low level
HLW: the period in which HSYNC is low level
DTST:the set up time for data transmission

Note: Data to be displayed must be written in the high-speed write mode (HWM = 1) in RGB I/F mode.

16-/18-bit RGB Interface Timing

The timing chart of 6-bit RGB interface is as follows.



VLW: the period in which VSYNC is low level
HLW: the period in which HSYNC is low level
DTST: the set up time for data transmission

Note 1) In 6-bit interface.mode, one pixel, which consists of R,G, and B, must be transmitted in synchronization with 3 DOTCLKs.
Note 2) VSYNC, HSYNC, EVABLE, DOTCLK, VLD, and PD17-2 should be all transmitted by three clocks.
Note 3) Data to be displayed must be written in the high-speed write mode (HWM =1) in RGB I/F mode.

6-bit RGB Interface Timing

Moving picture display

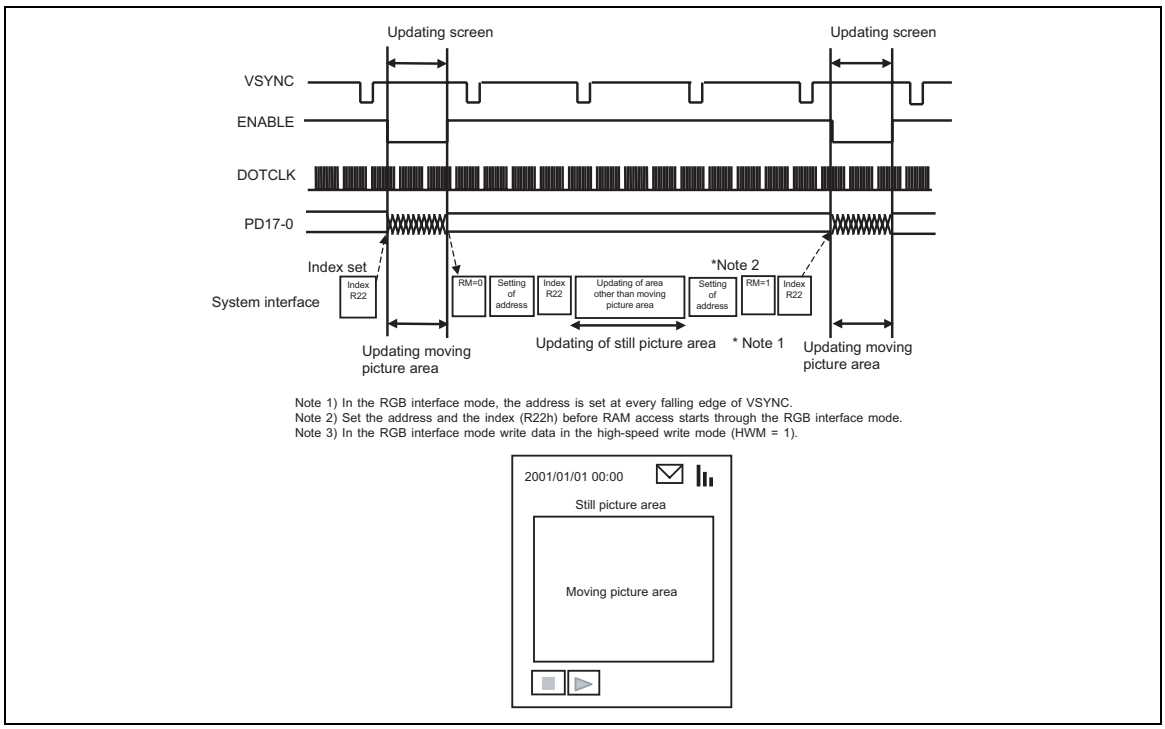
The HD66787 incorporates the RGB interface to display moving pictures and RAM to store display data, which provides the following merits in displaying moving pictures.

- The window address function enables the transfer of only the data for the moving picture area.
- The high-speed write modes enables high-speed access to RAM with low power consumption
- Only transmitting the data that are written over the moving picture area.
- By reducing the amount of data transmission, the power consumption of the whole system is reduced.
- In combination with a system interface the still picture area, such as an icon, can be updated while displaying moving pictures.

RAM access through system interface in RGB-I/F mode

RAM is accessible through a system interface in the RGB-I/F mode. In the RGB interface mode, data are being written to RAM in synchronization with the DOTCLK input while the ENABLE is "Low". When writing data to RAM through the system interface, it is necessary to set ENABLE to "High" to stop data write through the RGB-I/F. Setting RM = 0 allows RAM access through the system interface. When reverting to the RGB interface mode, wait a write/read bus cycle. Then, set RM = 1 and the index to R22h to start RAM access though the RGB-I/F. When the RAM writes through the RGB and system interface conflicts, it is not guaranteed that the data are properly written to RAM.

The following is an example of moving picture display through the RGB-I/F and updating still picture area through the system interface.

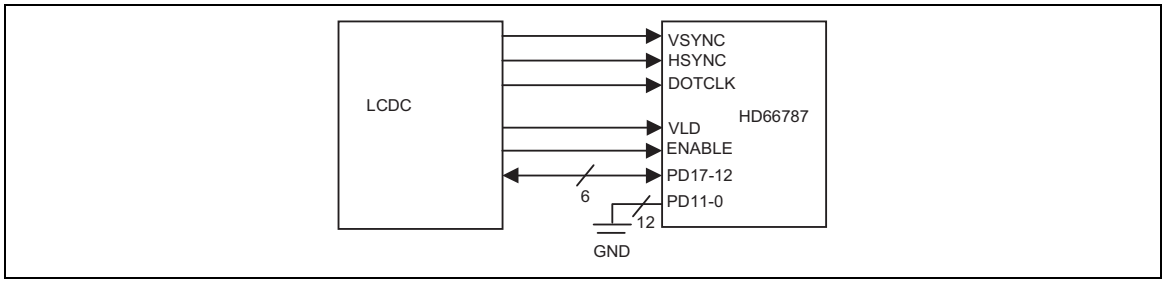


Updating Still Picture Area during Displaying Moving Picture

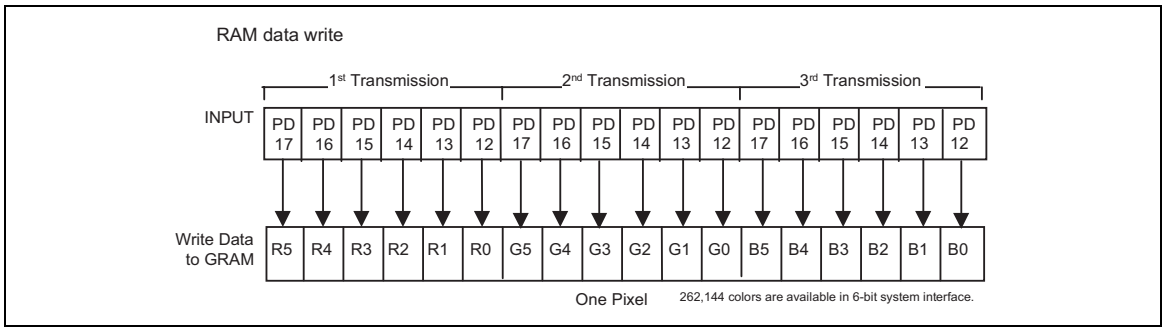
6-bit RGB interface

The 6-bit RGB interface is selected by setting RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through 6-bit RGB data bus (PD17-12) according to data valid signal (VLD), and the data enable signal (ENABLE). Unused pins (PD11 to 0) must be fixed to either IOVcc or GND level.

The instructions are set only through a system interface.



6-bit RGB interface

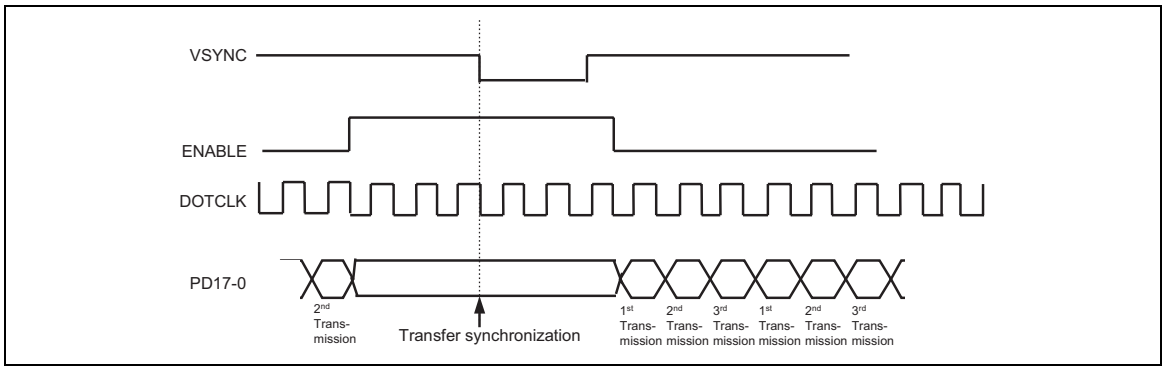


Data format for 6-bit interface

Data transmission synchronization in 6-bit RGB interface mode

The HD66787 incorporates a transmission counter to count the first, second, third data transmissions in the 6-bit RBG interface mode. The transmission counter is reset to the first transmission on the falling edge of VSYNC. When a discrepancy occurs in the transmission of first, second and third data, the counter is reset to the first data transmission at the start of each frame (on the falling edge of VSYNC) and the data transmission restarts in the correct order from the next frame. In case of displaying moving pictures, which requires consecutive data transfer, this function minimizes the effect from the discrepancy in the data transmission and makes it easy to return to the normal display.

The internal display operation is executed by pixel. Note that each DOTCLK input must correspond to a pixel. Otherwise data transmission discrepancies will occur and affect the displays of the current and ensuing frames.

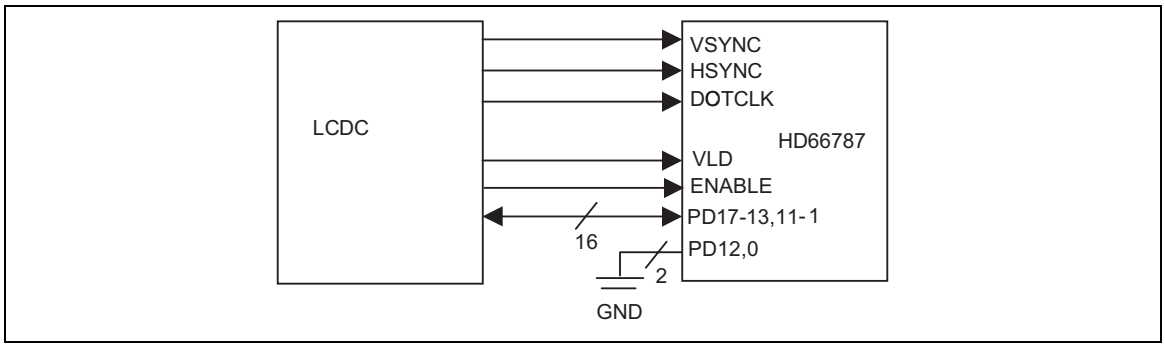


6-bit data transmission synchronization

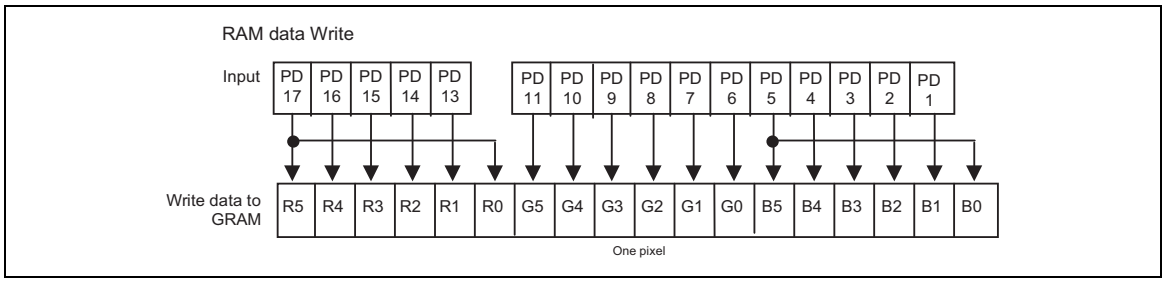
16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM1-0 bits to 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through 16-bit RGB data bus (PD17-13, 11-1) according to the data valid signal (VLD), and the data enable signal (ENABLE).

The instructions are set only through system interface.



16-bit RGB interface

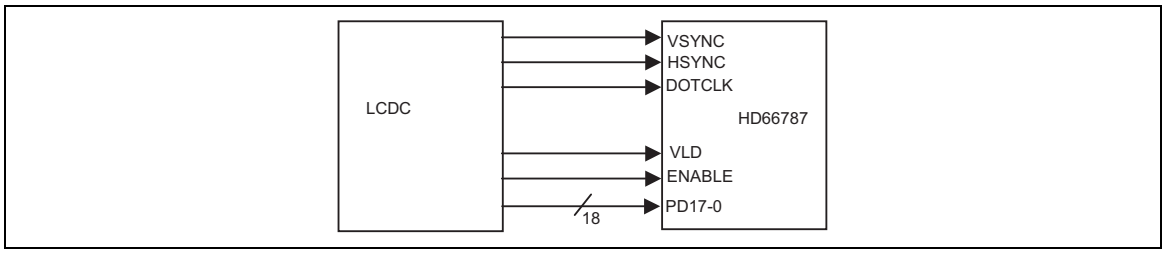


Data format for 16-bit interface

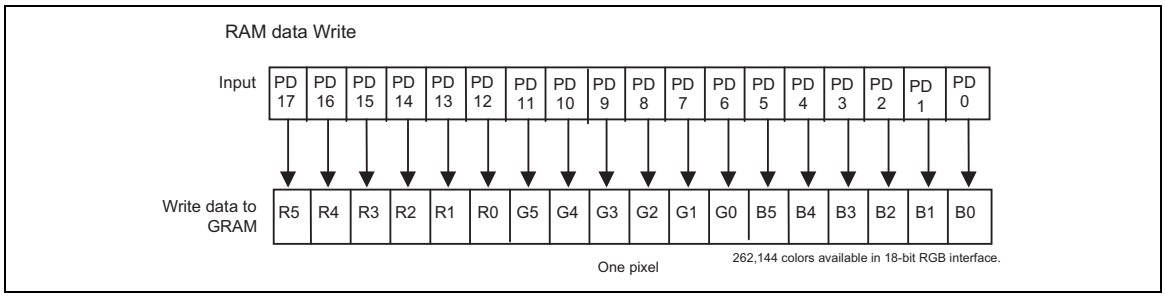
18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM1-0 bits to 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through 18-bit RGB data bus (PD17-0) according to the data valid signal (VLD), and the data enable signal (ENABLE).

The instructions are set only through a system interface.



18-bit RGB interface



Data format for 18-bit interface

Notes to the external display interface

1. While an external display interface is selected, the following functions are not available.

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Graphics operation function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied consecutively during display operation through the RGB-I/F.

3. When setting NO1-0, SDT1-0, and EQ1-0 bits in the RGB-I/F mode, the reference clock is the DOTCLK, not the internal operation clock.

4. In the 6-bit RGB-I/F mode, RGB (pixels) data are transmitted by three clocks. The data transmission, therefore, should be made by RGB.

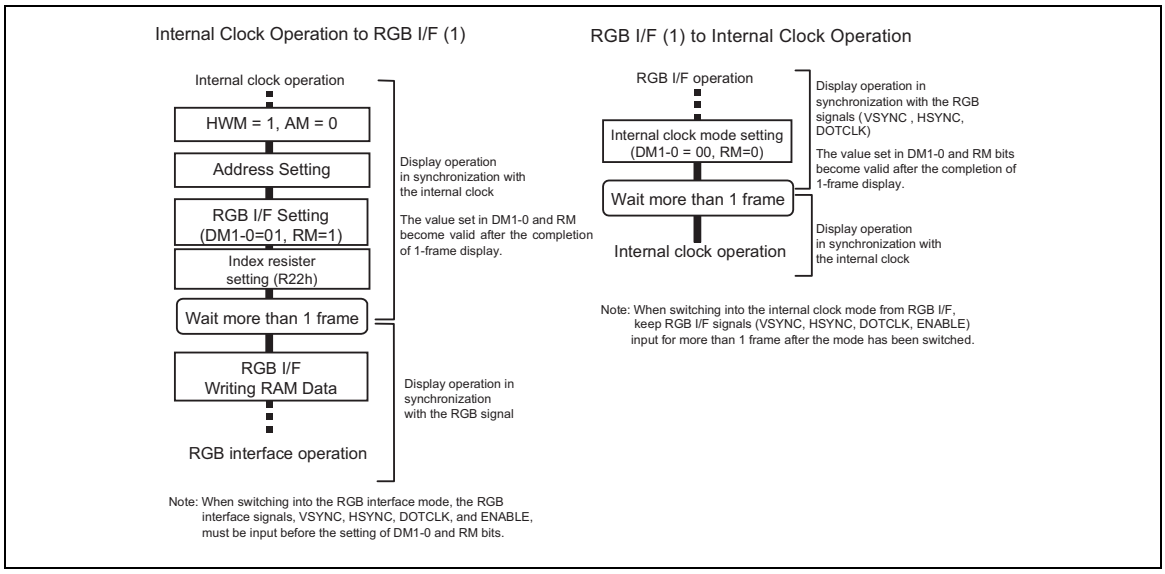
5. In the 6-bit RGB-I/F mode, the interface signals, VSYNC, HSYNC, DOTCL, ENABLE, VLD, and PD17-0, should be set in RGB (pixels) in convenience for transmitting RGB pixels.

6. The transitions between the internal operation mode and external display interface should be made according to the mode switching sequence below.

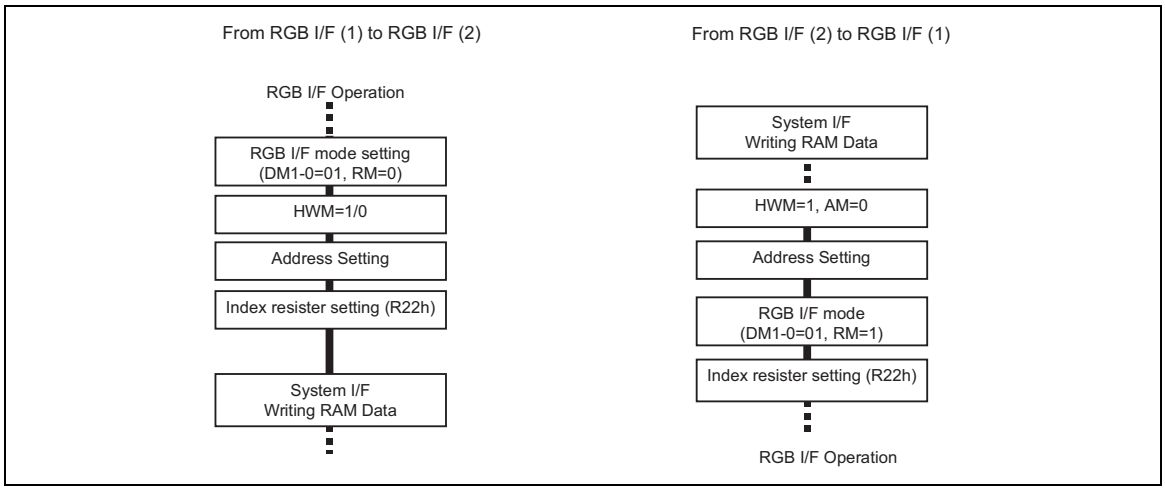
7. In the RGB-I/F mode, the front porch period continues after displaying one frame data until the next VSYNC signal input.

8. In the RGB-I/F mode, the data must be written in the high-speed write mode (HWM = 1).

9. In the RGB-I/F mode, the address is set every frame on the falling edge of VSYNC.



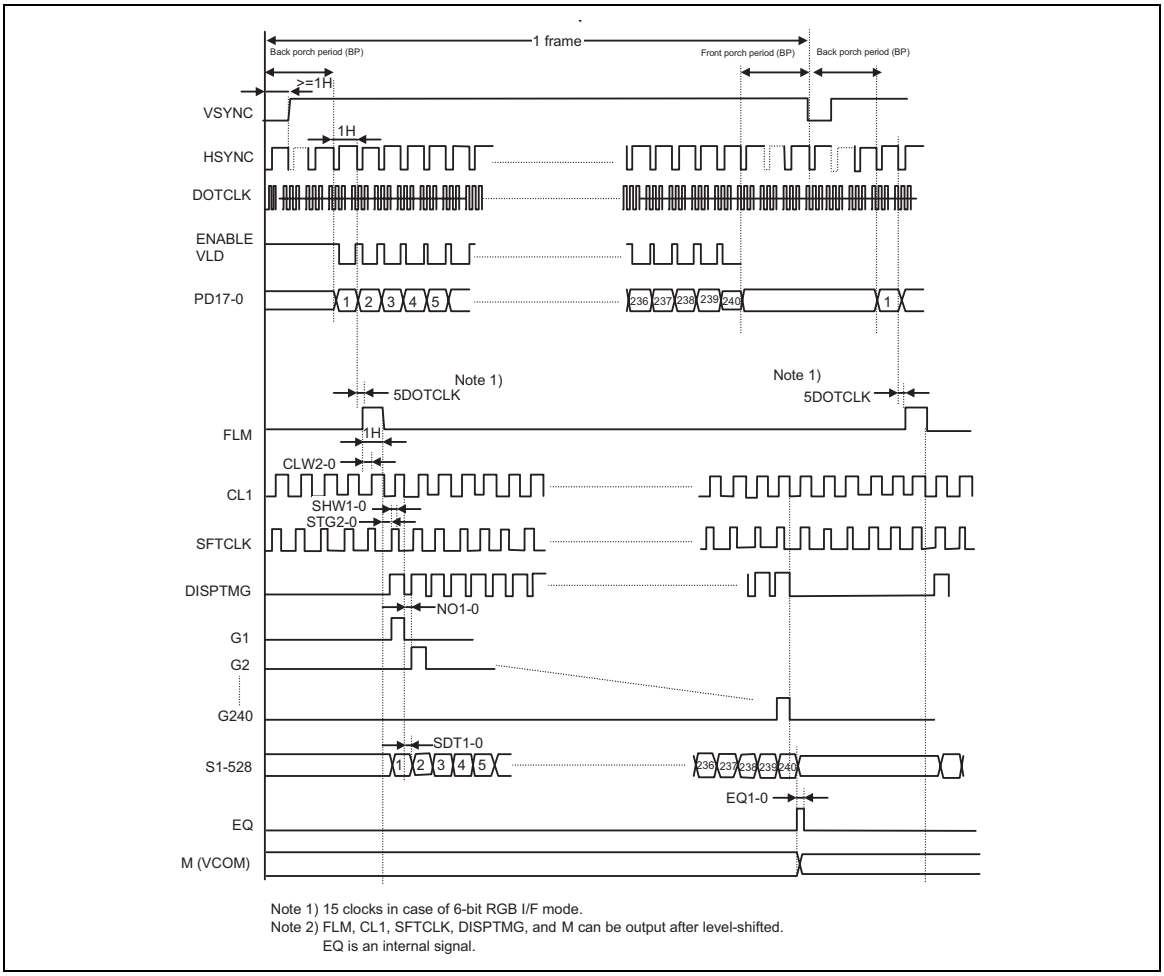
Transition between the Internal Clock Operation Mode and RGB Interface Mode



RAM data write sequence through system interface in RGB-I/F mode

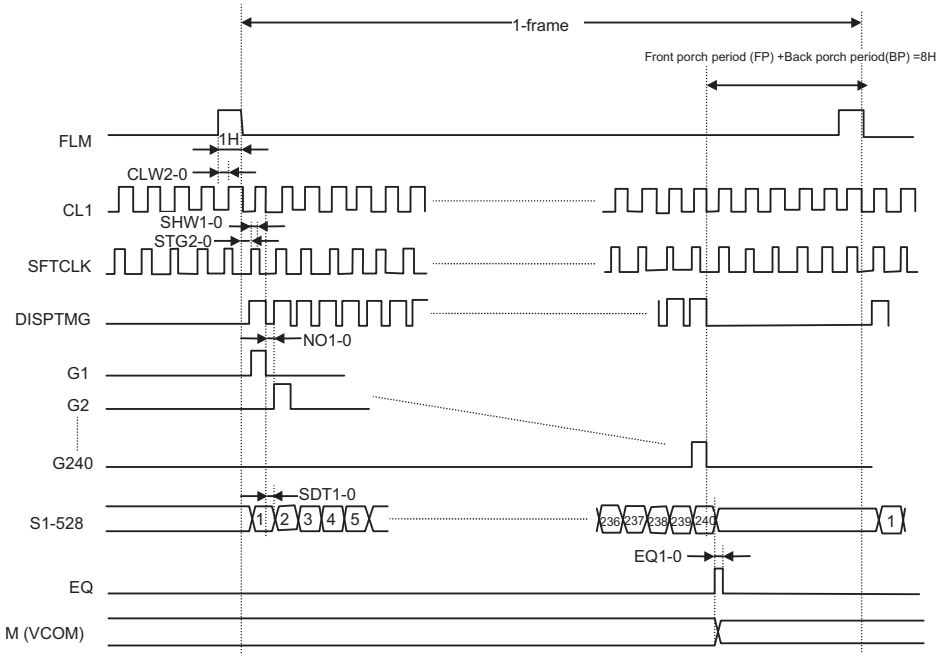
Timing Interfacing with Liquid Crystal Panel Signals

The relationship between RGB I/F signals and the liquid crystal panel signals in the RGB I/F mode is as follows (TG0 = “0”).



Relationship between RGB I/F signal and the liquid crystal panel signal (TG0 = “0”)

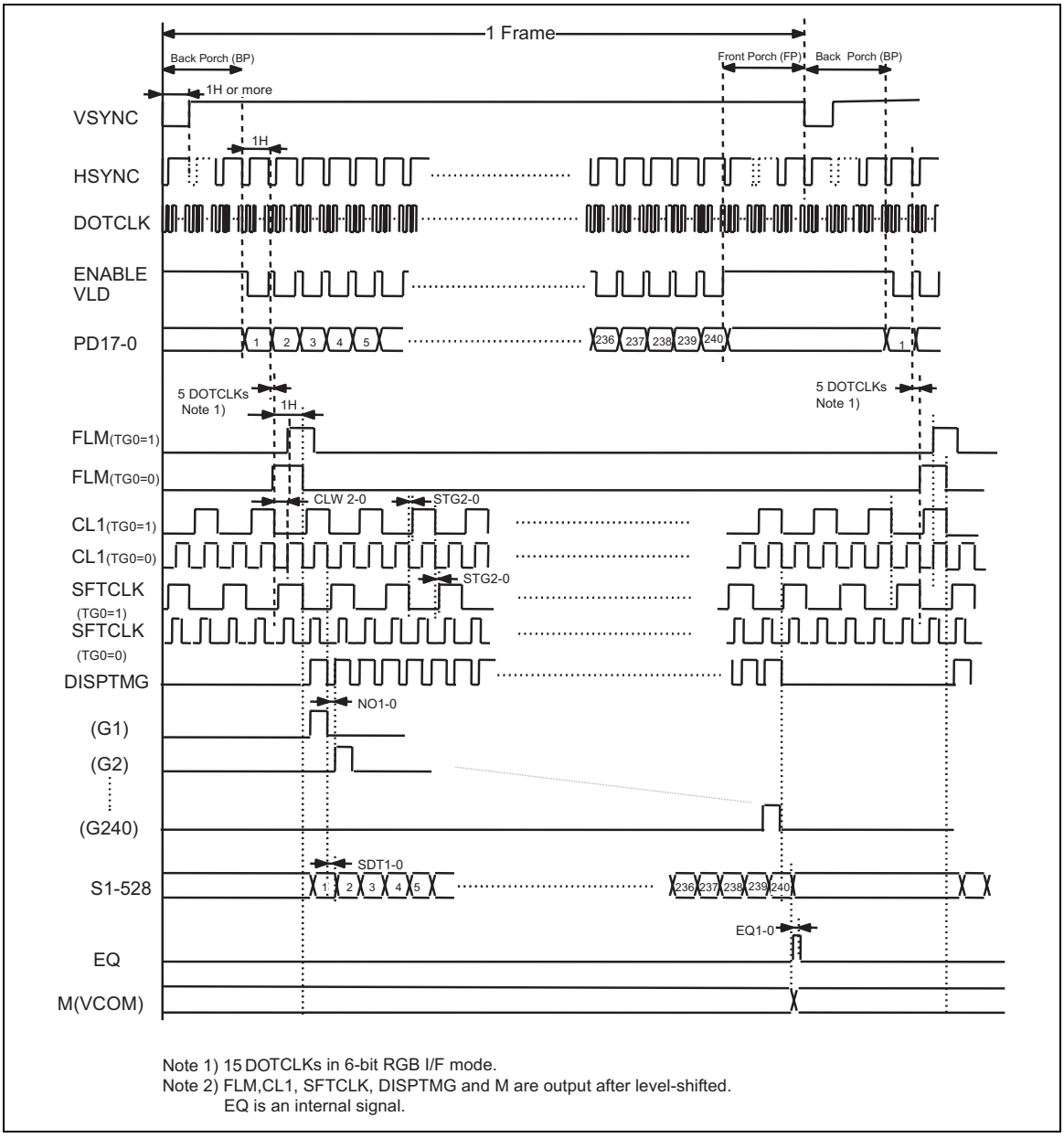
The timing interfacing with the liquid crystal panel signals in the internal clock operation mode is as follows (TG0 = “0”).



Note 1) 15 clocks in case of 6-bit RGB I/F mode.
Note 2) FLM, CL1, SFTCLK, DISPTMG, and M can be output after level-shifted.
EQ is an internal signal.

Interfacing with the liquid crystal panel signals in the internal clock operation mode (TG0 = “0”)

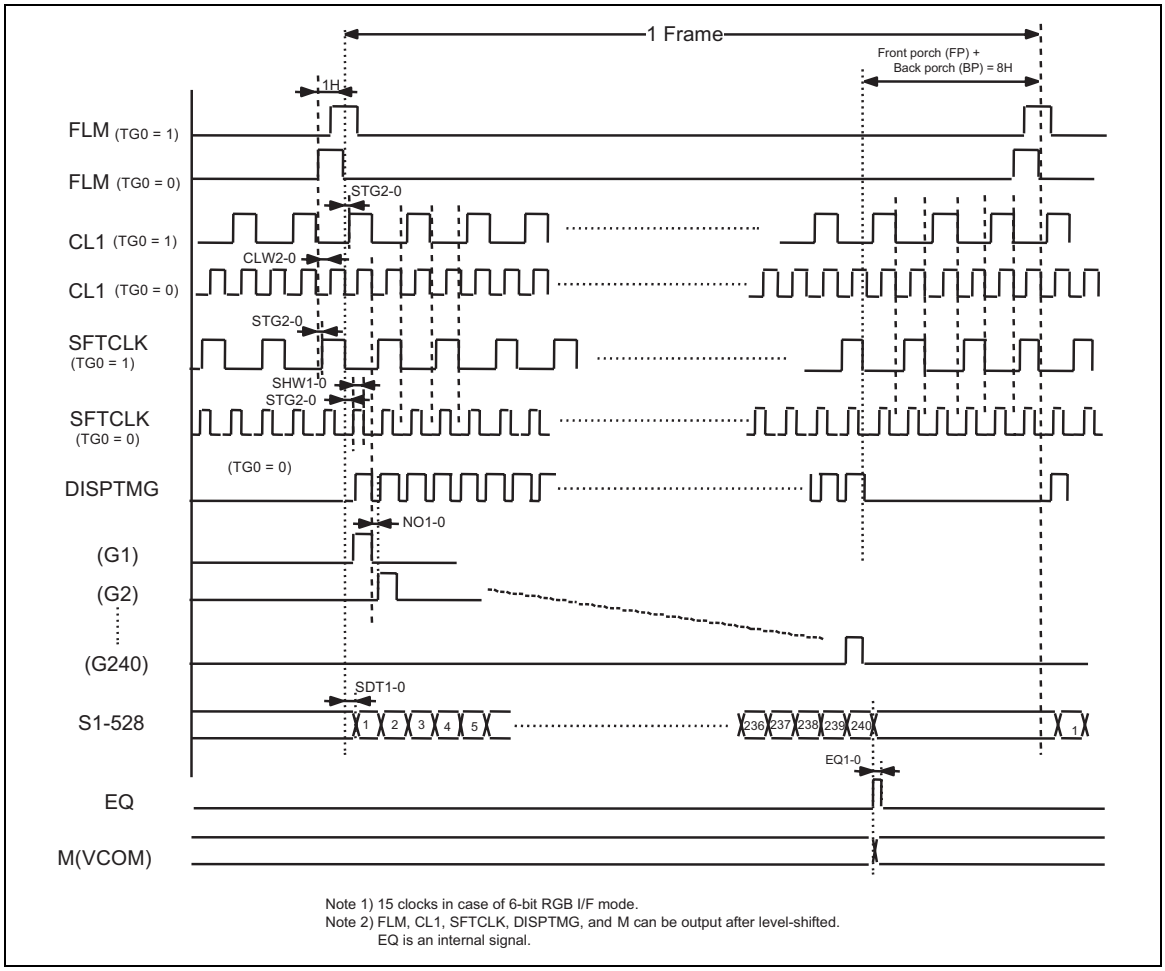
The timing interfacing with the liquid crystal panel signals in RGB interface mode is as follows (TG0 = "1").



Note 1) 15 DOTCLKs in 6-bit RGB I/F mode.
Note 2) FLM,CL1, SFTCLK, DISPTMG and M are output after level-shifted.
EQ is an internal signal.

Interfacing with the liquid crystal panel signals in RGB interface mode (TG0 = "1")

The timing interfacing with the liquid crystal panel signals in the internal clock operation mode is as follows (TG0 = "1").



Interfacing with the liquid crystal panel signals in the internal clock operation mode (TG0 = "1")

Register settings

CL1 signal: "Low" width

CLW 2	CLW 1	CLW 0	CL1 signal : pulse width during "Low"	
			internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	0	1 clock	8 clocks
0	0	1	2 clocks	16 clocks
0	1	0	3 clocks	24 clocks
0	1	1	4 clocks	32 clocks
1	0	0	5 clocks	40 clocks
1	0	1	6 clocks	48 clocks
1	1	0	7 clocks	56 clocks
1	1	1	8 clocks	64 clocks

Note 1) The number of clocks is counted from the falling edge of CL1 signal.

EQ signal: "High" width

EQ 1	EQ 0	EQ signal : pulse width during "High"	
		internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	No equalize	No equalize
0	1	1 clock	8 clocks
1	0	2 clocks	16 clocks
1	1	3 clocks	24 clocks

Source output delay

STD 1	STD 0	Source output delay	
		internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Note 1) The amount of source output delay is measured from the falling edge of CL1 signal.

Gate output non-overlap

STD 1	STD 0	Gate output non-overlap	
		internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	0 clock	0 clocks
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks

Note 1) The amount of gate output non-overlap is measured from the falling edge of CL1 signal.

SFTCLK signal: pulse output position

STG 2	STG 1	STG 0	SFTCLK signal : pulse output position	
			internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	0	0 clock	0 clock
0	0	1	1 clock	8 clocks
0	1	0	2 clocks	16 clocks
0	1	1	3 clocks	24 clocks
1	0	0	4 clocks	32 clocks
1	0	1	5 clocks	40 clocks
1	1	0	6 clocks	48 clocks
1	1	1	7 clocks	56 clocks

Note 1) The number of clocks is counted from the falling edge of the CLT signal.

SFTCLK signal: purse width during “High”

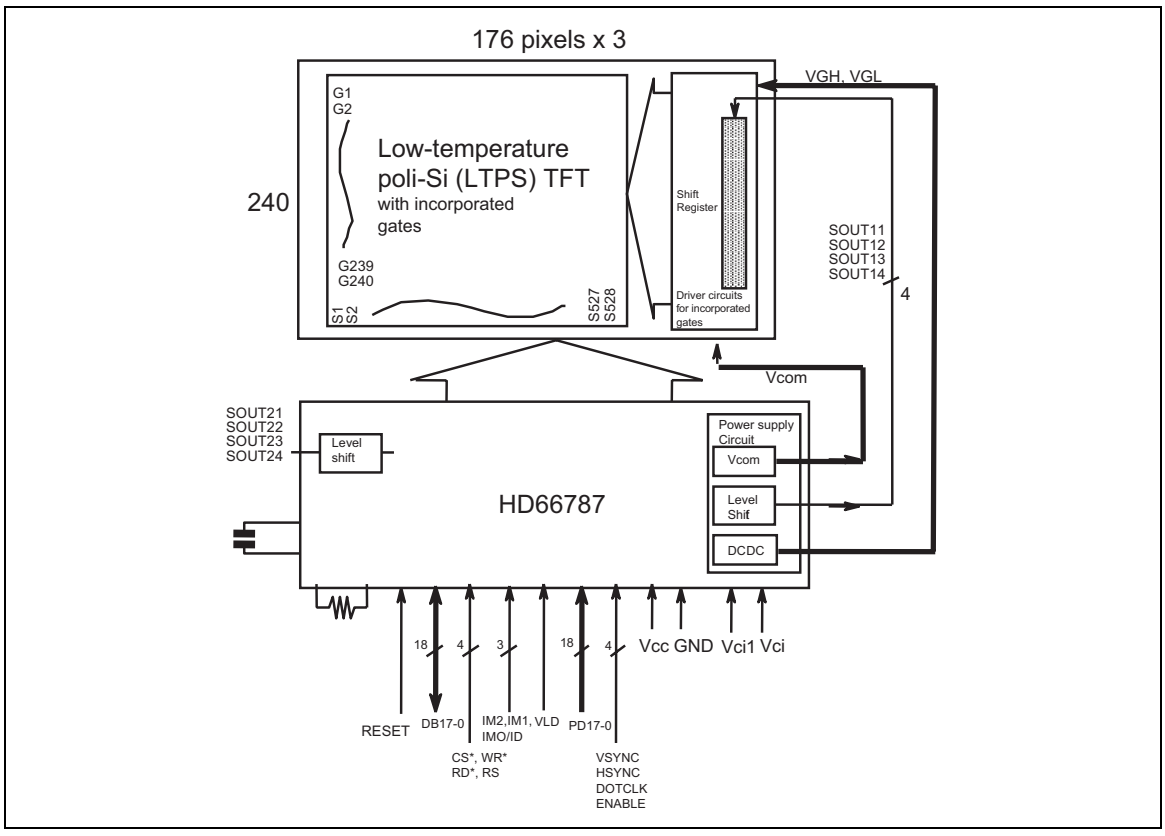
SHW 1	SHW 0	SFTCLK signal : purse width during “High”	
		internal operation (synchronized with the internal operating clock)	RGB interface operation (synchronized with DOTCLK)
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Low-temperature poli-Si TFT Panel Control

HD66787 outputs timing signals (FLM, CL1, SFTCLK) for controlling low-temperature poli-Si TFT (LTPS-TFT) panels with incorporated gates. By level-shifting the voltage of FLM, CL1, SFTCLK, and DISPTMG, the LTPS-TFT panel with incorporated gates becomes easily controllable.

■ Source drivers (HD66787)

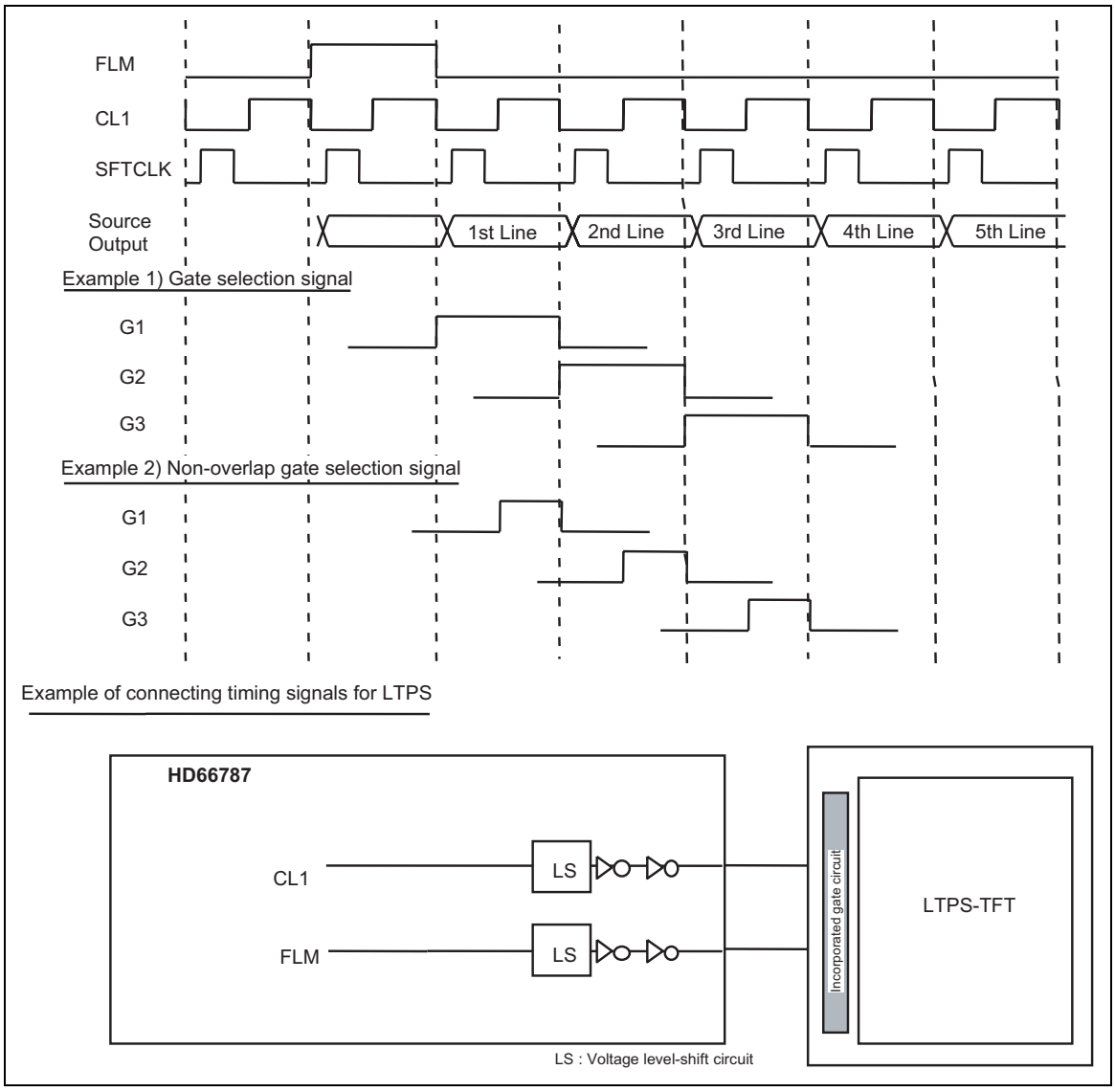
• Output control timing signals (internal signal)	FLM (Frame heading pulse) CL1 (Line cycle signal): "Low" width variable with CLW2-0 bits SFTCLK (Line cycle signal): output timing variable with STG2-0, SHW1-0 bits
• Level-shift output	VGH ~ VGL amplitude
• ports for LTPS	SOUT 11, SOUT 12, SOUT 13, SOUT 14, SOUT 21, SOUT 22, SOUT 23, SOUT 24



System configuration

■ Output timing (HD66787)

HD66787 outputs timing signals (FLM, CL1, SFTCLK) for controlling low-temperature poli-Si TFT (LTPS-TFT) panels with incorporated gates. The output timing of CL1 can be adjusted by instructions for controlling LTPS-TFT interface. Set an optimum timing for the configuration of gate circuits incorporated in the LTPS-TFT panel in use.



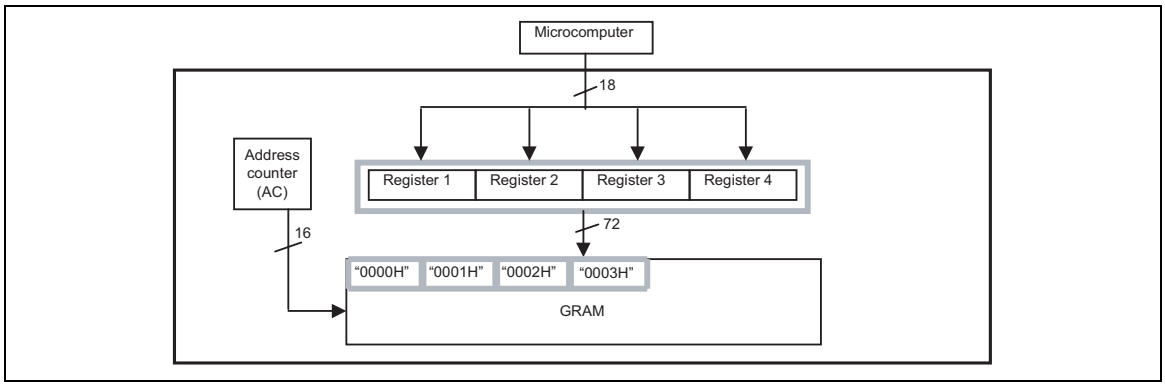
LTPS-TFT control

Note 1) Some gate circuit configuration incorporated in the LTPS-TFT may not allow the use of certain functions with HD66787.

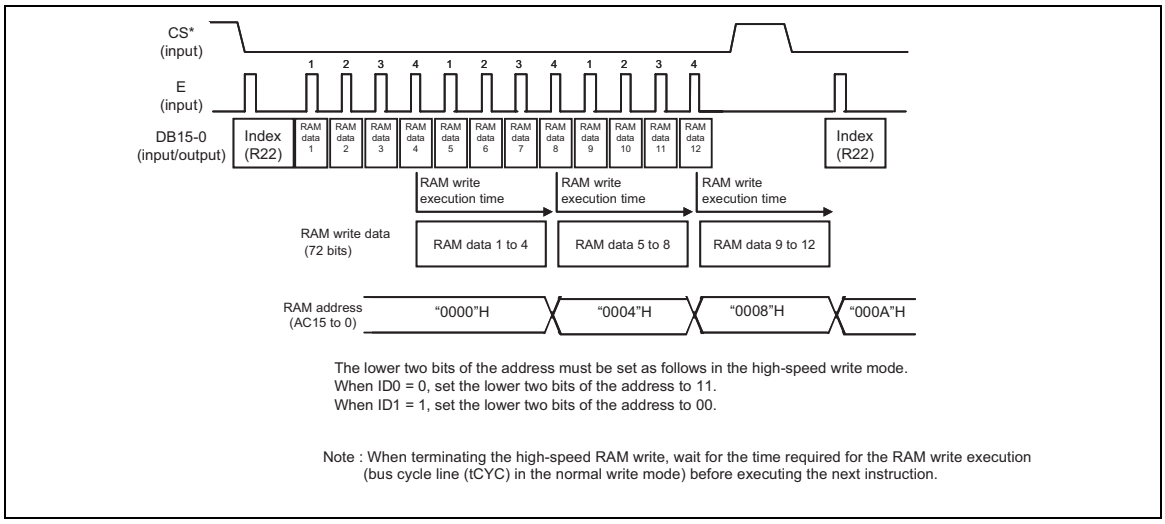
High-Speed Burst RAM Write Function

The HD66787 incorporates high-speed burst RAM-write function, which writes data to RAM in one-fourth the access time required for a standard RAM-write operation. This function is especially useful for applications which require the high-speed rewrite of the display data such as display of colored moving picture and so on.

In the high-speed RAM write mode (HWM), data to write to RAM is temporarily stored to the internal register of HD66787. The data storage in the register is executed by word. When the data storage operation is executed 4 times, all data stored in the register are written to RAM at once. While the data is being written from the register to RAM, another set of data is being written to the register. This function enables high-speed and consecutive RAM write, which are required in displaying moving pictures and so on.



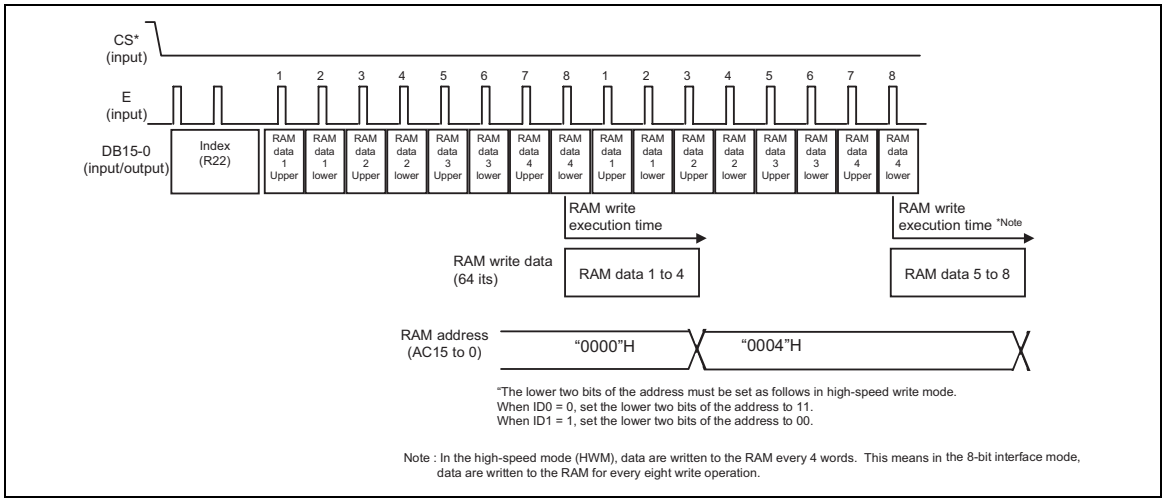
Operational flow of High-Speed Burst RAM Write



The lower two bits of the address must be set as follows in the high-speed write mode.
When ID0 = 0, set the lower two bits of the address to 11.
When ID1 = 1, set the lower two bits of the address to 00.

Note : When terminating the high-speed RAM write, wait for the time required for the RAM write execution (bus cycle line (tCYC) in the normal write mode) before executing the next instruction.

High-Speed Consecutive Write to RAM



Operation of High-Speed Consecutive Writing to RAM (8-Bit Interface)

Notes to the high-speed RAM write mode

1. The logical/compare operations are not available.

2. The RAM write operation is executed every four words. Set the lower 2 bits of the addresses as follows when setting addresses.

   *When ID0=0, the lower two bits in the address must be set to 11 before RAM write.
   *When ID0=1, the lower two bits in the address must be set to 00 before RAM write.

3. The RAM write operation is executed every four words. If RAM write operation is terminated before all four-word data is written to RAM, the last data will not be written to RAM.

4. When the index register is set to R22H (RAM data write), the first RAM write operation is always executed. In this case, RAM data read is not operable simultaneously. During RAM read, set the HWM to 0.

5. The high-speed RAM write mode is not compatible with the normal RAM write mode. When the mode must be switched to the other, make a new address set before starting RAM write.

6. When writing data in high speed RAM write mode within the range specified with the window address, some window-address range may require dummy write operation. See "High-Speed RAM Write with Window Address Function".

Comparison of Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
Logical operation function	Available	Not available
Compare operation function	Available	Not available
BGR function	Available	Available
Write mask function	Available	Available
RAM address set	Specified by one word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Read by one word	Not available
RAM write	Write by one word	Dummy write operations may be required depending on the specified window-address range
Window address	Set by one word	Horizontal range(HSA/HSE): more than four words Number of horizontal writing : 4N (N>=2)
External display interface	Available	Available
AM Setting	AM = 1/0	AM = 0

High-Speed RAM Write with Window Address Function

To rewrite the data in an arbitrary rectangular area of RAM consecutively in high speed, the number of RAM access should be made 4 multiple times. Accordingly some window-address range may require dummy write operation to make the RAM access 4 multiple times. The number of dummy write is set when setting the window address as follows.

The horizontal window-address range specifying bits (HSA1-0, HEA1-0) specify the number of dummy write operations executed at the start and end of the data to write to RAM. The total RAM access must be 4 multiple times per line.

Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations inserted
0	0	0
0	1	1
1	0	2
1	1	3

Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

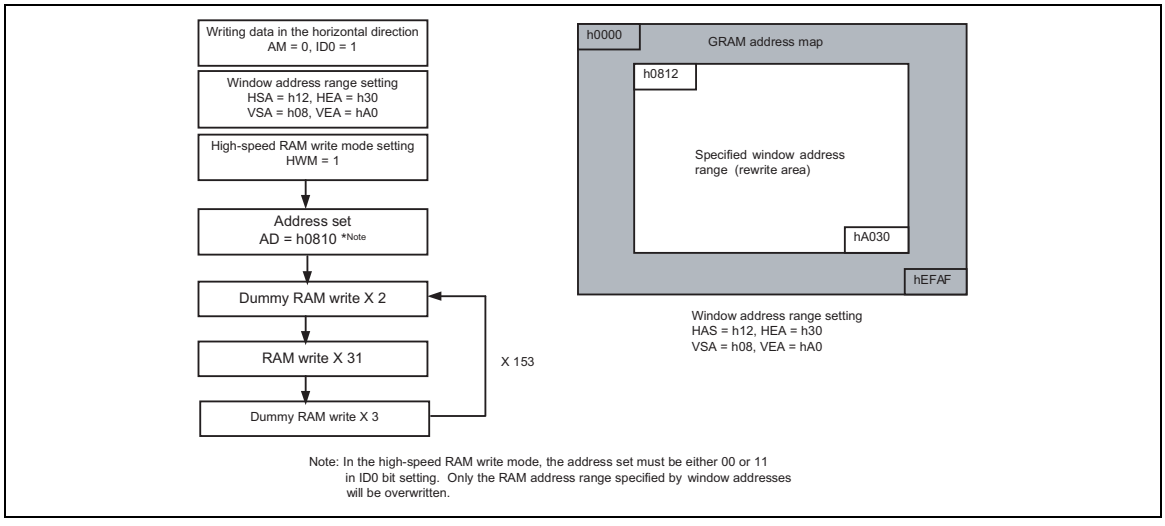
HEA1	HEA0	Number of Dummy Write Operations Inserted
0	0	3
0	1	2
1	0	1
1	1	0

The number of RAM access when writing data in the horizontal direction must be made 4 × N times by including the dummy writes.

Horizontal RAM write = start dummy write + write data + end dummy write = 4 × N (times)

An example of RAM write in high speed RAM write mode with the window address is as follows.

The RAM data in the specified window-address range is written over consecutively in high speed by inserting two dummy writes at the start of the line and three dummy writes at the end of the line. The number of dummy writes is specified with the window-address range specifying bits. In this case, set HSA1-0 to 10, HEA1-0 to 00.



High-Speed RAM Write with Window Address Function

Window Address Function

The window address function enables consecutive data write within the rectangular window-address area on the on-chip GRAM, which is specified with horizontal address registers (start: HSA7-0, end: HEA 7-0) and vertical address registers (start: VSA7-0, end: VEA7-0).

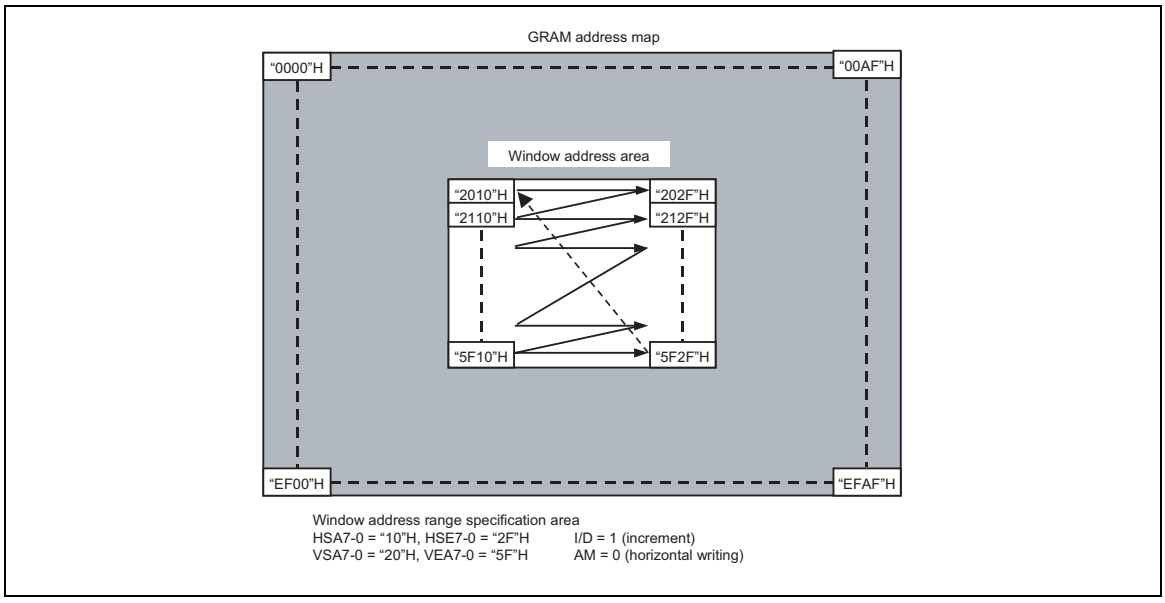
The address transition direction is determined with AM bits (either increment or decrement). Accordingly, the data, including picture data, are written consecutively without taking the data wrap position into consideration.

The window-address range must be specified within the GRAM address area. An address set must be set within the window-address range.

[Condition on setting window-address range]
(Horizontal direction) 00H ≤ HSA7-0 ≤ HSA7-0 ≤ AFH
(Vertical direction) 00H ≤ VSA7-0 ≤ VEA7-0 ≤ EFH

[Condition on making an address set within the window-address range]
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0
VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM write mode, the lower two bits of the address must be set as follows.
ID0=0: The lower two bits of the address must be set to 11.
ID0=1: The lower two bits of the address must be set to 00.



Address transition direction in specified window-address range

Graphics Operation Function

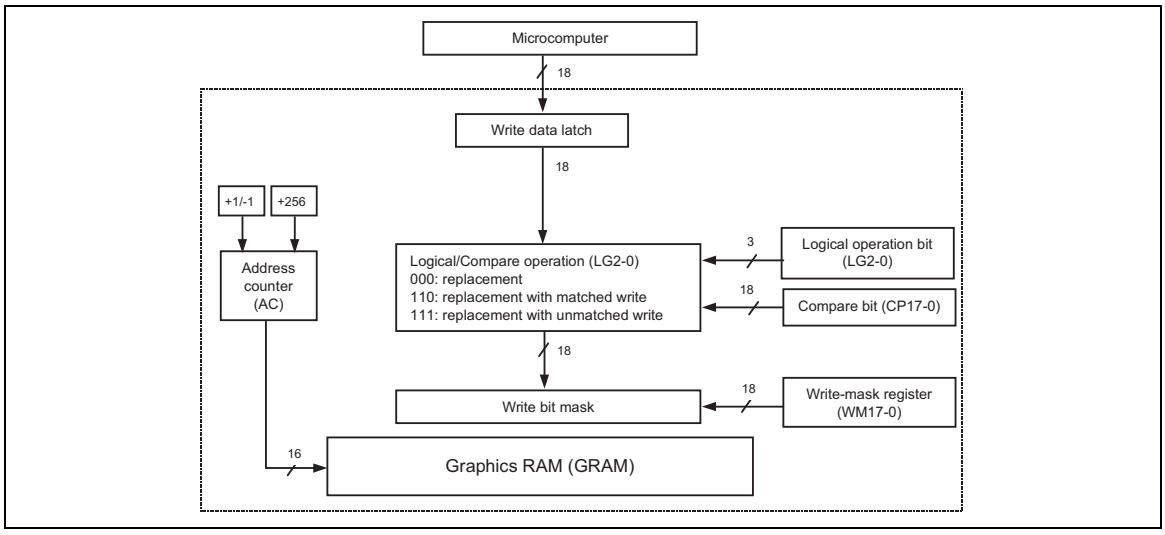
The HD66787 greatly reduces the load on the graphics-processing software in the microcomputer with the 18-bit bus architecture and the graphics bit operation. The graphics bit operation includes:

1. The write data mask function that selectively rewrites some bits of 18-bit write data.
2. The conditional rewrite function that compares the write data and the compare bit data and writes the data sent from the microcomputer only when the conditions are satisfied.

The graphics bit operation is controlled by setting bits in the entry mode register and RAM-write-data mask register, and the write operation from the microcomputer.

Graphics Operation

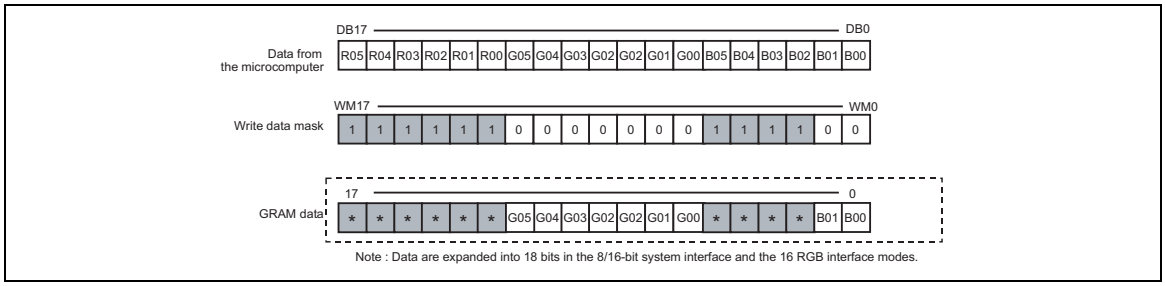
	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement
Write mode 2	0/1	1	000	Vertical data replacement
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement
Write mode 4	0/1	1	110 111	Conditional vertical data replacement



Graphics operation flow

Write-data Mask Function

The HD66787 expands the 16-bit data sent from the microcomputer into the 18-bit data. In the18-bit interface mode, data are not expanded. The write data mask function of the HD66787 controls the write operation of the 18-bit data from the microcomputer to GRAM by bit. The write data mask function write data in the bits whose corresponding bits in the write data mask resister (WM17–0) are assigned with "0" and does not write data in the bits whose corresponding bits in the write data mask register (WM17–0) are assigned with "1", and the corresponding data in GRAM are not overwritten but retained. This function is useful when only one-pixel data are rewritten or a particular color in the display is selectively changed.

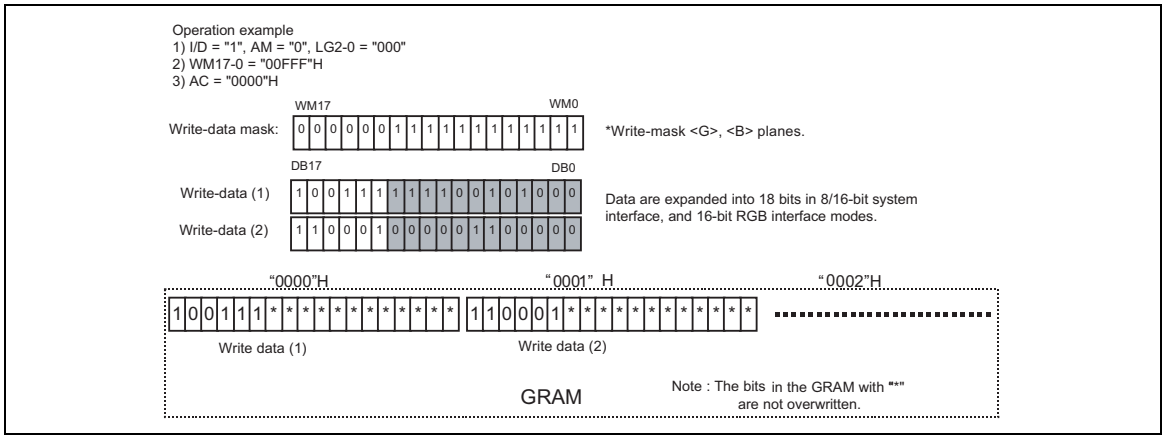


Write data mask function

Graphics Operation Processing Examples

1. Write mode 1: AM = 0, LG2–0 = 000

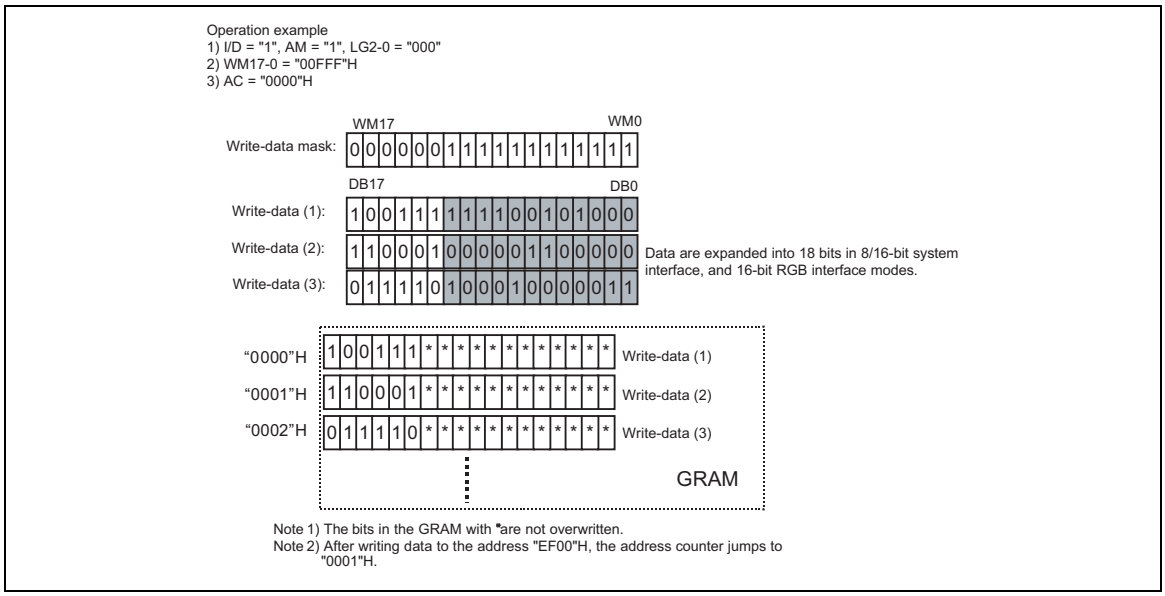
This mode is used when data are horizontally written in high speed mode. It is also used to initialize the graphics RAM (GRAM) or to draw a line horizontally. The write-data mask function (WM17–0) is also available in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.



Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

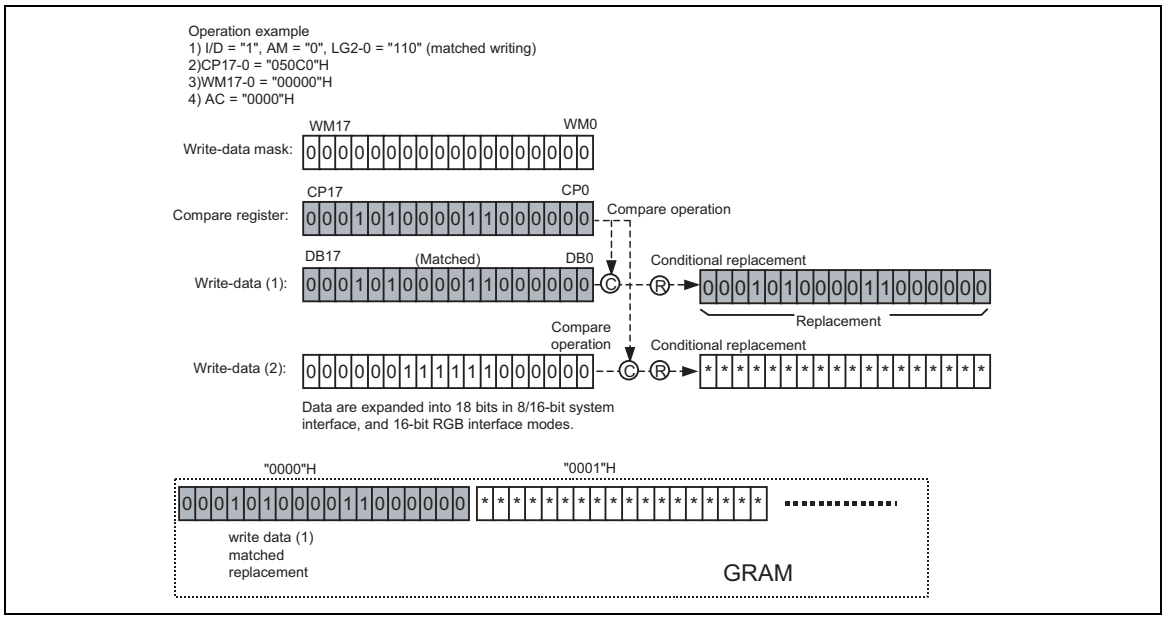
This mode is used when data are vertically written in high speed mode. It is also used to initialize the graphics RAM (GRAM), develop font patterns or to draw a line vertically. The write-data mask function (WM17–0) is also available in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or at the top of the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.



Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

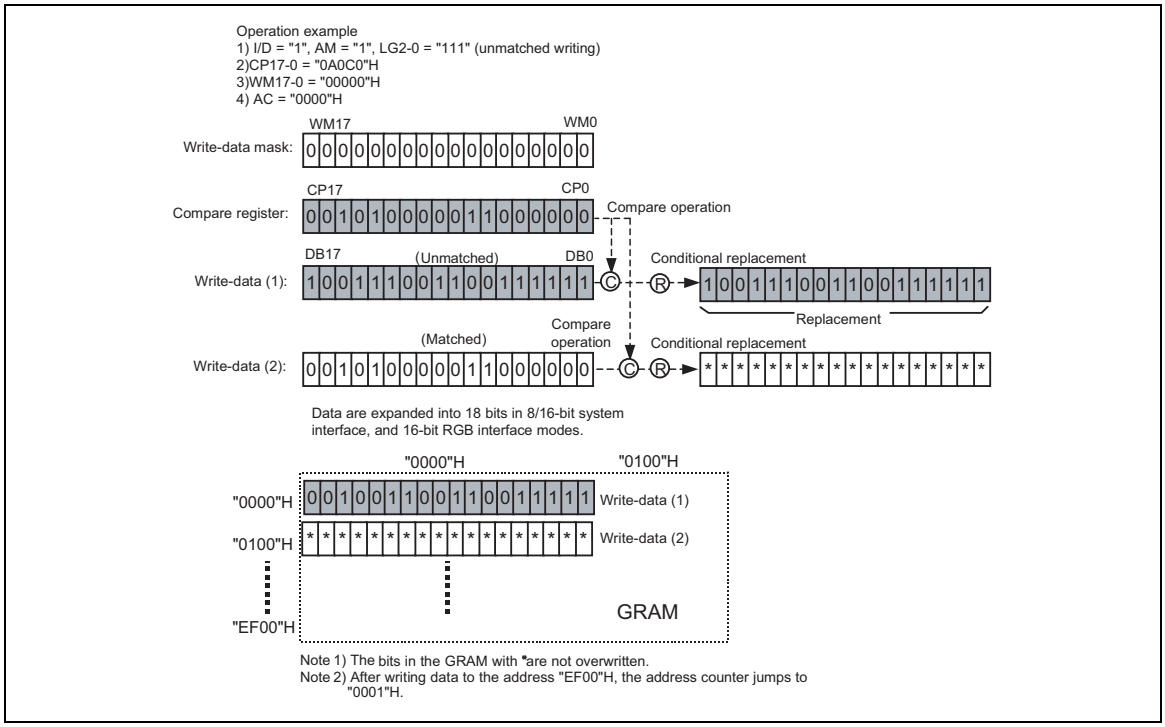
This mode is used when data are horizontally written with comparing the write data and the value set in the compare register (CP17–0) by R, G, B pixel. When the result of the comparison satisfies a condition, the write data sent from the microcomputer are written to GRAM. In this operation, the write-data mask function (WM17–0) is available. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the counter at the opposing edge of the next one-raster-row below after when the counter reaches either left or right edge of GRAM.



Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

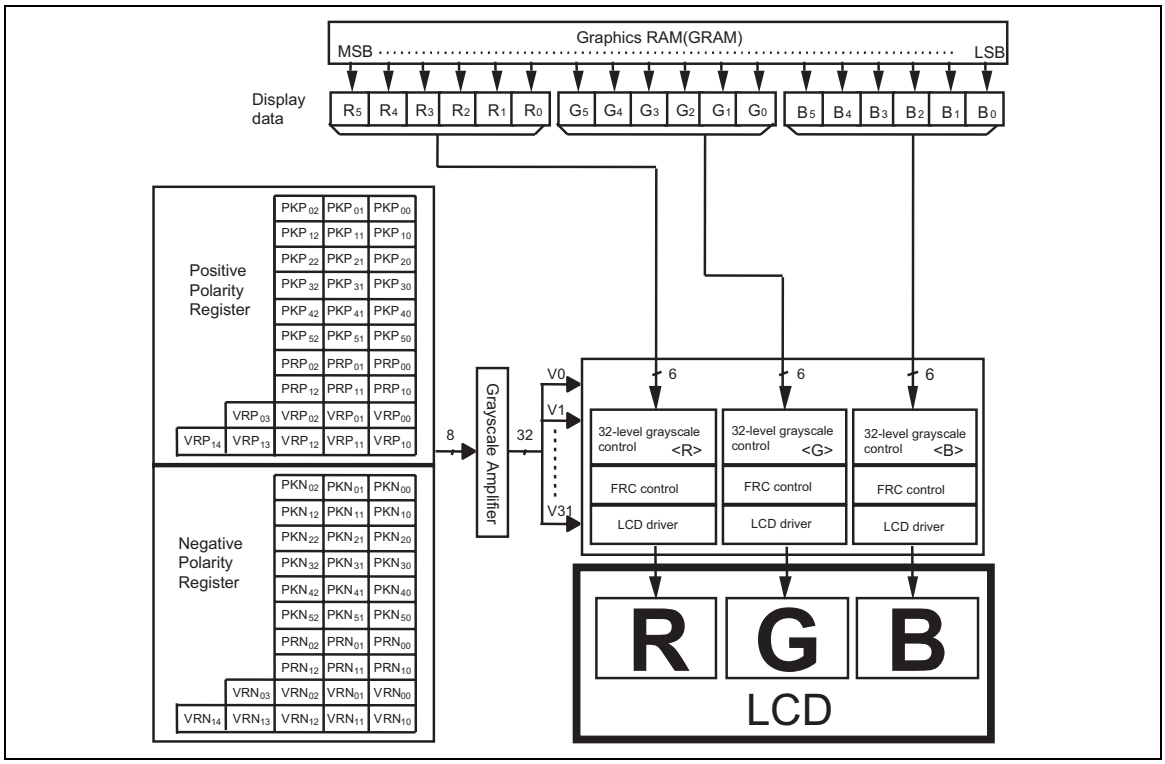
This mode is used when data are horizontally written with comparing the write data and the value set in the compare register (CP17–0) by R, G, B pixel. When the result of the comparison satisfies a condition, the write data sent from the microcomputer are written to GRAM. In this operation, the write-data mask function (WM17–0) is available. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the counter either at the top of the next right row (ID = 1) or at the top of the next left row (I/D = 0) according to the setting in the I/D bit, when the address reaches the bottom of GRAM.



Write Mode 4

γ-Correction Function

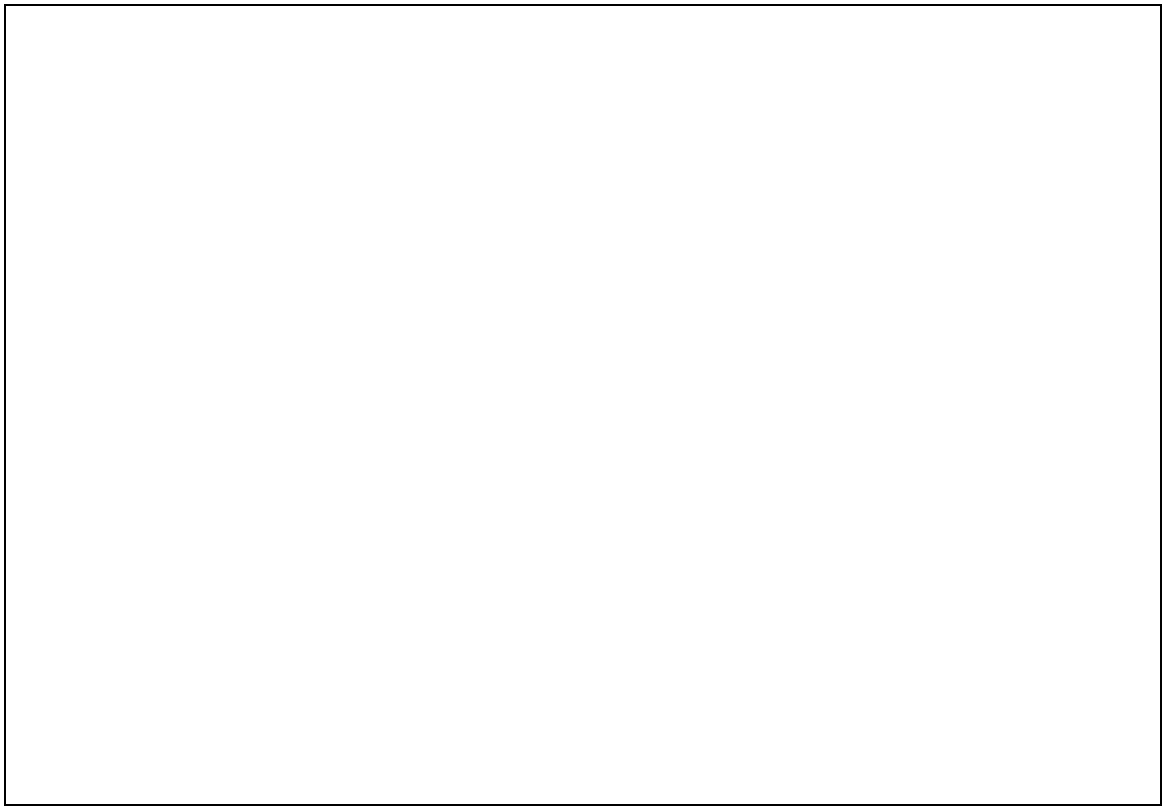
The HD66787 incorporates γ-correction function to simultaneously display 262,144 colors, by which 8-level grayscale is determined by the gradient-adjustment and fine-adjustment registers. Select either positive or negative polarity of the registers according to the characteristics of a liquid crystal panel.



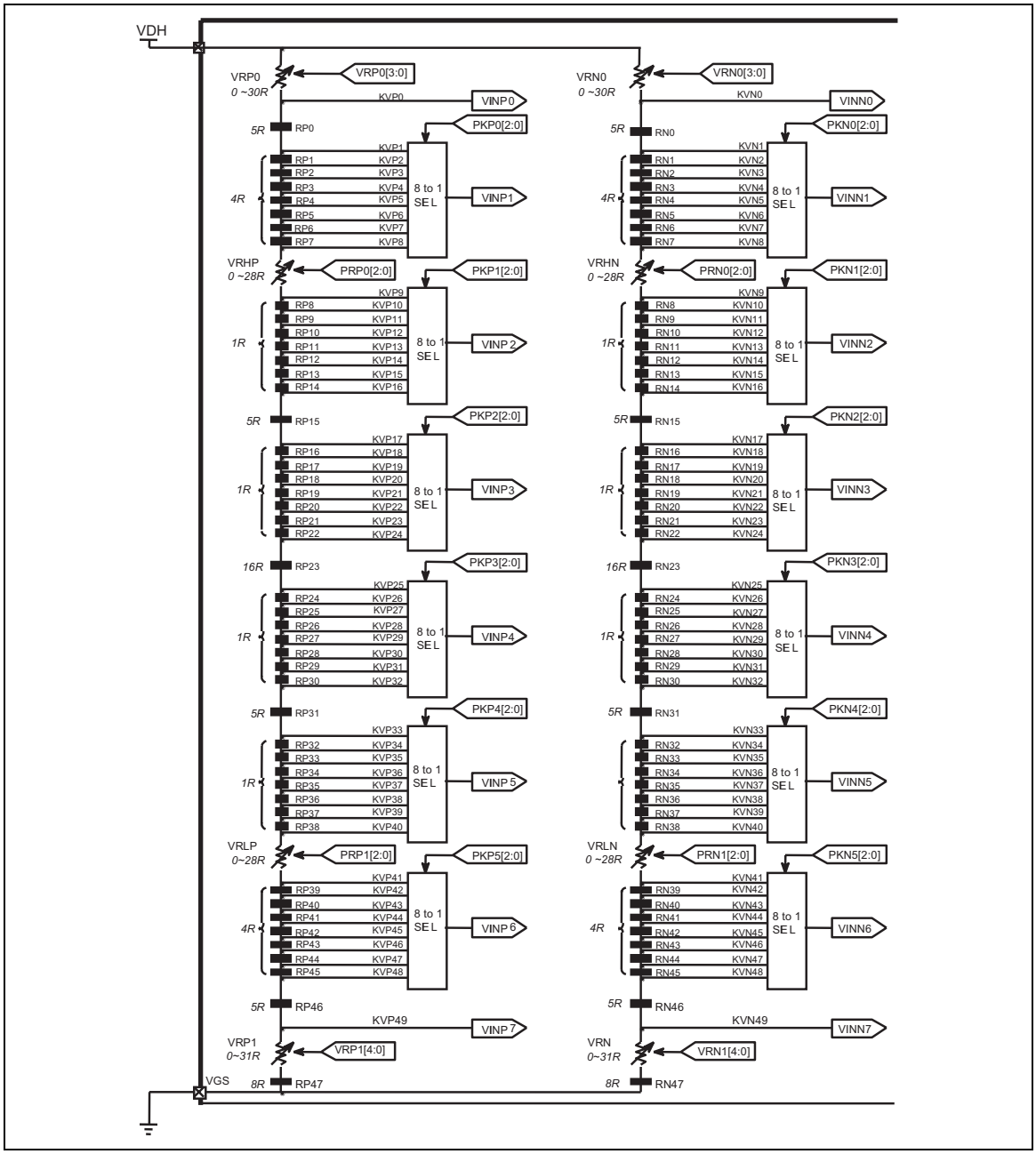
Grayscale control

Configuration of Grayscale Amplifier

The eight levels (VIN0-7) of grayscale are determined by the gradient adjustment and fine adjustment registers. The 8 levels are then divided into 32 levels (V0-31) by the ladder resistors placed between each level.



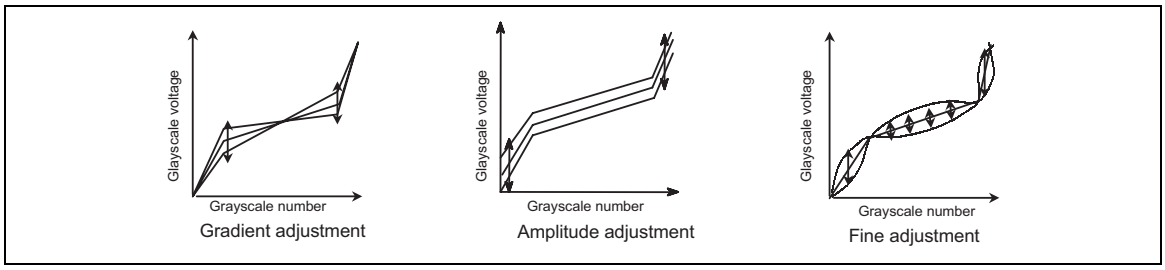
Grayscale amplifier



Ladder Resistors and 8-to-1 Selectors

γ-Correction Register

The γ-adjustment register is a group of registers to set an appropriate grayscale voltage for the γ-characteristics of a liquid crystal panel. The register group is categorized into the ones adjusting gradient, amplitude, and fine-tuning in relation to grayscale number and grayscale voltage characteristics. Each register can make an independent setting for the positive/negative polarity. The reference value and RGB are common to both polarities.



Gradient, Amplitude, Fine Adjustments

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient around the middle of the grayscale number and voltage characteristics without changing a dynamic range. To adjust a gradient, the values of the variable resistors (VRHP (N)/VRLP (N)) in the ladder resistor block for grayscale voltage generation are controlled. The registers incorporate separate registers for positive and negative polarities to be compatible with asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. To adjust the amplitude, the values of the variable resistors (VRP(N)1/0) in the bottom of the ladder resistor block for grayscale voltage generation are adjusted. Same with the gradient registers, the amplitude adjustment registers also incorporate separate registers for positive and negative polarities.

3. Fine adjustment registers

The fine adjustment register is to fine-adjust the grayscale voltage level. To fine-adjust the grayscale voltage level, each level of 8-level reference voltages generated from the ladder registers is controlled by 8-to-1 selector. Same with the other registers, the fine adjustment registers also incorporate separate registers for positive and negative polarities.

γ-Correction Registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 2 to 0	PRN0 2 to 0	Variable resistor VRHP (N)
	PRP1 2 to 0	PRN1 2 to 0	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 3 to 0	VRN0 3 to 0	Variable resistor VRP (N)0
	VRP1 4 to 0	VRN1 4 to 0	Variable resistor VRP (N)1
Fine adjustment	PKP0 2 to 0	PKN0 2 to 0	8-to-1 selector (voltage level of grayscale 1)
	PKP1 2 to 0	PKN1 2 to 0	8-to-1 selector (voltage level of grayscale 8)
	PKP2 2 to 0	PKN2 2 to 0	8-to-1 selector (voltage level of grayscale 20)
	PKP3 2 to 0	PKN3 2 to 0	8-to-1 selector (voltage level of grayscale 43)
	PKP4 2 to 0	PKN4 2 to 0	8-to-1 selector (voltage level of grayscale 55)
	PKP5 2 to 0	PKN5 2 to 0	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector

Block configuration

The block diagram of page **117** consists of two ladder resistors including variable resistors, and 8-to-1 selectors which select the voltage generated by the ladder resistors to output a reference voltage for the grayscale voltage. The variable resistors and the 8-to-1 selectors are controlled by the γ correction registers. Pins that are connected to a variable resistor are also provided to compensate the variation among the panels.

Variable resistor

There are three kinds of variable resistors for the gradient adjustment (VRHP(N)/VRLP(N)), the amplitude adjustment (1) (VRP(N)0), and the amplitude adjustment (2) (VRP(N)1). The resistance is determined by the gradient adjustment and amplitude adjustment registers as is shown below.

Gradient adjustment

Contents of Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment (1)

Contents of Register VRP(N)0[3:0]	Resistance VRP(N)0
0000	0R
0001	2R
0010	4R
⋮	⋮
1101	26R
1111	28R
1111	30R

Amplitude adjustment (2)

Contents of Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
⋮	⋮
11101	29R
11110	30R
11111	31R

8-to-1 selector

The 8-to-1 selectors select a voltage level generated by the ladder resistors according to fine adjustment registers, and output six kinds of reference voltage, VIN1 to VIN 6. The relationship between the fine adjustment register and the selected voltage is as follows.

Fine adjustment registers and selected voltage

The value of Register	Selected Voltage					
PKP(N)[2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels (V0-V31) are calculated according to the following formulas.

Formulas for calculating voltage (Positive polarity) (1)

Pin	Formula	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV* VRP0+5R)/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VREG1OUT - ΔV* VRP0+9R)/SUMRP	PKP02-00 = "001"	
KVP3	VREG1OUT - ΔV* VRP0+13R)/SUMRP	PKP02-00 = "010"	
KVP4	VREG1OUT - ΔV* VRP0+17R)/SUMRP	PKP02-00 = "011"	
KVP5	VREG1OUT - ΔV* VRP0+21R)/SUMRP	PKP02-00 = "100"	
KVP6	VREG1OUT - ΔV* VRP0+25R)/SUMRP	PKP02-00 = "101"	
KVP7	VREG1OUT - ΔV* VRP0+29R)/SUMRP	PKP02-00 = "110"	
KVP8	VREG1OUT - ΔV* VRP0+33R)/SUMRP	PKP02-00 = "111"	
KVP9	VREG1OUT - ΔV*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VREG1OUT - ΔV*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VREG1OUT - ΔV*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VREG1OUT - ΔV*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VREG1OUT - ΔV*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VREG1OUT - ΔV*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VREG1OUT - ΔV*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VREG1OUT - ΔV*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VREG1OUT - ΔV*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VREG1OUT - ΔV*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VREG1OUT - ΔV*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VREG1OUT - ΔV*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VREG1OUT - ΔV*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VREG1OUT - ΔV*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VREG1OUT - ΔV*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VREG1OUT - ΔV*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VREG1OUT - ΔV*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VREG1OUT - ΔV*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VREG1OUT - ΔV*(VRP0+73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VREG1OUT - ΔV*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VREG1OUT - ΔV*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VREG1OUT - ΔV*(VRP0+80R+VRHP)/SUMRP	PKP42-40 = "000"	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VREG1OUT - ΔV*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VREG1OUT - ΔV*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VREG1OUT - ΔV*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VREG1OUT - ΔV*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VREG1OUT - ΔV*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VREG1OUT - ΔV*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VREG1OUT - ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VREG1OUT - ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VREG1OUT - ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VREG1OUT - ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VREG1OUT - ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VREG1OUT - ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VREG1OUT - ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VREG1OUT - ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV : Voltage difference between VREG1OUT and VGS

Formulas for calculating voltage (Positive polarity) (2)

Grayscale Voltage	Formula
V0	VINP0
V1	V4+(VINP1-V4)*(15/24)
V2	V4+(VINP1-V4)*(8/24)
V3	V4+(VINP1-V4)*(4/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V20+(V8-V20)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(20/24)
V29	VINP6+(V27-VINP6)*(16/24)
V30	VINP6+(V27-VINP6)*(9/24)
V31	VINP7

Note : Make sure DDVDH - V0 > 0.5V
DDVDH - V4 > 1.1V

Formulas for calculating voltage (Negative polarity) (1)

Pin	Formula	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - ΔV*VRN0/SUMRN	-	VINN0
KVN1	VREG1OUT - ΔV* VRN0+5R)/SUMRN	PKN 02-00 = "000"	VINN1
KVN2	VREG1OUT - ΔV* VRN0+9R)/SUMRN	PKN 02-00 = "001"	
KVN3	VREG1OUT - Δ V* VRN0+13R)/SUMRN	PKN 02-00 = "010"	
KVN4	VREG1OUT - Δ V* VRN0+17R)/SUMRN	PKN 02-00 = "011"	
KVN5	VREG1OUT - Δ V* VRN0+21R)/SUMRN	PKN 02-00 = "100"	
KVN6	VREG1OUT - Δ V* VRN0+25R)/SUMRN	PKN 02-00 = "101"	
KVN7	VREG1OUT - Δ V* VRN0+29R)/SUMRN	PKN 02-00 = "110"	
KVN8	VREG1OUT - Δ V* VRN0+33R)/SUMRN	PKN 02-00 = "111"	
KVN9	VREG1OUT - Δ V*(VRN0+33R+VRHN)/SUMRN	PKN 12-10 = "000"	VINN2
KVN10	VREG1OUT - Δ V*(VRN0+34R+VRHN)/SUMRN	PKN 12-10 = "001"	
KVN11	VREG1OUT - Δ V*(VRN0+35R+VRHN)/SUMRN	PKN 12-10 = "010"	
KVN12	VREG1OUT - Δ V*(VRN0+36R+VRHN)/SUMRN	PKN 12-10 = "011"	
KVN13	VREG1OUT - Δ V*(VRN0+37R+VRHN)/SUMRN	PKN 12-10 = "100"	
KVN14	VREG1OUT - Δ V*(VRN0+38R+VRHN)/SUMRN	PKN 12-10 = "101"	
KVN15	VREG1OUT - Δ V*(VRN0+39R+VRHN)/SUMRN	PKN 12-10 = "110"	
KVN16	VREG1OUT - Δ V*(VRN0+40R+VRHN)/SUMRN	PKN 12-10 = "111"	
KVN17	VREG1OUT - Δ V*(VRN0+45R+VRHN)/SUMRN	PKN 22-20 = "000"	VINN3
KVN18	VREG1OUT - Δ V*(VRN0+46R+VRHN)/SUMRN	PKN 22-20 = "001"	
KVN19	VREG1OUT - Δ V*(VRN0+47R+VRHN)/SUMRN	PKN 22-20 = "010"	
KVN20	VREG1OUT - Δ V*(VRN0+48R+VRHN)/SUMRN	PKN 22-20 = "011"	
KVN21	VREG1OUT - Δ V*(VRN0+49R+VRHN)/SUMRN	PKN 22-20 = "100"	
KVN22	VREG1OUT - Δ V*(VRN0+50R+VRHN)/SUMRN	PKN 22-20 = "101"	
KVN23	VREG1OUT - Δ V*(VRN0+51R+VRHN)/SUMRN	PKN 22-20 = "110"	
KVN24	VREG1OUT - Δ V*(VRN0+52R+VRHN)/SUMRN	PKN 22-20 = "111"	
KVN25	VREG1OUT - Δ V*(VRN0+68R+VRHN)/SUMRN	PKN 32-30 = "000"	VINN4
KVN26	VREG1OUT - Δ V*(VRN0+69R+VRHN)/SUMRN	PKN 32-30 = "001"	
KVN27	VREG1OUT - Δ V*(VRN0+70R+VRHN)/SUMRN	PKN 32-30 = "010"	
KVN28	VREG1OUT - Δ V*(VRN0+71R+VRHN)/SUMRN	PKN 32-30 = "011"	
KVN29	VREG1OUT - Δ V*(VRN0+72R+VRHN)/SUMRN	PKN 32-30 = "100"	
KVN30	VREG1OUT - Δ V*(VRN0+73R+VRHN)/SUMRN	PKN 32-30 = "101"	
KVN31	VREG1OUT - Δ V*(VRN0+74R+VRHN)/SUMRN	PKN 32-30 = "110"	
KVN32	VREG1OUT - Δ V*(VRN0+75R+VRHN)/SUMRN	PKN 32-30 = "111"	
KVN33	VREG1OUT - Δ V*(VRN0+80R+VRHN)/SUMRN	PKN 42-40 = "000"	VINN5
KVN34	VREG1OUT - Δ V*(VRN0+81R+VRHN)/SUMRN	PKN 42-40 = "001"	
KVN35	VREG1OUT - Δ V*(VRN0+82R+VRHN)/SUMRN	PKN 42-40 = "010"	
KVN36	VREG1OUT - Δ V*(VRN0+83R+VRHN)/SUMRN	PKN 42-40 = "011"	
KVN37	VREG1OUT - Δ V*(VRN0+84R+VRHN)/SUMRN	PKN 42-40 = "100"	
KVN38	VREG1OUT - Δ V*(VRN0+85R+VRHN)/SUMRN	PKN 42-40 = "101"	
KVN39	VREG1OUT - Δ V*(VRN0+86R+VRHN)/SUMRN	PKN 42-40 = "110"	
KVN40	VREG1OUT - Δ V*(VRN0+87R+VRHN)/SUMRN	PKN 42-40 = "111"	
KVN41	VREG1OUT - Δ V*(VRN0+87R+VRHN+VRLP)/SUMRN	PKN 52-50 = "000"	VINN6
KVN42	VREG1OUT - Δ V*(VRN0+91R+VRHN+VRLP)/SUMRN	PKN 52-50 = "001"	
KVN43	VREG1OUT - Δ V*(VRN0+95R+VRHN+VRLP)/SUMRN	PKN 52-50 = "010"	
KVN44	VREG1OUT - Δ V*(VRN0+99R+VRHN+VRLP)/SUMRN	PKN 52-50 = "011"	
KVN45	VREG1OUT - Δ V*(VRN0+103R+VRHN+VRLP)/SUMRN	PKN 52-50 = "100"	
KVN46	VREG1OUT - Δ V*(VRN0+107R+VRHN+VRLP)/SUMRN	PKN 52-50 = "101"	
KVN47	VREG1OUT - Δ V*(VRN0+111R+VRHN+VRLP)/SUMRN	PKN 52-50 = "110"	
KVN48	VREG1OUT - Δ V*(VRN0+115R+VRHN+VRLP)/SUMRN	PKN 52-50 = "111"	
KVN49	VREG1OUT - Δ V*(VRN0+120R+VRHN+VRLP)/SUMRN	-	VINN7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV: Voltage difference between VREG1OUT and VGS

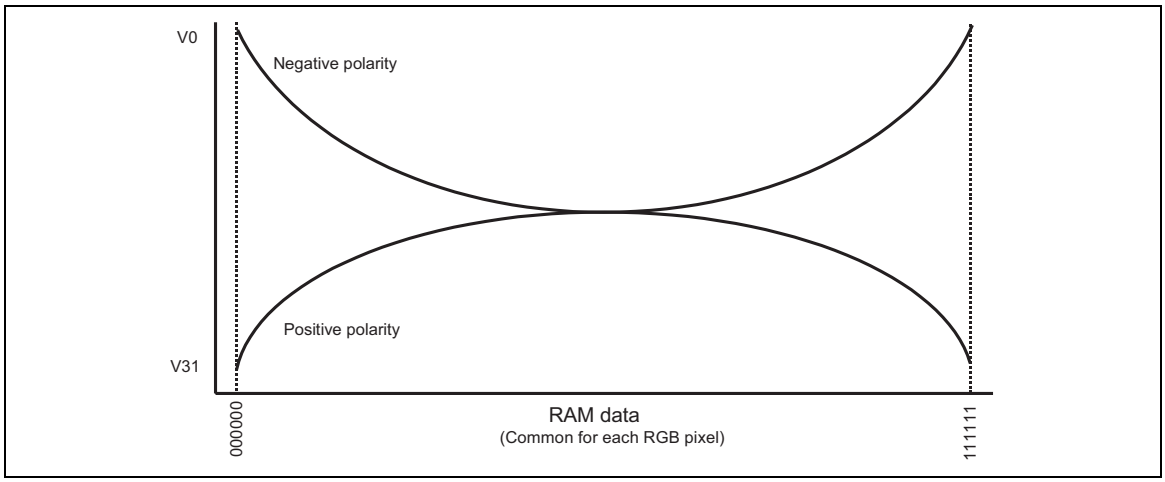
Formulas for calculating voltage (Negative polarity) (2)

Grayscale Voltage	Formula
V0	VINN0
V1	V4+(VINN1-V4)*(15/24)
V2	V4+(VINN1-V4)*(8/24)
V3	V4+(VINN1-V4)*(4/24)
V4	VINN2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V20+(V8-V20)*(4/24)
V10	VINN3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINN4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINN5
V28	VINN6 +(V27-VINN6)*(20/24)
V29	VINN6 +(V27-VINN6)*(16/24)
V30	VINN6 +(V27-VINN6)*(9/24)
V31	VINN7

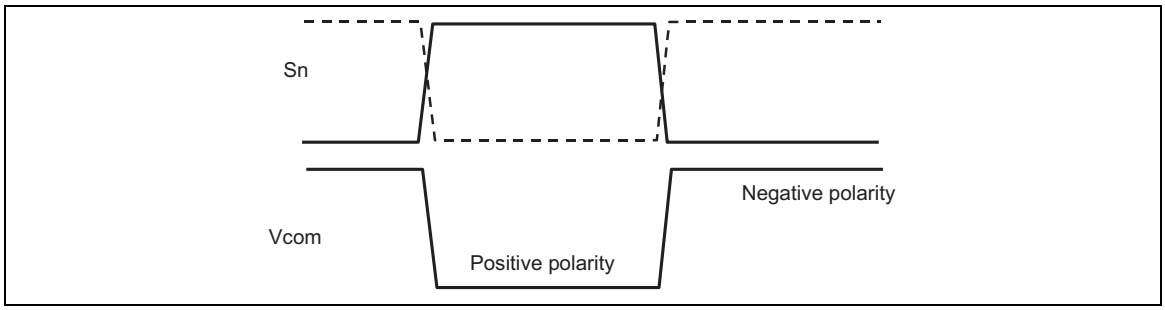
Note : Make sure DDVDH - V0 > 0.5V
DDVDH - V4 > 1.1V

Relationship between RAM data and output level

The relationship between the RAM data and the source output level is as follows.



RAM data and the output voltage

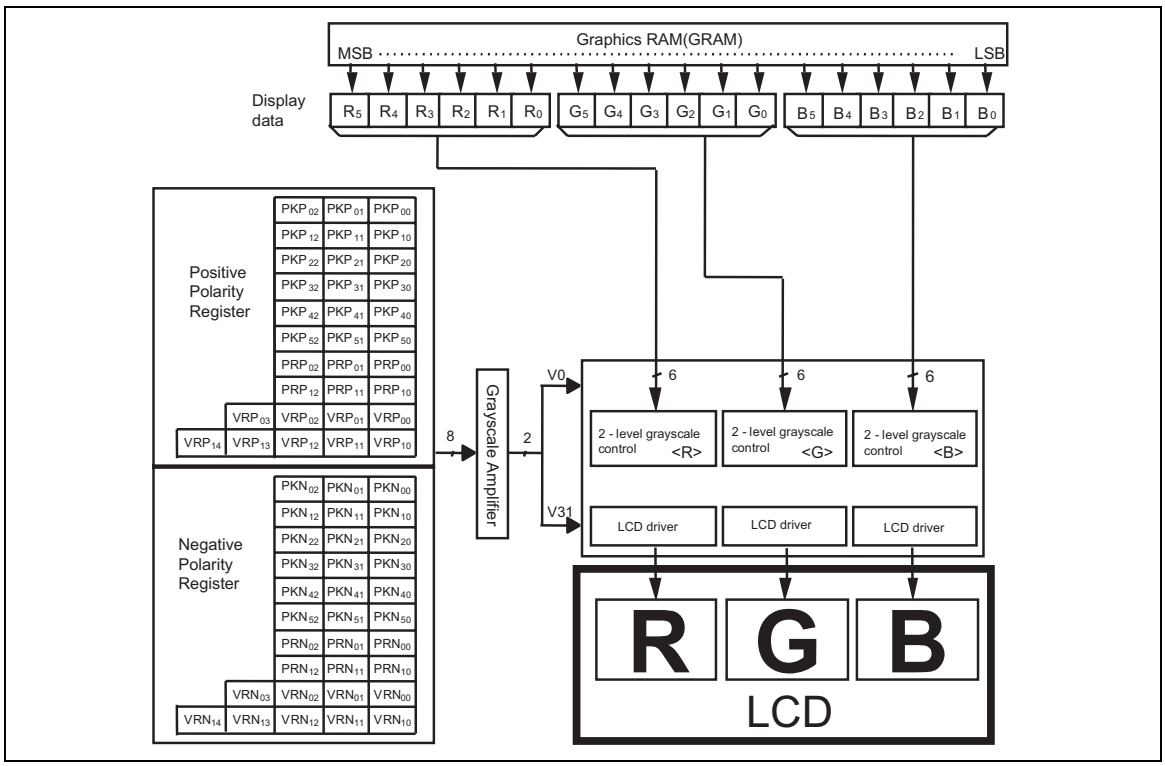


Source output and Vcom

8-color Display Mode

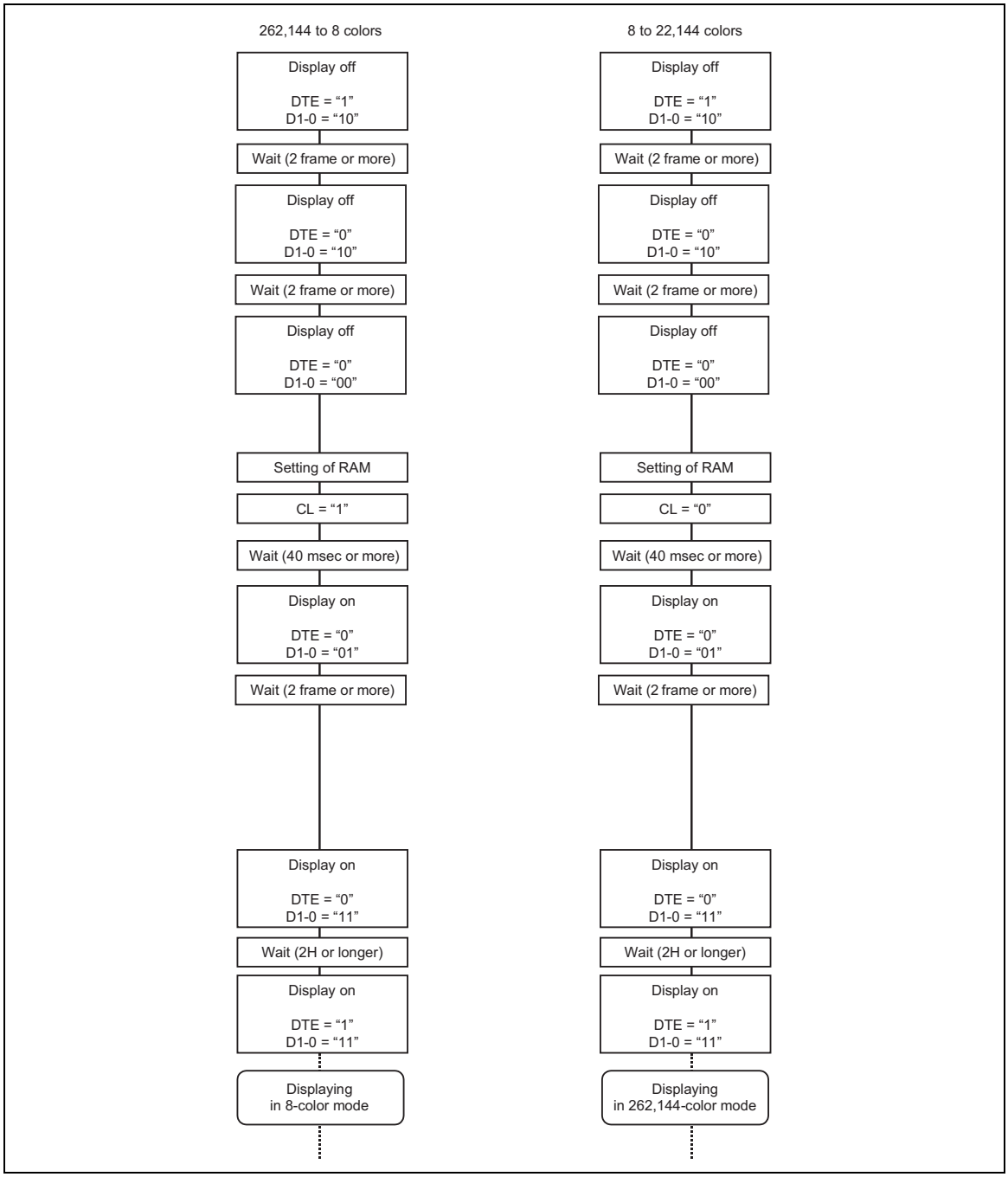
The HD66787 incorporates the 8-color display mode. The available grayscale levels are V0 and V31, and the voltages for the other levels (V1-V30) are halted to reduce power consumption.

The γ-fine-adjustment registers, PKP0-PKP5 and PKN0-PKN5 are not available in the 8-color display mode. Since the power supply for the levels V1-V30 are halted, RGB data in GRAM should be set to either "000000" or "111111" before setting this mode so that V0 or V31 is selected.



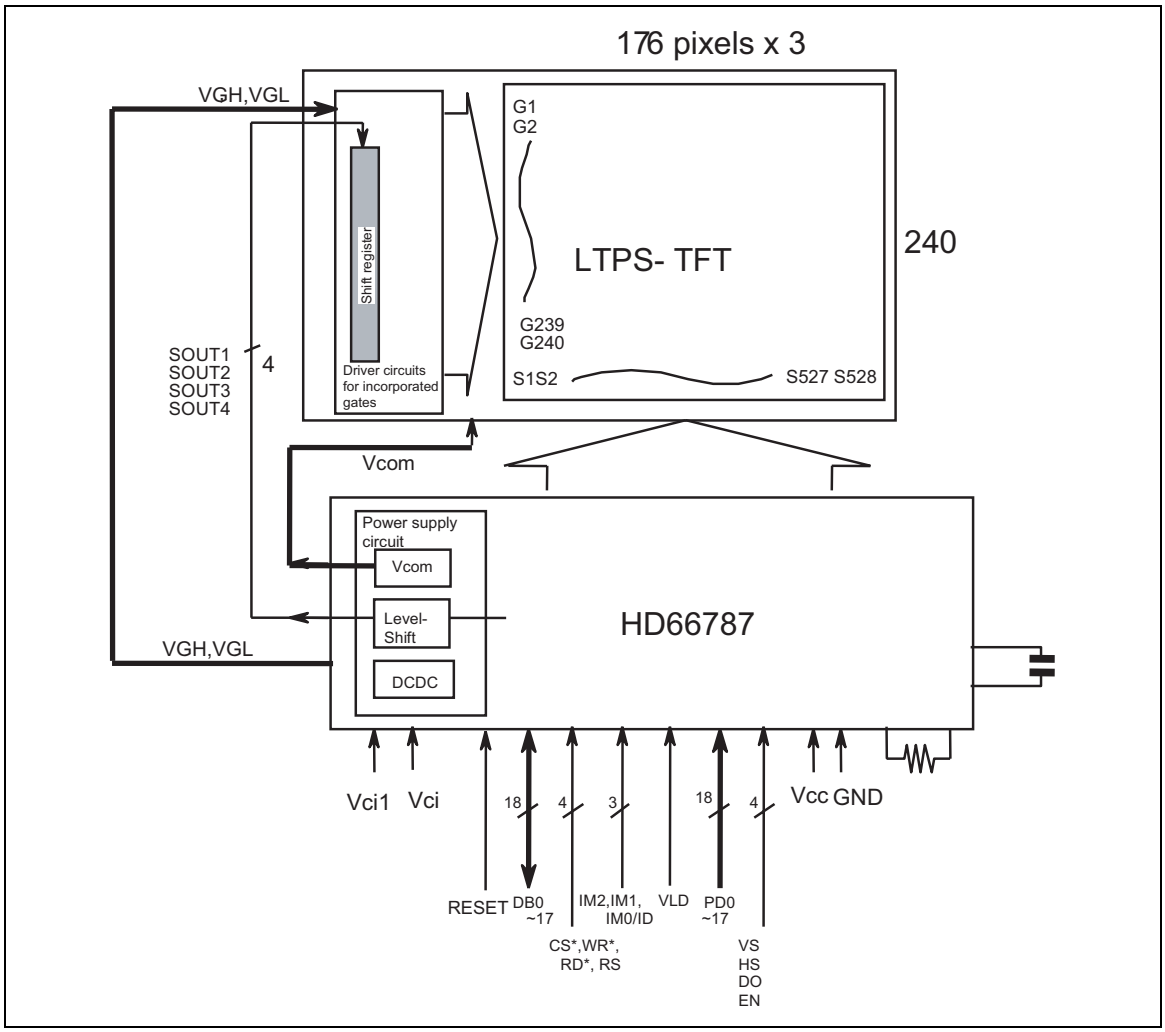
Grayscale control

To switch between the 262, 144-color mode and the 8-color mode, make settings according to the following sequences.



System Configuration

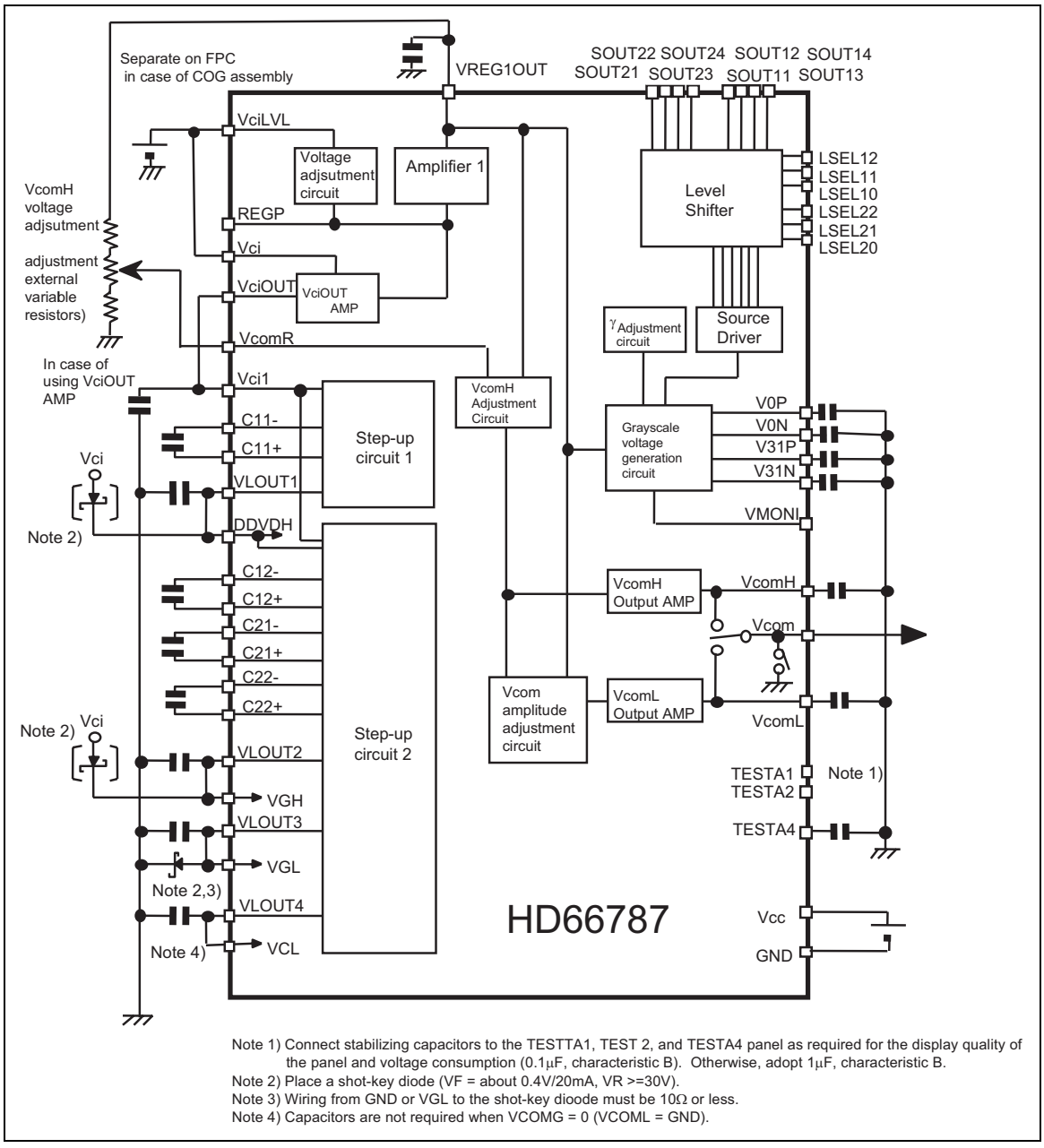
The following figure illustrates an example of configuring a TFT-LCD panel of 176x 240 dots withHD66787.



System configuration with HD66787

Configuration of Power Generation Circuit

The internal configuration of power generation circuit for driving liquid crystal with the HD66787 is as follows.



Note 1) Connect stabilizing capacitors to the TESTTA1, TEST 2, and TESTA4 panel as required for the display quality of the panel and voltage consumption (0.1μF, characteristic B). Otherwise, adopt 1μF, characteristic B.
Note 2) Place a shot-key diode (VF = about 0.4V/20mA, VR >=30V).
Note 3) Wiring from GND or VGL to the shot-key dioode must be 10Ω or less.
Note 4) Capacitors are not required when VCOMG = 0 (VCOML = GND).

Power generation circuit

Specification of External Elements Connected to HD66787 Power Supply

The following table shows specifications of external elements connected to HD66787 power supply.

Capacitor

Capacity	Recommended voltage	Connect pins
1 μF (B characteristic)	6V	VREG1OUT, VciOUT, VOUT4, VcomH, VcomL, C11+/-, C21+/-
	10V	VLOUT1, C21+/-, C22+/-
	25V	VLOUT2, VLOUT3
0.1 μF (B characteristic)	6V	V0P, V0N, V31P, V31N, TESTA4

Shot-key diode

Feature	Connect pin
VF < 0.4V / 20mA at 25 centigrade, VR>=30V (recommended diode : HSC226)	GND – VGL (Vci – VGH) (Vci – DDVDH)

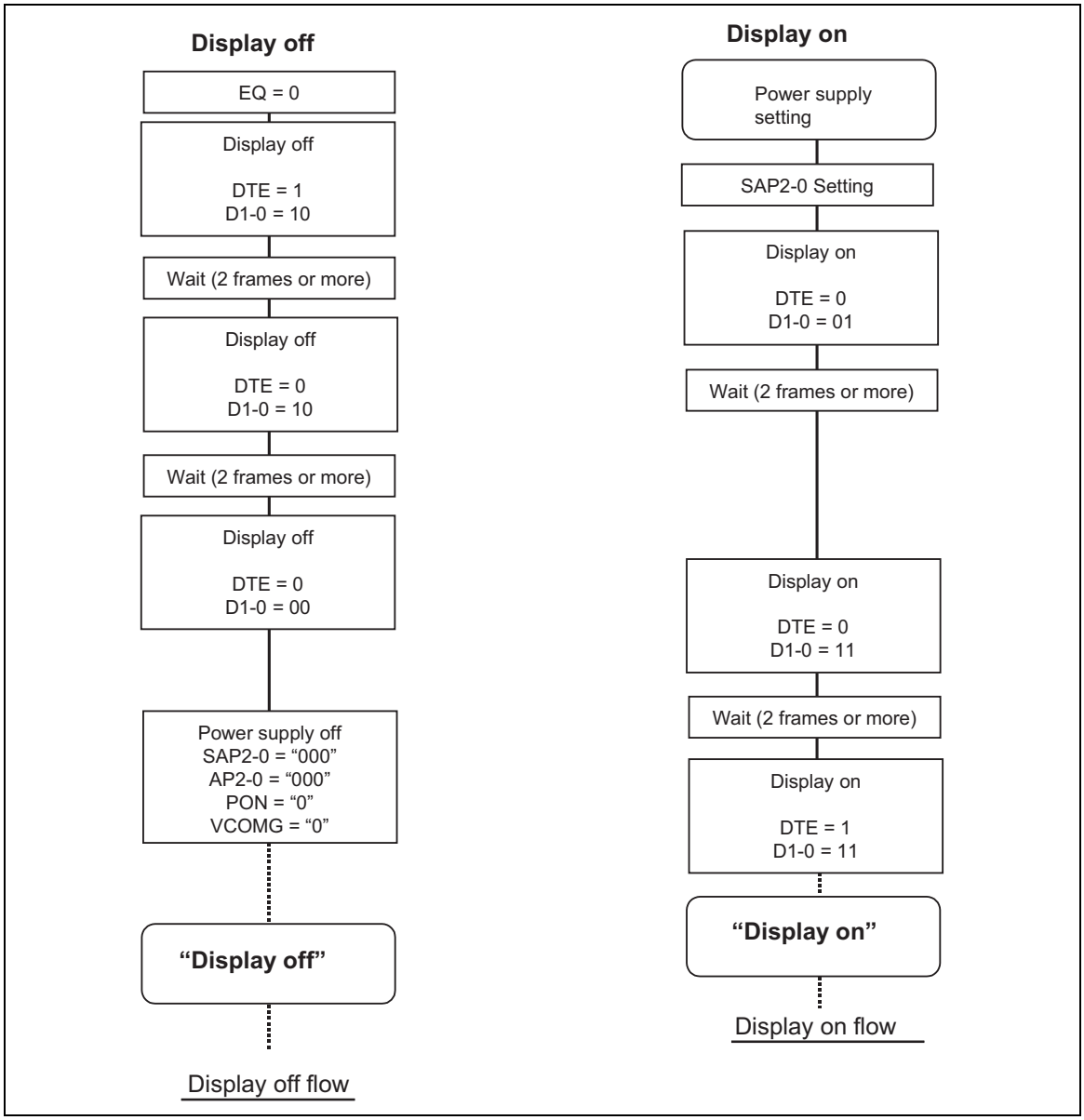
Variable resistor

Feature	Connect pin
> 200 kΩ	VcomR

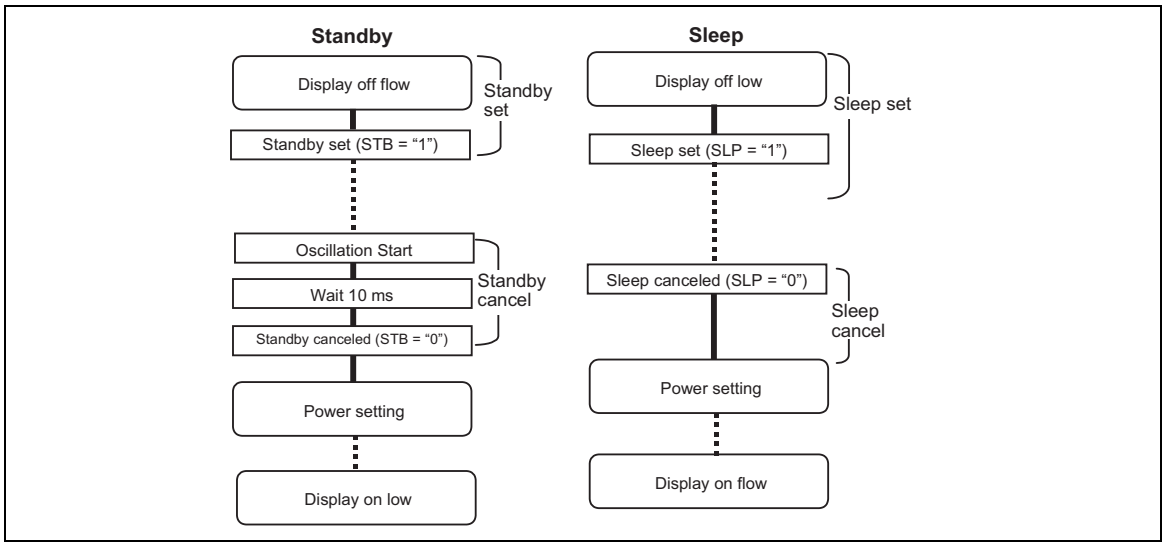
Instruction Setting Flow

Make a setting for each instruction according to the following sequence.

Display ON/OFF



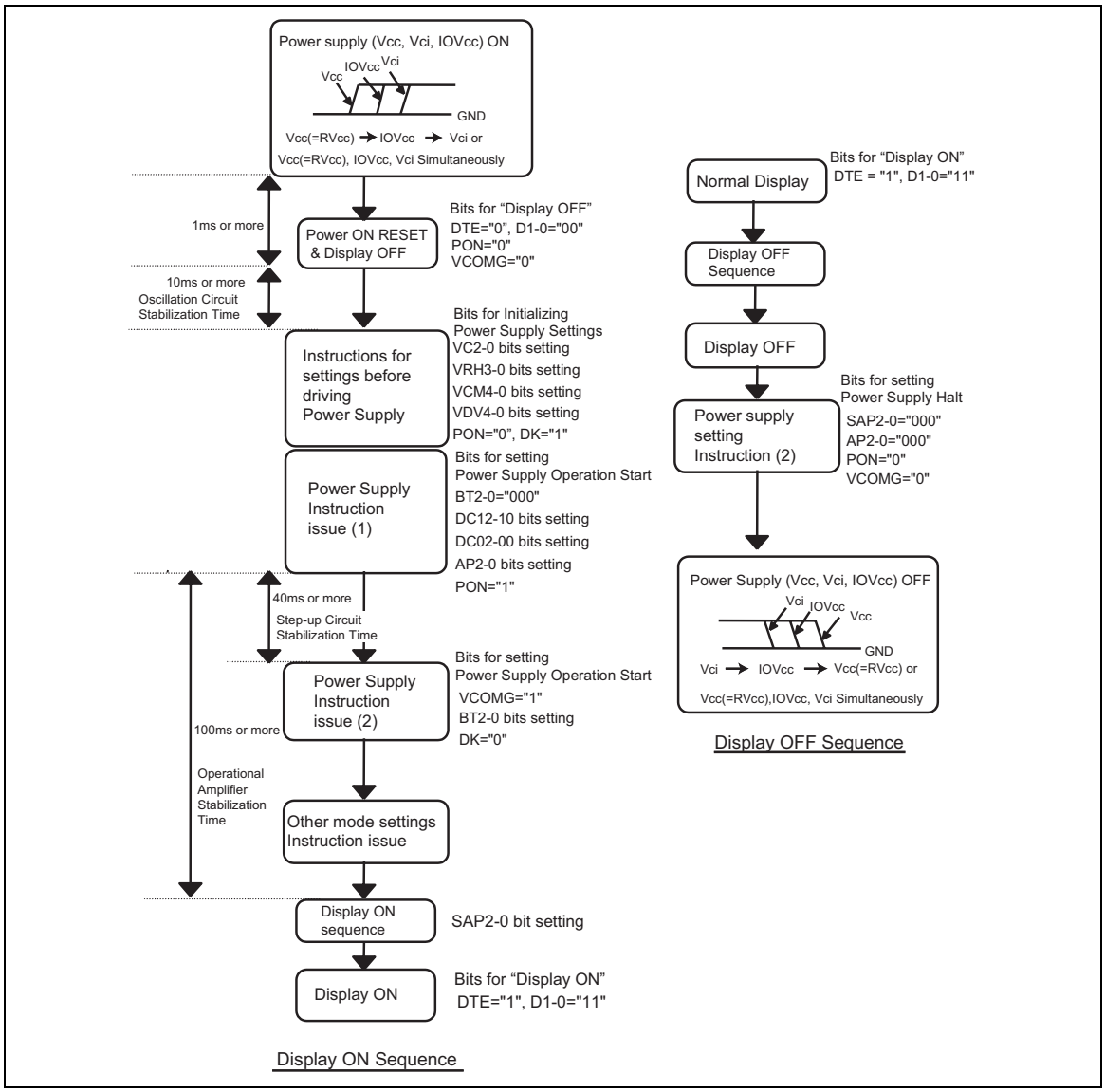
Standby and Sleep



Power Supply Setting Flow

Whenever turning on the power supply, it must be done in accordance to the following procedure.

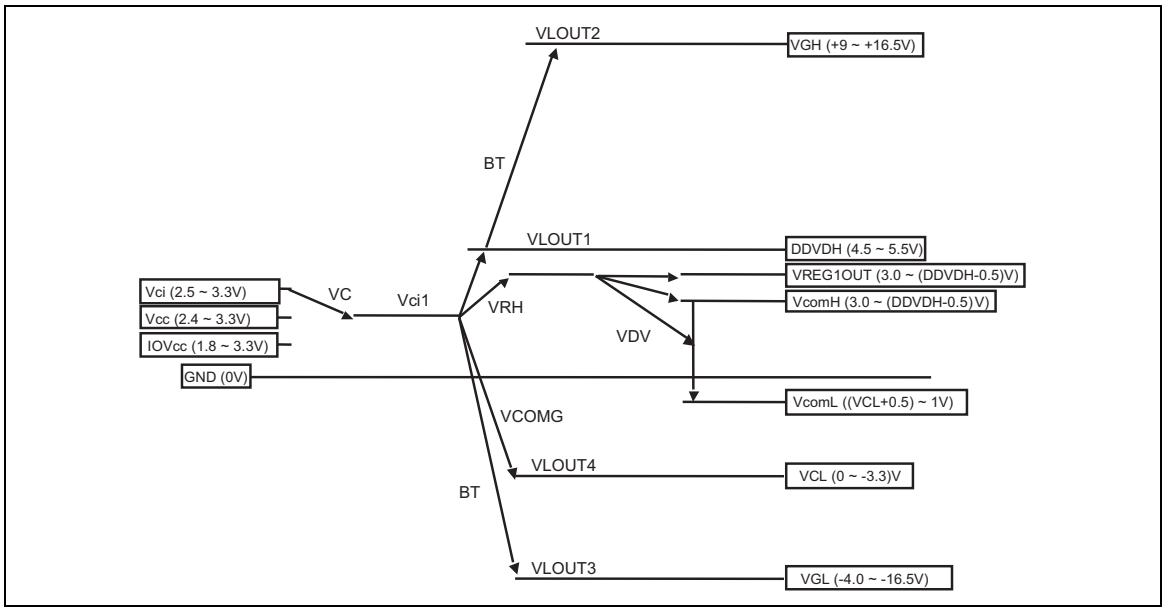
The stabilization time for the oscillation circuits, step-up circuits, and operational amplifiers depends on the external resistors and capacitors.



Power supply setting flow

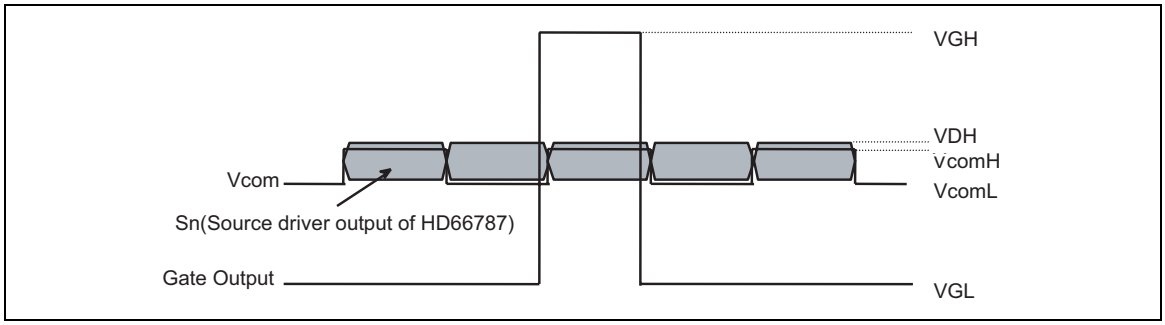
Pattern Diagram for Voltage Setting

The following figures are the pattern diagram of voltage setting for the HD66787 and the voltage waveforms.



Pattern diagram for voltage setting

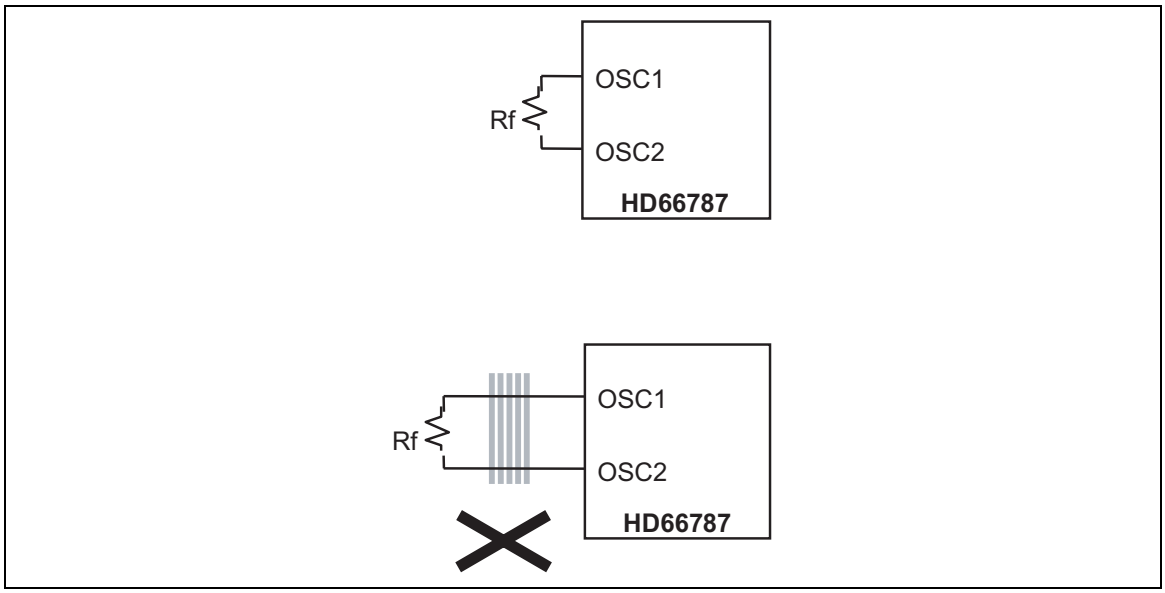
Note 1) Voltage drop occurs in relation to set voltage for each DDVDH, VGH, VGL, VCL output depending on current consumption required for each output. (DDVDH+VREG1OUT) > 0.5V and (VcomL – VCL) > 0.5V show the relationship in relation to the actual voltage. When AC frequency of Vcom1 and Vcom2 is high (e.g. alternation occurs by line), current consumption is also large. In this case, check voltage before use.



Applied voltage to the TFT display

Oscillation Circuit

The HD66787 generates oscillation by internal R-C oscillator with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of external resistor, the distance of wiring, and the power supply voltage for the oscillation. For example, the oscillation frequency becomes low when increasing the value of Rf resistor, or lowering the power supply voltage. See the "Electric Characteristics Notes" section for the relationship between the Rf resistor value and the oscillation frequency.



External Resistor Oscillation Mode

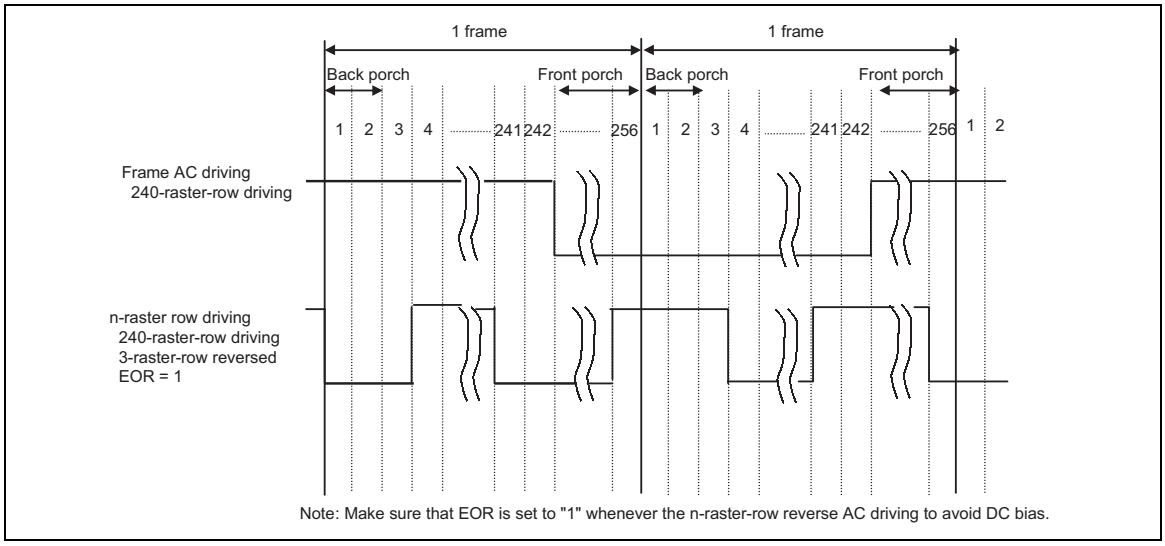
Note 1) Place the Rf resistor close to the OSC1, OSC2 pins.

Note 2) Make sure not to arrange other wiring beneath or close to OSC1-OSC2 wiring to avoid effects from coupling.

n-raster-row inversion AC drive

The HD66787, in addition to LCD inversion AC drive by frame, supports n-raster-row inversion AC drive where alternation occurs by n raster-rows, where n takes a number between 1 to 64. The n-raster-row inversion AC drive enables to overcome the problems related to display quality.

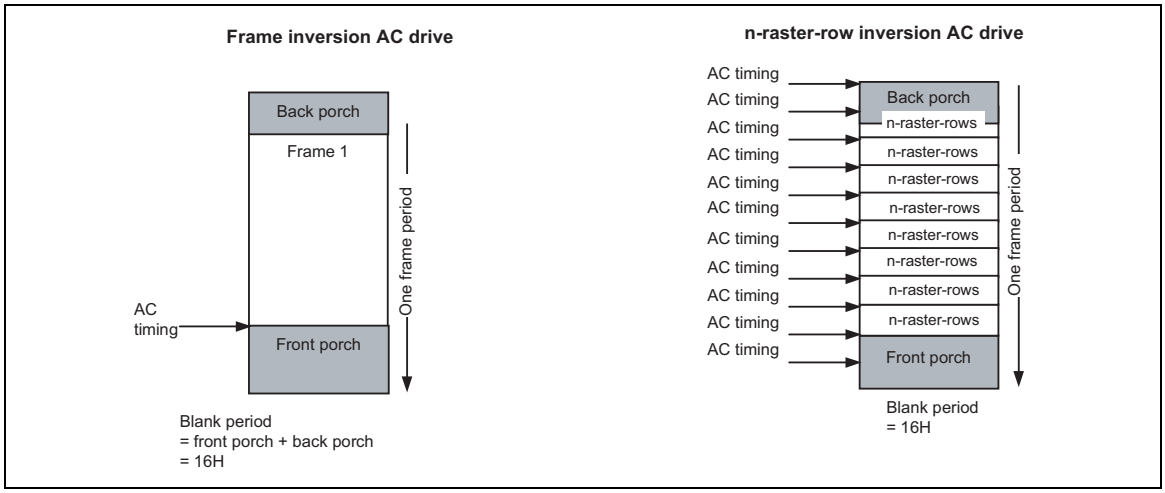
In determining n (the value set in the NW bit +1), the number of raster-rows by which alternation occurs, check the display quality on the actual liquid crystal panel. Setting a small number of raster-rows will raise the AC frequency of the liquid crystal and increase the charge/discharge current on the liquid crystal cells.



n-raster-rows inversion AC drive

AC Timing

The AC timings of frame inversion AC drive and n-raster-row inversion drive are illustrated as follows. In case of frame inversion AC drive, alternation occurs at the completion of drawing one frame, followed by a blank, which lasts for 16H periods. In case of n-raster-row, a blank lasting 16H period is inserted after drawing a full screen.



AC drive timing

Frame-Frequency Adjustment Function

The HD66787 incorporates frame frequency adjustment function. The frame frequency during the liquid crystal drive is adjusted by the instruction setting (DIV, RTN) while keeping the oscillation frequency fixed.

Setting the oscillation frequency high in advance allows switching the frame frequency in accordance to the kind of displayed picture (i.e. moving/still picture). When displaying a still picture, set the frame frequency low to save power consumption, while setting the frame frequency high when displaying a moving picture which requires high-speed switching of screens.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated by the following formula. The frame frequency is adjusted through the instruction setting with the 1-H period adjustment bit (RTN bit) and the operation clock division bit (DIV bit).

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line+BP+FP})} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency
Line: number of drive raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
The number of raster-rows for the front porch: FP
The number of raster-rows for the back porch: BP

Calculation Example The maximum frame frequency = 60 Hz

Number of driven raster-rows: 240
1-H period: 16 clock cycles (RTN3-0 = 0000)
Operation clock division ratio: 1 division

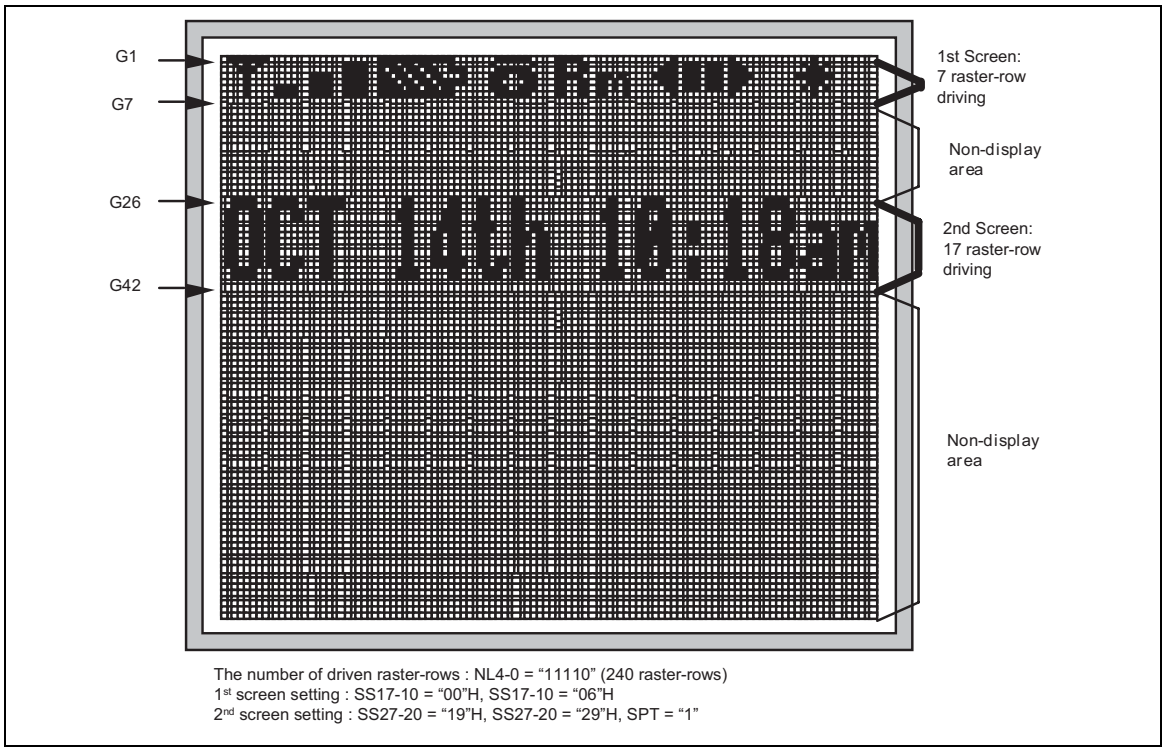
$$\text{fosc} = 60\ \text{Hz} \times (0 + 16)\ \text{clock} \times 1\ \text{division} \times (240 + 16)\ \text{lines} = 246\ (\text{kHz})$$

In this case, the R-C oscillation frequency becomes 246 kHz. Adjust the external resistor to the R-C oscillator to 246 kHz.

Screen–split Display Function

The HD66787 allows selectively driving two screens at arbitrary positions with the screen-drive position registers (R42 and R43). Only the raster-rows required to display two screens at arbitrary positions are selectively driven to reduce power consumption.

The first screen drive position register (R42) specifies the start line (SS17-10) and the end line (SE17-10) for displaying the first screen. The second screen drive position register (R43) specifies the start line (SS27-20) and the end line (SE27-20) for displaying the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of raster-rows driven for displaying the first and second screens must be less than the number of liquid crystal drive raster-rows.



Screen-split drive

Notes to the setting of 1st/2nd screen drive position registers

When making settings for the start line (SS17-10) and end line (SE17-10) of the first screen drive position register (R42), and the start line (SS27-20) and end line (SE27-20) of the second screen drive position register (R43) with the HD66787, it is necessary to satisfy the following conditions to display screens correctly.

One Screen Drive (SPT = 0)

Register Settings	Display Operation
(SE17-10) - (SS17-10) = NL	Full screen display The area of (SE17-10) - (SS17-10) is normally displayed.
(SE17-10) - (SS17-10) < NL	Partial screen display The area of (SE17-10) - (SS17-10) is normally displayed. The rest of the area is white display irrespective of data in RAM.
(SE17-10) - (SS17-10) > NL	Setting disabled

Note 1) SS17-10 ≤ SE17-0 ≤ "EF"H

Note 2) Setting disabled for SS27-20 and SE27-20.

Two Screen Drive (SPT = 1)

Register Settings	Display Operation
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) = NL	Full screen display The area of (SE27-20) - (SS17-10) is normally displayed.
((SE17-10) - (SS17-10)) + ((SE27-20) - (S27-20)) < NL	Partial screen display The area of (SE27-10) - (SS17-10) is normally displayed. The rest of the area is white display irrespective of data in RAM.
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) > NL	Setting disabled

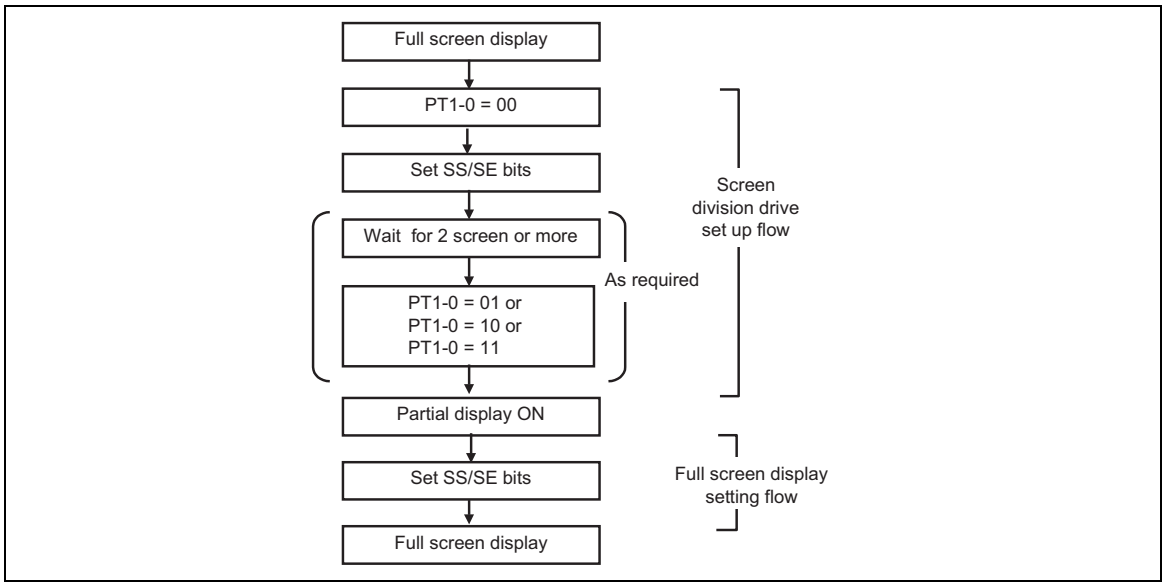
Note 1) Make sure that SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ EFH.

Note 2) Make sure that ((SE27-20) - (SS17-10)) ≤ NL.

The setting for the driver output in the non-display area during the partial display is changeable according to the characteristics of the display panel.

Source outputs in non-display area

		Source Output for Non-display Area	
PT1	**PT0**	**Positive Polarity**	**Negative Polarity**
0	0	V31	V0
0	1	V31	V0
1	0	GND	GND
1	1	High-Z	High-Z



Partial display setting flow

Absolute Maximum Values

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - GND	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (3)	DDVDH - GND	V	-0.3 ~ + 6.0	1, 2
Power supply voltage (4)	GND -VCL	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (5)	DDVDH - VCL	V	-0.3 ~ + 9.0	1
Power supply voltage (6)	VGH - GND	V	-0.3 ~ + 18.5	1, 2
Power supply voltage (7)	GND - VGL	V	-0.3 ~ + 18.5	1, 2
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 3
Storage temperature	Tstg	°C	-55 ~ + 110	1

Note 1) The LSI may be permanently damaged if it is used under the condition exceeding the above absolute maximum values. It is also recommended to use the LSI within the limit of its electric characteristics during normal operation. Exceeding the conditions may lead to malfunction of LSI and affect its credibility.

Note 2) The voltage from GND.

Note 3) The DC and AC characteristics of chip and wafer products are guaranteed at 85 °C.

Electric Characteristics (T.B.D.)

DC Characteristics

(V_{CC} = 1.8 to 3.7 V, Ta = –40 to +85°C [Note 1])

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	V_{CC} = 1.8 to 3.7 V	0.7 V_{CC}	—	V_{CC}	2, 3
Input low voltage (1) (OSC1 pin)	$V_{IL}1$	V	V_{CC} = 1.8 to 3.7 V	–0.3	—	0.15V_{CC}	2, 3
Input low voltage (2) (Except OSC1 pin)	$V_{IL}2$	V	Vcc=1.8V to 2.4V	-0.3	—	0.15Vcc	2,3
			Vcc=2.4V to 3.7V	-0.3	—	0.2Vcc	2,3
Output high voltage (1) (DB0-17 pins)	V_{OH1}	V	I_{OH} = –0.1 mA	0.75V_{CC}	—	—	2
Output low voltage (1) (DB0-17 pins)	V_{OL1}	V	V_{CC} = 1.8 to 2.4 V, I_{OL} = 0.1 mA	—	—	0.2 V_{CC}	2
			VCC = 2.4 to 3.7 V, I_{OL} = 0.1 mA	—	—	0.15V_{CC}	2
I/O leakage current	I_{Li}	µA	Vin = 0 to V_{CC}	–1	—	1	4
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	µA	R-C oscillation; fosc = 250kHz (240line) V_{CC} = 3.0 V, Ta = 25°C, RAM data 00[illegible]h	—	190	300	5,6
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	µA	Vcc = 3V, Ta<=50°C	—	0.1	5	5
			Vcc = 3V, Ta>50°C	—	—	20	
Liquid Crystal Power Current (DDVDH-GND)	I_{LCD}	µA	Vcc=3V, VLCD=5.5V, VDH=5.0V, CR Oscillation; fosc=250kHz(240line), Ta=25°C, RAMdata:0000h, REV="0", SAP="001", VRN4-0="0", PKP52-00="0", PRP12-00="0", VRN4-0=VRP4-0="0" PKP52-00="0", PRP12-00="0"	—	500	650	5,6
Liquid Crystal Drive Voltage(DDVDH-GND)	V_{LCD}	V	—	4.5	—	5.5	—
Output Voltage deviation	∠Vo	mV	—	—	5	—	7
Variation of average output voltage		mV	—	—	—	35	8

AC Characteristics

(V_{CC} = 1.7 to 3.7 V, Ta = –40 to +85°C [Note 1])

Clock Characteristics (V_{CC} = 1.8 to 3.7 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	fcp	kHz	VCC = 1.8 to 3.3 V	100	270	600	9
External clock duty ratio	Du	%	VCC = 1.8 to 3.3 V	45	50	55	9
External clock rise time	trcp	µs	VCC = 1.8 to 3.3 V	—	—	0.2	9
External clock fall time	tfcp	µs	VCC = 1.8 to 3.3 V	—	—	0.2	9
R-C oscillation clock	fOSC	kHz	Rf = TBD VCC = 3 V	244	305	366	10

T.B.D.

80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (Vcc = 1.8 to 2.4 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	600	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 2	0	—	—
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
VLD setup time		t_{VS}	ns	Figure 2	60	—	—
VLD hold time		t_{VH}	ns	Figure 2	15	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{H}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

T.B.D.

High-Speed Write Mode (HWM=1) (Vcc = 1.8 to 2.4 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 2	0	—	—
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
VLD setup time		t_{VS}	ns	Figure 2	60	—	—
VLD hold time		t_{VH}	ns	Figure 2	15	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_H	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

T.B.D.

Normal Write Mode (HWM=0) : Vcc = 2.4 to 3.7 V

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	250	—	—
	Read	t_{CYCR}	ns	Figure 2	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 2	0	—	—
	Read (RS to CS*, WR*)				10	—	—
Address hold time		t_{AH}	ns	Figure 2	2	—	—
VLD set up time		t_{VS}	ns	Figure 2	25	—	—
VLD hold time		t_{VH}	ns	Figure 2	2	—	—
Write data setup time		t_{DSW}	ns	Figure 2	25	—	—
Write data hold time		t_H	ns	Figure 2	2	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

T.B.D.

High-Speed Write Mode (HWM=1) : Vcc = 2.4 to 3.7 V

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	100	—	—
	Read	t_{CYCR}			500	—	—
Write low-level pulse width		PW_{Lw}	ns	Figure 2	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	250	—	—
Write high -level pulse width		PW_{HW}	ns	Figure 2	40	—	—
Read high -level pulse width		PW_{HR}	ns	Figure 2	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	—
Set up time	Write (RS to CS*, WR*)	t_{WR}	ns	Figure 2	0	—	25
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 2	2	—	—
VLD set-up time		t_{VS}	ns	Figure 2	25	—	—
VLD hold time		t_{VH}	ns	Figure 2	2	—	—
Write data set up time		t_{DSW}	ns	Figure 2	25	—	—
Write data hold time		t_H	ns	Figure 2	2	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

T.B.D.

Serial Peripheral Interface Timing Characteristics

Vcc = 1.8 to 2.4 V

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 3	0.1	—	20
	Read (transmitted)	t_{SCYC}	us	Figure 3	0.5	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 3	230	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 3	230	—	—
Serial clock rise/fall time		$t_{scr, tscf}$	ns	Figure 3	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t_{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 3	30	—	—
Serial input data delay time		t_{SOD}	ns	Figure 3	—	—	200
Serial input data hold time		t_{SOH}	ns	Figure 3	5	—	—

T.B.D.

Vcc = 2.4 to 3.3 V

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	Write (receive))	t_{SCYC}	us	Figure 3	0.1	—	20
	Read (send)	t_{SCYC}	us	Figure 3	0.35	—	20
Serial clock high-level pulse width	Write (receive)	t_{SCH}	ns	Figure 3	40	—	—
	Read (send)	t_{SCH}	ns	Figure 3	150	—	—
Serial clock low-level pulse width	Write (receive)	t_{SCL}	ns	Figure 3	40	—	—
	Read (send)	t_{SCL}	ns	Figure 3	150	—	—
Serial clock rise/fall time		$t_{scr, scf}$	ns	Figure 3	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t_{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 3	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure 3	—	—	130
Serial output data hold time		t_{SOH}	ns	Figure 3	5	—	—

T.B.D.

Reset Timing Characteristics (V_{CC} = 1.8 to 3.7 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 4	1	—	—
Reset rise time	t_{rRES}	us	Figure 4	—	—	10

T.B.D.

RGB interface timing characteristics

18/16 bit RGB interface (HWM =1), Vcc = 1.8V to 2.4V

Item	Symbol	Unit	Test Condition	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 5	0	—	1
ENABLE Set up time	tENS	ns	Figure 5	20	—	—
ENABLE Hold time	tENH	ns	Figure 5	80	—	—
VLD Set up time	tVLS	ns	Figure 5	20	—	—
VLD Hold time	tVLH	ns	Figure 5	80	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 5	90	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 5	90	—	—
DOTCLK cycle time	tCYCD	ns	Figure 5	200	—	—
Data Set up time	tPDS	ns	Figure 5	20	—	—
Data Hole time	tPDH	ns	Figure 5	80	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 5	—	—	25

T.B.D.

18/16 bit RGB interface (HWM = 1), Vcc = 2.4V to 3.7 V

Item	Symbol	Unit	Test Condition	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 5	0	—	1
ENABLE Set up time	tENS	ns	Figure 5	10	—	—
ENABLE Hold time	tENH	ns	Figure 5	20	—	—
VLD Set up time	tVLS	ns	Figure 5	10	—	—
VLD Hold time	tVLH	ns	Figure 5	40	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 5	40	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 5	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 5	100	—	—
Data Set up time	tPDS	ns	Figure 5	10	—	—
Data Hole time	tPDH	ns	Figure 5	40	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 5	—	—	25

T.B.D.

6 bit RGB interface (HWM = 1), Vcc = 1.8V to 2.4 V

Item	Symbol	Unit	Test Condition	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 5	0	—	1
ENABLE Set up time	tENS	ns	Figure 5	20	—	—
ENABLE Hold time	tENH	ns	Figure 5	50	—	—
VLD Set up time	tVLS	ns	Figure 5	20	—	—
VLD Hold time	tVLH	ns	Figure 5	65	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 5	50	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 5	50	—	—
DOTCLK cycle time	tCYCD	ns	Figure 5	120	—	—
Data Set up time	tPDS	ns	Figure 5	20	—	—
Data Hold time	tPDH	ns	Figure 5	65	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 5	—	—	25

T.B.D.

6 bit RGB interface (HWM = 1), Vcc = 2.4V to 3.3 V

Item		Symbol	Unit	Test Condition	min.	typ.	max.
VSYNC/HSYNC Set up time		tSYNCS	clock	Figure 5	0	—	1
ENABLE Set up time		tENS	ns	Figure 5	10	—	—
ENABLE Hold time		tENH	ns	Figure 5	20	—	—
VLD Set up time		tVLS	ns	Figure 5	10	—	—
VLD Hold time	Vcc=2,4 to2,7V	tVLH	ns	Figure 5	40	—	—
	Vcc=2,7 to 3,7V	tVLH	ns	Figure 5	30	—	—
DOTCLK “Low” Level pulse width		PWDL	ns	Figure 5	30	—	—
DOTCLK “High” Level pulse width		PWDH	ns	Figure 5	30	—	—
DOTCLK cycle time		tCYCD	ns	Figure 5	70	—	—
Data Set up time		tPDS	ns	Figure 5	10	—	—
Data Hole time	Vcc=2,4 to 2,7V	tPDH	ns	Figure 5	40	—	—
	Vcc=2,7 to 3,7V	tPDH	ns	Figure 5	30	—	—
DOTCLK, VSYNC, HSYNC rising and falling time		trgbr, trgbf	ns	Figure 5	—	—	25

T.B.D.

Liquid crystal driver output characteristics

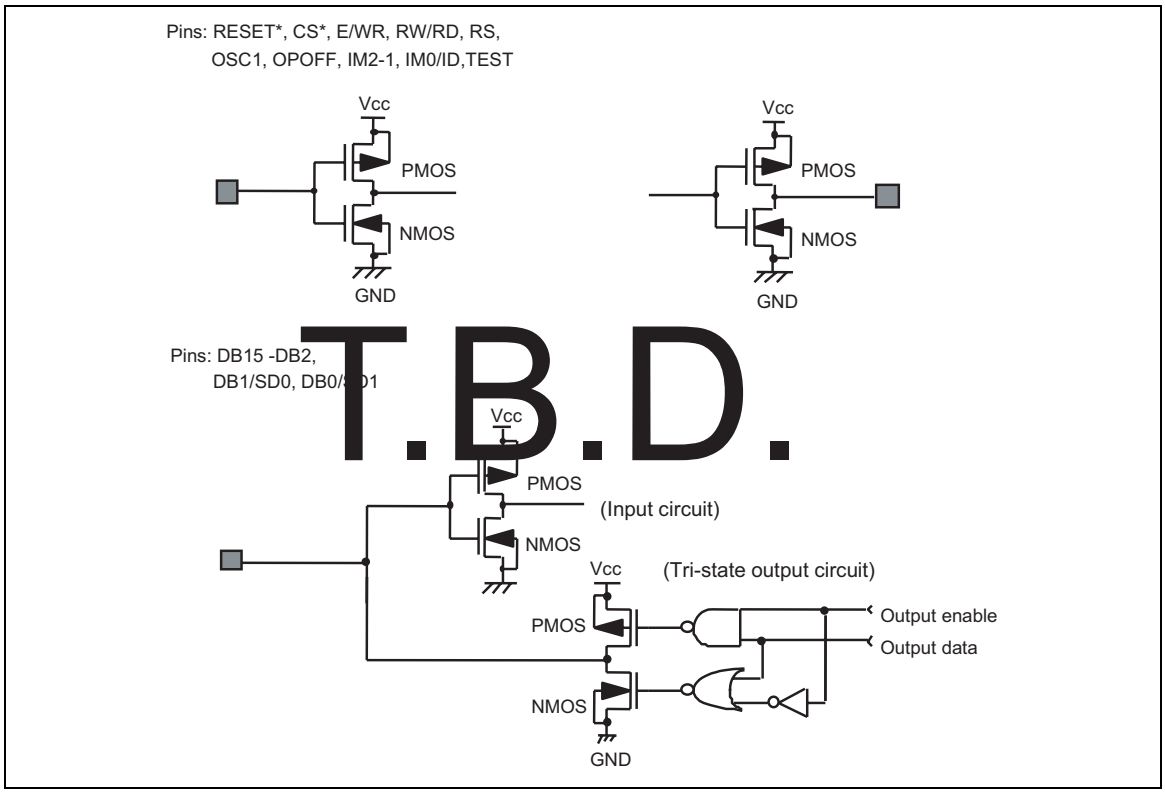
Item	Symbol	Unit	Test conditions	min.	typ.	max.	Note
Driver output delay time	tdd	µs	Vcc=3V, VLCD=5.5V, VDH=5.0V, CR oscillation ;fosc=270kHz(240 lines), Ta=25℃, REV="0", SAP="001", VRN4-0="0",VRP4-0="0" PKP52-00="0",PRP12-00="0" PKP52-00="0",PRP12-00="0" All pins changes at the same time from same grayscale. The time till output level reaches ±35mV when VCOM polarity changes. Load resistance R=10kΩ、 Load capacitance C=20pF	—	40	—	(11)

T.B.D.

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.

2. The following three circuits are I pin, I/O pin, O pin configurations.



T.B.D.

T.B.D.

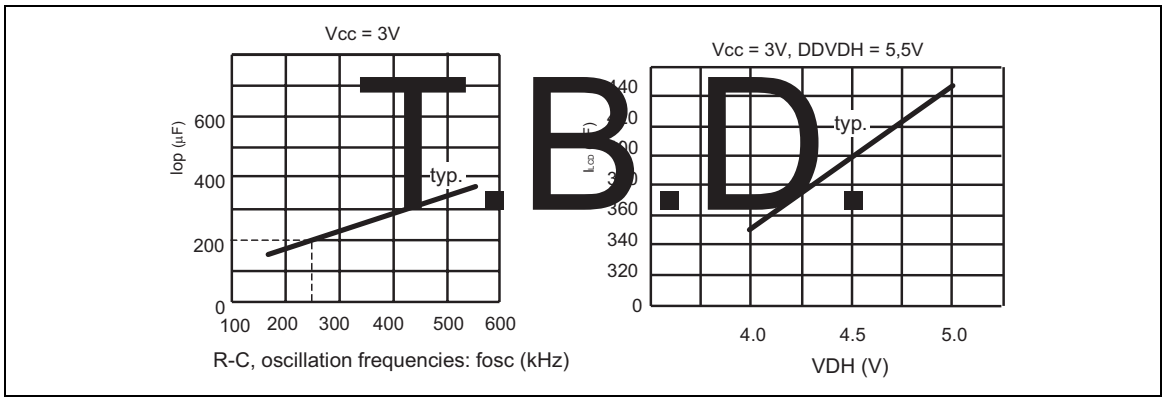
3. The TEST pin must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.

4. Applies to the resistor value (RSEG) between VSH, GND pins and segment signal pins.

T.B.D.

5. This excludes the current flowing through output drive MOSs. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.

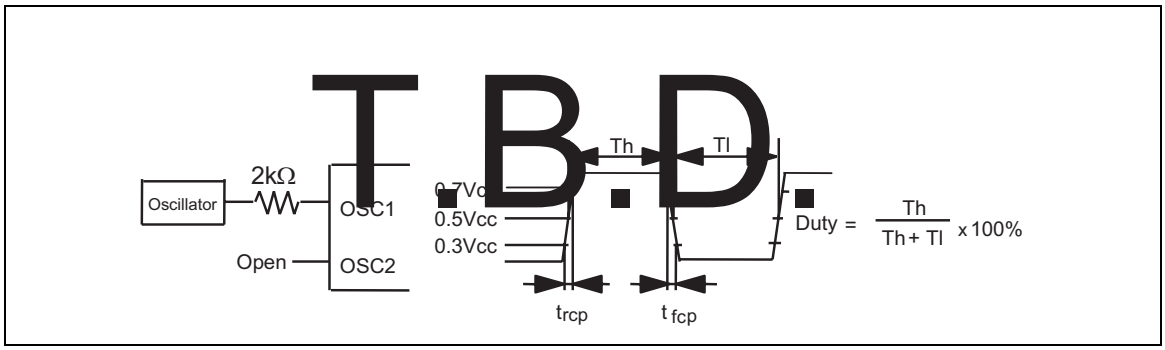
6. The following figure shows the relationship between the operation frequency and current consumption.



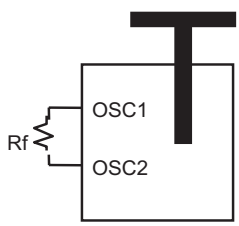
7. This is a voltage difference for the neighboring outputs under the same display condition. The output voltage deviation is a reference value.

8. The fluctuation of average output voltage indicates the difference of average output voltage between chips. The average output voltage is an average voltage within a chip under the same display condition.

9. Applies to the case when clocks are supplied internally (figure).



10. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



T.B.D.

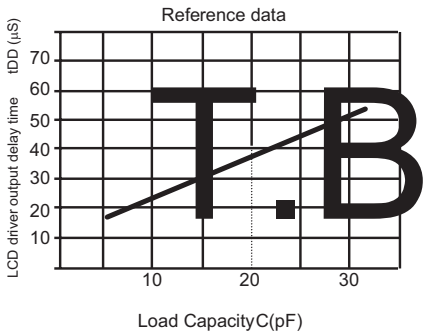
The oscillation frequency may vary depending on the capacitors for OSC1, OSC2 pins.
Place OSC1 and OSC2 close to each other.

External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance	R-C Oscillation Frequency: fosc				
(Rf)	Vcc = 1.8 V	Vcc = 2 V	Vcc = 2.4 V	Vcc = 3 V	Vcc = 3.3 V
110 kΩ	299	333	372	401	411
150 kΩ	234	258	284	305	311
180 kΩ	202	222	243	258	263
200 kΩ	186	20[illegible]	222	235	240
240 kΩ	160	17[illegible]	188	198	202
270 kΩ	145	15[illegible]	169	177	181
300 kΩ	132	143	153	161	163
390 kΩ	106	113	121	126	128
430 kΩ	97	104	110	115	116

T.B.D.

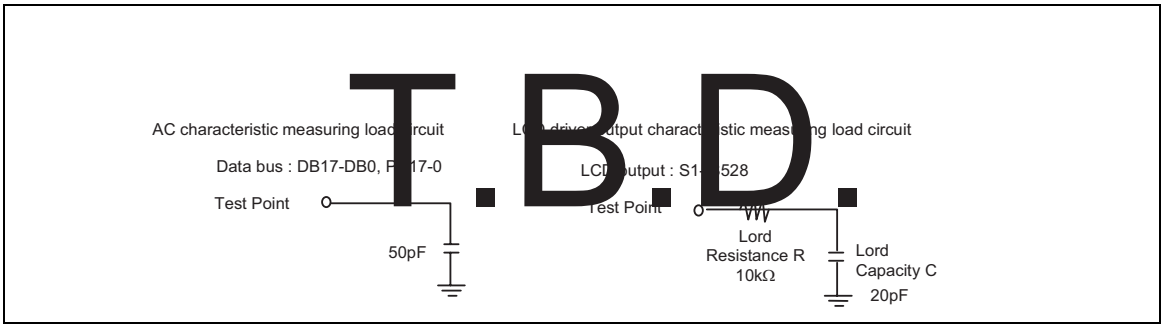
11. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



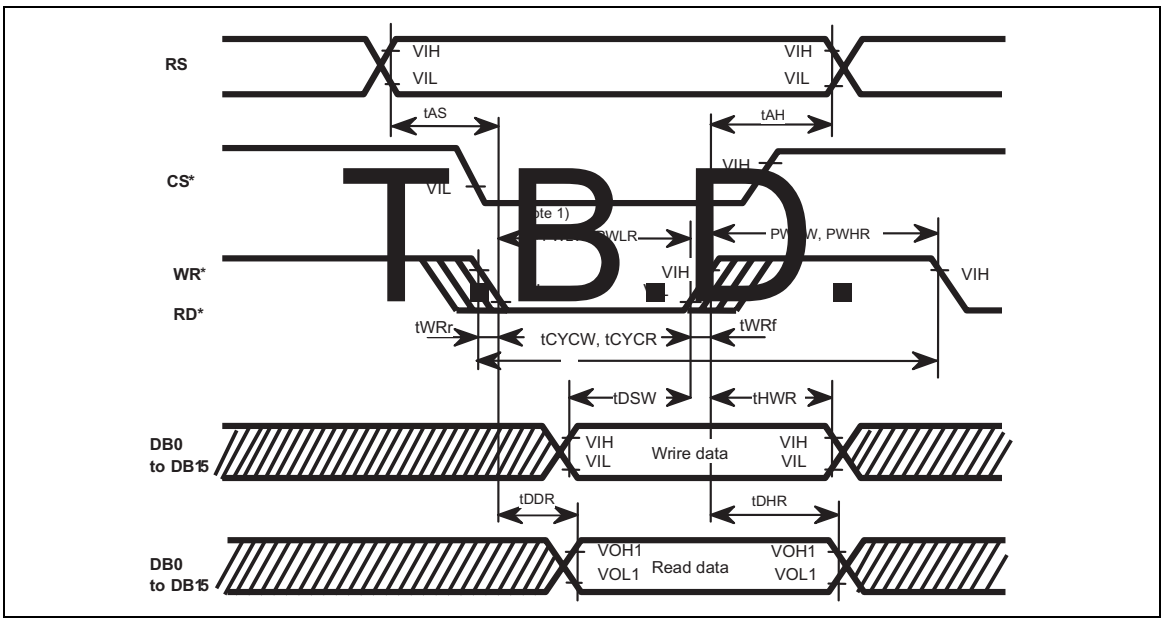
T.B.D.

Vcc =3V, VLCD = 5.5V, VDH = 5.0V,
R-C Oscillation; fosc = 270kHz (240line),
Ta = 25 Centigrade, REV = "0", SAP ="001",
VRN4-0 = "0", VRP4-0 = "0",
PKP52-00 = "0", PRP12-00 ="0",
PKN52-00 = "0", PRN12-00 ="0",
All pins change at the same time from same grayscale.
The time till output level reaches +/-35mV when VCOM polarity changes.
Load resistance R = 10kΩ/pin

Load circuits for measuring AC characteristics



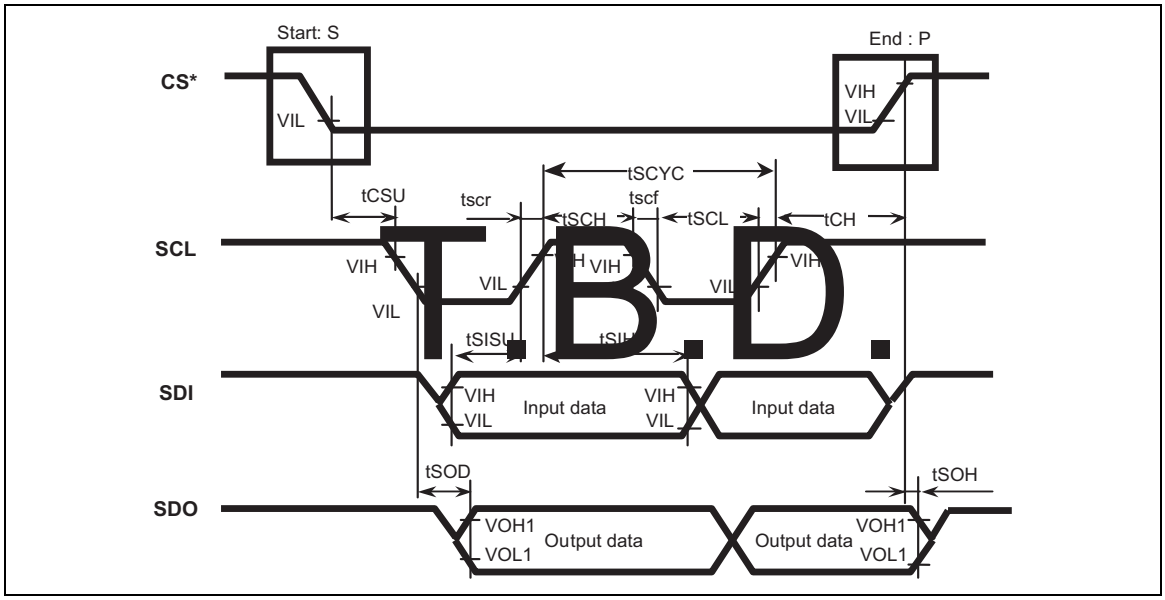
80-system Bus Operation



Note 1) PWLW and PWLR is specified in the overlapped period when CS* is low and WR* or RD* is low.

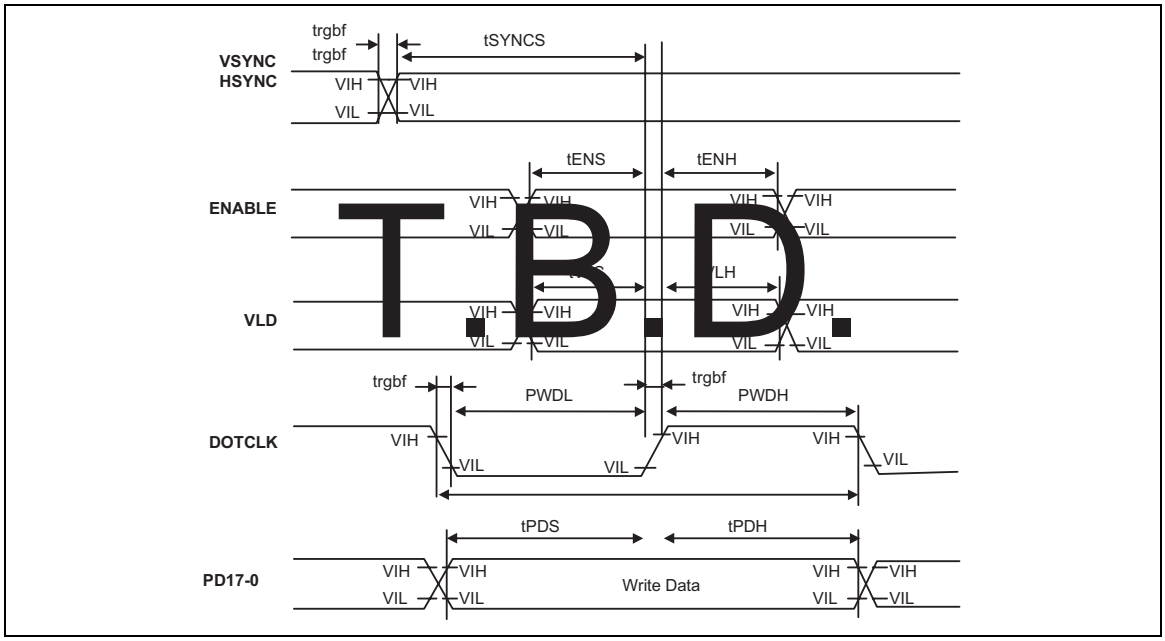
Note 2) Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used. Fix the DB7-0 pins to Vcc or GND.

Clock Synchronized Serial Interface Operation

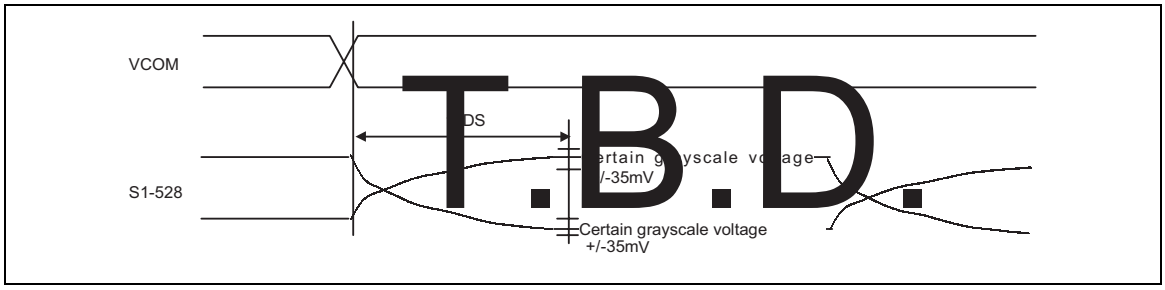


RESET Operation

RGB I/F Operation



Liquid Crystal Driver Output



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Colophon 0.0

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.1	2003.05.08	First issue		