DATA SHEET

NEC

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS

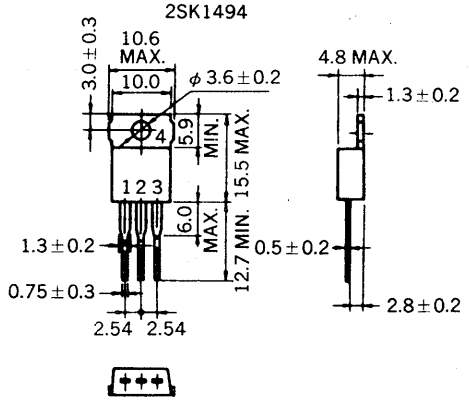
2SK1493,2SK1493-Z/2SK1494,2SK1494-Z

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

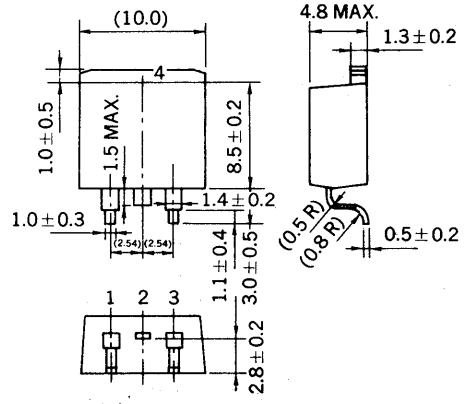
PACKAGE DIMENSIONS

(Unit: mm)

2SK1493
2SK1494

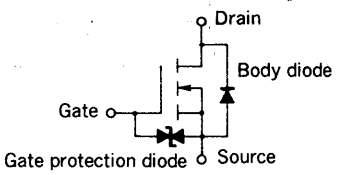


2SK1493-Z
2SK1494-Z



PIN CONNECTIONS

1. Gate
2. Drain
3. Source
4. Fin (Drain)



DESCRIPTION

The 2SK1495/2SK1496 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 2.8 Ω MAX./3.0 Ω MAX. (V_{GS} = 10 V, I_D = 3 A)
- Low C_{iss} C_{iss} = 350 pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Storage Temperature	T_{stg}	−55 to +150	°C
Channel Temperature	T_c	150	°C MAX.
Maximum power Dissipation			
Total Power Dissipation (T_A = 25 °C)	P_T	50	W
Maximum Voltages and Currents (T_A = 25 °C)			
Drain to Source Voltage	V_{DSS}	450/500 (2SK1493/2SK1494)	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±3	A
Drain Current (pulse)	$I_{D(pulse)}$*	±12	A

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

Maximum Avalanche Capability Ratings**			
Single Avalanche Current	I_{AS}	4.5	A
Single Avalanche Energy	E_{AS}	57	mJ

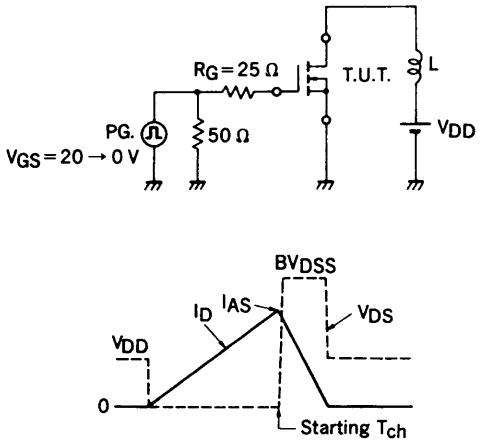
** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

Document No. D13000EJ2V0DS00(2nd edition)
(Previous No. TC-2375)
Date Published October 1997 M
Printed in Japan

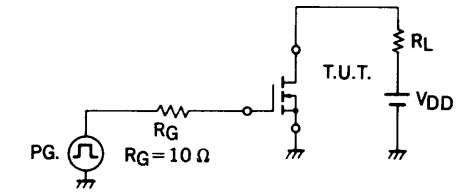
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

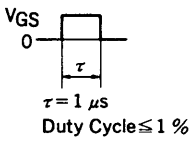
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		2.2	2.8	Ω	V_{GS} = 10 V, I_D = 2 A
(2SK1493/2SK1494)			2.4	3.0	Ω	
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	1.0			S	V_{DS} = 10 V, I_D = 2 A
Drain Leackage Current	I_{DSS}			100	μA	V_{DS} = 450 V/500 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		350		pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output Capacitance	C_{oss}		120		pF	
Reverse Transfer Capacitance	C_{rss}		45		pF	
Turn-On Delay Time	$t_{d(on)}$		5		ns	V_{GS} = 10 V, V_{DD} = 150 V, I_D = 2 A, R_G = 10 Ω, R_L = 75 Ω
Rise Time	t_r		10		ns	
Turn-Off Delay Time	$t_{d(off)}$		30		ns	
Fall Time	t_f		15		ns	
Total Gate Charge	Q_G		12		nC	V_{GS} = 10 V, I_D = 3 A, V_{DD} = 400 V
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		7		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 3 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		310		ns	I_F = 3 A, di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		1.2		μC	

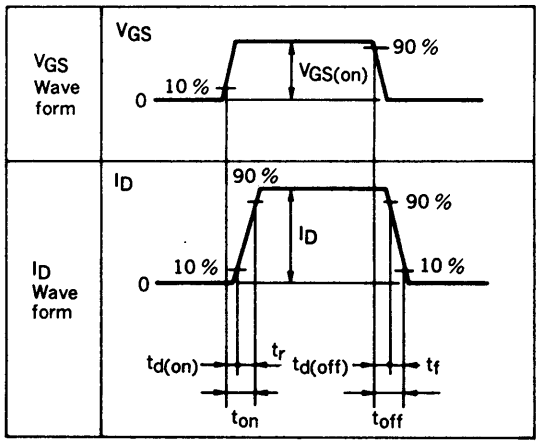
Test Circuit 1: Avalanche Capability



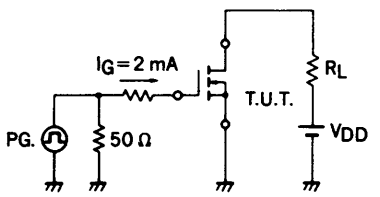
Test Circuit 2: Switching Time





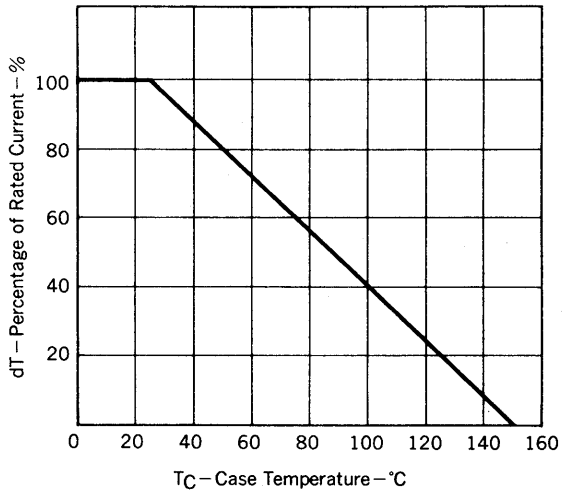


Test Circuit 3: Gate Charge

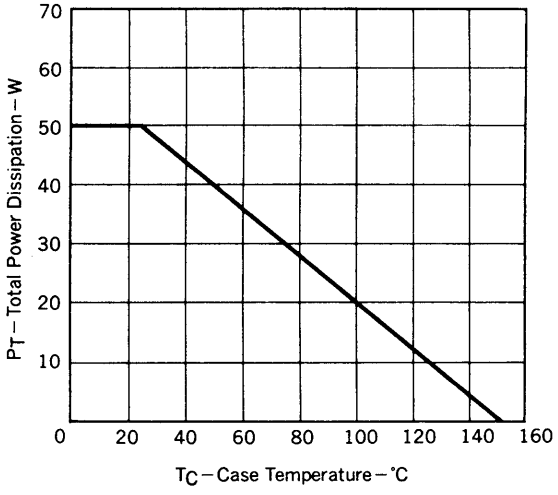


TYPICAL CHARACTERISTICS (T_A = 25 °C)

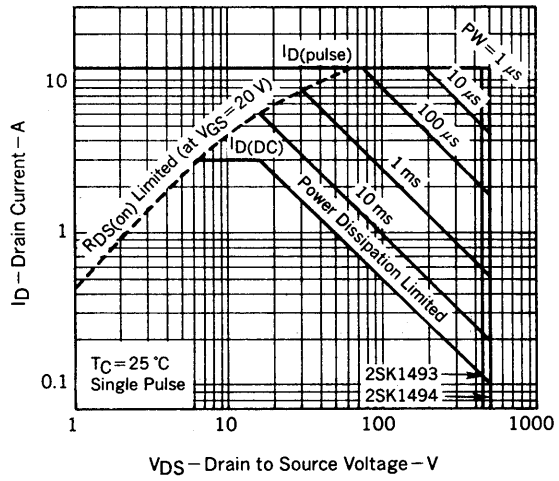
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



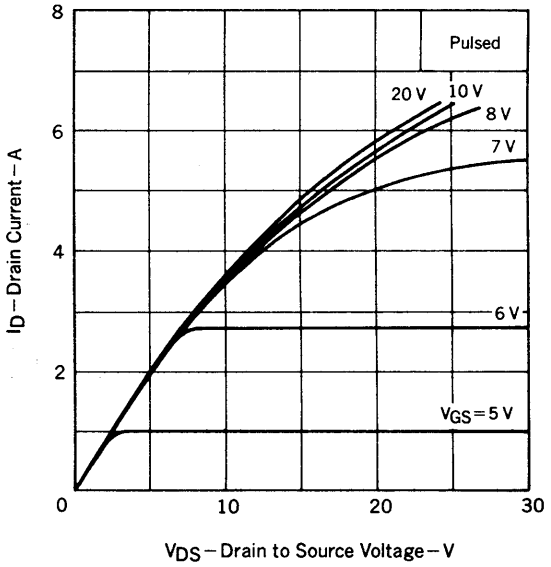
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



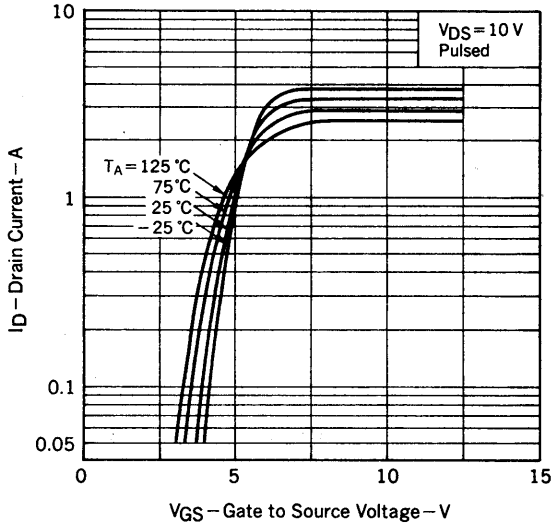
FORWARD BIAS SAFE OPERATING AREA



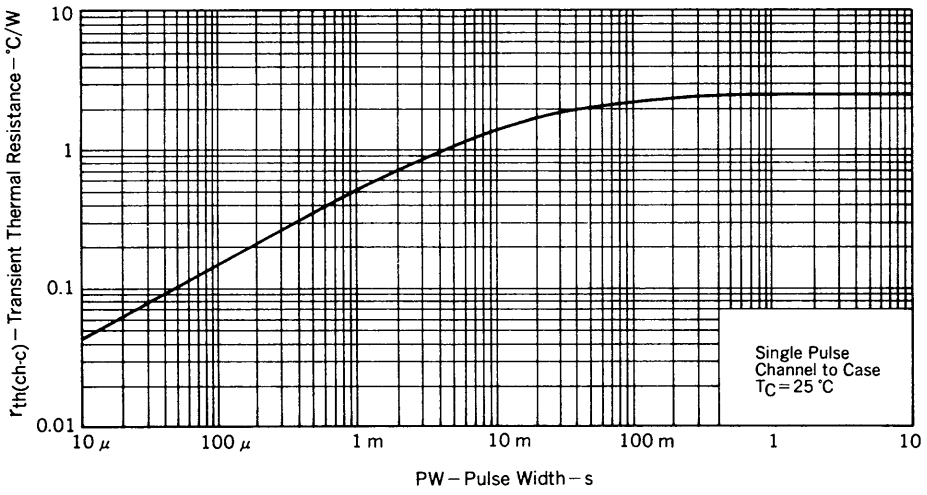
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



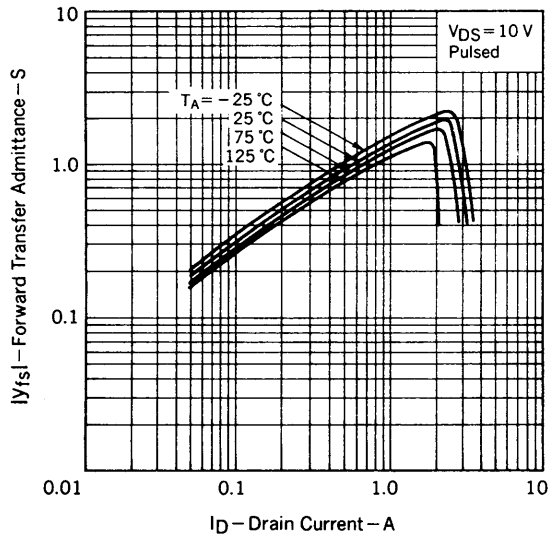
TRANSFER CHARACTERISTICS



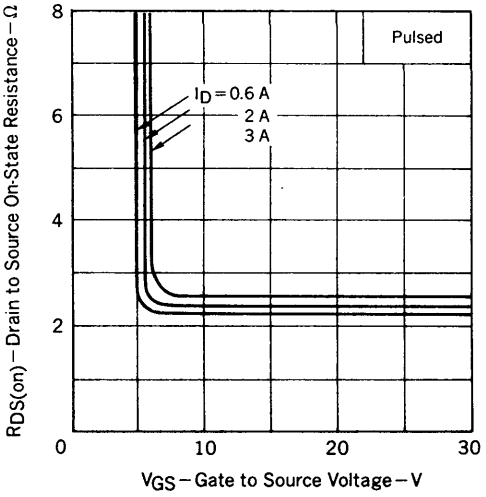
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



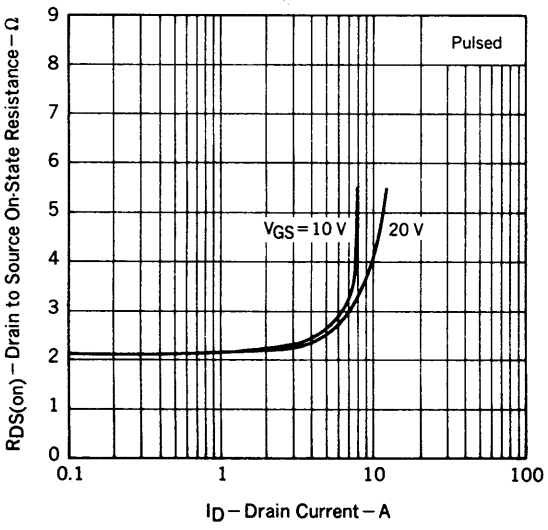
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



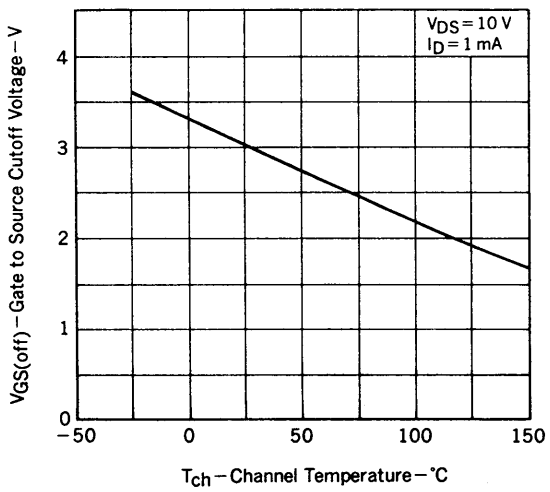
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



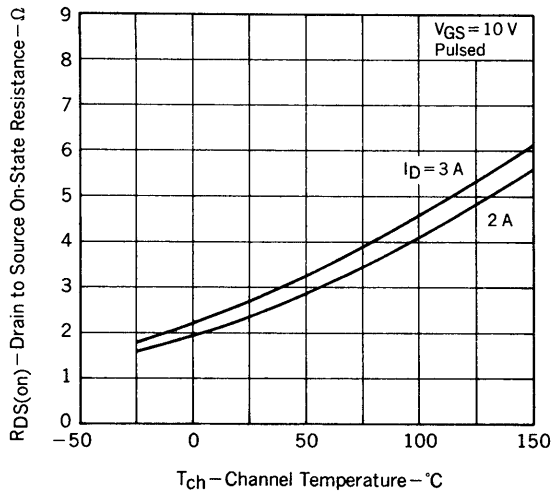
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



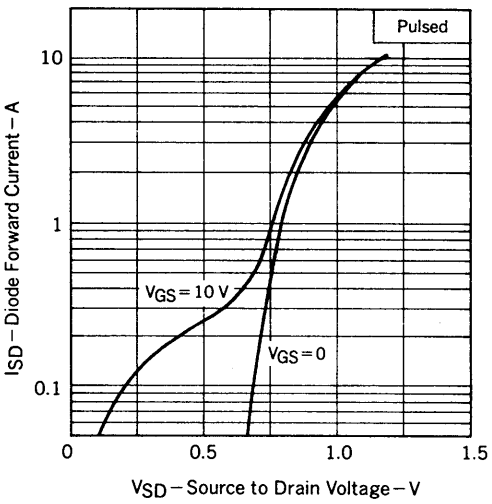
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



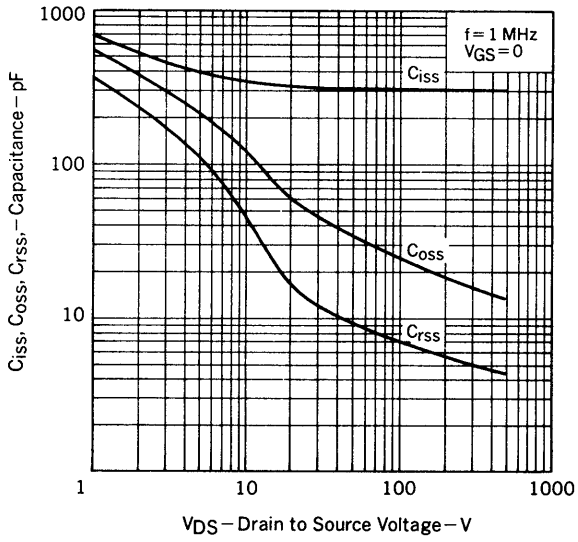
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



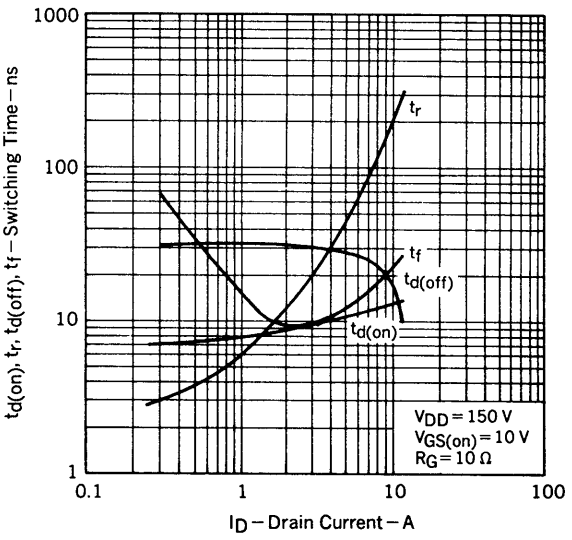
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



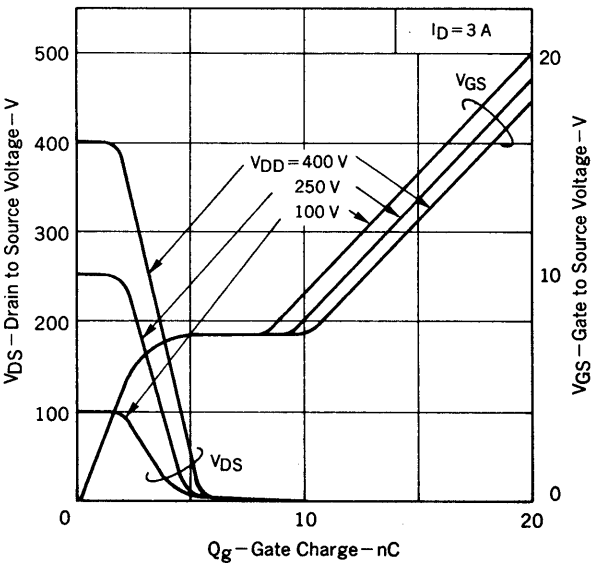
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



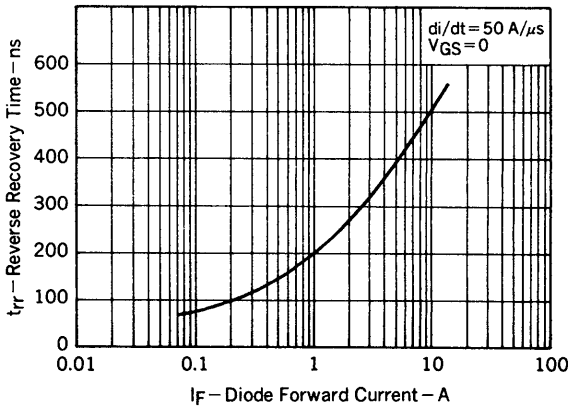
SWITCHING CHARACTERISTICS



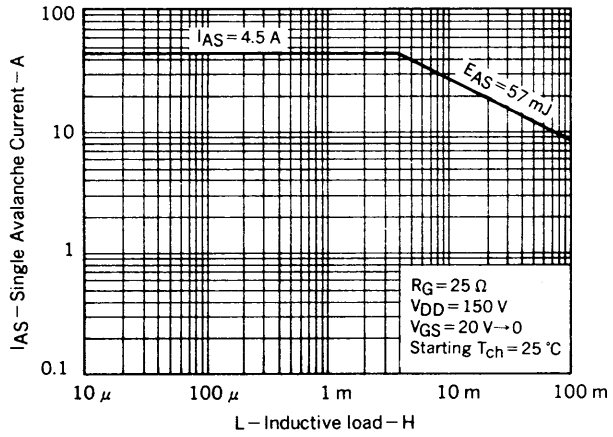
DYNAMIC INPUT CHARACTERISTICS



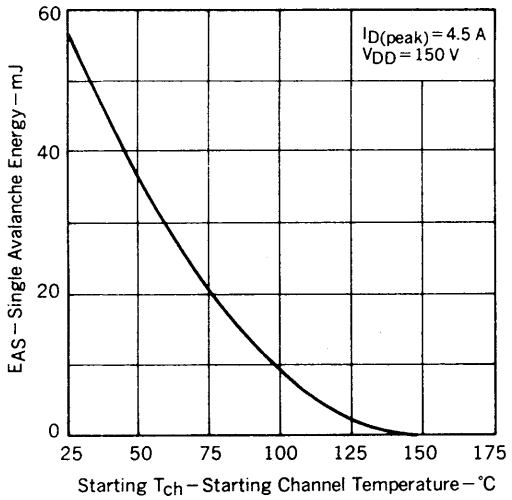
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



REFERENCE

Application note name	No.
Guide to quality assurance for semiconductor device	MEI-1202
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

[MEMO]

M4 96.5