

Low-Power Audio Amplifier for Telephone Applications

Description

The integrated circuit, U4083B, is a low-power audio amplifier for telephone loudspeakers. It has differential speaker outputs to maximize the output swing at low supply voltages. There is no need for coupler capacitors.

The U4083B has an open loop gain of 80 dB whereas the closed loop gain is adjusted with two external resistors. A chip disable pin permits powering down and/or muting the input signal.

Features

- Wide operating voltage range: 2 to 16 V
- Battery-powered application due to low quiescent supply current: 2.7 mA typical
- Chip disable input to power down the integrated circuit
- Low power-down quiescent current
- Drives a wide range of speaker loads
- Output power, $P_o = 250 \text{ mW} @ R_L = 32 \Omega$ (speaker)
- Low harmonic distortion (0.5% typical)
- Wide gain range: 0 dB to 46 dB

Benefits

- Low number of external components
- Low current consumption

Block Diagram / Application Circuit

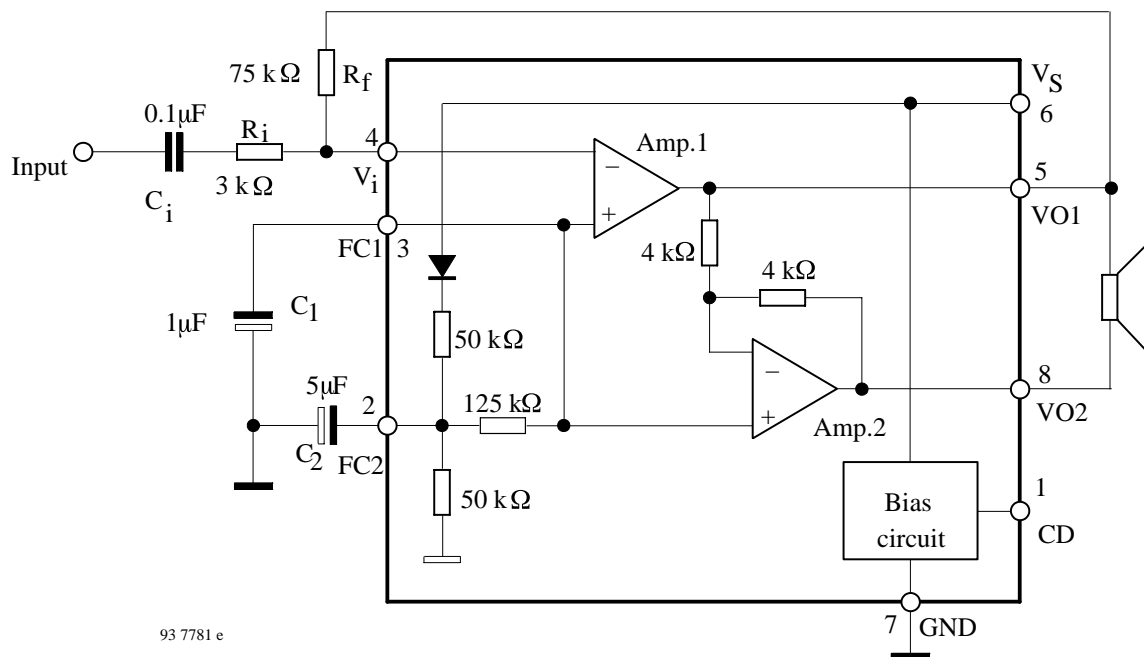
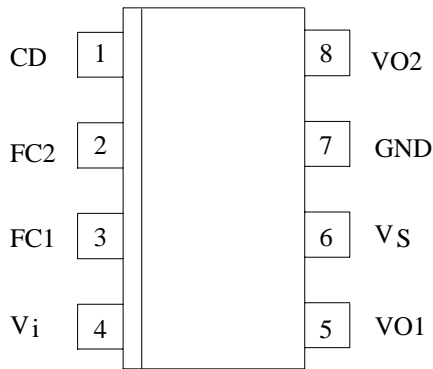


Figure 1. Block diagram/ application circuit

Order Information

| Extended Type Number | Package | Remarks |
|----------------------|---------|------------------|
| U4083B-AFP | SO8 | Tube |
| U4083B-AFPG3 | SO8 | Taped and reeled |

Pin Description



94 8022

Figure 2. Pinning

| Pin | Symbol | Function |
|-----|--------|-----------------------------------|
| 1 | CD | Chip disable |
| 2 | FC2 | Filtering, power supply rejection |
| 3 | FC1 | Filtering, power supply rejection |
| 4 | V_i | Amplifier input |
| 5 | VO1 | Amplifier output 1 |
| 6 | V_S | Voltage supply |
| 7 | GND | Ground |
| 8 | VO2 | Amplifier output 2 |

Functional Description Including External Circuitry

Pin 1: Chip disable – digital input (CD)

Pin 1 (chip disable) is used to power down the IC to conserve power or muting or both.

Input impedance at Pin 1 is typically 90 k Ω .

Logic 0 < 0.8 V IC enabled (normal operation)

Logic 1 > 2 V IC disabled

Figure 15 shows the power supply current diagram. The change in differential gain from normal operation to muted operation (muting) is more than 70 dB.

Switching characteristics are as follows:

turn-on time $t_{on} = 12$ to 15 ms

turn-off time $t_{off} \leq 2$ μ s

They are independent of C_1 , C_2 and V_S .

Voltages at Pins 2 and 3 are supplied from V_S and therefore do not change when the U4083B is disabled. Outputs – V_{O1} (Pin 5) and V_{O2} (Pin 8) – turn to a high impedance condition by removing the signal from the speaker.

When signals are applied from an external source to the outputs (disabled), they must not exceed the range between the supply voltage, V_S , and ground.

Pins 2 and 3: Filtering, power supply rejection

Power supply rejection is provided by capacitors C_1 and C_2 at Pin 3 and Pin 2, respectively. C_1 is dominant at high frequencies whereas C_2 is dominant at low frequencies (figures 4 to 7). The values of C_1 and C_2 depend on the conditions of each application. For example, a line-powered speakerphone (telephone amplifier) will require more filtering than a system powered by regulated power supply.

The amount of rejection is a function of the capacitors and the equivalent impedance at Pin 3 and Pin 2 (see electrical characteristic equivalent resistance, R).

Apart from filtering, capacitors C_1 and C_2 also influence the turn-on time of the circuit at power-up since capacitors are charged up through the internal resistors (50 k Ω and 125 k Ω) as shown in the block diagram.

Figure 1 shows turn-on time versus C_2 at $V_S = 6$ V, for two different C_1 values.

Turn-on time is 60% longer when $V_S = 3$ V and 20% shorter when $V_S = 9$ V.

Turn-off time is less than 10 μ s

Pin 4: Amplifier input V_i

Pin 5: Amplifier output 1 V_{O1}

Pin 8: Amplifier output 2 V_{O2}

There are two identical operational amplifiers. Amp.1 has an open-loop gain ≥ 80 dB at 100 Hz (figure 2), whereas the closed-loop gain is set by external resistors, R_f and R_i (figure 3). The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. A closed-loop gain of 46 dB is recommended for a frequency range of 300 to 3400 Hz (voice band). Amp.2 is internally set to a gain of -1.0 (0 dB). The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. Output voltage swing is between 0.4 V and $V_S - 1.3$ V at maximum current (figures 18 and 19).

The output dc offset voltage between Pins 5 and 8 ($V_{O1} - V_{O2}$) is mainly a function of the feedback resistor, R_f , because the input offset voltage of the two amplifiers neutralize each other.

Bias current of Amp. 1 which is constant with respect to V_S , however, flows out of Pin 4 (V_i) and through R_f , forcing V_{O1} to shift negative by an amount equal to $R_f I_B$ and V_{O2} positive to an equal amount.

The output offset voltage specified in the electrical characteristics is measured with the feedback resistor ($R_f = 75$ k Ω) shown in typical application circuit. It takes into account bias current as well as internal offset voltages of the amplifiers.

Pin 6: Supply and power dissipation

Power dissipation is shown in figures 8 to 10 for different loads. Distortion characteristics are given in figures 11 to 13.

$$P_{\text{totmax}} = \frac{T_{\text{jmax}} - T_{\text{amb}}}{R_{\text{thJA}}}$$

where

T_{jmax} = Junction temperature = 140°C

T_{amb} = Ambient temperature

R_{thJA} = Thermal resistance, junction-ambient

Power dissipated within the IC in a given application is found from the following equation:

$$P_{\text{tot}} = (V_S \times I_S) + (I_{\text{RMS}} \times V_S) - (R_L \times I_{\text{RMS}}^2)$$

I_S is obtained from figure 15

I_{RMS} is the RMS current at the load R_L .

The IC's operating range is defined by a peak operating load current of ± 200 mA (figures 8 to 13). It is further specified with respect to different loads (see figure 14). The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the integrated circuit. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above mentioned equation.

Layout Considerations

Normally, a snubber is not needed at the output of the IC, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and be not more than a few cm (or inches) in length.

Absolute Maximum Ratings

Reference point Pin 7, $T_{\text{amb}} = 25^\circ\text{C}$ unless otherwise specified.

| Parameters | Symbol | Value | Unit |
|--|------------------|-------------------|------|
| Supply voltage Pin 6 | V_S | -1.0 to +18 | V |
| Voltages Pins 1, 2, 3 and 4 | | -1.0 to (VS +1.0) | V |
| Disabled Pins 5 and 8 | | -1.0 to (VS +1.0) | V |
| Output current Pins 5 and 8 | | ± 250 | mA |
| Junction temperature | T_j | +140 | °C |
| Storage temperature range | T_{stg} | -55 to +150 | °C |
| Ambient temperature range | T_{amb} | -20 to +70 | °C |
| Power dissipation: $T_{\text{amb}} = 60^\circ\text{C}$ SO8 | P_{tot} | 440 | mW |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|----------------------|-------------------|-------|------|
| Junction ambient SO8 | R_{thJA} | 180 | K/W |

Operation Recommendation

| Parameters | Symbol | Value | Unit |
|---------------------------------------|------------------|------------|----------|
| Supply voltage Pin 6 | V_S | 2 to 16 | V |
| Load impedance Pins 5 to 8 | R_L | 8.0 to 100 | Ω |
| Load current | I_L | ± 200 | mA |
| Differential gain (5.0 kHz bandwidth) | ΔG | 0 to 46 | dB |
| Voltage @ CD Pin 1 | V_{CD} | VS | V |
| Ambient temperature range | T_{amb} | -20 to +70 | °C |

Electrical Characteristics

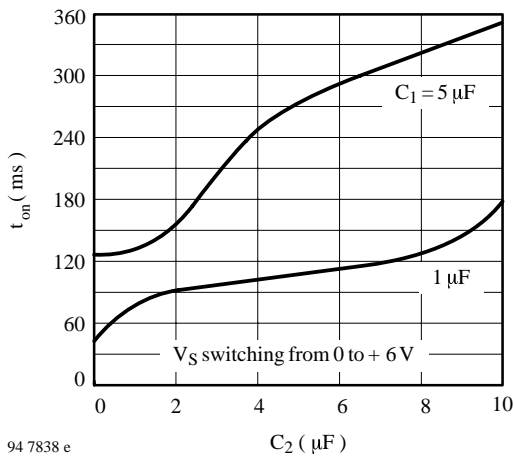
T_{amb} = +25°C, reference point Pin 7, unless otherwise specified

| Parameters | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|--|---|------------------|----------------------|-------------------|----------------|
| Amplifiers (AC Characteristics) | | | | | | |
| Open-loop gain (Amp. 1, f < 100 Hz) | | G _{VOL1} | 80 | | | dB |
| Closed-loop gain (Amp. 2) | V _S = 6.0 V, f = 1.0 kHz, R _L = 32 Ω | G _{V2} | -0.35 | 0 | +0.35 | dB |
| Gain bandwidth product | | G _{BW} | | 1.5 | | MHz |
| Output power | V _S = 3.0 V, R _L = 16 Ω, d < 10% V _S = 6.0 V, R _L = 32 Ω, d < 10% V _S = 12 V, R _L = 100 Ω, d < 10% | P _o P _o P _o | 55 250 400 | | | mW |
| Total harmonic distortion (f = 1.0 kHz) | V _S = 6.0 V, R _L = 32 Ω, P _o = 125 mW V _S > 3.0 V, R _L = 8 Ω, P _o = 20 mW V _S > 12 V, R _L = 32 Ω, P _o = 200 mW | d d d | | 0.5 0.5 0.6 | 1.0 | % |
| Power supply rejection ratio | V _S = 6.0 V, ΔV _S = 3.0 V C ₁ = ∞, C ₂ = 0.01 μF C ₁ = 0.1 μF, C ₂ = 0, f = 1.0 kHz C ₁ = 1.0 μF, C ₂ = 5.0 μF, f = 1.0 kHz | PSRR PSRR PSRR | 50 | 12 52 | | dB |
| Muting | V _S = 6.0 V, 1.0 kHz < f < 20 kHz, CD = 2.0 V | G _{MUTE} | | >70 | | dB |
| Amplifiers (DC Characteristics) | | | | | | |
| Output DC level at V _{O1} , V _{O2} R _f = 75 kW | V _S = 3.0 V, R _L = 16 Ω V _S = 6.0 V V _S = 12 V | V _O V _O V _O | 1.0 | 1.15 2.65 5.65 | 1.25 | V |
| Output high level | I _O = -75 mA, 2.0 V < V _S < 16 V | V _{OH} | | V _S -1 | | V |
| Output low level | I _O = 75 mA, 2.0 V < V _S < 16 V | V _{OL} | | 0.16 | | V |
| Output DC offset voltage (V _{O1} - V _{O2}) | V _S = 6.0 V, R _f = 75 kW, R _L = 32 Ω | ΔV _O | -30 | 0 | +30 | mV |
| Input bias current at V _i | V _S = 6.0 V | -I _{IB} | | 100 | 200 | nA |
| Equivalent resistance at Pin 3 | V _S = 6.0 V | R | 100 | 150 | 220 | kΩ |
| Equivalent resistance at Pin 2 | V _S = 6.0 V | R | 18 | 25 | 40 | kΩ |
| Chip disable Pin 1 Input voltage – low Input voltage – high Input resistance | V _S = V _{CD} = 16 V | V _{IL} V _{IH} R _{CD} | 2.0 50 | 90 | 0.8 175 | V V kΩ |
| Power supply current | V _S = 3.0 V, R _L = ∞, CD = 0.8 V V _S = 16 V, R _L = ∞, CD = 0.8 V V _S = 3.0 V, R _L = ∞, CD = 2.0 V | I _S I _S I _S | | 65 | 4.0 5.0 100 | mA mA μA |

Typical Temperature Performance

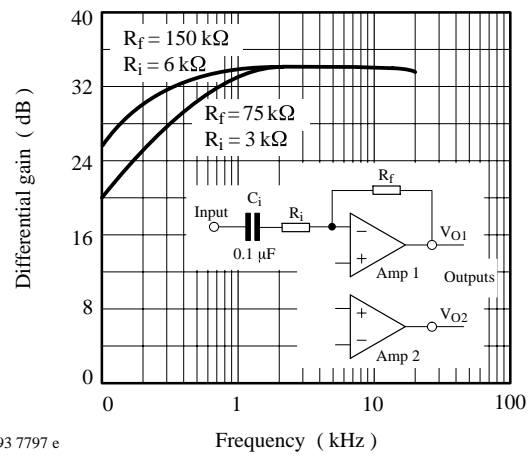
$T_{amb} = -20$ to $+70^{\circ}\text{C}$

| Function | Typical Change | Units |
|--|---------------------|--|
| Input bias current at V_i | ± 40 | $\mu\text{A}/^{\circ}\text{C}$ |
| Total harmonic distortion $V_S = 6.0\text{ V}$, $R_L = 32\ \Omega$, $P_o = 125\text{ mW}$, $f = 1.0\text{ kHz}$ | $+ 0.003$ | $\%/^{\circ}\text{C}$ |
| Power supply current $V_S = 3.0\text{ V}$, $R_L = \infty$, $CD = 0\text{ V}$ $V_S = 3.0\text{ V}$, $R_L = \infty$, $CD = 2.0\text{ V}$ | $- 2.5$ $- 0.03$ | $\mu\text{A}/^{\circ}\text{C}$ $\mu\text{A}/^{\circ}\text{C}$ |



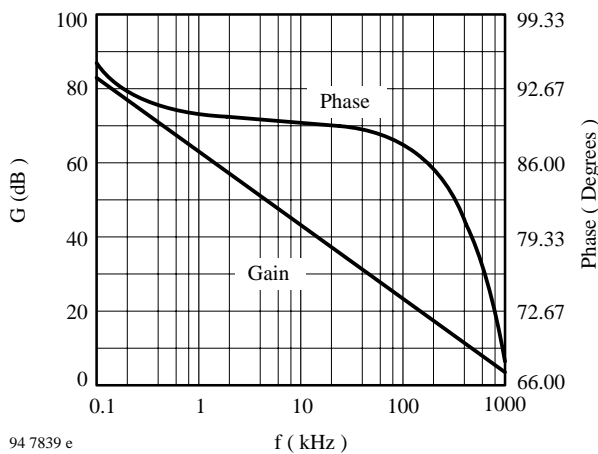
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Figure 1. Turn-on time vs. C_1 , C_2 at power on



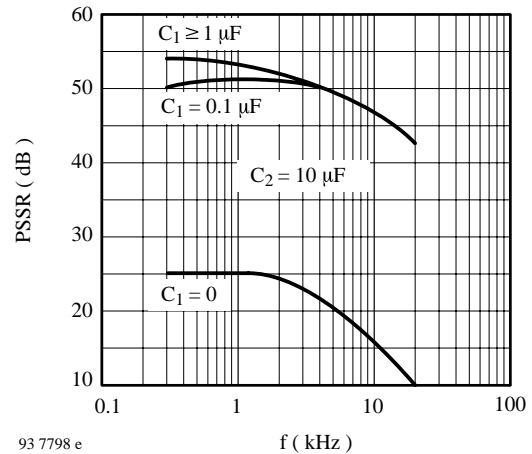
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Figure 3. Differential gain vs. frequency



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Figure 2. Amplifier 1 – open-loop gain and phase



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Figure 4. Power supply rejection vs. frequency

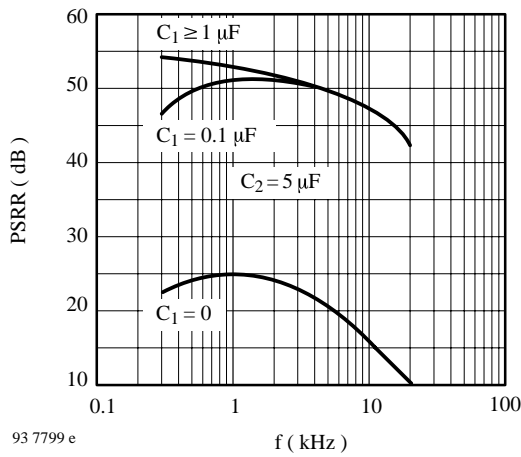


Figure 5. Power supply rejection vs. frequency

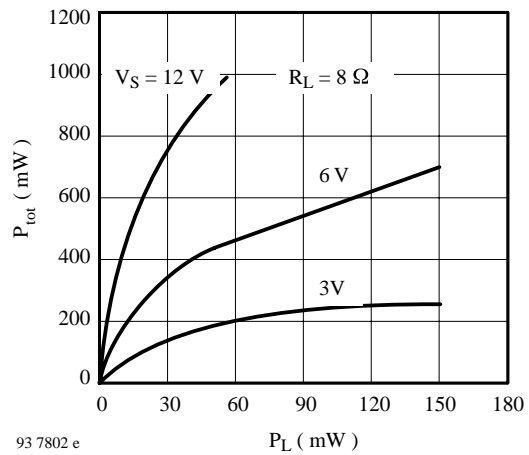


Figure 8. Device dissipation

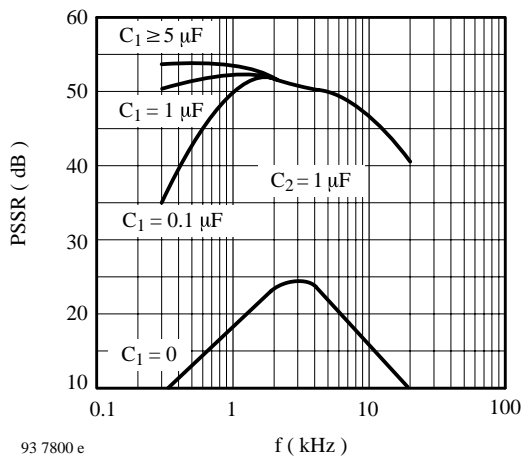


Figure 6. Power supply rejection vs. frequency

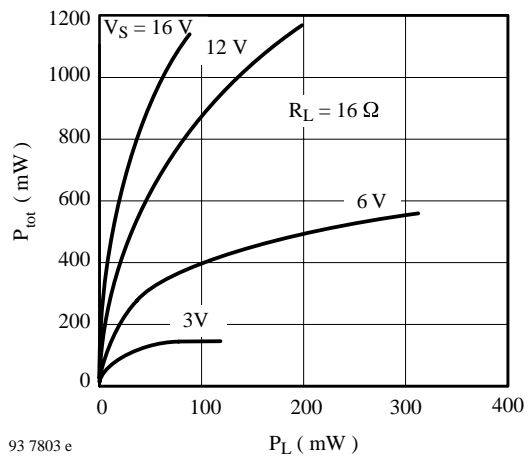


Figure 9. Device dissipation

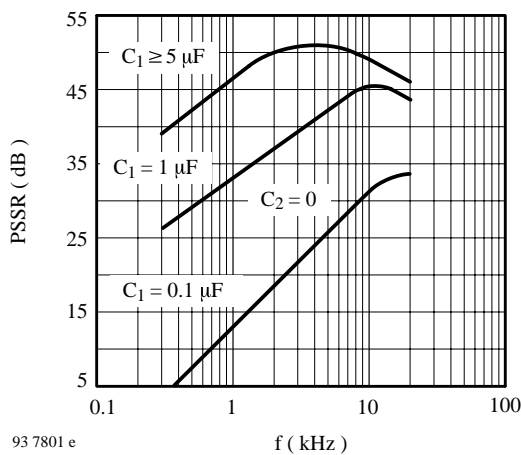


Figure 7. Power supply rejection vs. frequency

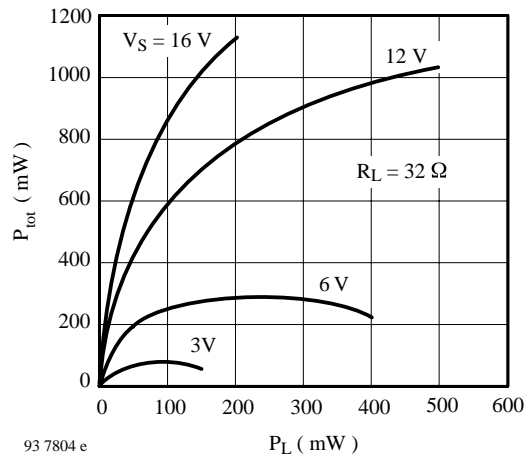


Figure 10. Device dissipation

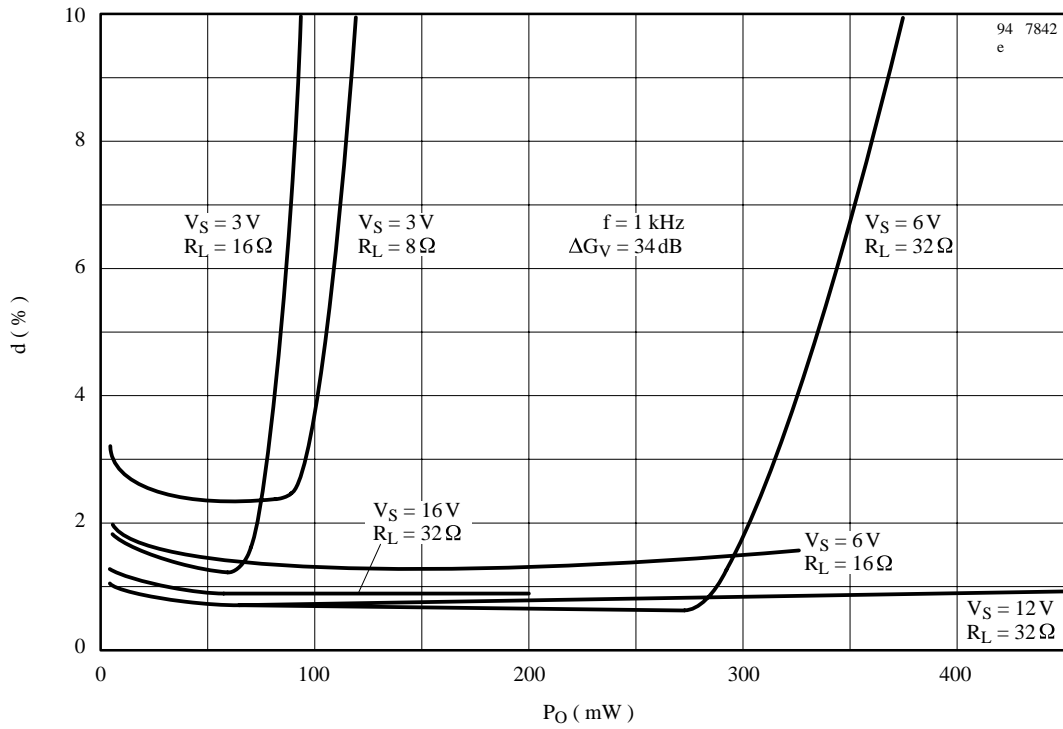


Figure 11. Distortion vs. power

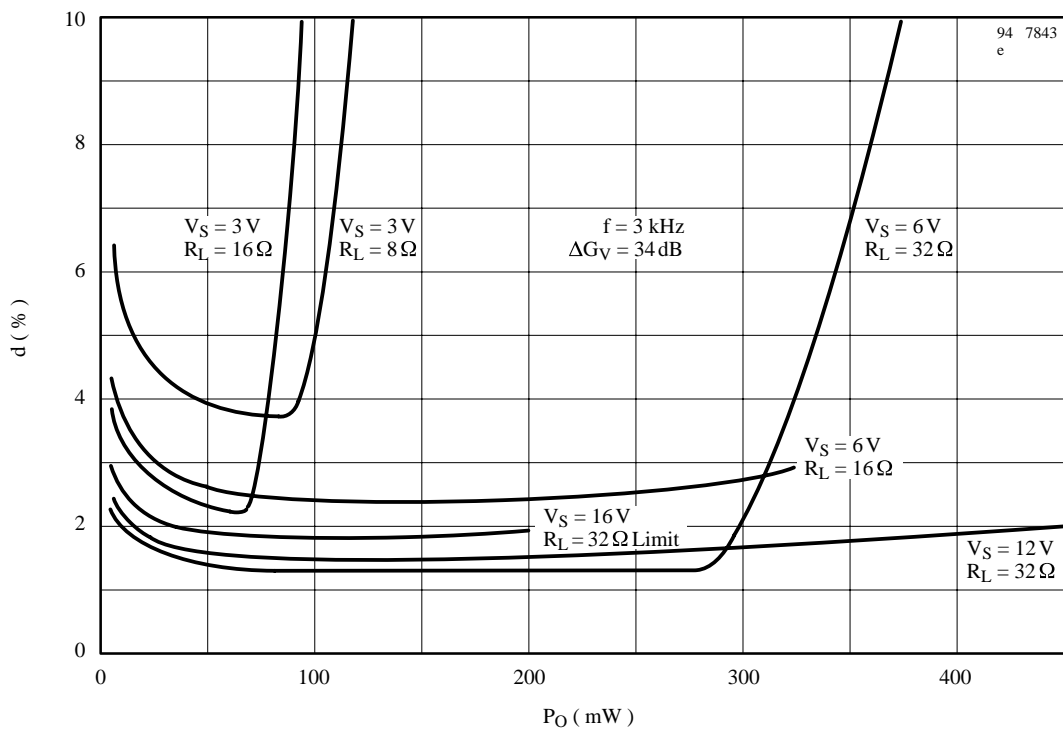


Figure 12. Distortion vs. power

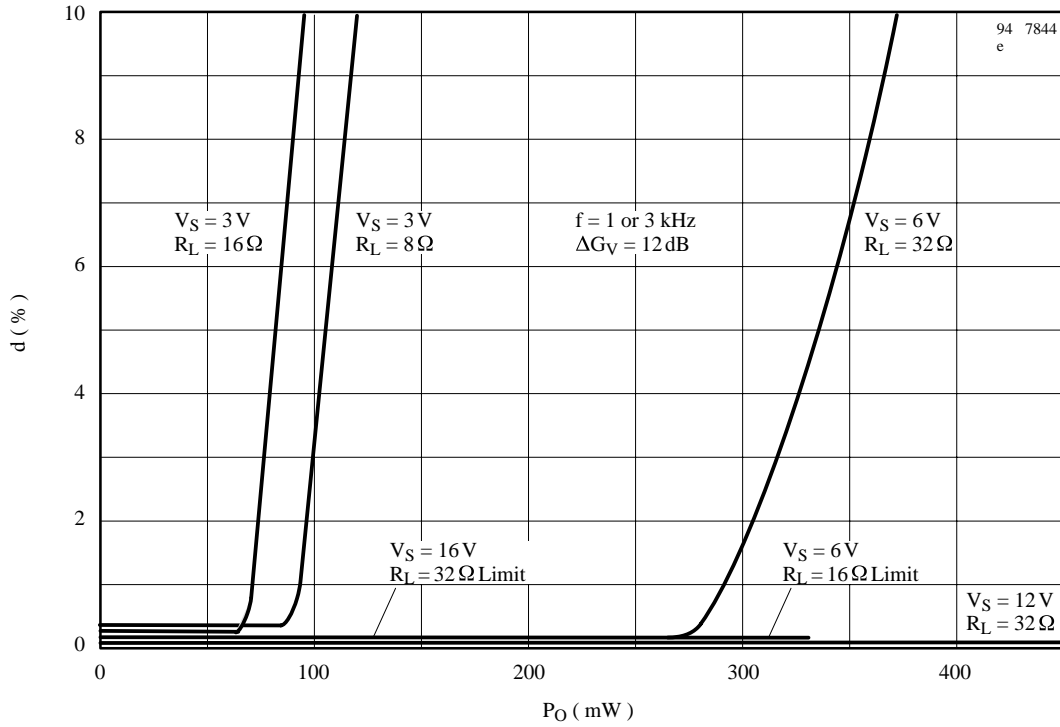


Figure 13. Distortion vs. power

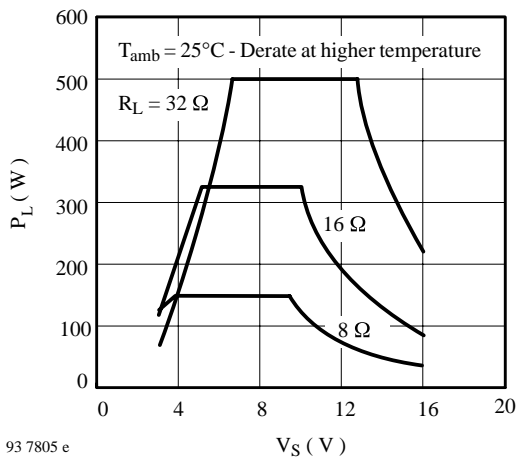


Figure 14. Maximum allowable load power

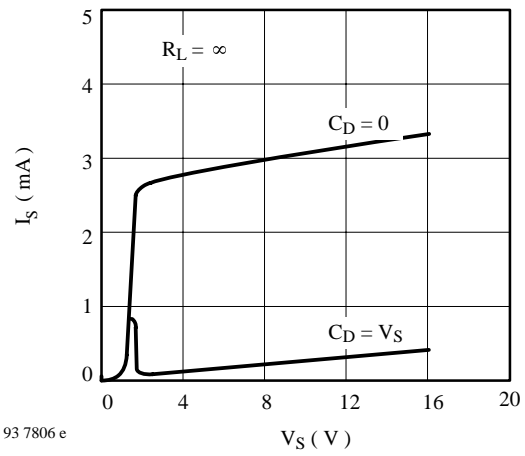


Figure 15. Power-supply current

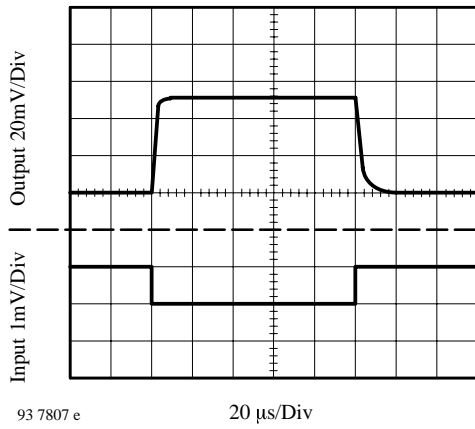


Figure 16. Small signal response

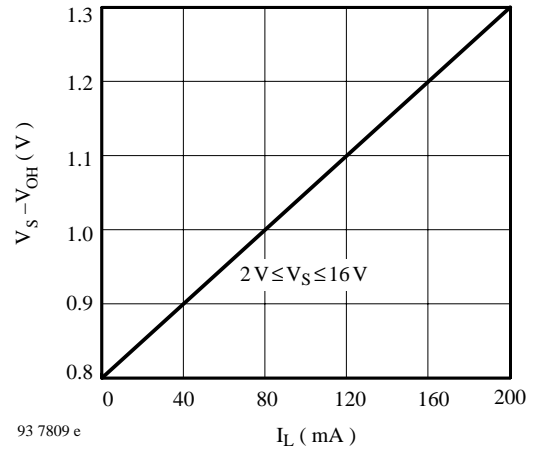


Figure 18. $V_S - V_{OH}$ vs. load current

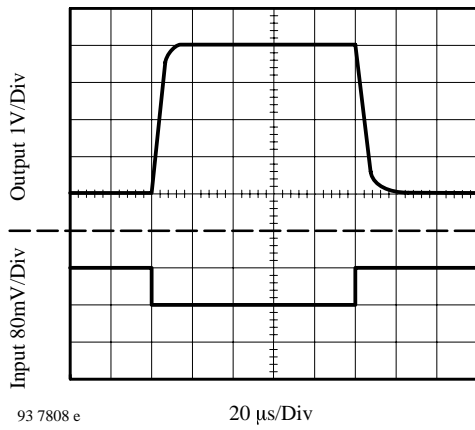


Figure 17. Large signal response

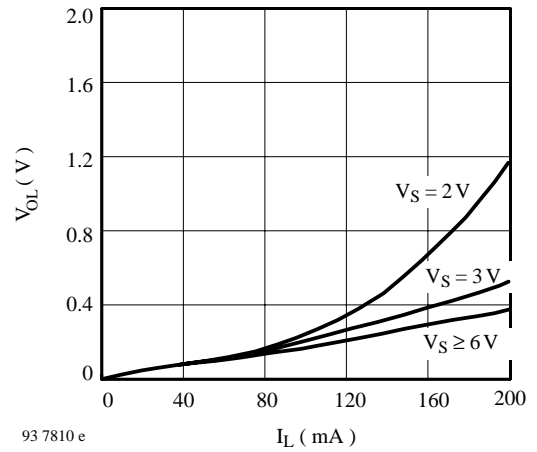
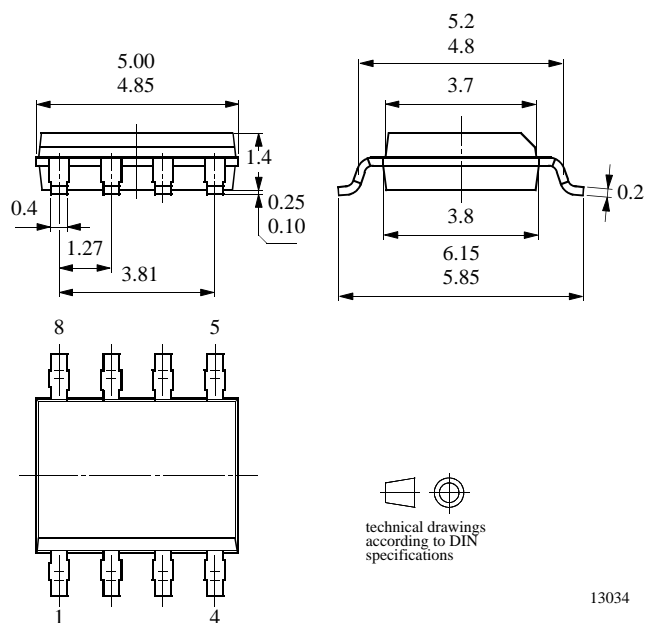


Figure 19. V_{OL} vs. load current

Package Information

Package SO8

Dimensions in mm



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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

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TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423