



## LC3564CM, 3564CT-55U/70U

### 64K (8192-word × 8-bit) SRAM with $\overline{OE}$ , $\overline{CE1}$ , and $\overline{CE2}$ Control Pins

#### Overview

The LC3564CM and LC3564CT-55U/70U are 8192-word × 8-bit asynchronous silicon gate CMOS SRAMs. These are full CMOS type SRAMs that adopt a six-transistor memory cell and feature fast access times, low operating power dissipation, and an ultralow standby current. These SRAMs provide three control signal inputs: an  $\overline{OE}$  input for high-speed memory access, and two chip enable lines,  $\overline{CE1}$  and  $\overline{CE2}$ , for low power mode and device selection. These means that these SRAMs are ideal for systems that require low power and battery backup, and that they support easy memory expansion. The ultralow standby current that is a feature of these SRAMs allows them to be used with capacitor backup as well. Since these SRAMs support 3-V operation, they are also appropriate for use in portable battery operated systems.

#### Features

- Supply voltage range: 2.7 to 5.5 V
  - In 5-V operation mode: 5.0 V ±10%
  - In 3-V operation mode: 3.0 V ±10%
- Address access time ( $t_{AA}$ )
  - In 5-V operation mode:
 

LC3564CM, and CT-55U:	55 ns (max)
LC3564CM, and CT-70U:	70 ns (max)
  - In 3-V operation mode:
 

LC3564CM, and CT-70U:	200 ns (max)
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- Ultralow standby current
  - In 5-V operation mode: 1.0 μA ( $T_a \leq 70^\circ\text{C}$ ),  
3.0 μA ( $T_a \leq 85^\circ\text{C}$ )
  - In 3-V operation mode: 0.8 μA ( $T_a \leq 70^\circ\text{C}$ ),  
2.5 μA ( $T_a \leq 85^\circ\text{C}$ )
- Operating temperature range
  - In 5-V operation mode: -40 to 85°C
  - In 3-V operation mode: -40 to 85°C
- Data retention supply voltage: 2.0 to 5.5 V
- All input and output levels:
  - In 5-V operation mode: TTL compatible levels
  - In 3-V operation mode:  $V_{CC} - 0.2 \text{ V}/0.2 \text{ V}$
- Three control inputs:  $\overline{OE}$ ,  $\overline{CE1}$ , and  $\overline{CE2}$
- Shared input and output pins, three-state outputs
- No clock required
- Packages
  - 28-pin SOP (450 mil) plastic package: LC3564CM
  - 28-pin TSOP (8 × 13.4 mm) plastic package: LC3564CT

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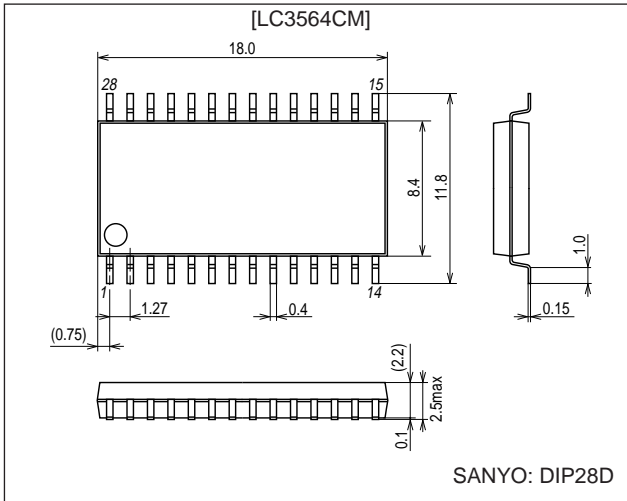
**SANYO Electric Co., Ltd. Semiconductor Company**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Package Dimensions

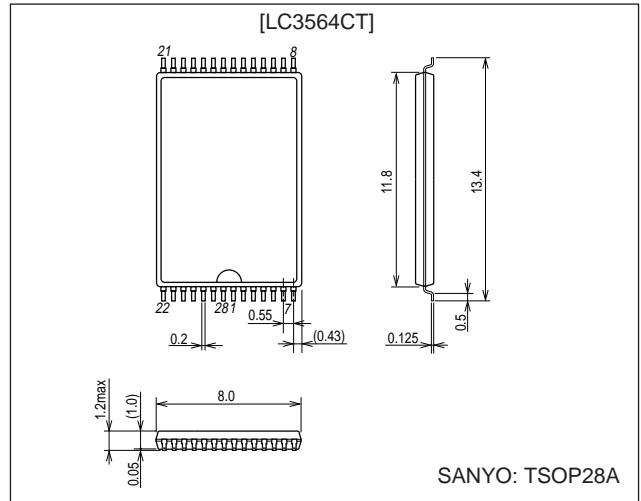
unit: mm

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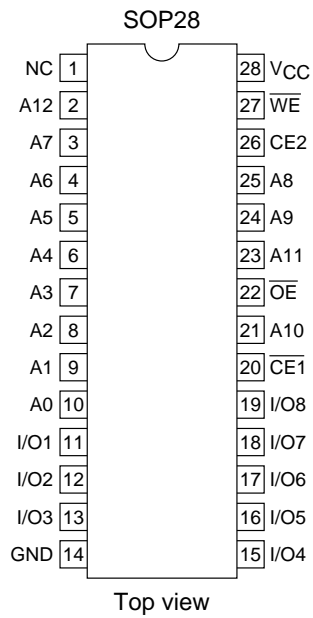


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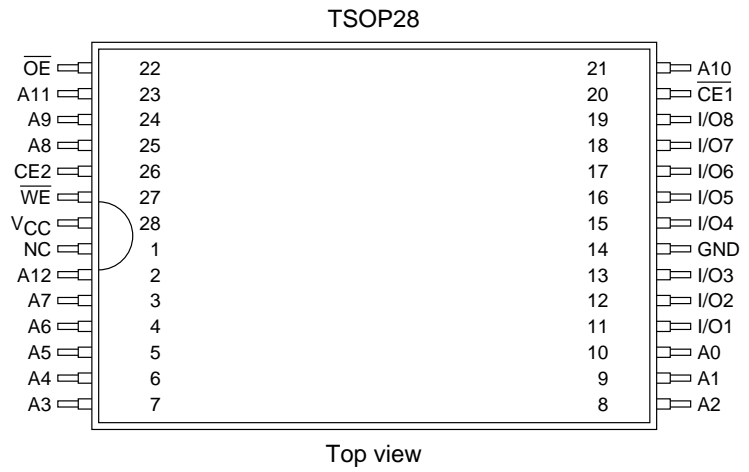
### 3221-TSOP28A



## Pin Assignments



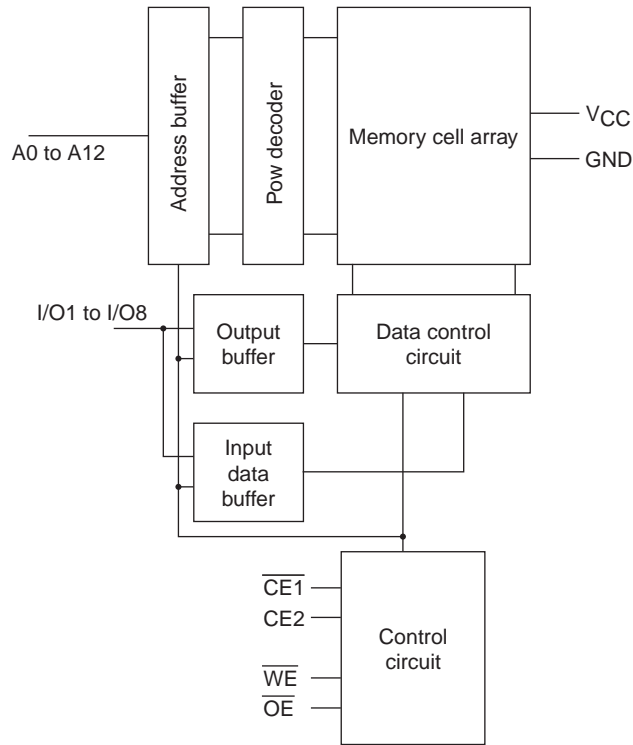
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## LC3564CM, CT-55U/70U

### Block Diagram



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### Pin Functions

A0 to A12	Address inputs
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE1}$ , $\overline{CE2}$	Chip enable inputs
I/O1 to I/O8	Data I/O
$V_{CC}$ , GND	Power supply and ground

### Function Table

Mode	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	$I_{CCA}$
Write cycle	L	H	X	L	Data input	$I_{CCA}$
Output disable	L	H	H	H	High impedance	$I_{CCA}$
Not selected	H	X	X	X	High impedance	$I_{CCS}$
	X	L	X	X	High impedance	$I_{CCS}$

X : H or L

## LC3564CM, CT-55U/70U

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		7.0	V
Input voltage	$V_{IN}$		$-0.3^*$ to $V_{CC} + 0.3$	V
I/O voltage	$V_{I/O}$		$-0.3$ to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$		$-40$ to $+85$	$^\circ\text{C}$
Storage temperature	$T_{stg}$		$-55$ to $+125$	$^\circ\text{C}$

Note: For pulse widths less than 30 ns:  $-3.0$  V

#### Input and Output Capacitances at $T_a = 25^\circ\text{C}$ , $f = 1$ MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		6	10	pF
Input pin capacitance	$C_{IN}$	$V_{IN} = 0$ V		6	10	pF

Note: These parameters are sampled, and are not measured for every unit.

[5-V Operation]

#### DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 4.5$ to $5.5$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{CC}$		4.5	5.0	5.5	V
Input voltage	$V_{IH}$		2.2		$V_{CC} + 0.3$	V
	$V_{IL}$		$-0.3^*$		+0.8	V

Note: For pulse widths less than 30 ns:  $-3.0$  V

#### DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 4.5$ to $5.5$ V

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ *	max		
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	$-1.0$		$+1.0$	$\mu\text{A}$	
I/O leakage current	$I_{LO}$	$V_{CE1} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$ , $V_{I/O} = 0$ to $V_{CC}$	$-1.0$		$+1.0$	$\mu\text{A}$	
Output high-level voltage	$V_{OH}$	$I_{OH} = -1.0$ mA	2.4			V	
Output low-level voltage	$V_{OL}$	$I_{OL} = 2.0$ mA			0.4	V	
Operating supply current	$V_{CC} - 0.2$ V/ $0.2$ V inputs	$I_{CCA1}$		$T_a \leq 70^\circ\text{C}$	0.01	1.0	$\mu\text{A}$
				$T_a \leq 85^\circ\text{C}$		3.0	
		$I_{CCA4}$	$V_{CE1} \leq 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V, $I_{I/O} = 0$ mA, DUTY = 100%	min	LC3564CM, CT-55U		45
	cycle			LC3564CM, CT-70U		35	
	1 $\mu\text{s}$ cycle				4		
	TTL inputs	$I_{CCA2}$	$V_{CE1} = V_{IL}$ , $V_{CE2} = V_{IH}$ , $I_{I/O} = 0$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$			7	mA
$I_{CCA3}$						$V_{CE1} = V_{IL}$ , $V_{CE2} = V_{IH}$ , $I_{I/O} = 0$ mA, DUTY = 100%	
	cycle	LC3564CM, CT-70U	40				
1 $\mu\text{s}$ cycle		7					
Standby mode supply current	$V_{CC} - 0.2$ V/ $0.2$ V inputs	$I_{CCS1}$	$V_{CE2} \leq 0.2$ V or $V_{CE1} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V	$T_a \leq 70^\circ\text{C}$	0.01	1.0	$\mu\text{A}$
				$T_a \leq 85^\circ\text{C}$		3.0	
	TTL inputs	$I_{CC2}$	$V_{CE2} = V_{IL}$ or $V_{CE1} = V_{IH}$ , $V_{IN} = 0$ to $V_{CC}$			2.0	mA

Note \*: Reference values at  $V_{CC} = 5$  V,  $T_a = 25^\circ\text{C}$

## LC3564CM, CT-55U/70U

### AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 4.5$ to $5.5$ V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	$V_{IH} = 2.4$ V, $V_{IL} = 0.6$ V
Input rise and fall times	5 ns
Input and output timing level	1.5 V
Output load	LC3564CM and CT-55U/70U: 30 pF + 1 TTL gate (Including the jig capacitance.)

### Read Cycle

Parameter	Symbol	LC3564CM, CT				Unit
		-55U		-70U		
		min	max	min	max	
Read cycle time	$t_{RC}$	55		70		ns
Address access time	$t_{AA}$		55		70	ns
$\overline{CE1}$ access time	$t_{CA1}$		55		70	ns
CE2 access time	$t_{CA2}$		55		70	ns
$\overline{OE}$ access time	$t_{OA}$		30		35	ns
Output hold time	$t_{OH}$	10		10		ns
$\overline{CE1}$ output enable time	$t_{COE1}$	5		10		ns
CE2 output enable time	$t_{COE2}$	5		10		ns
$\overline{OE}$ output enable time	$t_{OOE}$	5		5		ns
$\overline{CE1}$ output disable time	$t_{COD1}$		20		30	ns
CE2 output disable time	$t_{COD2}$		20		30	ns
$\overline{OE}$ output disable time	$t_{OOD}$		20		25	ns

### Write Cycle

Parameter	Symbol	LC3564CM, CT				Unit
		-55U		-70U		
		min	max	min	max	
Write cycle time	$t_{WC}$	55		70		ns
Address setup time	$t_{AS}$	0		0		ns
Write pulse width	$t_{WP}$	40		50		ns
$\overline{CE1}$ setup time	$t_{CW1}$	50		60		ns
CE2 setup time	$t_{CW2}$	50		60		ns
Write recovery time	$t_{WR}$	0		0		ns
$\overline{CE1}$ write recovery time	$t_{WR1}$	0		0		ns
CE2 write recovery time	$t_{WR2}$	0		0		ns
Data setup time	$t_{DS}$	25		35		ns
Data hold time	$t_{DH}$	0		0		ns
$\overline{CE1}$ data hold time	$t_{DH1}$	0		0		ns
CE2 data hold time	$t_{DH2}$	0		0		ns
$\overline{WE}$ output enable time	$t_{WOE}$	5		5		ns
$\overline{WE}$ output disable time	$t_{WOD}$		30		30	ns

## LC3564CM, CT-55U/70U

[3-V Operation]

### DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.3$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{CC}$		2.7	3.0	3.3	V
Input voltage	$V_{IH}$		$V_{CC} - 0.2$		$V_{CC}$	V
	$V_{IL}$		0		0.2	V

### DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.3$ V

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ *	max		
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$	
I/O leakage current	$I_{LO}$	$\overline{V_{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $\overline{V_{OE}} = V_{IH}$ or $\overline{V_{WE}} = V_{IL}$ , $V_{I/O} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$	
Output high-level voltage	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{CC} - 0.2$			V	
Output low-level voltage	$V_{OL}$	$I_{OL} = 1.0$ mA			0.2	V	
Operation supply current	$V_{CC} - 0.2$ V/0.2 V inputs	$I_{CCA1}$	$\overline{V_{CE1}} \leq V_{IL}$ , $V_{CE2} \geq V_{IH}$ , $I_{I/O} = 0$ mA, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$	$T_a \leq 70^\circ\text{C}$	0.01	0.8	$\mu\text{A}$
				$T_a \leq 85^\circ\text{C}$		2.5	
		$I_{CCA4}$	$\overline{V_{CE1}} \leq V_{IL}$ , $V_{CE2} \geq V_{IH}$ , $I_{I/O} = 0$ mA, DUTY = 100%	min cycle 1 $\mu\text{s}$ cycle	LC3564CM, CT-70U		20
Standby mode supply current	$V_{CC} - 0.2$ V/0.2 V inputs	$I_{CCS1}$	$V_{CE2} \leq 0.2$ V or $\overline{V_{CE1}} \geq V_{IH}$ $V_{CE2} \geq V_{IH}$	$T_a \leq 70^\circ\text{C}$	0.01	0.8	$\mu\text{A}$
				$T_a \leq 85^\circ\text{C}$		2.5	

Note \*: Reference values at  $V_{CC} = 3$  V,  $T_a = 25^\circ\text{C}$

## LC3564CM, CT-55U/70U

### AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.3$ V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	$V_{IH} = V_{CC} - 0.2$ V, $V_{IL} = 0.2$ V
Input rise and fall times	10 ns
Input and output timing level	1.5 V
Output load	LC3564CM, CT-70U : 30pF (Including the jig capacitance.)

### Read Cycle

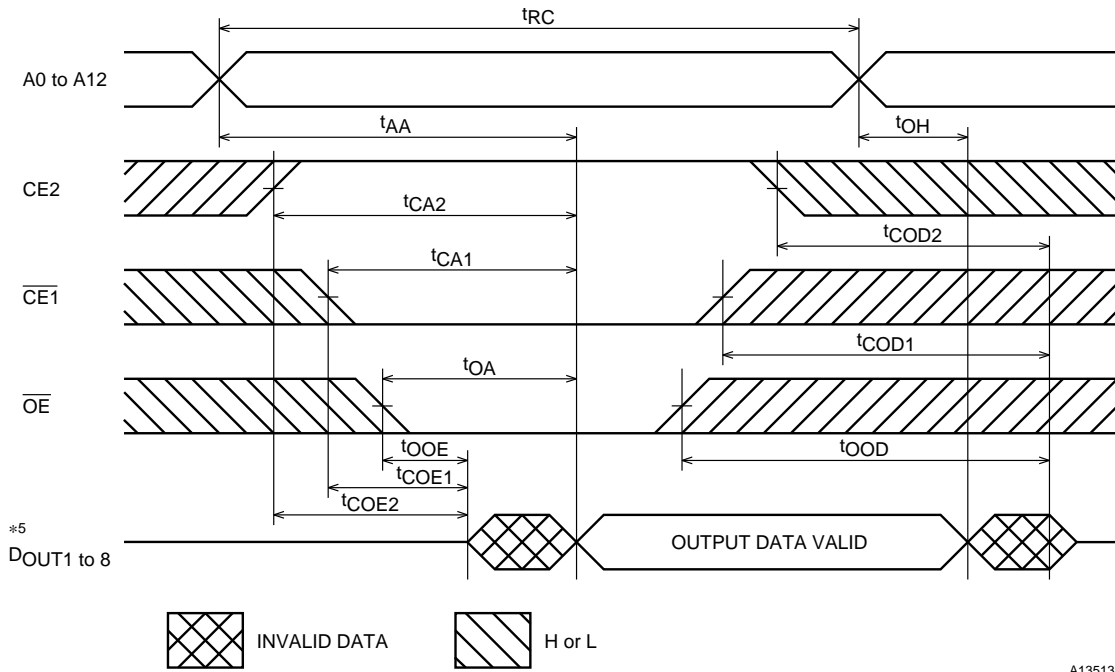
Parameter	Symbol	LC3564CM, CT-70U		Unit
		-10		
		min	max	
Read cycle time	$t_{RC}$	200		ns
Address access time	$t_{AA}$		200	ns
$\overline{CE1}$ access time	$t_{CA1}$		200	ns
CE2 access time	$t_{CA2}$		200	ns
$\overline{OE}$ access time	$t_{OA}$		100	ns
Output hold time	$t_{OH}$	20		ns
$\overline{CE1}$ output enable time	$t_{COE1}$	20		ns
CE2 output enable time	$t_{COE2}$	20		ns
$\overline{OE}$ output enable time	$t_{OOE}$	10		ns
$\overline{CE1}$ output disable time	$t_{COD1}$		60	ns
CE2 output disable time	$t_{COD2}$		60	ns
$\overline{OE}$ output disable time	$t_{OOD}$		50	ns

### Write Cycle

Parameter	Symbol	LC3564CM, CT-70U		Unit
		-70		
		min	max	
Write cycle time	$t_{WC}$	200		ns
Address setup time	$t_{AS}$	0		ns
Write pulse width	$t_{WP}$	140		ns
$\overline{CE1}$ setup time	$t_{CW1}$	150		ns
CE2 setup time	$t_{CW2}$	0		ns
Write recovery time	$t_{WR}$	0		ns
$\overline{CE1}$ write recovery time	$t_{WR1}$	0		ns
CE2 write recovery time	$t_{WR2}$	130		ns
Data setup time	$t_{DS}$	0		ns
Data hold time	$t_{DH}$	0		ns
$\overline{CE1}$ data hold time	$t_{DH1}$	0		ns
CE2 data hold time	$t_{DH2}$	10		ns
$\overline{WE}$ output enable time	$t_{WOE}$			ns
$\overline{WE}$ output disable time	$t_{WOD}$		60	ns

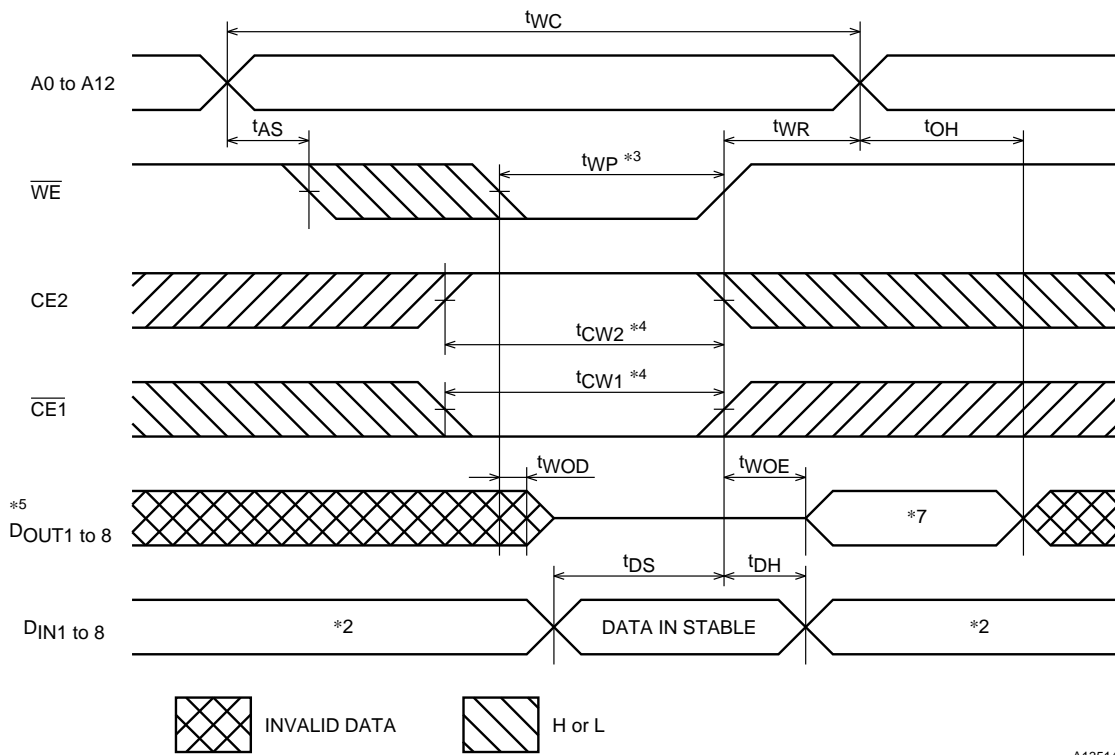
Timing Charts

Read Cycle \*1



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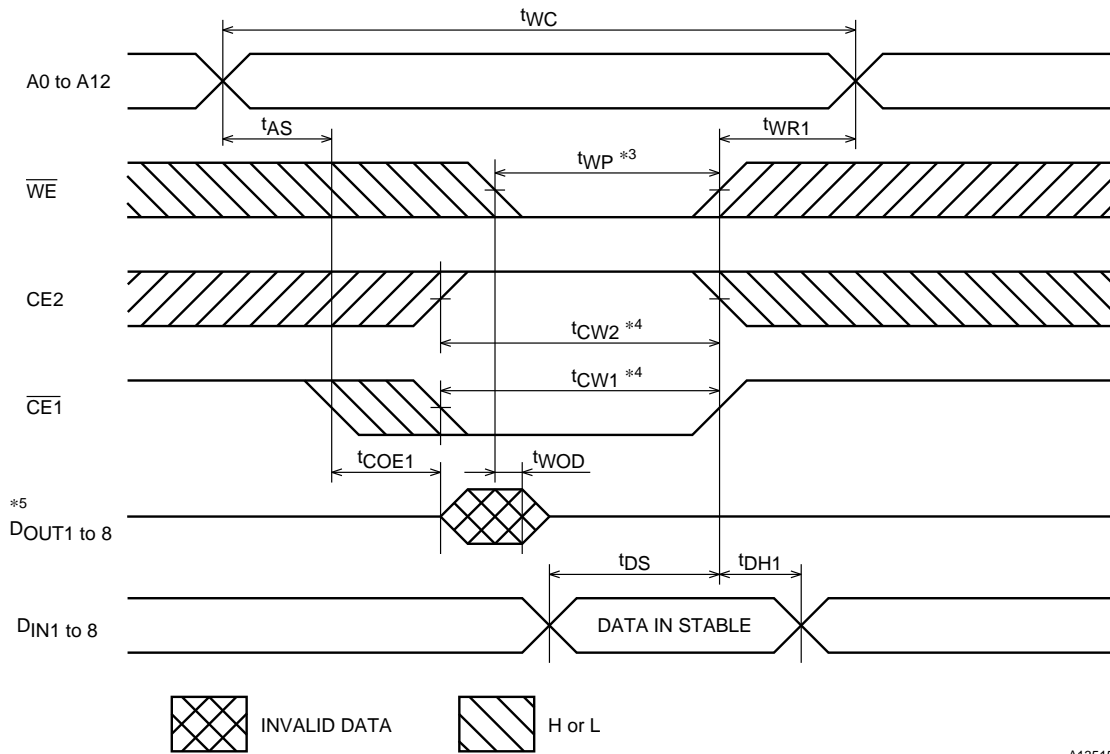
Write Cycle (1):  $\overline{WE}$  Write \*6



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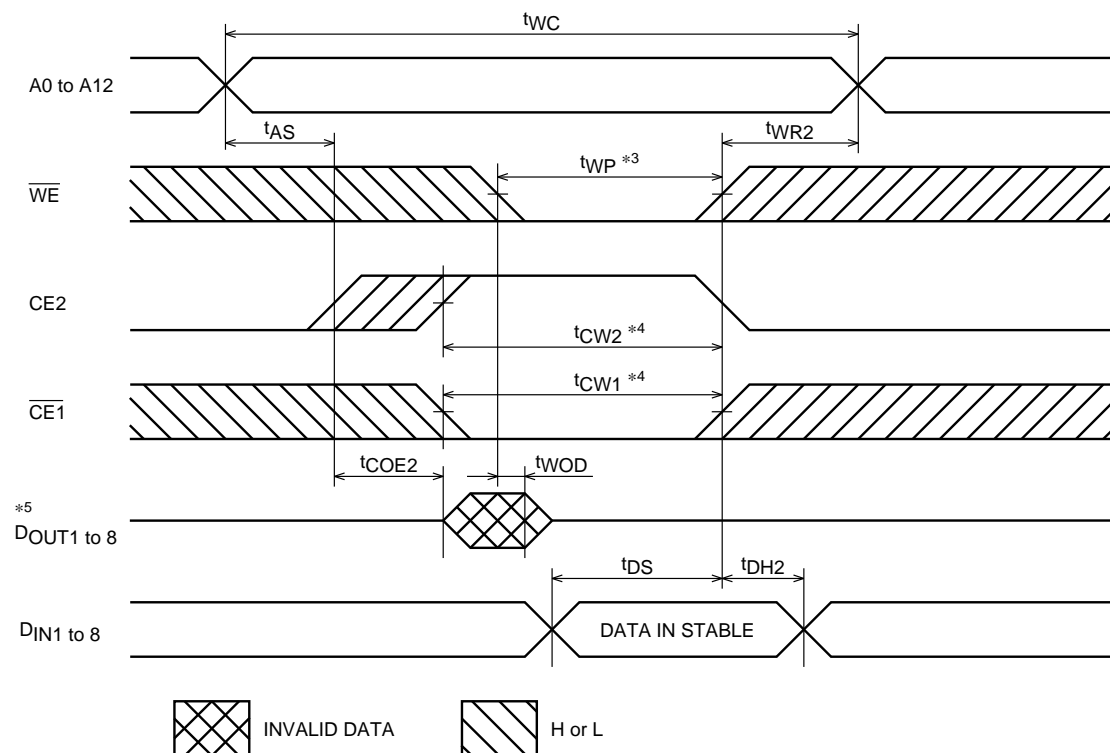


Write Cycle (2):  $\overline{\text{CE1}}$  Write \*6



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Write Cycle (3):  $\text{CE2}$  Write \*6



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- Notes:
1. Hold  $\overline{\text{WE}}$  high during the read cycle.
  2. Applications must not apply reverse phase signals to the  $\text{D}_{\text{OUT}}$  pins when those pins are in the output state.
  3. The time  $t_{\text{WP}}$  is the period when  $\overline{\text{CE1}}$  and  $\overline{\text{WE}}$  are low and  $\text{CE2}$  is high, and is defined as the time from the fall of  $\overline{\text{WE}}$  until either  $\overline{\text{CE1}}$  or  $\overline{\text{WE}}$  rises, or  $\text{CE2}$  falls, whichever occurs first.
  4. The times  $t_{\text{CW1}}$  and  $t_{\text{CW2}}$  are periods when  $\overline{\text{CE1}}$  and  $\overline{\text{WE}}$  are low and  $\text{CE2}$  is high. They are defined as the times from the fall of  $\overline{\text{CE1}}$  or the rise of  $\text{CE2}$  to the rise of  $\overline{\text{CE1}}$  and  $\overline{\text{WE}}$ , or the fall of  $\text{CE2}$ , whichever occurs first.
  5. The  $\text{D}_{\text{OUT}}$  pins will be in the high-impedance state if either  $\overline{\text{OE}}$  is high,  $\overline{\text{CE1}}$  is high,  $\text{CE2}$  is low, or  $\overline{\text{WE}}$  is low.
  6.  $\overline{\text{OE}}$  must be held either at  $V_{\text{IH}}$  or  $V_{\text{IL}}$  during the write cycle.
  7. The  $\text{D}_{\text{OUT}}$  pins have the same phase as the write cycle write data.

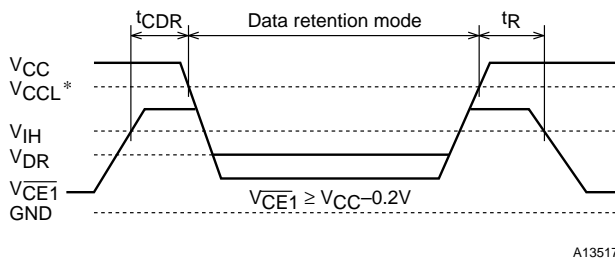
## LC3564CM, CT-55U/70U

### Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

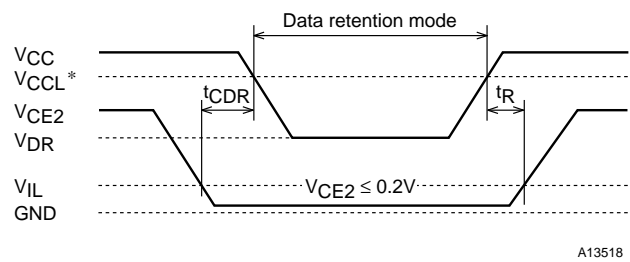
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Data retention supply voltage	$V_{DR}$	$V_{CE2} \leq 0.2\text{ V}$ or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$ , $V_{CE2} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	$\mu\text{A}$
Data retention supply current	$I_{CCDR}$	$V_{CC} = 3\text{ V}$ , $V_{CE2} \leq 0.2\text{ V}$ , or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$ , $V_{CE2} \geq V_{CC} - 0.2\text{ V}$			0.8	$\mu\text{A}$
		$T_a \leq 70^\circ\text{C}$			2.5	
Chip enable setup time	$t_{CDR}$		0			ns
Chip enable hold time	$t_R$		$t_{RC}^*$			ns

Note \*:  $t_{RC}$  is the read cycle time.

Data Retention Waveforms (1):  $\overline{\text{CE1}}$  Control



Data Retention Waveforms (2): CE2 Control



Note \*: In 5-V operation: 4.5 V  
In 3-V operation: 2.7 V

### Notes on Circuit Design

When actually design a circuit using these devices, take the following points into consideration and design the circuit so that none of the maximum rating items are ever exceeded.

- Variations in the supply voltage
- Variations in the electrical characteristics of components such as semiconductor devices, resistors, and capacitors.
- Ambient temperature
- Variations in input and clock signals
- Possible application of abnormal pulses

Also, these devices must be operated within the ranges stipulated in the allowable operating ranges.

If CMOS IC input pins are left open, intermediate potential input voltages may occur leading to incorrect operation due to through currents or other phenomenon. Applications must handle unused input pins appropriately.

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