Data Sheet
May 2001

L8576B Dual Ringing SLIC

Features

- Two SLIC channels for multiple tip/ring interfaces
- On-chip balanced ringing generator, no ring relay required
- Single battery operation or optional automatic battery switch
- Quiet battery reversal for on-hook signaling
- Disconnect state
- Distortion-free, on-hook transmission
- 24 mA loop current limiter
- Ring trip detector
- Switchhook detector
- Immune to channel crosstalk and impulse noise
- Allows rail overvoltages for ease of protection
- Thermal protection
- 44-pin, surface-mount, plastic package (PLCC)

Applications

- POTS for ISDN
- Terminal adapters (TA)
- Digital loop carrier (DLC) systems
- PABX

Description

The Agere Systems Inc. L8576B electronic dual subscriber line interface circuit (SLIC) provides all the functions that are necessary to interface a codec to the tip and ring of a subscriber loop, integrating two battery feeds and ringing generators in one low-cost package. The L8576B device is optimized to meet the needs of short loop, customer premises applications and features balanced ringing from the single battery supply. The device is built using a 90 V complementary bipolar (CBIC) process. It is available in a 44-pin PLCC package.

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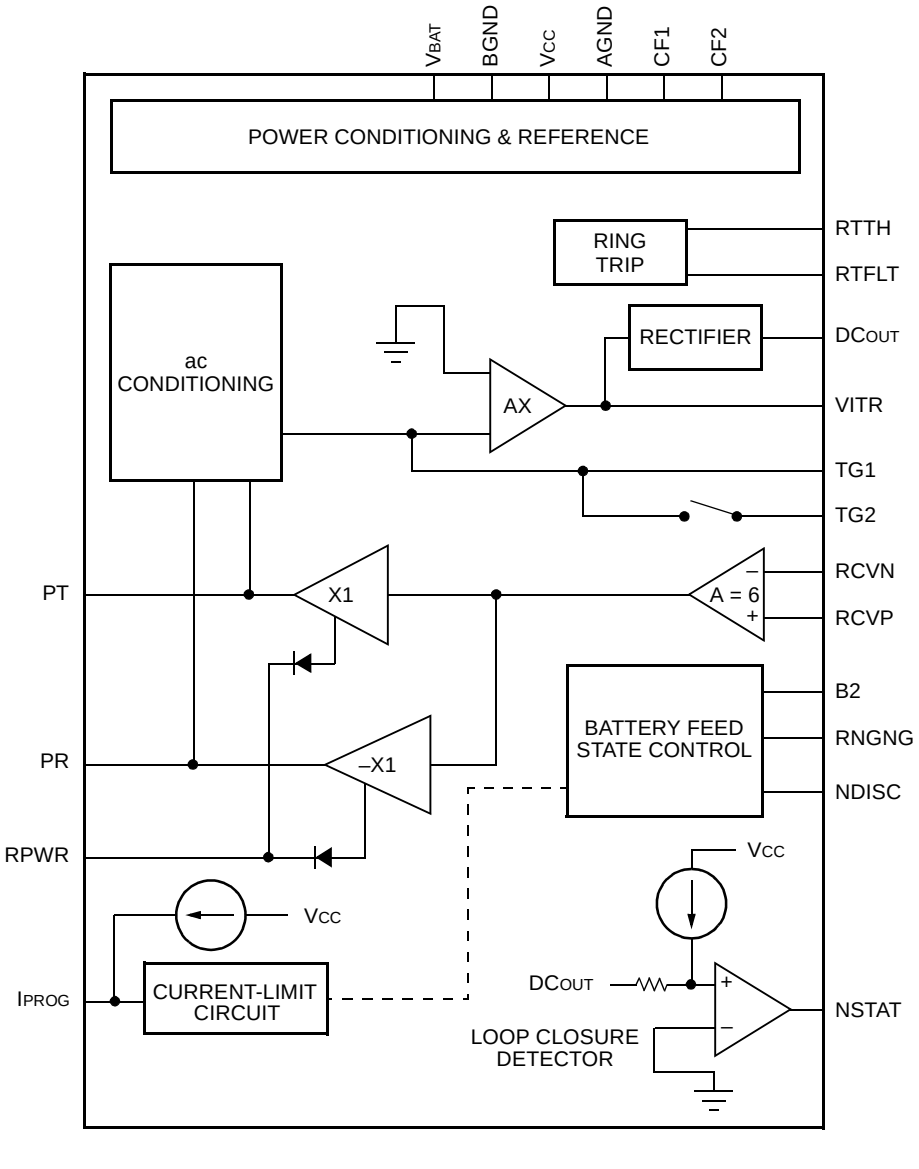
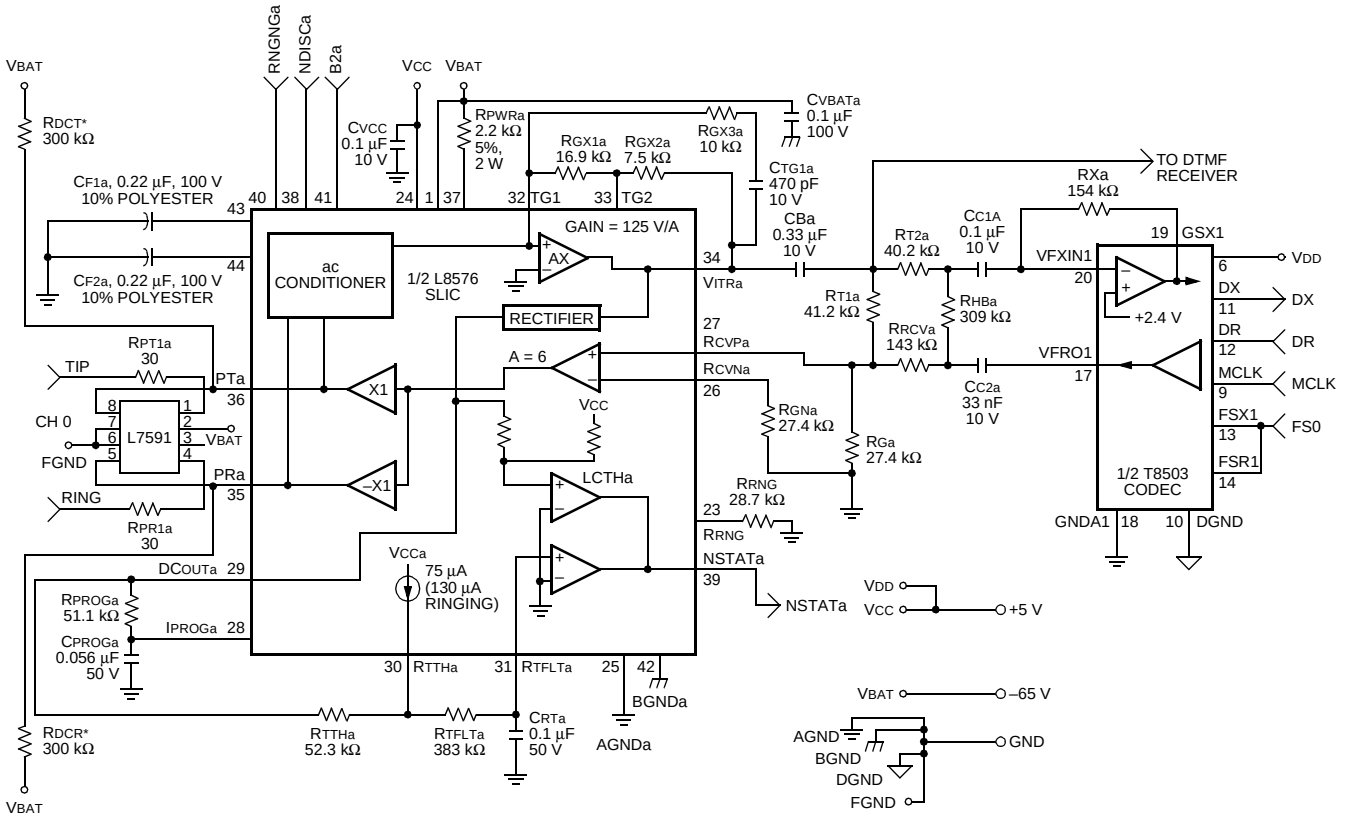


Figure 1. Architectural Diagram

Description (continued)



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* RDCT and RDCR (optional) are only required to keep the NSTAT output at a steady state during the disconnect state.

Notes:
TX = –2 dB.
RX = –4 dB.
Termination = 600 Ω.
Hybrid balance = 600 Ω.
Ring trip optimized for 20 Hz.

Figure 2. Typical 600 Ω Application Circuit (Only One Channel Shown)

Pin Information

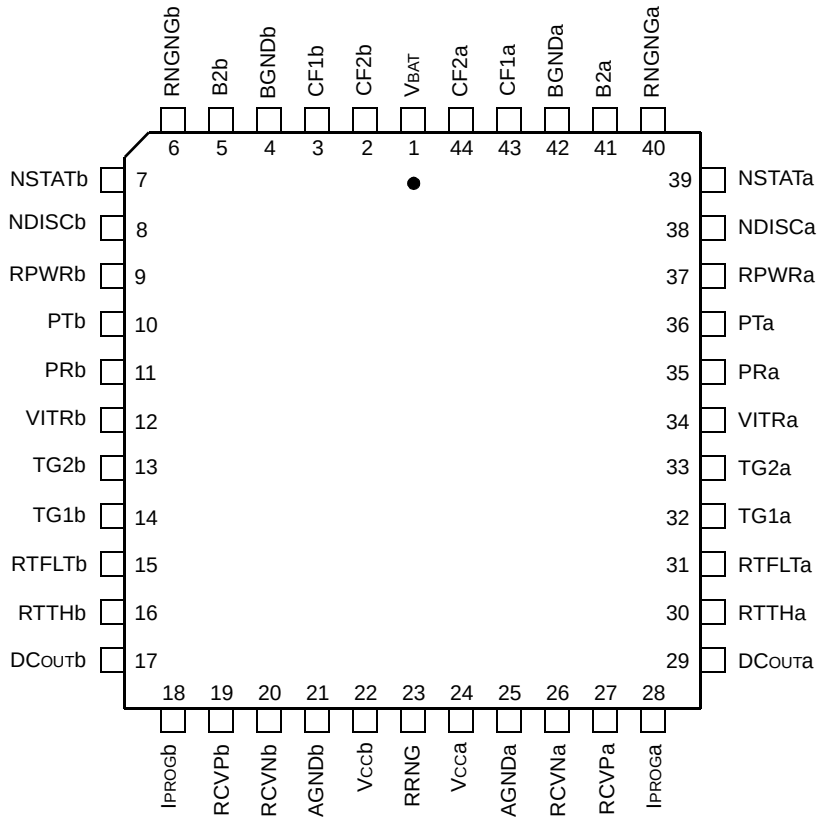

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Figure 3. 44-Pin PLCC Pin Diagram

Table 1. Pin Descriptions

Pin, Circuit a	Pin, Circuit b	Symbol	Type	Name/Function
1	1	V_{BAT}*	—	**Office Battery Supply.** Negative high-voltage power supply, nominally –65 V.
44	2	CF2	—	**Filter Capacitor 2.** Connect 0.22 µF capacitor to AGND.
43	3	CF1	—	**Filter Capacitor 1.** Connect 0.22 µF capacitor to AGND.
42	4	BGND*	—	**Battery Ground.** Ground return for the battery supply and fault ground.
41	5	B2	I^u	**State Input.** Refer to Operating States section. A pull-up device is included.

* On the printed-wiring board (PWB), make the leads to BGND and V_{BAT} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PWB copper on all leads connected to this device for the lowest operating temperature.

Note: I^u and O^u indicate a pull-up device is included on this lead.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin, Circuit a	Pin, Circuit b	Symbol	Type	Name/Function
40	6	RNGNG	I^u	**Ringing Input.** Refer to Operating States section. A pull-up device is included.
39	7	NSTAT	O^u	**Loop Detector Output/Ring Trip Detector Output.** When low, this lead indicates an off-hook condition. When in ringing mode, a low output on this lead indicates a ring trip. A pull-up device is included.
38	8	NDISC	I^u	**Disconnect Input**. Refer to Operating States section. A pull-up device is included.
37	9	RPWR	—	**Power Resistor.** Connect a resistor between this pin and V_{BAT}. A 2.2 kΩ, 2 W resistor should be used for a V_{BAT} of –68.5 V. See the Applications section to calculate resistor values for other V_{BAT} potentials.
36	10	PT	I/O	**Protected Tip.** The input to the tip fault protection and output of tip current drive amplifier. Connect this pin to the tip of the loop through a 30 Ω overvoltage protection resistor.
35	11	PR	I/O	**Protected Ring.** The input to the ring fault protection and output of ring current drive amplifier. Connect this pin to the ring of the loop through a 30 Ω overvoltage protection resistor.
34	12	VITR	O	**Transmit ac Output Voltage.** This output is a voltage that is directly proportional to the differential tip/ring current.
33	13	TG2	—	**Transmit Gain 2.** Transmit gain and current limiting for ringing is set by the value of R_{GX2}. R_{GX2} is connected between TG2 and VITR.
32	14	TG1	—	**Transmit Gain 1.** Transmit gain is set by the series resistor combination of R_{GX1} and R_{GX2} from this lead to TG2.
31	15	RTFLT	—	**Ring Trip Filter.** Connect this lead to RTTH via a resistor and to AGND with a capacitor to filter the ring trip circuit to prevent spurious responses.
30	16	RTTH	—	**Ring Trip Threshold.** Connect this lead to DC_{OUT} via a resistor to set the ring trip threshold.
29	17	DC_{OUT}	O	**dc Voltage Out**. This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current.
28	18	I_{PROG}	I	**Current-Limit Program Input.** A resistor to DC_{OUT} sets the dc current limit of the circuit.
27	19	RCVP	I	**Receive Signal Input (+).** This high-impedance input controls the ac differential voltage on tip/ring.
26	20	RCVN	I	**Receive Signal Input (–).** This high-impedance input controls the ac differential voltage on tip/ring.
25	21	AGND	—	**Analog Signal Ground.**
24	22	V_{CC}	—	**Analog 5 V Power Supply.**
23	23	RRNG	—	**Ringing Slope Resistor.** Connect this lead to AGND with a resistor to set the slope of the ringing waveform. Note that this pin is shared with both sections.

* On the printed-wiring board (PWB), make the leads to BGND and V_{BAT} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PWB copper on all leads connected to this device for the lowest operating temperature.

Note: I^u and O^u indicate a pull-up device is included on this lead.

Functional Description

Refer to the architectural and application diagrams (Figures 1 and 2, respectively).

General

The L8576B is a dual subscriber line interface circuit with each half of the device providing battery feed, supervision, and balanced ringing. It is designed to support short loops, typically on customer premises. The use of a single battery for both battery feed and ringing makes this device particularly advantageous where it is desirable to minimize power supply costs in small systems, such as terminal adapters. The tip and ring drive amplifiers are used with a very relaxed current limit to develop a trapezoidal, balanced ringing signal. Use of a nominal –65 V power supply allows for ringing of normal phones, whether equipped with a mechanical ringer, or a peak-detection type of ringing detector. While balanced ringing is not the norm worldwide, its use in short, customer premises loops is gaining popularity.

In addition to the ringing and battery functions, the L8576B device provides the ac receive and transmit paths. Also, integral within the device is an off-hook detection circuit and a ring trip detection circuit that have their outputs multiplexed on a single lead.

Thermal protection within the device is also provided, and an external resistor is used to drop the high battery voltage before applying loop current, thus allowing a significant portion of the power to be dissipated outside of the device. Removing much of this power makes it possible to incorporate two complete circuits in a 44-pin, surface-mount package.

Protection

The L8576B contains some overvoltage protection in addition to the thermal protection within the device. This protection, along with the associated tip and ring protection resistors, may be sufficient in some benign environments. However, if power line cross or lightning protection is desired, the use of an external protection circuit (such as the L7591 device from Agere) is highly recommended.

The integrated thermal protection consists of a thermal shutdown circuit which places the tip/ring drivers in a high-impedance state when the temperature of the die exceeds 160 °C. In thermal shutdown, all supervision states are undefined.

Tip/Ring Drivers

The L8576B has two tip/ring drivers whose outputs are PT and PR. Each driver operates as a current source capable of sinking or sourcing adequate ac signal bias current. In the normal talk operating mode, these drivers are current-limited at a nominal 24 mA to minimize the power dissipation of short loops. These amplifiers are also used to drive balanced ringing. During ringing, the current limit is raised to approximately 85 mA.

The external resistor connected to the R_{PWR} pin is used to dissipate power externally and also to drop the battery voltage which is higher than normal in order to support balanced ringing. Note that this external power dissipation is present during both ringing or normal battery feed operation. Power limitations restrict the dual device to actively ringing only one channel at a time; thus, ringing cadence must be used to ensure that only one channel is actively ringing at any given instant of time. In other words, to ring both channels at the same time, ring each channel during the quiet interval of the other channel.

Battery Operation

There are two V_{BAT} inputs to the device. Pin 1 (V_{BAT}) provides voltage to the entire SLIC and pins 9 and 37 (R_{PWR}) provide voltage to the individual tip and ring amplifiers of each channel through R_{PWR} resistors. A shared current sourcing scheme is employed within the device. For loop currents below 20 mA, the V_{BAT} applied to pin 1 sources all of the loop current in addition to driving internal circuitry. For loop currents greater than 20 mA, loop current is primarily provided through the R_{PWR} resistors and the pin 1 V_{BAT} mainly powers internal circuitry. The R_{PWR} resistors can be replaced by a lower-voltage auxiliary battery. Operation with an auxiliary battery is described in the Applications section of this document.

Transmit and Receive Interface

The interface is suitable for direct coupling to a ±5 V only codec. When interfacing a 5 V only codec, coupling capacitors are required.

The transmit interface circuitry couples the differential voltage on tip and ring to transmit output VITR. The inverting input of the driving amplifier is available on lead TG1, so connecting a resistance between VITR and TG1 allows adjustment of the transmit gain (transconductance).

Functional Description (continued)

Transmit and Receive Interface (continued)

A second gain setting is provided to accommodate ring trip. A switch is built into TG2. In ringing mode, TG1 and TG2 are internally connected, thus shorting out the external gain resistor R_{GX1}. This provides a lower transmit gain for ringing since ring trip is accomplished by monitoring the voltage at DC_{OUT}. This lower gain sets DC_{OUT} at the appropriate level to accommodate the higher currents of the ring trip.

The receive interface circuitry couples the differential signal on receive inputs RCVP and RCVN to the tip/ring drivers.

Data Interface

A 4-wire parallel interface (B2, RNGNG, NDISC, and NSTAT) is provided for each channel to control signals to and from the system controller. B2 controls the forward/reverse battery in normal talk mode while RNGNG enables the balanced ringing mode of operation, and NDISC performs a disconnect state. NSTAT reflects either the loop detector output or the ring trip detector output, depending on the mode of the section. It is the responsibility of the system controller to recognize ring trip detection and set RNGNG to a logic 0 state to terminate ringing. The system controller should also use RNGNG to set ringing cadence.

Loop Current Detector

Each section of the device has an integral loop current detector set at a nominal 12 mA of dc current. This is used to detect off-hook transitions in the normal talk state. When current less than the current threshold (including no current) is flowing, NSTAT is at logic 1. When loop current exceeds 12 mA, the output NSTAT switches to a logic 0. No hysteresis is included.

Operating States

The L8576B device has four operating states:

- Talk state—normal battery:
  - — Normal talk state.
  - — Battery feed is connected to the battery supply (V_{BAT}).
  - — Both receive and transmit transmission paths are powered up.
  - — dc loop and instantaneous current limiters are powered up and active.
  - — NSTAT reflects the status of the switchhook detector.
  - — PR is negative with respect to PT.
- Talk state—reverse battery:
  - — Normal talk state.
  - — Battery feed is connected to the battery supply (V_{BAT}).
  - — Both receive and transmit transmission paths are powered up.
  - — dc loop current limiter is powered up and active.
  - — NSTAT reflects the status of the switchhook detector.
  - — PR is positive with respect to PT.
- Ringing state:
  - — Normal ringing state.
  - — Both receive and transmit transmission paths are inactive.
  - — Balanced ringing is applied to PR and PT, in accordance with B2.
  - — Current limiter is set for ringing limit.
  - — NSTAT reflects the status of the ring trip detector.
  - — Only one channel should be in this state at a time to control power dissipation.
- Disconnect state:
  - — Tip and ring drive amplifiers are powered down.
  - — Pins PT and PR are high impedance (>100 kΩ).
  - — NSTAT is undefined.
  - — PT and PR voltage is undefined.

Operating States (continued)

These states are selected using three logic inputs, B2, RNGNG, and NDISC. B2 sets normal operation, either with forward or reverse battery. RNGNG overrides B2 and applies ringing with the polarity of tip and ring reversed on edges of the B2 signal. The slope of the waveform is determined by a resistor from RRNG to AGND. Logic input NDISC puts the device into a loop current denial state (disconnect). Tip and ring amplifiers are saturated against ground with about a 100 µA current source. This creates a level in the loop current sensing circuitry that approaches a loop closed state. Some conditions on the tip and ring could cause the circuit to indicate loop closed even though the loop is open. This situation can be prevented by connecting a 300 kΩ resistor from V_{BAT} to each of the outputs of the tip and ring amplifiers (see Figure 2). This will pull the amplifier output to about 30 V above V_{BAT}, keeping the NSTAT output at a steady high (on-hook indication) level. If the disconnect state is not used or the NSTAT output during the disconnect state is not recognized or used, then the resistors are not needed.

Table 2 below summarizes the operating input state coding.

Table 2. Input State Coding

NDISC	RNGNG	B2	State
1	0	1	**Forward Battery, Normal Talk, and Feed State.** Pin PT is positive with respect to PR.
1	0	0	**Reverse Battery, Normal Talk, and Feed State.** Pin PT is negative with respect to PR.
1	1	1 ↑	**Ringing Is Applied to PT and PR.** On the transition, PT starts towards a positive voltage (with respect to PR). The endpoint of this state is PT at BGND and PR at V_{BAT}.
1	1	0 ↓	**Ringing Is Applied to PT and PR.** On the transition, PT starts towards a negative voltage (with respect to PR). The endpoint of this state is PT at V_{BAT} and PR at BGND.
0	0/1	0/1	**Disconnect State.** The tip and ring amplifiers are turned off, and the SLIC goes into a high-impedance state (>100 kΩ).

Absolute Maximum Ratings (at T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
5 V dc Supplies	V_{CC}	–0.5	—	7.0	V
Office Battery Supply	V_{BAT}	–75	—	0.5	V
Logic Input Voltage	—	–0.5	—	V_{CC} + 0.5	V
Logic Input Clamp Diode Current, per Pin	—	—	±20	—	mA
Logic Output Voltage	—	–0.5	—	V_{CC} + 0.5	V
Logic Output Current, per Pin	—	—	±35	—	mA
Analog Input Voltage	—	–7.0	—	7.0	V
Maximum Junction Temperature	—	—	165	—	°C
Storage Temperature Range	T_{stg}	–40	—	125	°C
Relative Humidity Range (noncondensing)	—	5	—	95	%
Ground Potential Difference (BGND to AGND)	—	—	±3	—	V
PT or PR Fault Voltage (dc)	—	V_{BAT} – 5	—	3	V
PT or PR Fault Voltage (10 µs x 1000 µs)	—	V_{BAT} – 15	—	15	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds its ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Electrical Characteristics

Generally, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (0 °C to 70 °C) and entire battery range (to –72 V). Unless otherwise specified, typical values are defined as 20 °C, V_{CC} = 5.0 V, V_{BAT} = –68.5 V. Positive currents flow into the device.

Table 3. Operating Conditions and Powering

Parameter	Min	Typ	Max	Unit
Temperature Range	0	—	70	°C
Humidity Range	5	—	95[1]	%RH
Supply Voltages:				
V_{CC}	4.75	5.0	5.25	V
V_{BAT}	–24[2]	–65	–72	V
Loop Closure Threshold—Detection Range	9.5	12	14.5	mA
ac Termination Impedance Programming Range	300	600	1000[3]	Ω
On- and Off-hook 2-wire Signal Level	—	3.14	—	dBm
Power Supply—Powerup, No Loop Current (per section):				
I_{CC}	—	4.5	5.5	mA
I_{BAT} (V_{BAT} = –65 V)	—	3.0	4.0	mA
Total power (one channel, V_{BAT} = –65 V)	—	230	290	mW
Power-supply Rejection (See Figures 6 and 7.):				
V_{CC} (1 kHz)	35	—	—	dB
V_{BAT} (500 Hz—3 kHz)	45	—	—	dB
Thermal[4]:				
Thermal Resistance (still air) T_j	—	47	—	°C/W
Operating T_j	—	—	150	°C
Thermal Shutdown Temperature	—	160	—	°C

1. Noncondensing.
2. The L8576B will operate below –24 V; –24 V is used for production test.
3. The termination impedance can be programmed up to 1200 Ω; 1000 Ω are used for production test.
4. This parameter is not tested in production. It is guaranteed by design and device characterization.

Table 4. Ring Trip Detector[1]

Parameter[2]	Min	Typ	Max	Unit
Ringing Source:				
Frequency (f) R_{RNG} = 28.7 kΩ, R_{TTH} = 52.3 kΩ	17	20	23	Hz
Frequency (f) Contact Agere for Specific Component Values	20	—	50	Hz
C-message Weighted Noise (900 Ω)	—	—	90	dBrnC
REN Load (1386 Ω + 40 μF) with Loop Resistance = 30 Ω, R_{PT} = 30 Ω, R_{PR} = 30 Ω	—	—	40	Vrms
Detection Interval:				
20 Hz	—	—	200	ms
≥25 Hz	—	—	150	ms

1. This table is provided for information purposes only.
2. These parameters are not tested in production.

Electrical Characteristics (continued)

Pretrip will not occur for the circuits shown below, per GR-909, 4.5.9.

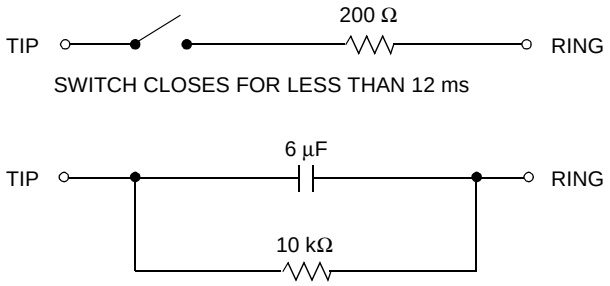


Figure 4. Pretrip Circuit

Table 5. Battery Feed

Parameter	Min	Typ	Max	Unit
Loop Resistance Range[1] (3.17 dBm overload into 600 Ω): I_{LOOP} = 20 mA at V_{BAT} = –65 V	1000	—	—	Ω
Longitudinal Current Capability per Wire[2]	8.5	15	—	mArms
Current Limit[3] R_{LOOP} = 100 Ω: dc Loop	20	24	28	mA
Instantaneous[4]	50	60	70	mA
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current	5	—	—	mArms
Powerup Open Loop Voltage Level Differential Voltage (RNGNG = 0, NDISC = 1, B2 = 1, V_{BAT} = –65 V)	$\|V_{BAT} + 10\|$	—	—	V
Disconnect State: PT or PR Current ($V_{BAT} < V_{PT} < 0$ V)	–1	—	1	mA
PT or PR Resistance ($V_{BAT} < V_{PT} < 0$ V)	100	—	—	kΩ
dc Feed Resistance	—	60	70	Ω
Longitudinal to Metallic Balance—*IEEE*[5] Standard 455[6]: 200 Hz to 1 kHz	54	67	—	dB
1 kHz to 3 kHz	48	62	—	dB
Metallic to Longitudinal (Harm) Balance[7]: 200 Hz to 4 kHz	35	—	—	dB

1. Assumes 2 x 30 Ω external protection resistors. Note the useful range of the device may be determined by the ringing or supervision range rather than the ac characteristics.
2. The longitudinal current is independent of dc loop current.
3. Current limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin IPROG to pin DCOUT R_{PROG} (kΩ) = 3.5 x (I_{LIM} – 9.2) mA. The current limit has a slope vs. loop voltage of 6 kΩ. To control power dissipation, it is recommended that the default current limits be utilized, i.e., R_{PROG} = 51.1 kΩ for 24 mA nominal loop current limit.
4. Instantaneous current limit minimizes inrush current at the onset of an off-hook condition. Inrush current is only limited when in the forward battery state. The device will settle into a dc loop current-limit value within 400 ms after off-hook.
5. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
6. Assumes the external protection resistors are matched to 1%.
7. This parameter is not tested during production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 6. Analog Signal Pins

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DC_{OUT})				
Gain (PT/PR to DC_{OUT}):				
Forward Battery (R_{GX1} = 16.9 kΩ, R_{GX2} = 7.5 kΩ)	–235	–250	–265	V/A
Reverse Battery (R_{GX1} = 16.9 kΩ, R_{GX2} = 7.5 kΩ)	235	250	265	V/A
PT/PR to VITR Gain with				
R_{GX1} = 16.9 kΩ, R_{GX2} = 7.5 kΩ:				
Forward Battery	–121	–125	–129	V/A
Reverse Battery	121	125	129	V/A
Loop Closure Detector Threshold:				
Programming Accuracy	—	—	±20	%
RCVN, RCVP:				
Input Bias Current	—	—	–1.0	µA
Gain RCVP to PT/PR	11.62	12	12.38	—
Gain RCVN to PT/PR	–11.62	–12	–12.38	—
RCVN, RCVP Input Compliance	–2.5	—	V_{CC}	V

Table 7. ac Feed Characteristics

Parameter[1]	Min	Typ	Max	Unit
ac Termination Impedance[2]	300	600	1000	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[3]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1 kHz) (See Figure 5.):				
Transmit Accuracy in Percent	–3.0	0	3.0	%
Transmit Accuracy in dB (relative to 2/3)	–0.24	0	0.24	dB
Receive Gain (f = 1 kHz) (See Figure 5.):				
Receive Accuracy in Percent	–3.0	0	3.0	%
Receive Accuracy in dB	–0.24	0	0.24	dB
Tip/Ring Signal Level (600 Ω reference)	—	—	3.14	dBm
Gain vs. Frequency (transmit and receive; 1 kHz reference)[3]:				
200 Hz—3.4 kHz	–1.00	0	0.05	dB
300 Hz—3.4 kHz	–0.30	0	0.05	dB
3.4 kHz—20 kHz	–3.0	–0.1	2.0	dB
3.4 kHz—266 kHz	—	—	2.0	dB

1. Requires external components connected as shown in the Applications section. Transmission characteristics are specified assuming a 600 Ω resistive termination and ±1% external resistors.
2. Transmission characteristics are specified assuming a 600 Ω resistive termination; however, feedback using external components allows the user to adjust the termination impedance from 600 Ω. Any complex impedance R1 + R2 || C between 300 Ω and 1000 Ω can be synthesized using external components.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 7. ac Feed Characteristics (continued)

Parameter[1]	Min	Typ	Max	Unit
Gain vs. Level (transmit and receive; 0 dBV reference)[2]:				
–50 dB to +3 dB	–0.05	0	0.05	dB
Return Loss[3]:				
200 Hz—500 Hz	20	24	—	dB
500 Hz—3400 Hz	26	29	—	dB
Transhybrid Loss[3]:				
200 Hz—500 Hz	20	24	—	dB
500 Hz—2500 Hz	26	29	—	dB
2500 Hz—3400 Hz	26	29	—	dB
Idle-channel Noise (Tip/Ring):				
Psophometric[2]	—	—	–77	dBmp
C-message	—	—	12	dBrnC
3 kHz Flat[2]	—	—	20	dBrn
Idle-channel Noise (XMT):				
Psophometric[2]	—	—	–77	dBmp0
C-message	—	—	12	dBrnC0
3 kHz Flat[2]	—	—	20	dBrn0

1. Requires external components connected as shown in Figure 2. Transmission characteristics are specified assuming a 600 Ω resistive termination and ±1% external resistors.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance components.

Table 8. Isolation Between Channels

Parameter[1]	Min	Typ	Max	Unit
Interchannel Small-signal Crosstalk. (Both channels in forward or reverse battery state.) (2-wire to 2-wire, 2-wire to 4-wire, 4-wire to 4-wire.)	—	–90	–80	dB
Impulse Noise. (One channel ringing, other channel in forward or reverse battery state.)	—	40	47	dBrnC0

1. These parameters are not tested in production. They are guaranteed by design and device characterization.

Table 9. Data Interface and Logic

Parameter[1]	Symbol	Min	Typ	Max	Unit
High-level Input Voltage (B2, RNGNG, and NDISC)	V_{IH}	2	—	V_{CC}	V
Low-level Input Voltage (B2, RNGNG, and NDISC)	V_{IL}	0	—	0.7	V
Input Bias Current (high) (B2, RNGNG, and NDISC)	I_{IH}	–40	—	–100	µA
Input Bias Current (low) (B2, RNGNG, and NDISC)	I_{IL}	–75	—	–200	µA
High-level Output Voltage (NSTAT, open collector with internal pull-up resistor):					
(I_{OUT} = –20 µA)	V_{OH}	2.4	4.3	V_{CC}	V
(I_{OUT} = –1 µA)	V_{OH}	—	5.0	—	V
Low-level Output Voltage (NSTAT, open collector with internal pull-up resistor) (I_{OUT} = 200 µA)	V_{OL}	0	0.2	0.4	V

1. All logic voltages are referenced to AGND.

Test Configurations

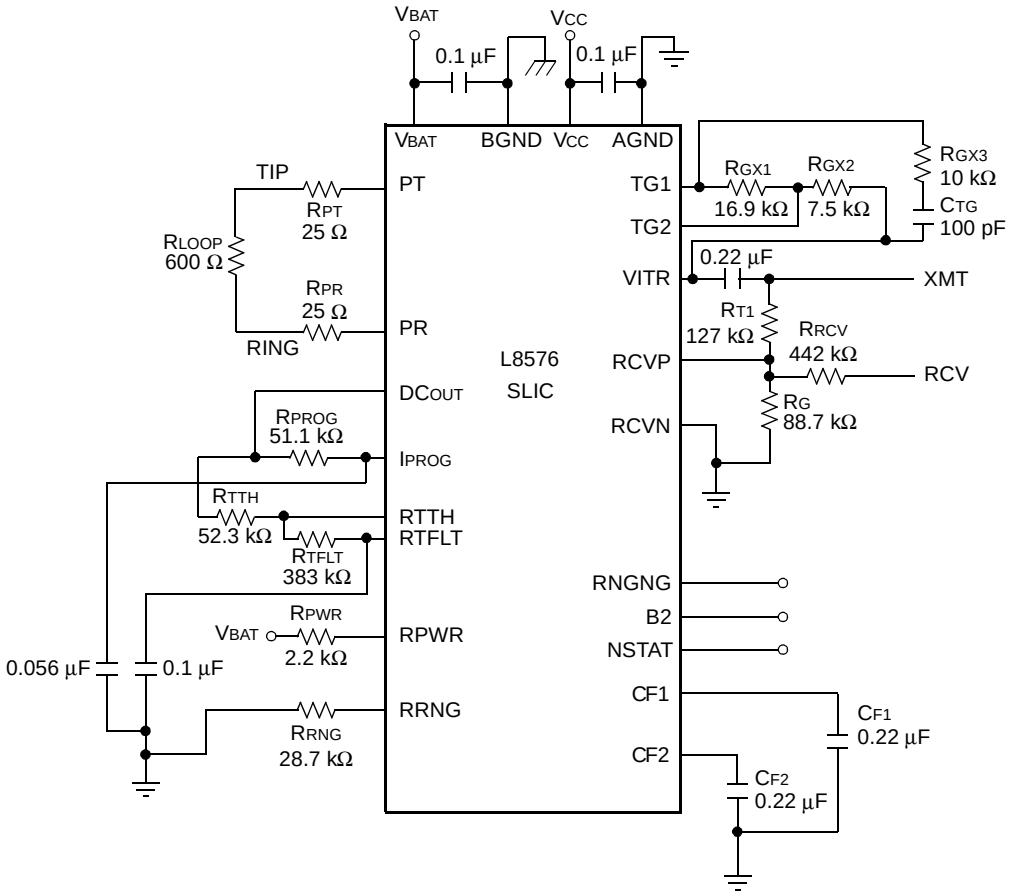


Figure 5. Basic Test Circuit

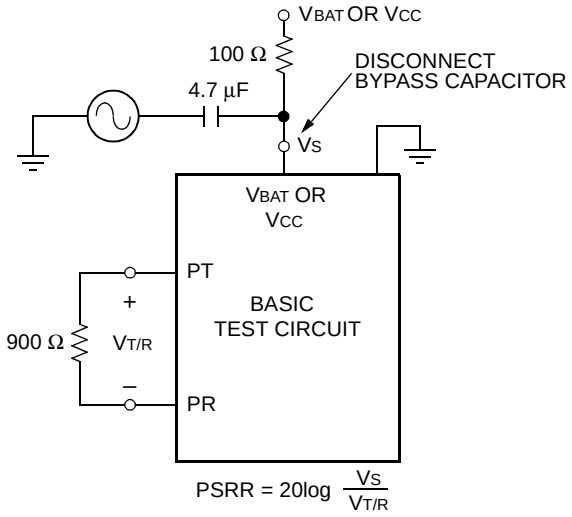


Figure 6. Metallic PSRR

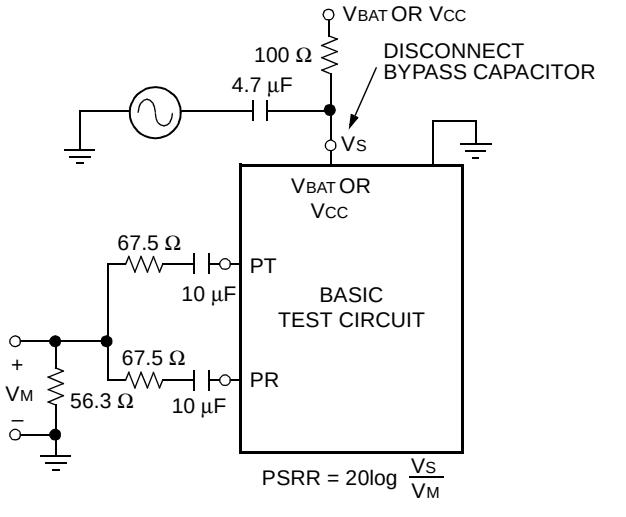


Figure 7. Longitudinal PSRR

Test Configurations (continued)

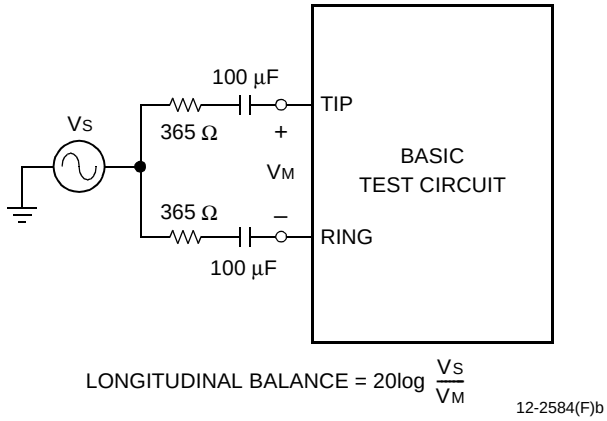


Figure 8. Longitudinal Balance

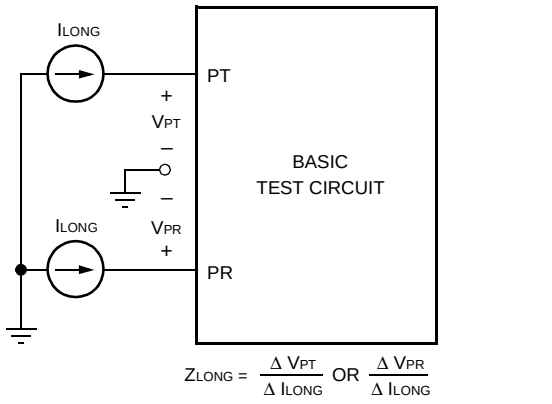


Figure 9. Longitudinal Impedance

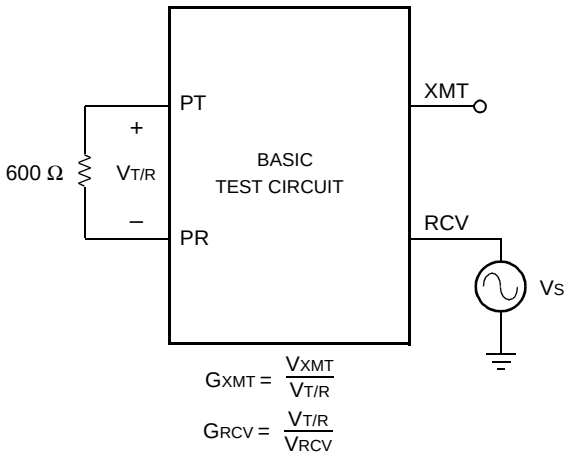
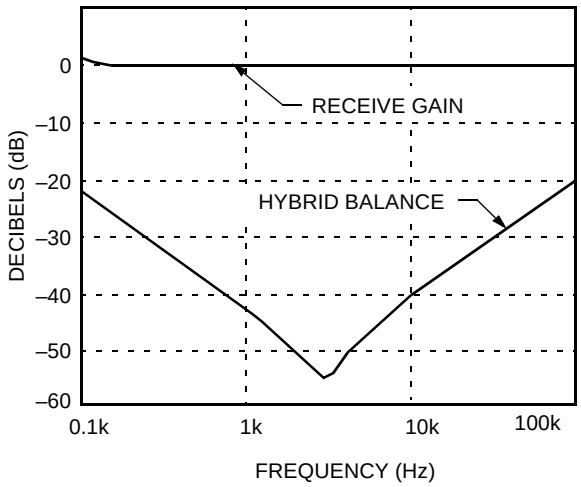


Figure 10. ac Gains

Applications

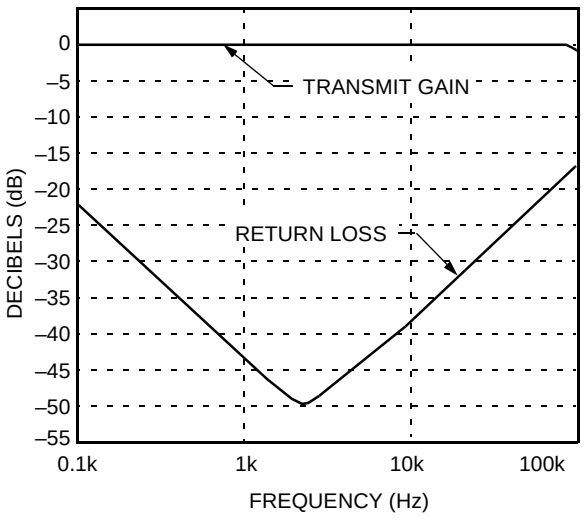
Characteristic Curves

Figures 11—16 display typical room temperature readings.



Note: Gain is normalized to 0 dB.

Figure 11. Receive Gain and Hybrid Balance vs. Frequency

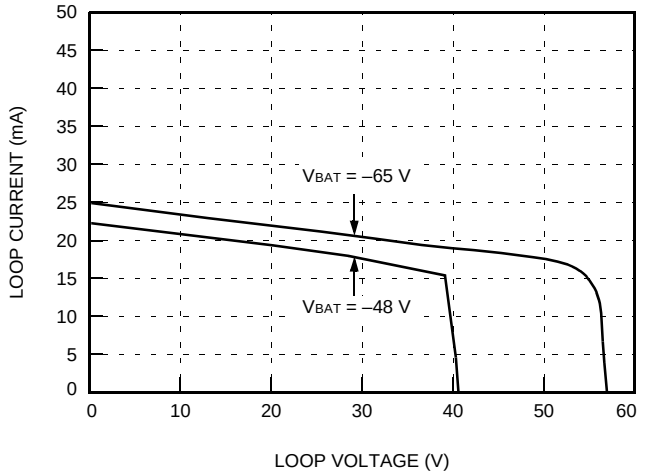


Note: Gain is normalized to 0 dB.

Figure 12. Transmit Gain and Return Loss vs. Frequency

Applications (continued)

Characteristic Curves (continued)



Note: RPROG = 51.1 kΩ.

Figure 13. Loop Current vs. Loop Voltage

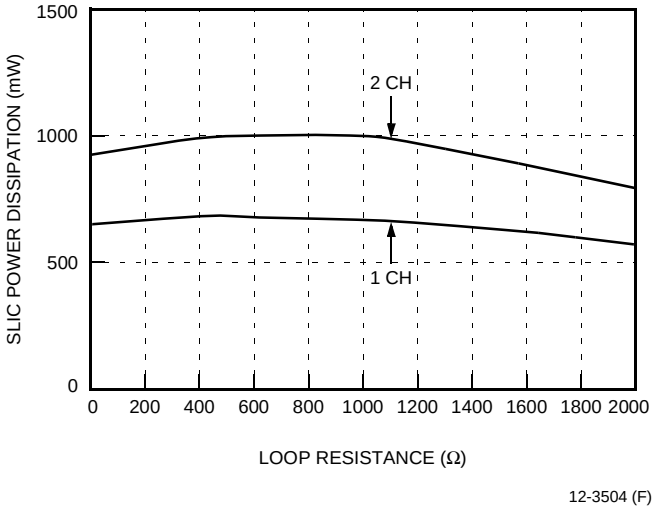
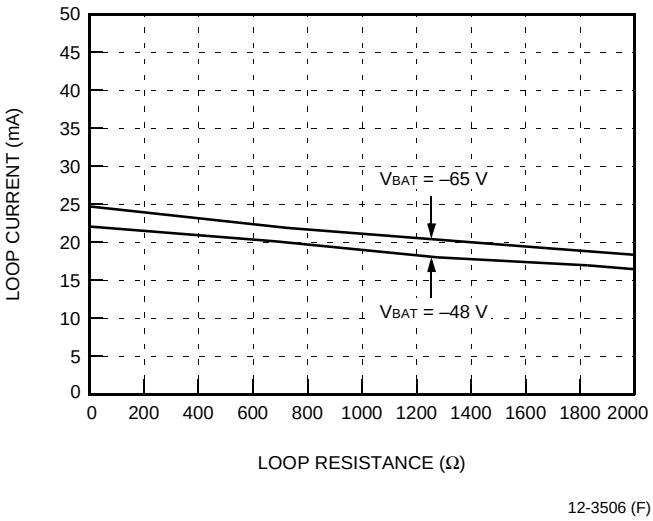


Figure 15. SLIC Power Dissipation vs. Loop Resistance (VBAT = –48 V)



Note: RPROG = 51.1 kΩ.

Figure 14. Loop Current vs. Loop Resistance

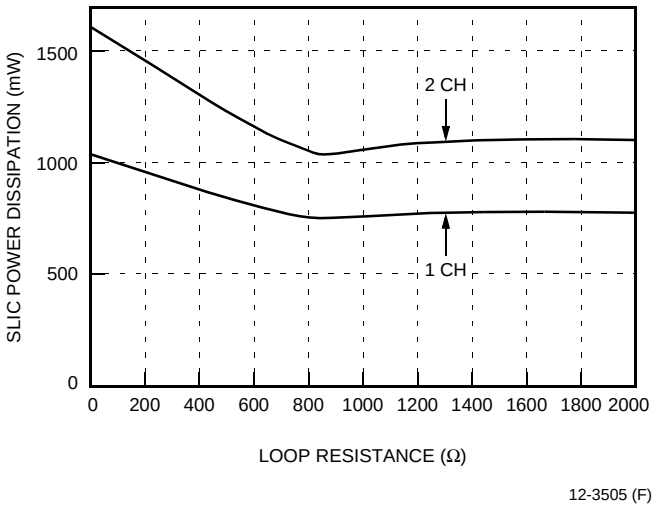


Figure 16. SLIC Power Dissipation vs. Loop Resistance (VBAT = –65 V)

Applications (continued)

dc Design

Battery Feed

The dc feed characteristic can be described by:

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

Where:
I_L = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.
V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop tip/ring voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
R_{dc} = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 17.

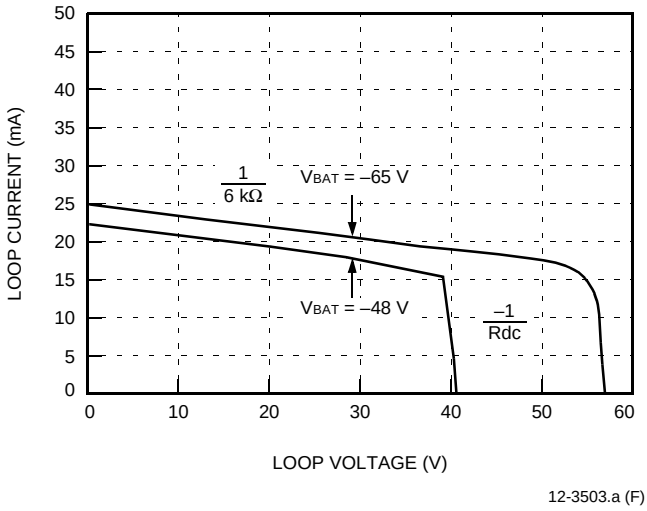


Figure 17. Loop Current vs. Loop Voltage

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1: On-hook and low loop currents. In this region, the slope corresponds to the dc resistance of the SLIC, R_{dc} (typically 60 Ω). The open circuit voltage is the battery voltage less the overhead voltage of the device, V_{OH} (default is 7.1 V typical). These values are suitable for most applications.

Region 2: Current limit. The dc current is limited to a value determined by external resistor R_{PROG}. This region of the dc template has a high resistance (6 kΩ).

Calculate the external resistor as follows:

$$R_{PROG}\ (k\Omega) = 3.5 \times (I_{LIM} - 9.2)\ mA^*$$

To control power dissipation, it is recommended that a 51.1 kΩ R_{PROG} resistor be used to set a default current-limit value of 24 mA.

RPWR

The R_{PWR} resistors dissipate the excess power associated with a single power supply, short-loop application. The resistor provides V_{BAT} to tip and ring amplifiers. There is one resistor associated with each channel. The value of R_{PWR} is dependent upon the battery potential and the current-limit value. The value of R_{PWR} can be determined by using the following equation:

$$R_{PWR} = \frac{|V_{BAT}| - 22.3}{I_{LIM} - 0.003}$$

Power dissipation of the resistor is:

$$W_{RPWR} = (I_{LIM} - 0.003)^2\ R_{PWR}.$$

For the recommended –68.5 V V_{BAT} and 24 mA I_{LIM} design, a 2.2 kΩ, 2 W resistor is suitable. 2 W resistors are available as surface-mount components.

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the tip and ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage and is expressed as:

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The L8576 is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900 Ω loop impedance.

The drive amplifiers are capable of 4 Vrms minimum (V_{AMP}). So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4\ V\left(\frac{|Z_{T/R}|}{|Z_{T/R}| + 2R_P}\right)$$

For normal forward or reverse battery operation, overhead voltage is internally set to about 8 V. In ringing mode, the overhead voltage is automatically decreased to about 4 V to permit passage of a larger ring signal.

* During the balanced ringing mode, the current limit is increased from the value predicted by this equation by a factor of 3.5.

Applications (continued)

dc Design (continued)

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. The loop closure detection threshold is internally set at 12 mA.

Power Ringing

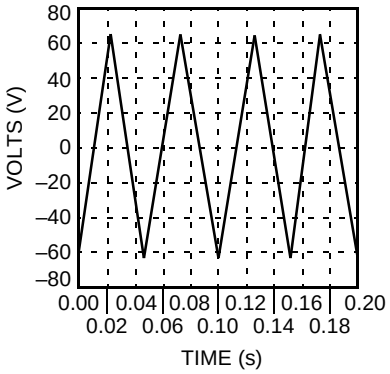
The L8576B is designed to generate a balanced trapezoidal power ring signal to tip and ring. Because the L8576B generates the power ringing signal, no ring relay is needed in this mode of operation. Alternatively, the L8576B SLIC can be used in a battery-backed, unbalanced ringing application. In this case, the ring signal is generated by a central ring generator and is bused to individual tip/ring pairs. A ringing relay is used during ringing to disconnect the L8576B from, and apply the ring generator to, the tip and ring pair.

This section discusses in detail the use of the L8576B in the balanced mode of operation.

Crest Factor

The balanced ring signal is generated by simply toggling between the powerup forward and reverse battery states. The state change is done by applying a square wave (whose frequency is the desired ring frequency) to logic input B2. Capacitors CF1 and CF2 and resistor R_{RNG} are used to control or ramp the speed of the transition of the battery reverse, thus shaping the balanced ring signal. Setting capacitor CF1 = CF2 = 0.22 µF and setting R_{RNG} to 28.7 kΩ provides a crest factor of 1.3 for a 20 Hz ring frequency. This satisfies the *Telcordia** GR-909 requirement of ringing waveform crest factor between 1.2 and 1.6. Crest factor is defined as the peak to rms voltage ratio of the ring signal. Ringing waveforms of crest factors 1.6 and 1.2 are shown in Figures 18 and 19. The crest factor can be adjusted by the value of R_{RNG} and will be influenced slightly by the value of V_{BAT}. The CF1 and CF2 capacitors should not be changed because these affect the dc feedback loop stability in current limit. An R_{RNG} value of 22.6 kΩ will lower the crest factor to about 1.2 with a –65 V or –72 V battery for a 20 Hz ring frequency. Likewise, an R_{RNG} value of 34.8 kΩ will raise the crest factor to about 1.4. For ring frequencies greater than 20 Hz, the R_{RNG} value should be lowered until the desirable crest factor is achieved. Note the RRNG is common to both sections of the device.

CF1 and CF2 must exhibit a stable capacitance value over its voltage range to ensure a properly shaped waveform. Do not use a ceramic capacitor for CF1 and CF2; use a capacitor with a polyester, polypropylene, polycarbonate, or polystyrene dielectric.



12-3346a (F)

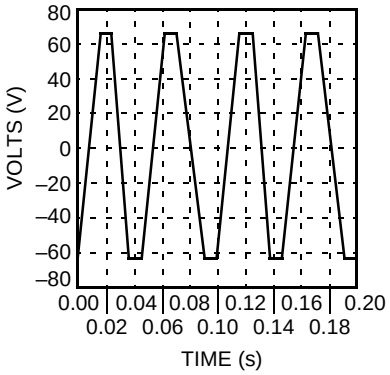
Notes:
Slew rate = 5.65 V/ms.

trise = tfall = 23 ms.

pwidth = 2 ms.

period = 50 ms.

Figure 18. Ringing Waveform Crest Factor = 1.6



12-3347a (F)

Notes:
Slew rate = 10.83 V/ms.

trise = tfall = 12 ms.

pwidth = 13 ms.

period = 50 ms.

Figure 19. Ringing Waveform Crest Factor = 1.2

* *Telcordia* is a registered trademark of Telcordia Technologies, Inc.

Applications (continued)

Power Ringing (continued)

Power Ringing Load

Telcordia GR-909 specifies that a minimum 40 Vrms must be delivered to a 5 REN ringing load of 1386 Ω + 40 µF. For 5 REN load, it is recommended that V_{BAT} be set to –68.5 Vdc. During the power ring state, the dc current limit is automatically boosted by a factor of 3.5 over the current limit set by resistor R_{PROG}. Both of these factors are necessary to ensure delivery of 40 Vrms to the North American 5 REN ringing load of 1386 Ω + 40 µF.

Ring Trip

Ring trip is accomplished by filtering the voltage seen at node DC_{OUT} and applying it to the integrated ring trip comparator. DC_{OUT} is a voltage proportional to the tip/ring current, and under short dc loop conditions, on-hook ringing current and off-hook current provide sufficient voltage differential at DC_{OUT} to distinguish that a ring trip condition has occurred. The ring trip comparator threshold is set via a resistor between the ring trip comparator and DC_{OUT}.

The output of NSTAT is automatically set to detect ring trip during the balanced ring mode. During quiet intervals of ringing, the output of NSTAT is automatically determined by the loop closure detector.

Refer to Figure 2 for the following discussion.

Capacitor C_{RT} in conjunction with resistor R_{TFLT} form a single-pole, low-pass filter that smooths the voltage seen at DC_{OUT}. The pole of the filter will influence both the ripple seen at DC_{OUT} and the speed of the transition of the voltage at DC_{OUT} from the pretrip to the tripped level.

To determine the low-pass pole:

$$f(Hz) = \frac{1}{2\pi(R_{TFLT})(C_{RT})}$$

Using the recommended 383 kΩ R_{TFLT} resistor and the 0.1 µF C_{RT} capacitor, the low-pass pole is set at 4.15 Hz.

The loop current at ring trip is given by:

$$I_{LOOP(TRIP)} = 7.76\ mA \left(\frac{R_{TTH}}{R_{GX2}}\right)$$

Using the recommended 52.3 kΩ R_{TTH} resistor and the 7.5 kΩ R_{GX2} resistor in a 20 Hz ringing application, the ring trip threshold current is set for 54 mA.

Reference Design for ISDN TA Applications

For a complete reference design, please refer to the *POTS for ISDN, WLL, and FITL/FITH Applications, Featuring Ringing SLIC Solutions* Application Note, which provides a detailed discussion of the reference design functionality. The design presented utilizes a dc to dc converter and requires only a +5 V and a +12 V supply to operate. The schematic in Figure 2 of this document portrays the SLIC and codec portions of that design.

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize signal reflections back to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is measured from the PCM highway to the 2-wire port or telephone loop. Finally, the **hybrid balance** circuit cancels the unwanted amount of the received signal that appears at the transmit port.

Applications (continued)

ac Design (continued)

Example 1, Real Termination

The following design equations refer to the circuit in Figure 20. Use these to synthesize real termination impedance.

Termination impedance:

$$Z_t = \frac{V_{T/R}}{-I_{T/R}}$$

$$Z_t = 2R_P + \frac{1500}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive gain:

$$G_{RCV} = \frac{V_{T/R}}{V_{FRO}}$$

$$G_{RCV} = \frac{12}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_t}{Z_{T/R}}\right)}$$

Transmit gain:

$$G_{TX} = \frac{V_{GSX}}{V_{T/R}}$$

$$G_{TX} = \frac{R_X}{R_{T2}} \times \frac{125}{Z_{T/R}}$$

Hybrid balance:

$$h_{bal} = 20\log\left(\frac{V_{GSX}}{V_{T/R}}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFxIN input of the codec op amp should be set to 0. The following expressions assume the hybrid balance network is the same as the termination impedance:

$$R_{HB} = \frac{R_X}{G_{RCV} \times G_{TX}}$$

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - G_{RCV} \times G_{TX}\right)$$

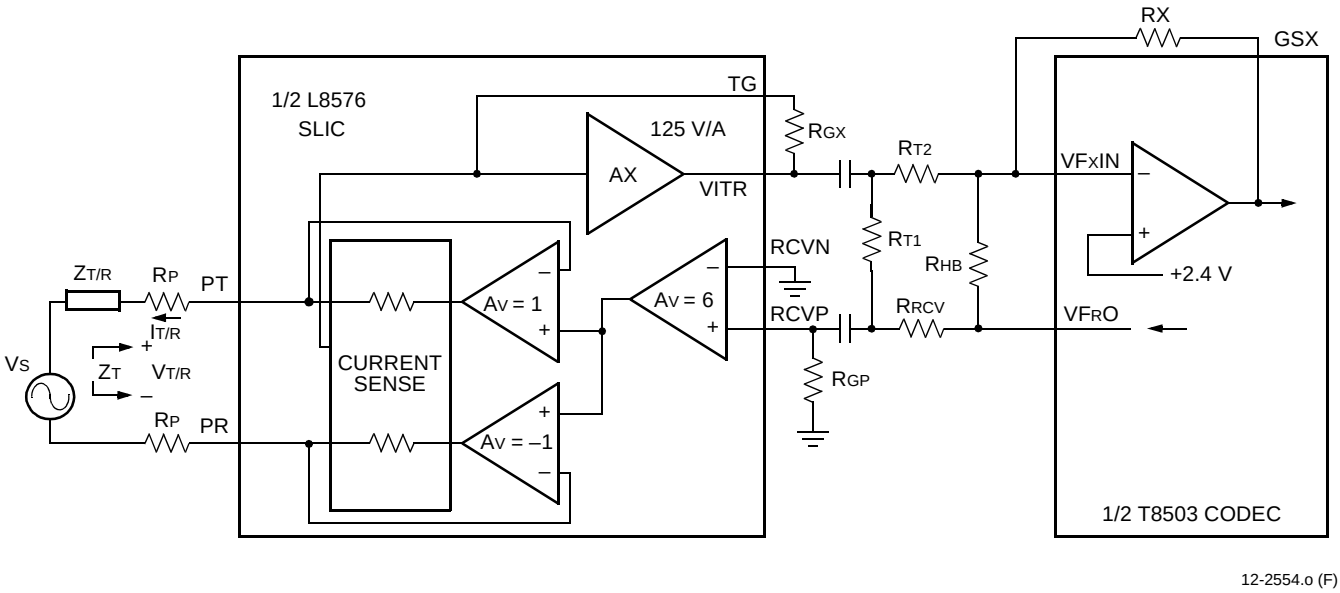


Figure 20. ac Equivalent Circuit Using a T8503 Codec

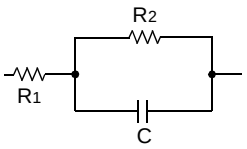
Applications (continued)

ac Design (continued)

Example 2, Complex Termination

The gain shaping required of a complex termination impedance can be synthesized using the internal AX amplifier. The following discussion and equations present a method for selecting proper component values for the SLIC/codec interface when using a complex termination.

Complex termination is usually of the form:



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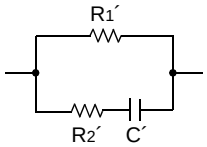
To work with this application, convert termination to the form:



5-6397(F)

where:

$R_1' = R_1 + R_2$

$R_2' = \frac{R_1}{R_2}(R_1 + R_2)$

$C' = \left(\frac{R_2}{R_1 + R_2}\right)^2 C$

For the following discussion, refer to Figure 21.

$R_{TGP}/R_{TGS}/C_{TGS}$ (Z_{TG}): These components give gain shaping to get good gain flatness. These components are a scaled version of the specified complex termination impedance. Note for pure (600 Ω) resistive terminations, components R_{TGS} and C_{TGS} are not used. Resistor R_{TGP} is used and is the series resistance combination of R_{GX1} and R_{GX2} or 24.4 kΩ.

R_X/R_{T2}: With other components set, the transmit gain (for complex and resistive terminations) R_X and R_{T2} are varied to give specified transmit gain.

$R_{T1}/R_{RCV}/R_{GP}$: For both complex and resistive terminations, the ratio of these resistors set the receive gain. For resistive terminations, the ratio of these resistors set the return loss characteristic. For complex terminations, the ratio of these resistors set the low-frequency return loss characteristic.

$C_N/R_{N1}/R_{N2}$: For complex terminations, these components provide high-frequency compensation to the return loss characteristic. For resistive terminations, these components are not used. R_{CVN} is connected to ground via a resistor.

R_{HB}: Sets hybrid balance for all terminations.

Set Z_{TG} — gain shaping:

$Z_{TG} = R_{TGP} \parallel R_{TGS} + C_{TGS}$ which is a scaled version of $Z_{T/R}$ (the specified termination resistance) in the $R_1' \parallel R_2' + C'$ form.

R_{TGP} must be 24.4 kΩ to set SLIC transconductance to 125 V/A.

$R_{TGP} = 24.4\ k\Omega$

At dc, C_{TGS} and C′ are open.

$R_{TGP} = M \times R1'$

where M is the scale factor.

$M = \frac{24.4\ k\Omega}{R_1'}$

It can be shown:

$R_{TGS} = M \times R2'$

and

$C_{TGS} = \frac{C'}{M}$

Applications (continued)

ac Design (continued)

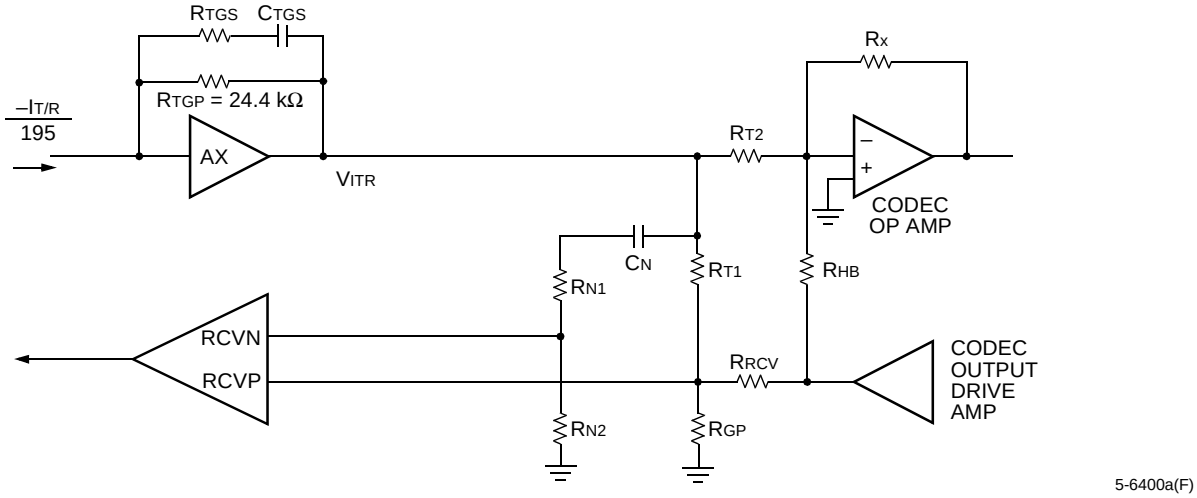
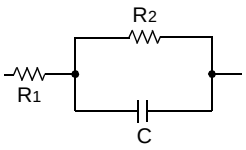


Figure 21. ac Interface Circuit Using First-Generation Codec (Blocking Capacitors Not Shown)

Transmit Gain

Transmit gain will be specified as a gain from T/R to PCM, T_X (dB). Since PCM is referenced to 600 Ω and assumed to be 0 dB, and in the case of T/R being referenced to some complex impedance other than 600 Ω resistive, the effects of the impedance transformation must be taken into account.

Again specified complex termination impedance at T/R is of the form:



First calculate the equivalent resistance of this network at the midband frequency of 1000 Hz.

$$R_{EQ} = \sqrt{\left(\frac{(2\pi f)^2 C_1^2 R_1 R_2^2 + R_1 + R_2}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2 + \left(\frac{2\pi f R_2^2 C_1}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2}$$

Using R_{EQ}, calculate the desired transmit gain, taking into account the impedance transformation:

$$T_X\ (dB) = T_{X\ (specified[dB])} + 20\log\sqrt{\frac{600}{R_{EQ}}}$$

$T_{X\ (specified[dB])}$ is the specified transmit gain. 600 Ω is the impedance at the PCM and R_{EQ} is the impedance at the T/R. $20\log\sqrt{\frac{600}{R_{EQ}}}$ represents the power loss/gain due to the impedance transformation.

Note in the case of a 600 Ω pure resistive termination at T/R $20\log\sqrt{\frac{600}{R_{EQ}}} = 20\log\sqrt{\frac{600}{600}} = 0.$

Thus, there is no power loss/gain due to impedance transformation and T_X (dB) = $T_{X\ (specified[dB])}$.

Finally, convert T_X (dB) to a ratio, G_{TX}:

$T_X\ (dB) = 20\log G_{TX}$

The ratio of R_X/R_{T2} is used to set the transmit gain:

$$\frac{R_X}{R_{T2}} = G_{TX} \times \frac{195}{M}$$

with a dual Agere codec such as T8503

$R_X < 200\ k\Omega$

Applications (continued)

ac Design (continued)

Receive Gain

Ratios of R_{RCV}, R_{T1}, R_{GP} will set both the low-frequency termination and receive gain for the complex case. In the complex case, additional high-frequency compensation, via C_N, R_{N1}, and R_{N2}, is needed for the return loss characteristic. For resistive termination, C_N, R_{N1}, and R_{N2} are not used and R_{CVN} is tied to ground and a resistor.

Determine the receive gain, G_{RCV}, taking into account the impedance transformation in a manner similar to transmit gain.

$$R_X \text{ (dB)} = R_{X\,(\text{specified[dB]})} + 20\log \sqrt{\frac{R_{EQ}}{600}}$$

$$R_X \text{ (dB)} = 20\log G_{RCV}$$

Then:

$$G_{RCV} = \frac{6}{1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}}$$

and low-frequency termination

$$Z_{TER(low)} = \frac{1500}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}} + 2R_P$$

$Z_{TER(low)}$ is the specified termination impedance assuming low frequency (C or C´ is open).

R_P is the series protection resistor.

These two equations are best solved using a computer spreadsheet.

Next, solve for the high-frequency return loss compensation circuit, C_N, R_{N1}, and R_{N2}:

$$C_N \times R_{N2} = \frac{2R_P}{1500} \; C_{TGS} \times R_{TGP}$$

$$R_{N1} = R_{N2}\left[\frac{1500}{2R_P}\left(\frac{R_{TGS}}{R_{TGP}}\right) - 1\right]$$

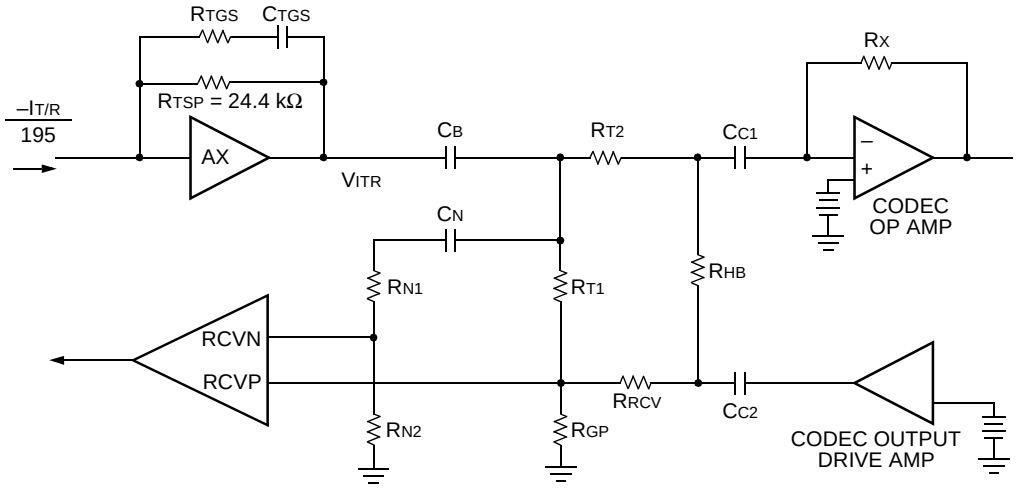
There is an input offset voltage associated with nodes R_{CVN}, R_{CVP}. To minimize the effect of the mismatch of this voltage at T/R, the equivalent resistance to ac ground at R_{CVN} should be approximately equal to that at R_{CVP}. Refer to Figure 22 (schematic with dc blocking capacitors). To meet this requirement, $R_{N2} = R_{GP} \parallel R_{T1}$.

Hybrid Balance

Set the hybrid cancellation via R_{HB}.

$$R_{HB} = \frac{R_X}{G_{RCV} \times G_{TX}}$$

If a +5 V only codec such as an Agere T8503 is used, dc blocking capacitors must be added as shown in Figure 22. This is because the codec is referenced to +2.5 V and the SLIC to ground. With the ac coupling, a dc bias at T/R is eliminated and power associated with this bias is not consumed.



5-8413 (F)

Figure 22. ac Interface Circuit Using First-Generation Codec (Including Blocking Capacitors)

Applications (continued)

ac Design (continued)

Typically, values of 0.1 µF to 0.47 µF capacitors are used for dc blocking. The addition of blocking capacitors will cause a shift in the return loss and hybrid balance frequency response toward higher frequencies, degrading the lower-frequency response. The lower the value of the blocking capacitor, the more pronounced the effect is, but the cost of the capacitor is lower. It may be necessary to scale resistor values higher to compensate for the low-frequency response. This effect is best evaluated via simulation. A *PSPICE** model for the L8576B is available.

Design equation calculations seldom yield standard component values. Conversion from the calculated value to standard value may have an effect on the ac parameters. This effect should be evaluated and optimized via simulation.

Use of an Auxiliary Battery Supply

A second lower-voltage battery supply can be used with the L8576B in order to lower the overall power consumption on a short-loop design. For long loops, any power savings will be negated, since long loops are supplied by the main battery voltage. The auxiliary battery would be connected to pins 9 and 37 in lieu of the R_{PWR} resistors. When the external R_{PWR} resistors are removed, more power will be dissipated in the SLIC so internal SLIC power dissipation must be examined.

First, determine the auxiliary battery voltage:

The auxiliary battery should be set 8 V greater than the maximum tip/ring loop voltage on the longest allowed loop, when both channels are off-hook and in current limit.

$\text{Aux Bat}_{(MAX)} = [(I_{LIM} \times R_{LOOP}) + V_{OH}]\ TOL_{VBAT}$

Where:

I_{LIM} = dc current limit set by R_{PROG} (usually 0.024).
R_{LOOP} = maximum loop resistance supported (telephone plus line resistance plus protection resistors).
V_{OH} = overhead voltage.
TOL_{VBAT} = battery tolerance, for a battery tolerance of ±5%, use 1.1.

For example, using the recommended 24 mA current limit, an overhead voltage of 8 V, and a maximum loop length of 550 Ω, the maximum auxiliary battery voltage is 23.3 V.

Next, calculate the power dissipated in the SLIC:

Components of the SLIC power dissipation are quiescent power of V_{CC} and V_{BAT} and loop current associated with V_{BAT} and Aux Bat. These can be calculated as follows:

$W_{VCC(quiescent)} = V_{CC} \times I_{CC(Max)(quiescent)}$ x 2 channels.
$W_{VBAT(quiescent)} = |V_{BAT(Max)}| \times I_{BAT(Max)(quiescent)}$ x 2 channels.
$W_{VBAT(loop\ current)} = (|V_{BAT(Max)}| - 4\ V) \times 3\ mA$ x 2 channels.
$W_{Aux\ Bat(loop\ current)} = (|\text{Aux Bat}_{(Max)}| - 4\ V) \times (I_{LIM} - 3\ mA)$ x 2 channels.

Where:

4 V is the minimum overhead voltage, and 3 mA is V_{BAT}'s contribution to loop current.

For example, substituting values from the data sheet:

$V_{CC} = 5\ V$
$I_{CC(Max)(quiescent)} = 5.5\ mA$
$V_{BAT(Max)} = -70\ V$
$I_{BAT(Max)(quiescent)} = 4\ mA$
$\text{Aux Bat}_{(Max)} = -23.3\ V$
$I_{LIM} = 24\ mA$

The following powers are calculated:

$W_{VCC(quiescent)} = 5 \times 0.0055 \times 2 = 0.055$
$W_{VBAT(quiescent)} = |-70| \times 0.004 \times 2 = 0.56$
$W_{VBAT(loop\ current)} = (|-70| - 4) \times 0.003 \times 2 = 0.396$
$W_{Aux\ Bat(loop\ current)} = (|-23.3| - 4) \times (0.024 - 0.003) \times 2 = 0.8106$

The sum of the four powers is 1.822 W.

Finally, calculate the maximum ambient temperature allowed for the calculated power dissipation:

$T_{A(max)} = T_j - (R_{\theta JA} \times P_{DISS\ SLIC(max)})$

The L8576's 44-pin PLCC exhibits a 43 °C/W thermal resistance if in an enclosure with natural airflow. The maximum operating temperature of the SLIC is 150 °C. Thermal shutdown occurs typically at 160 °C.

For example:

$T_{A(max)} = 150 - (43 \times 1.822)$
$= 150 - 78.4$
$= 71.7\ °C$

The above scenario would allow operation up to 70 °C.

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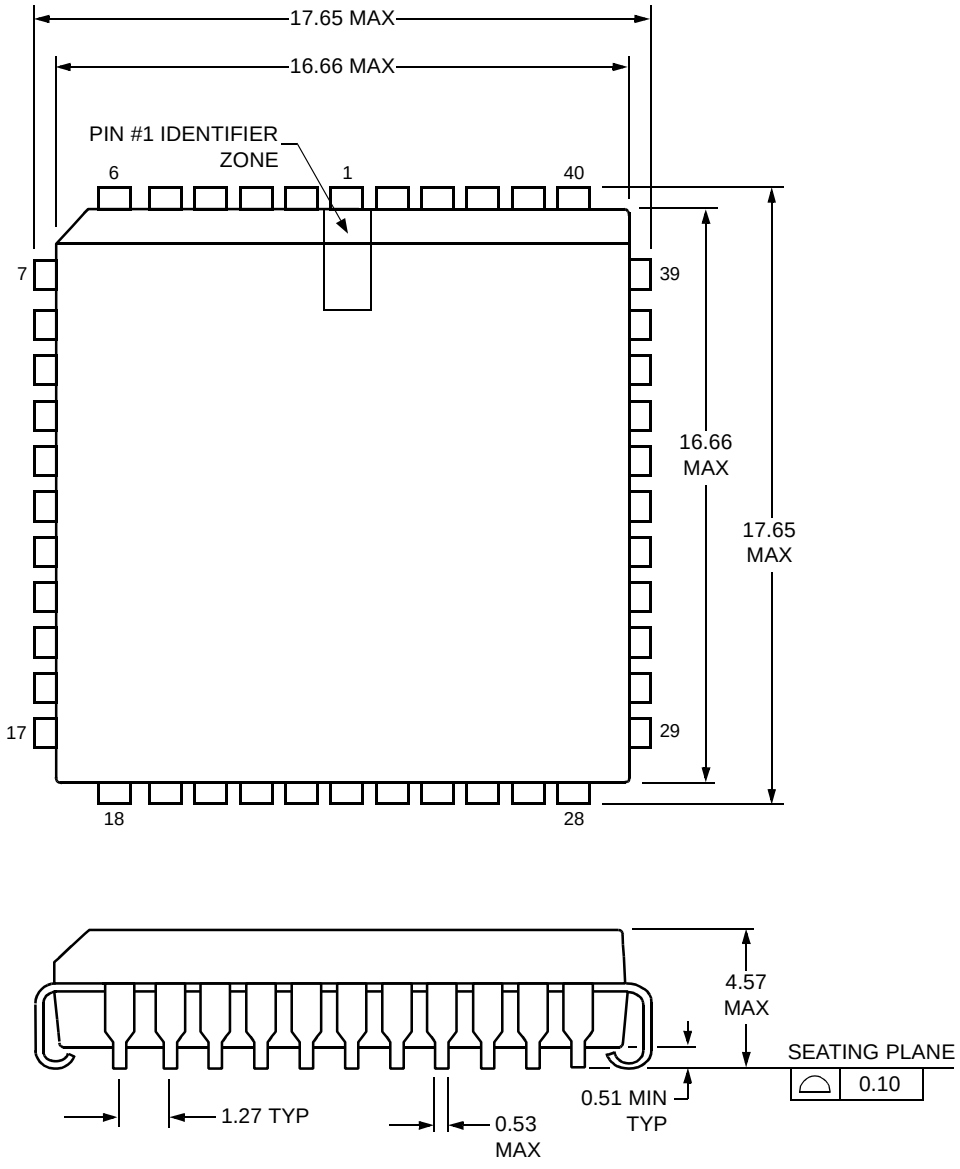
Outline Diagram

44-Pin PLCC

Dimensions are in millimeters.



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Ordering Information

Device Part No.	Description	Package	Comcode
LUCL8576BP-D	Dual SLIC	44-Pin PLCC (Dry-bagged)	108131285
LUCL8576BP-DT	Dual SLIC	44-Pin PLCC (Tape and Reel, Dry-bagged)	108131293

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