



1M x 4 Static RAM

Features

- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - 1018 mW (max.)
- Low CMOS standby power(L version)
  - 2.75 mW (max.)
- 2.0V Data Retention (400  $\mu$ W at 2.0V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features

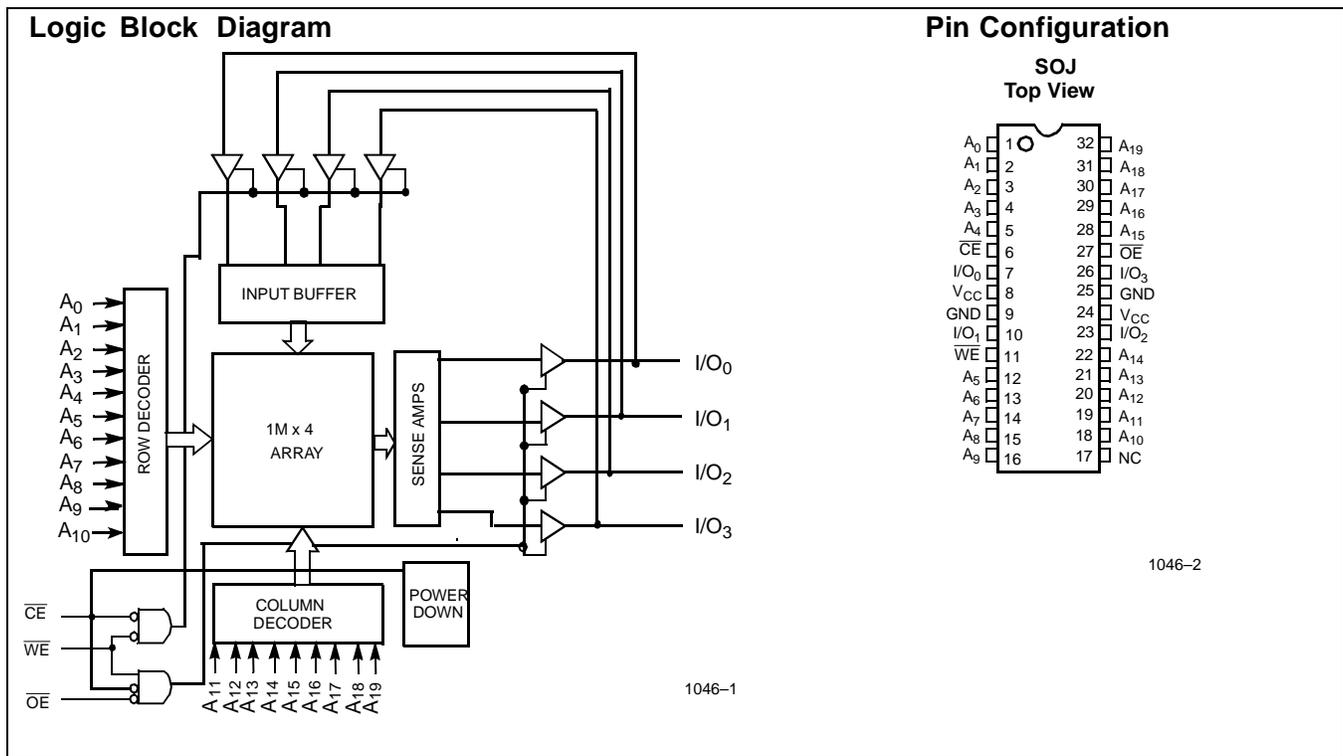
Functional Description

The CY7C1046 is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the four I/O pins (I/O<sub>0</sub> through I/O<sub>3</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O<sub>0</sub> through I/O<sub>3</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1046 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

	7C1046-10	7C1046-12	7C1046-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	185	170	150
Maximum CMOS Standby Current (mA)	Com'l	8	8
	L version	0.5	0.5

Shaded areas contain pre-release information.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> + 0.5V

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V–5.5V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1046-10		7C1046-12		7C1046-15		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		185		170		150	mA	
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		20		20		20	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0	Com'l		8		8		8	mA
			L version		0.5		0.5		0.5	

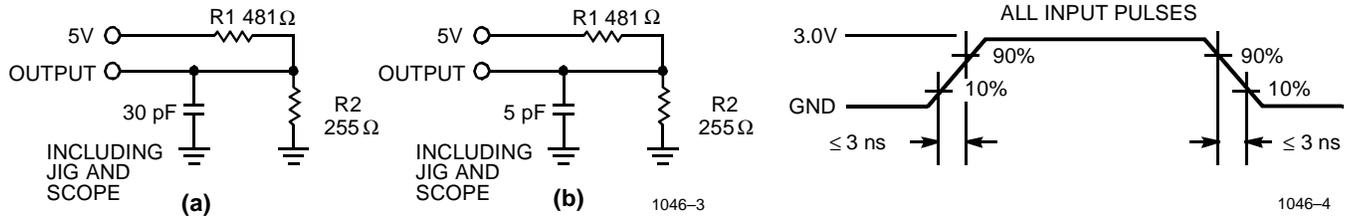
Shaded areas contain pre-release information.

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	6	pF
C <sub>OUT</sub>	I/O Capacitance		6	pF

**Note:**

1. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
2. T<sub>A</sub> is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  
 OUTPUT  $\text{---} \frac{167\Omega}{\text{---}} \text{---} 1.73\text{V}$

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	7C1046-10		7C1046-12		7C1046-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	10		12		15		ns
$t_{AA}$	Address to Data Valid		10		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		4		6		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low $Z^{[6]}$	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High $Z^{[5, 6]}$		5		6		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low $Z^{[6]}$	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High $Z^{[5, 6]}$		5		6		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
<b>WRITE CYCLE<sup>[7, 8]</sup></b>								
$t_{WC}$	Write Cycle Time	10		12		15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7		8		10		ns
$t_{AW}$	Address Set-Up to Write End	7		8		10		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		10		ns
$t_{SD}$	Data Set-Up to Write End	5		6		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low $Z^{[6]}$	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High $Z^{[5, 6]}$		5		6		7	ns

Shaded areas contain pre-release information.

**Notes:**

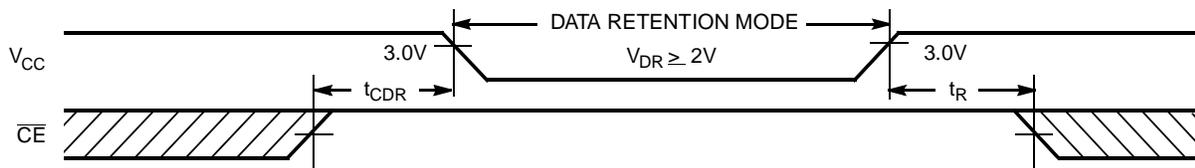
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range

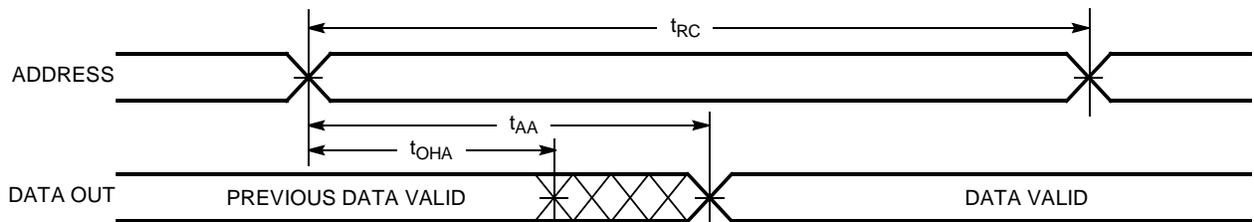
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l		200	$\mu$ A
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[9]}$	Operation Recovery Time		10		$\mu$ s

**Notes:**

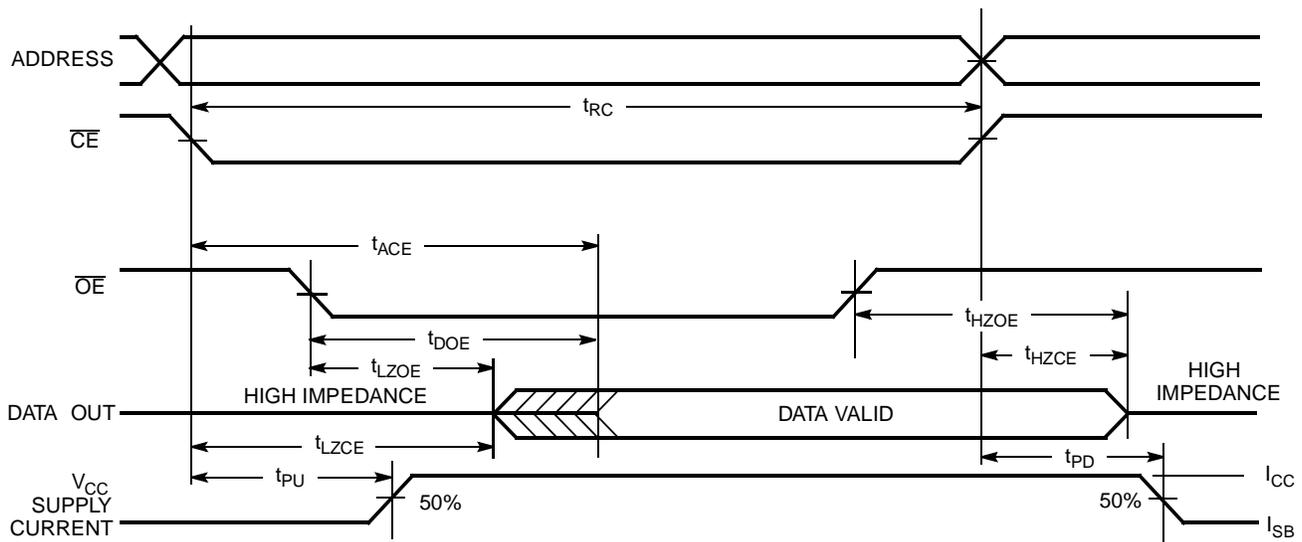
9.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 ns and slower speeds.  
 10. No input may exceed  $V_{CC} + 0.5V$ .

**Data Retention Waveform**


1046-5

**Switching Waveforms**
**Read Cycle No. 1<sup>[11, 12]</sup>**


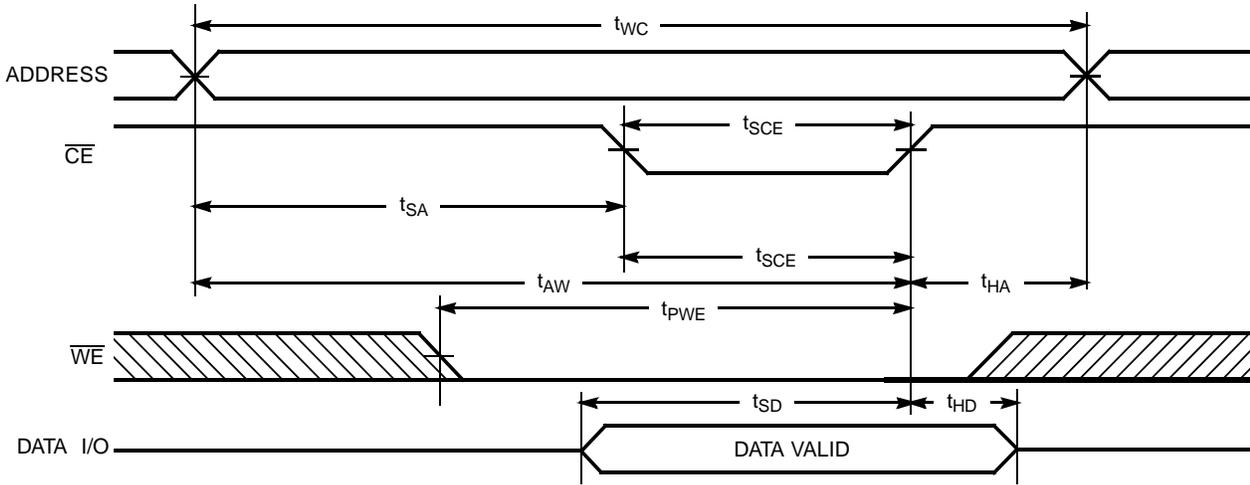
1046-6

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>**


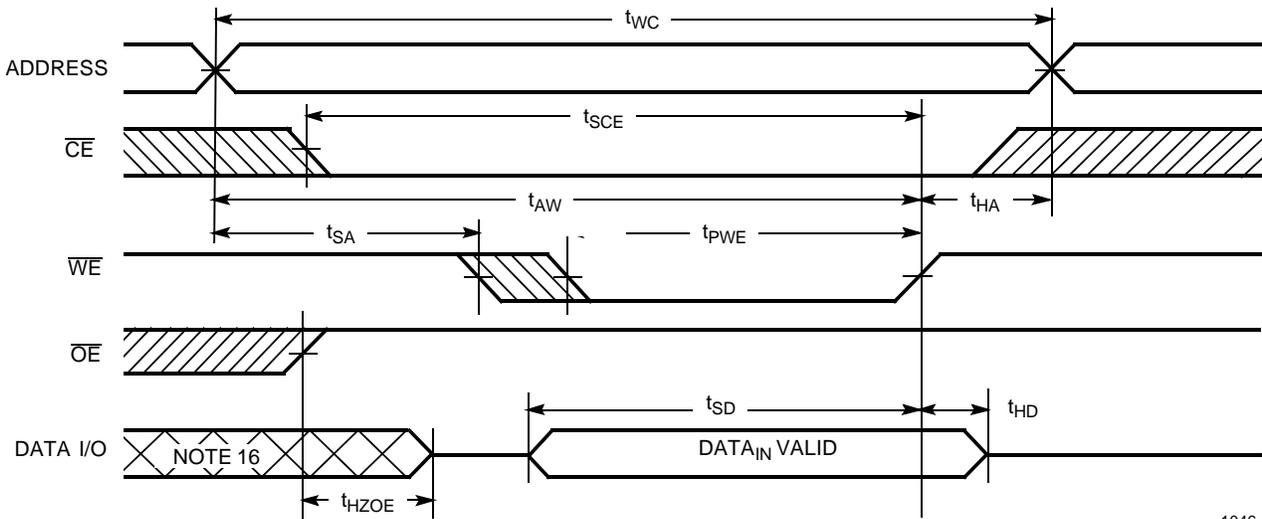
1046-7

**Notes:**

11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .  
 12.  $\overline{WE}$  is HIGH for read cycle.  
 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[14, 15]</sup>**


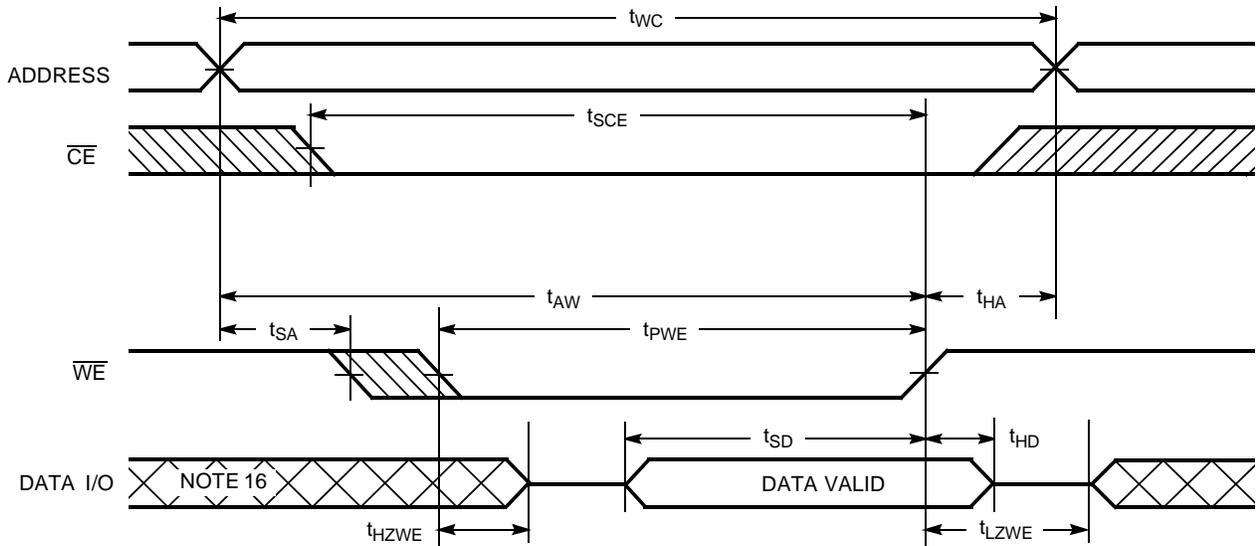
1046-8

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[14, 15]</sup>**


1046-9

**Notes:**

14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[15]</sup>**


1046-10

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1046-10VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
12	CY7C1046-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046-15VC	V33	32-Lead (400-Mil) Molded SOJ	
10	CY7C1046L-10VC	V33	32-Lead (400-Mil) Molded SOJ	
12	CY7C1046L-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046L-15VC	V33	32-Lead (400-Mil) Molded SOJ	

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**Package Diagram**
**32-Lead (400-Mil) Molded SOJ V33**
