Weltrend Semiconductor, Inc.

WT9102

150 MHz I²C RGB Video Preamplifier with Internal OSD and 4 DAC

Data Sheet

REV. 0.9

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General Description

The WT9102 pre-amp is an integrated CMOS CRT preamp and On Screen Display (OSD) generator. It has an I^2C interface which allows control of all the parameters necessary to directly setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs which are well matched to the integrated bias clamp ICs. The WT9102
pre-amp is also designed to be compatible with the high gain driver family.
Black level clamping of the signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional black level clamp capacitors. Horizontal and vertical blanking of the outputs is provided and the length of the vertical blanking is register programmable. The IC is packaged in an industry standard 24 lead DIP molded plastic package.

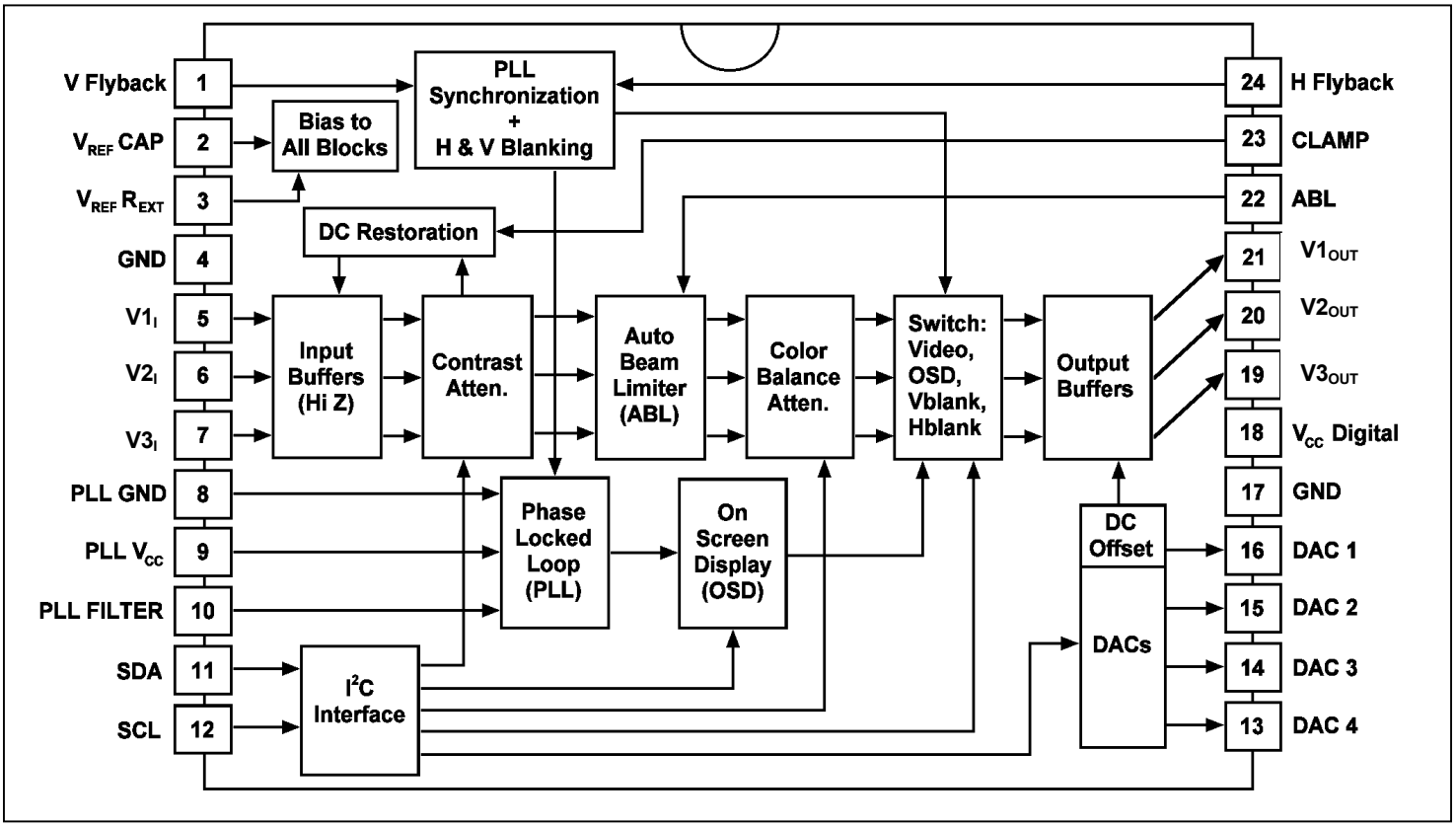
Features

- I^2C compatible interface.
- Internal 254 character OSD (190x2 plus 64x4 color).
- OSD override allows OSD messages to replace video and the use of burn-in screens.
- 4 DAC outputs (8 bit resolution) for bus controlled CRT bias and brightness.
- Spot killer which blanks the video outputs when V_{CC} falls below the specified threshold.
- Suitable for use with discrete or integrated clamp, with software configurable brightness mixer.
- H and V blanking (V width is register programmable).
- Power Save (Green) Mode with 80% power reduction.

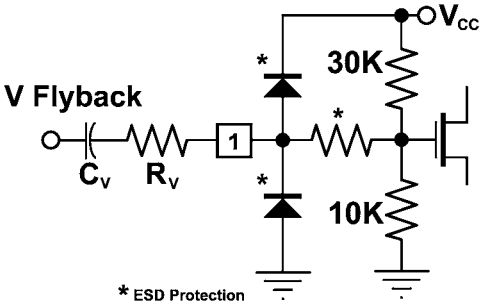
Applications

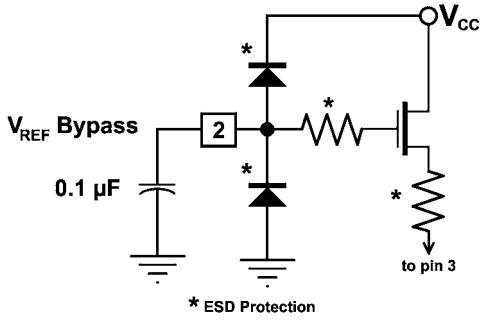
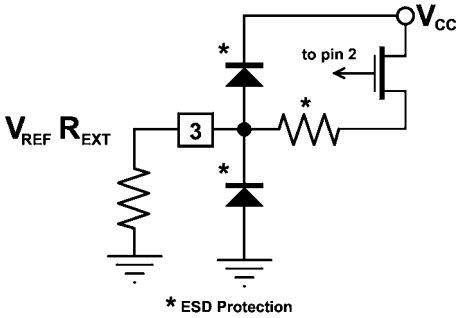
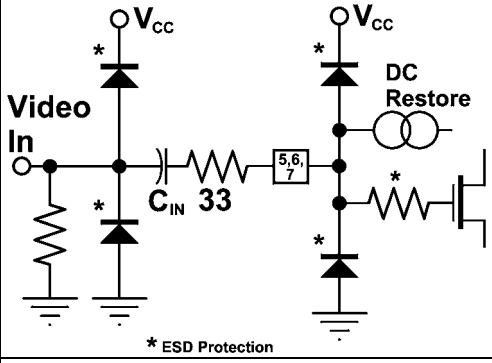
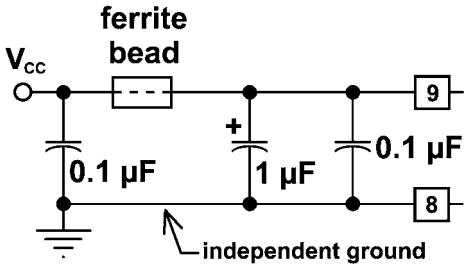
- Color monitors with OSD.
- 1280 x 1024 displays up to 75Hz
- Pixel clock frequencies up to 135MHz
- Monitors requiring cathode blanking

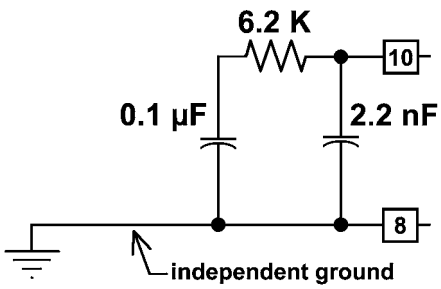
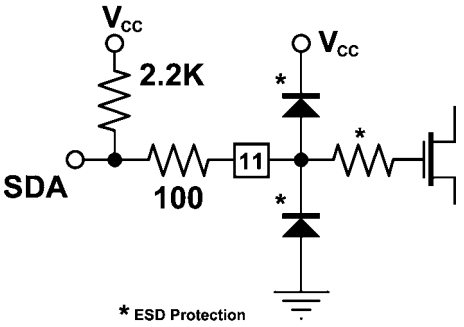
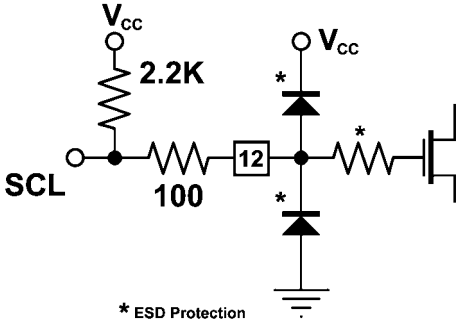
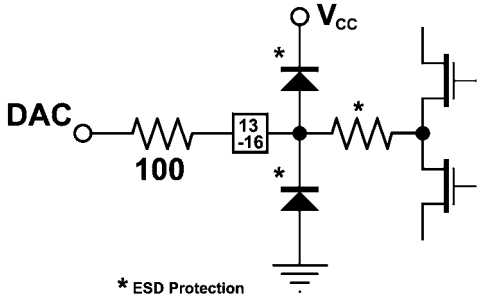
Block Diagram

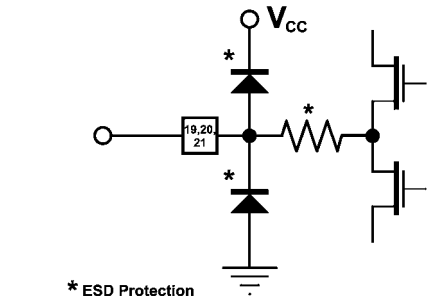
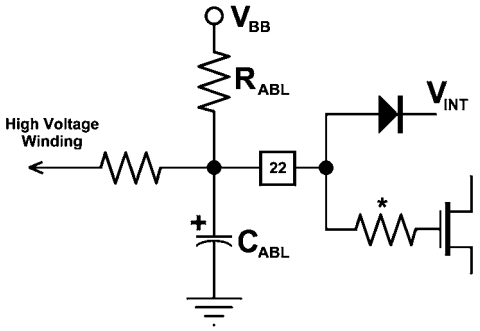
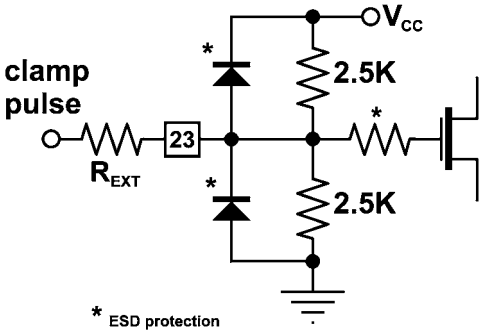
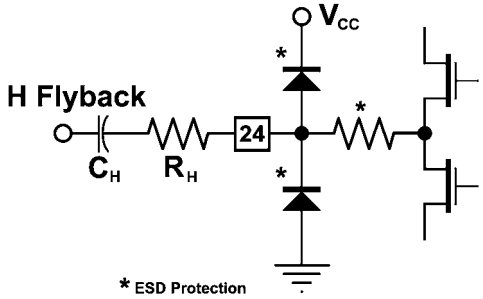


Pin Descriptions and Application Information

Pin No.	Pin Name	Input Equivalent	Description
1	V Flyback		Required for OSD synchronization and is also used for vertical blanking of the video outputs. The switching threshold is about 25% of V_{CC}. An AC coupled differentiator is recommended, where R_V is large enough to limit the peak to peak voltage at pin 1 to be within the supply rails. C_V should be small enough to flatten the vertical rate ramp at pin 1.

2	V_{REF} Bypass		**Provides filtering for the internal voltage which sets the internal bias current in conjunction with R_{EXT}. A minumum of 0.1 µF is recommended for proper filtering. This capacitor should be placed as close to pin 2 and the pin 4 ground return as possible.**
3	V_{REF} Current Set		**External resistor, 10 K 1%, sets the internal bias current level for optimum performance of the WT9102. This resistor should be placed as close to pin 3 and the pin 4 ground return as possible.**
4	Analog Ground		**This is the ground for the analog portions of the WT9102 internal circuitry.**
5 6 7	Video 1 Input Video 2 Input Video 3 Input		**These video inputs must be AC coupled with a 0.0047 µF cap. Internal DC restoration is done at these inputs. A series resistor of about 33 ohms and external ESD protection diodes should also be used for protection from ESD damage.**
8 9	PLL Ground PLL V_{CC}		**The ground pin should be connected to the rest of the circuit ground by a short but independent PCB trace to prevent contamination by extraneous signals. The V_{CC} pin should be isolated from the rest of the V_{CC} line by a ferrite bead and bypassed to pin 8 with an electrolytic capacitor and a high frequency ceramic.**

10	**PLL Filter**		**Recommended topology and values are shown in this figure. It is recommended that both filter branches be bypassed to the independent ground as close to pin 8 as possible.**
11	**SDA**		**The I^2C data line. A pull-up resistor of about 2 Kohms should be connected between this pin and V_{CC}. A resistor of at least 100 ohms should be connected in series with the data line for protection against arcing.**
12	**SCL**		**The I^2C clock line. A pull-up resistor of about 2 Kohms should be connected between this pin and V_{CC}. A resistor of at least 100 ohms should be connected in series with the clock line for protection against arcing.**
13 **14** **15** **16**	**DAC 4 Output** **DAC 3 Output** **DAC 2 Output** **DAC 1 Output**		**DAC outputs for cathode cut-off adjustments and brightness control. DAC 4 can be set to change the outputs of the other three DACs, acting as a brightness control. The DAC values and the special DAC 4 function are set through the I^2C bus. A resistor of at least 100 ohms should be connected in series with these outputs for protection against arcing.**
17	**Ground**		**Ground pin for the digital portion of the WT9102 circuitry.**
18	**Digital V_{CC}**		**Power supply pin for both analog and digital sections of the WT9102.**

19 20 21	Video 3 Output Video 2 Output Video 1 Output		These are the three video output pins. They are intended to drive the LM246x family of cathode drivers. Nominally, about 2 volts peak to peak will produce 40 volts peak to peak of cathode drive.
22	ABL		The Automatic Beam Limiter input is biased to the desired beam current limit by R_{ABL} and V_{BB} and normally keeps D_{INT} forward biased. When the current resupplying the CRT capacitance (averaged by C_{ABL}) exceeds this limit, then D_{INT} begins to turn off and the voltage at pin 22 begins to drop. The WT9102 then lowers the gain of the three video channels until the beam current reaches an equilibrium value.
23	CLAMP		This pin accepts either TTL or CMOS logic levels. The internal switching threshold is approximately one-half of V_{CC}. An external series resistor, R_{EXT}, of about 1K is recommended to avoid overdriving the input devices.
24	H Flyback		Required for OSD synchronization and is also used for horizontal blanking of the video outputs. Proper switching requires current reversal, so AC coupling is recommended, a capacitor for logic level input or a flyback transformer winding for deflection input. See ratings for maximum current levels and make sure R_H is large enough to limit these currents appropriately. C_H should be large enough to make the time constant, R_HC_H significantly larger than the horizontal period.