Product Brief
SQP 6186

Satellite Receiver for DVB-S / DSS

The SQP 6186 is a Digital Satellite Receiver device which is fully compliant with the DVB-S (ETSI 300 421) and DSS (ITU 10-11/S86) standards for satellite transmission systems.

The SQP 6186 integrates all analog and digital data processing functions from baseband input to the transport stream output.

Applications
- Digital satellite TV Sets
- Digital satellite STB's

System Integration
- Analog baseband inputs
- DVB-S/DSS compliant transport stream (TS) output
- DiSEqC 2.x interface
- I^2C bus interface (400 kbit/s) including bus loop through for tuner control
- Six general purpose I/Os, including two PDMs
- Single free running oscillator

Features
- Fully compliant to DVB-S and DSS
- Demodulation of MCPC and SCPC signals
- Symbol rates from 1 to 45 Msym/s
- Buffered analog I/Q baseband single ended inputs
- Integrated anti-alias filters
- Integrated 6 bit ADCs
- DAC based tuner AGC control output
- Integrated FEC
- Fully digital symbol clock and carrier recoveries
- Automatic symbol rate and carrier offset acquisition
- LNB offset tracking up to ±1/2 of sampling frequency
- Matched filters
- BER measurement

Benefits
- Direct conversion tuner support
- Integrated analog baseband filters
- Integrated analog AGC circuitry
- Fast automatic acquisition and tracking modes
- Automatic LNB frequency offset compensation for fast channel switching
- Dynamic transport stream gap reduction
- No real time software required
- Minimum external components required

Technology
- Based on Infineon mixed signal technology
- 3.3 V power supply
- 5 V tolerant digital IO pins
- Low cost P-MQFP-100-package

SQP 6186: Block Diagram
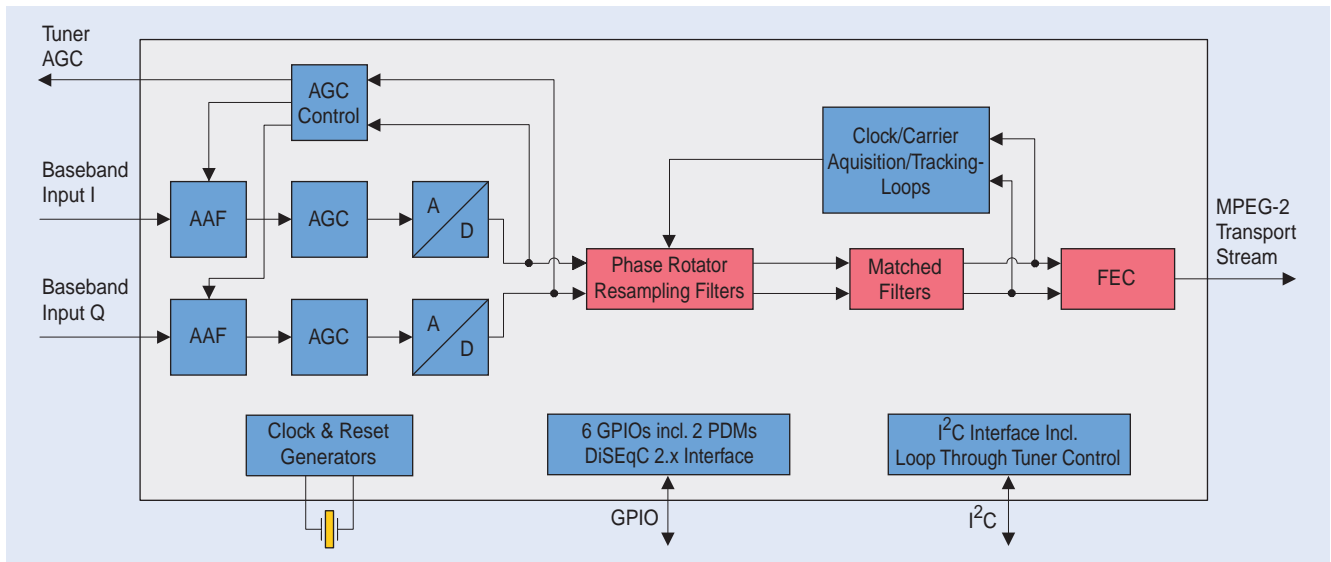
Signal Processing of the Single-Chip Satellite Receiver SQP 6186

The baseband input signals are fed into the digital satellite receiver SQP 6186. Internal anti-alias filters suppress neighboring channels. The internal AGC circuit controls the amplification of the analog signal for optimal ADC performance. The tuner AGC is controlled by a D/A converted signal generated by the AGC control.

The automatic detection of variable symbol rates and large carrier offsets is accomplished by recovery loops, which control resampling filters and a rotator. These loops are optimized for fast acquisition after channel changes and for high performance when running in their tracking modes of operation. The demodulation of MCPC and SCPC is supported. The SQP 6186 performs all inverse functions to regenerate the MPEG-2 transport stream (TS) out of the transmitted signals including FEC. The TS is fed out via a configurable parallel interface with additional TS control signals.

All required clock signals are derived from the free running crystal oscillator. The configuration and the status of the SQP 6186 are accessible via the I^2C-bus interface. Six general purpose I/Os including a DiSEqC 2.x interface are provided.

SQP 6186: Application Examples for Digital Satellite Receivers
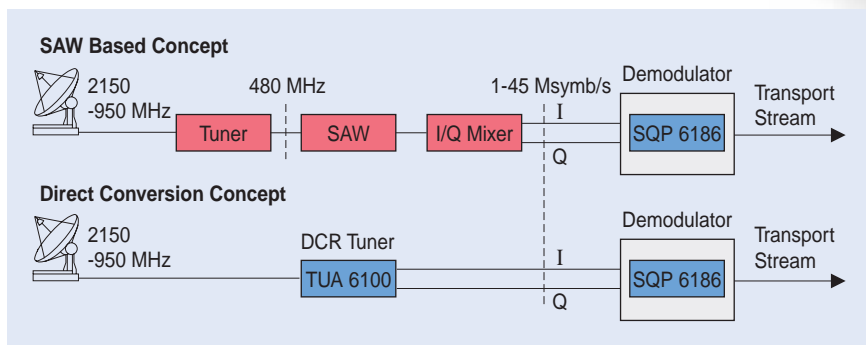
The above figure shows two different tuner concepts for DVB-S/DSS receivers. A satellite dish receives the incoming signal and a LNB converts it to a 1st IF signal.

In the SAW based concept the 1st IF signal is converted to 2nd IF by a tuner. Adjacent channels are suppressed by a SAW filter. An I/Q mixer splits up the 2nd IF signal into I and Q components and converts the signals to baseband.

The DCR concept is based on a DCR tuner, which converts the 1st IF signal directly into baseband I/Q signals, with no need of an additional SAW filter.

For both concepts the SQP 6186 provides analog baseband filtering and digital processing of the DVB-S/DSS baseband signals. The SQP 6186 digital satellite receiver may be used with a minimum number of additional components in both concepts. All major devices for the complete DCR receiver are available from Infineon Technologies AG.