Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

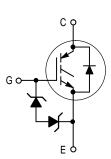
N-Channel Enhancement-Mode Silicon Gate

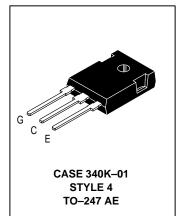
This Insulated Gate Bipolar Transistor (IGBT) is co-packaged with a soft recovery ultra-fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Its new 600V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low VCE(on). It also provides fast switching characteristics and results in efficient operation at high frequencies. Co-packaged IGBTs save space, reduce assembly time and cost. This new E-series introduces an energy efficient, ESD protected, and rugged short circuit device.

- Industry Standard TO-247 Package
- High Speed: E_{off} = 65 μJ/A typical at 125°C
- High Voltage Short Circuit Capability 10 μs minimum at 125°C, 400 V
- Low On-Voltage 2.1 V typical at 20 A, 125°C
- · Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes

MGW21N60ED

IGBT IN TO-247
21 A @ 90°C
31 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
ON-VOLTAGE





MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit	
Collector–Emitter Voltage	VCES	600	Vdc	
Collector–Gate Voltage (R _{GE} = 1.0 MΩ)	VCGR	600	Vdc	
Gate-Emitter Voltage — Continuous	VGE	±20	Vdc	
Collector Current — Continuous @ T _C = 25°C — Continuous @ T _C = 90°C — Repetitive Pulsed Current (1)	I _{C25} I _{C90} I _{CM}	31 21 42	Adc Apk	
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	142 1.14	Watts W/°C	
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 150	°C	
Short Circuit Withstand Time (V _{CC} = 400 Vdc, V _{GE} = 15 Vdc, T _J = 125°C, R _G = 20 Ω)	t _{sc}	10	μs	
Thermal Resistance — Junction to Case – IGBT — Junction to Diode — Junction to Ambient	R _θ JC R _θ JC R _θ JA	0.88 1.4 45	°C/W	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C	
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)			

⁽¹⁾ Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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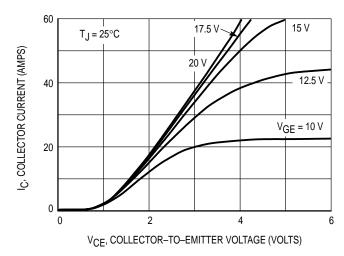
Ch	aracteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		1				
Collector-to-Emitter Breakdown \	/oltage	V(BR)CES	000			Vdc
(V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positiv	re)		600 —	— 870	_ _	mV/°C
Emitter-to-Collector Breakdown \	/oltage ($V_{GE} = 0 \text{ Vdc}, I_{EC} = 100 \text{ mAdc}$)	BVECS	15	_	_	Vdc
Zero Gate Voltage Collector Curre	nt	ICES				μAdc
	$(V_{CE} = 600 \text{ Vdc}, V_{GE} = 0 \text{ Vdc})$ $(V_{CE} = 600 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}, T_{J} = 125^{\circ}\text{C})$		_	_	10 200	
Gate-Body Leakage Current (VGI	= = ± 20 Vdc, V _{CE} = 0 Vdc)	IGES	_	_	50	μAdc
ON CHARACTERISTICS (1)						
Collector-to-Emitter On-State Vo	ltage	VCE(on)				Vdc
(V _{GE} = 15 Vdc, I _C = 10 Adc) (V _{GE} = 15 Vdc, I _C = 10 Adc, T _c	ı − 125°C)			1.7 1.5	2.1	
(VGE = 15 Vdc, IC = 10 Adc, IC (VGE = 15 Vdc, IC = 20 Adc)	j = 125 G)		_	2.2	2.5	
Gate Threshold Voltage		V _{GE(th)}				Vdc
(VCE = VGE, IC = 1.0 mAdc) Threshold Temperature Coeffici	ont (Nogotivo)		4.0	6.0 10	8.0 —	mV/°C
·						-
Forward Transconductance (VCE	= 10 Vdc, IC = 20 Adc)	9fe	_	8.6	_	Mhos
Input Capacitance		T C:	_	1605	Ι	pF
Output Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc,	Cies			_	Pi
	f = 1.0 MHz)	Coes	_	146	_	
Transfer Capacitance		C _{res}	_	23		
SWITCHING CHARACTERISTICS	(1) 	1 .		l 00		
Turn–On Delay Time	4	td(on)		29	_	ns
Rise Time	_	t _r	_	60	_	
Turn-Off Delay Time	(V _{CC} = 360 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc, L = 300 μH,	td(off)	_	238	_	
Fall Time	$R_G = 20 \Omega$	t _f	_	140		
Turn–Off Switching Loss	Energy losses include "tail"	E _{off}		0.8	1.15	mJ
Turn–On Switching Loss		E _{on}		0.6	_	
Total Switching Loss		E _{ts}	_	1.4	_	
Turn-On Delay Time		td(on)	_	28	_	ns
Rise Time		t _r	_	62	_	
Turn-Off Delay Time	(V _{CC} = 360 Vdc, I _C = 20 Adc,	^t d(off)	_	338	_	
Fall Time	V_{GE} = 15 Vdc, L = 300 μH, R _G = 20 Ω, T _J = 125°C)	t _f	_	220	_	
Turn-Off Switching Loss	Energy losses include "tail"	E _{off}	_	1.3		mJ
Turn-On Switching Loss	- - -	E _{on}	_	0.8	_	
Total Switching Loss		E _{ts}	_	2.1	_	
Gate Charge		QT	_	86	_	nC
	(V _{CC} = 360 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc)	Q ₁	_	18	_	
	GE 15 125,	Q ₂	_	39	_	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop		VFEC				Vdc
(I _{EC} = 10 Adc) (I _{EC} = 10 Adc, T _J = 125°C)			_	1.6 1.3	1.9	
(IEC = 10 Adc, TJ = 125 C)			1.7	2.0	2.3	
-		•		•		

(1) Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

(continued)

ELECTRICAL CHARACTERISTICS — **continued** ($T_J = 25$ °C unless otherwise noted)

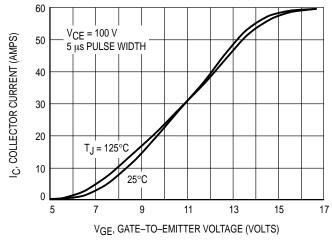
Cha	racteristic	Symbol	Min	Тур	Max	Unit
DIODE CHARACTERISTICS — con	tinued					
Reverse Recovery Time		t _{rr}	_	94		ns
	(I _F = 20 Adc, V _R = 360 Vdc, dI _F /dt = 200 A/μs)	ta	_	32	_	
		t _b	_	62	_	
Reverse Recovery Stored Charge		Q _{RR}	_	0.16	_	μC
Reverse Recovery Time	(I _F = 20 Adc, V _R = 360 Vdc, dI _F /dt = 200 A/μs, T _J = 125°C)	t _{rr}	_	145	_	ns
		t _a	_	50	_	
		t _b	_	95	_	
Reverse Recovery Stored Charge		Q _{RR}	_	0.75	_	μC
INTERNAL PACKAGE INDUCTANC	E					
Internal Emitter Inductance (Measured from the emitter lead	0.25" from package to emitter bond pad)	LE	_	13	_	nΗ



60 T_J = 125°C 17.5 V 15 V 12.5 V 12

Figure 1. Output Characteristics

Figure 2. Output Characteristics





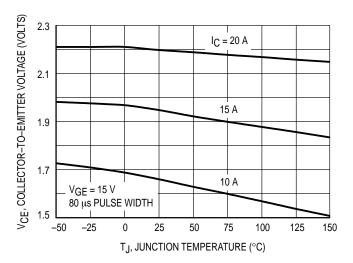


Figure 4. Collector–To–Emitter Saturation Voltage versus Junction Temperature

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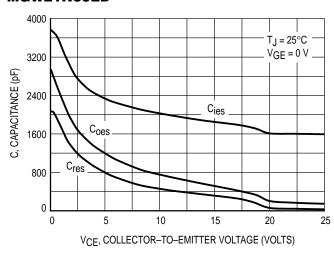


Figure 5. Capacitance Variation

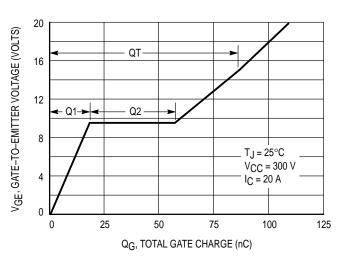


Figure 6. Gate-To-Emitter Voltage versus
Total Charge

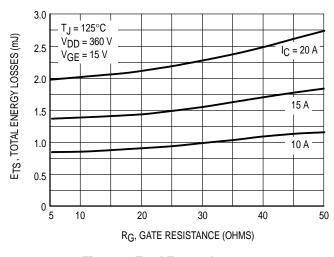


Figure 7. Total Energy Losses versus

Gate Resistance

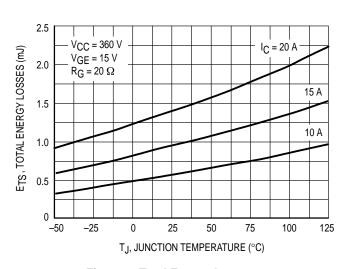


Figure 8. Total Energy Losses versus Junction Temperature

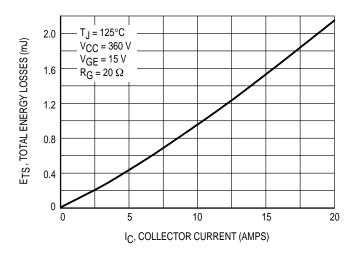


Figure 9. Total Energy Losses versus Collector Current

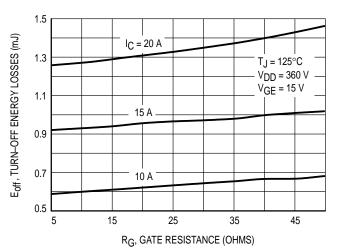


Figure 10. Turn-Off Losses versus
Gate Resistance

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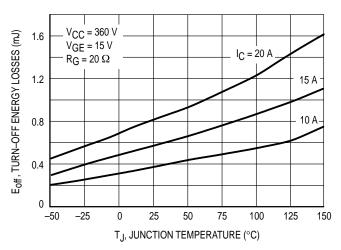


Figure 11. Turn-Off Losses versus Junction Temperature

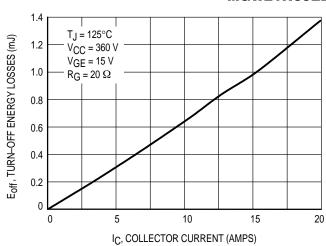


Figure 12. Turn-Off Losses versus
Collector Current

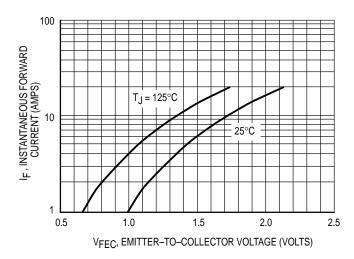


Figure 13. Forward Characteristics versus Current

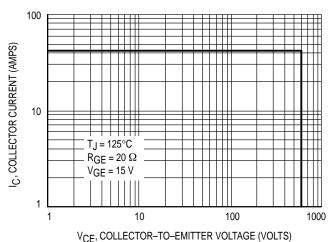
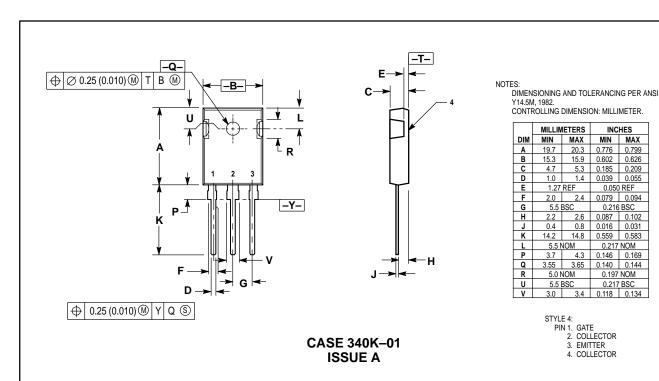


Figure 14. Reverse Biased Safe Operating Area

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