FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23004-1E

ASSP
CMOS

3 V Single Power Supply Audio Interface Unit (AIU)

MB86435

■ DESCRIPTION

The FUJITSU MB86435 is an AIU (audio interface unit) LSI for +3 V single-power source digital telephone devices, manufactured using CMOS process technology. The codec transmission filter characteristics meet G.712 standards, and can handle input and output in A-Law, μ-Law and linear conversion modes. The MB86435 also contains the necessary DTMF, microphone and receiver amps for telephone devices.

■ FEATURES

- +3 V single power supply
- Low power consumption: muting settings for each operating mode
  Normal operation : 6.0 mA TYP (speaker amp mute)
  Tone generation : 1.8 mA TYP (speaker amp mute)
  Standby mode : 0.5 μA TYP
- On-chip codec filter meets G.712 standards
- Selection of codec conversion methods (A-law, μ-law, linear)
- On-chip low-noise microphone amp (2-channel) (0 to 35 dB amplification)
- On-chip receiver speaker amps (32 ΩBTL type: 6.4 mW MIN)
- On-chip tone speaker amp (25 ΩBTL type: 10 mW MIN)
- On-chip earphone speaker amps (32 Ω single type: 2 mW MIN)

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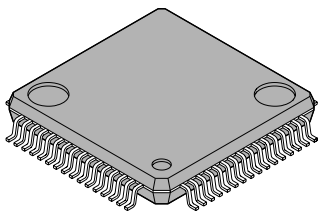
■ PACKAGE

64 pin, Plastic LQFP



(FPT-64P-M03)

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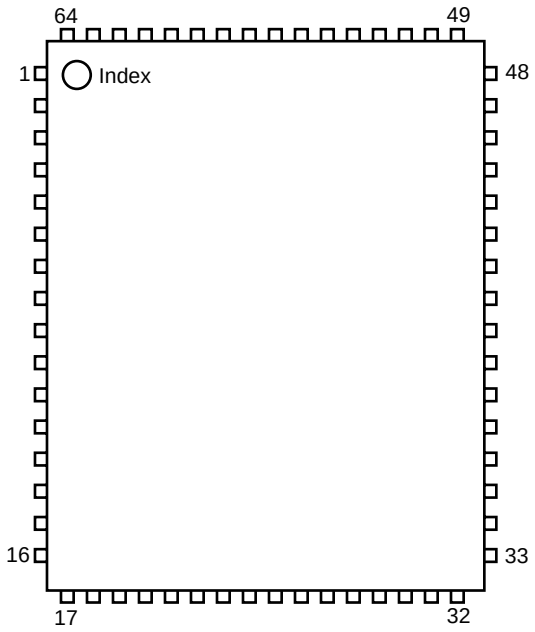
- On-chip electronic volume gain adjustments (sending, receiving, tone)
- On-chip accessory input/output circuits
- DTMF generator function
- Service tone generation
- CMOS compatible input/output

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	A/D	Description
1	VRH	O	A	Bypass capacitor connector pin for the A/D D/A reference voltage generator circuit. Place capacitor between VRH and CAG pins.
2	SGC	O	A	Bypass capacitor connector pin for the signal ground potential generator circuit. Place capacitor between SGC and CAG pins.
3	VDDAC	P	A	Analog power supply pin for codec block. To be set within range 2.7 to 3.6 V.
6	SYNC	I	D	PCM codec send/receive synchronization signal input pin. Operating clock frequency 8 kHz. CMOS interface. Constant H/L level signal will cause part of codec block to power-down.
7	CLK	I	D	Send/receive PCM signal series bit rate setting input pin. Data rate for μ-law, A-law modes may be set to any level in the range 64 k to 3.152 MHz, and for linear mode in the range 256 k to 3.152 MHz. Constant H or L level signal will cause part of codec block to power-down. CMOS interface.
8	DIN	I	D	PCM signal input pin. This signal is picked up internally at the fall of the CLK signal. CMOS interface.
9	DOUT	O	D	PCM signal output pin. Data is output in sync with the rise of the CLK signal. After data output, loses PLL synchronization, and at power-down this signal is fixed at H level. CMOS interface.
10	VDD	P	D	Digital power supply pin. To be set within range 2.7 to 3.6 V.
11	DG	G	D	Digital ground pin. To be set to 0V.
12	PSC0	I	D	Power-down control signal input pin. CMOS interface. Used with PSC1,2 pins for power-down settings.
13	PSC1	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,2 pins for power-down settings.
14	PSC2	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,1 pins for power-down settings.
				PSC 2 1 0 0 0 0 Full power-down 1 0 0 V_{REF} operating — 1 0 Tone operating —— 1 All operations available (—: value not determined)
15	SRD	I	D	9-bit serial data input pin. CMOS interface. Data is written at the rise of the signal from this pin.
16	SRC	I	D	Clock input pin for 9-bit serial data writing. CMOS interface. Data is written at the rise of this pin.
17	STB	I	D	Serial data latch strobe signal. Data is latched by the L level signal. CMOS interface.
18	XPRST	I	D	Digital reset signal input pin. CMOS interface. L level: internal latch initialization H level: normal operation
19	LO0	O	D	External control latch output pin. Outputs value D_0 of address 1000. CMOS interface.
20	LO1	O	D	External control latch output pin. Outputs value D_1 of address 1000. CMOS interface.

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Pin No.	Symbol	I/O	A/D	Description
21	LO2	O	D	External control latch output pin. Outputs value D_2 of address 1000. CMOS interface.
22	LO3	O	D	External control latch output pin. Outputs value D_3 of address 1000. CMOS interface.
23	TCLK	I	D	Tone generator clock input pin. Can be used as a tone CLK signal by using address 1110 D4D3 to subdivide the internal clock signal by factors of 1/1, 1/2, 1/4. CMOS interface.
24	TONC	I	D	Tone generator cycle control input pin. CMOS interface. Hlevel signal outputs tone.
25	LED	O	D	Ring LED control output pin. CMOS interface.
26	DSCK	I/O	A	Can be connected to EXSD or TAUD by switching bus.
27	EXSD	I/O	A	Can be connected to DSCK or TAUD by switching bus.
28	TAUD	I/O	A	Can be connected to EXSD or DSCK by switching bus.
29	DSDT	I	A	Can be connected to RAUD by switching bus.
30	TONEO	O	A	Tone signal output pin.
31	RAUD	O	A	Output pin for external speaker, or audio test signal. Can be connected to DSDT by switching paths.
32	VDDSP1	P	A	Speaker amp power supply pin. To be set within range 2.7 to 3.6 V.
33	JEAR		O	Earphone speaker amp output pin. Capable of 2 mW output at 32 Ω load.
34	XEAR	O	A	Receiver speaker amp output pin. Internally connected to EAR and BTL. Maximum output of 6.4 mW can be obtained at 32 Ω load by connecting speaker between EAR and XEAR.
35	EAR	O	A	Receiver speaker amp output pin. Connected to XEAR and BTL.
36	SPG1	G	A	Speaker amp ground pin. To be set to 0 V.
37	SPG2	G	A	Speaker amp ground pin. To be set to 0 V.
38	XTONE	O	A	Speaker amp tone output pin. Internally connected to TONE and BLT. Maximum output of 10 mW can be obtained at 25 Ω load by connecting speaker between TONE and XTONE.
39	TONE	O	A	Speaker amp tone output pin. When speaker amp is not used for tone, TONE should be shorted to IMTON.
40	IMTON	I	A	Speaker drive inverted (–) signal input pin. Can be used to adjust gain by connecting resistance to TONE and IMTON.
41	VDDSP2	P	A	Speaker amp power supply pin. To be set within range 2.7 to 3.6 V.
42	BBI	O	A	AMP3 output pin. Should be included in HPF together with IM3, to prevent DC offset from entering speakers.
43	IM3	I	A	AMP3 inverted (–) signal input pin.
44	BTO	O	A	Receiving volume adjustment circuit output pin.

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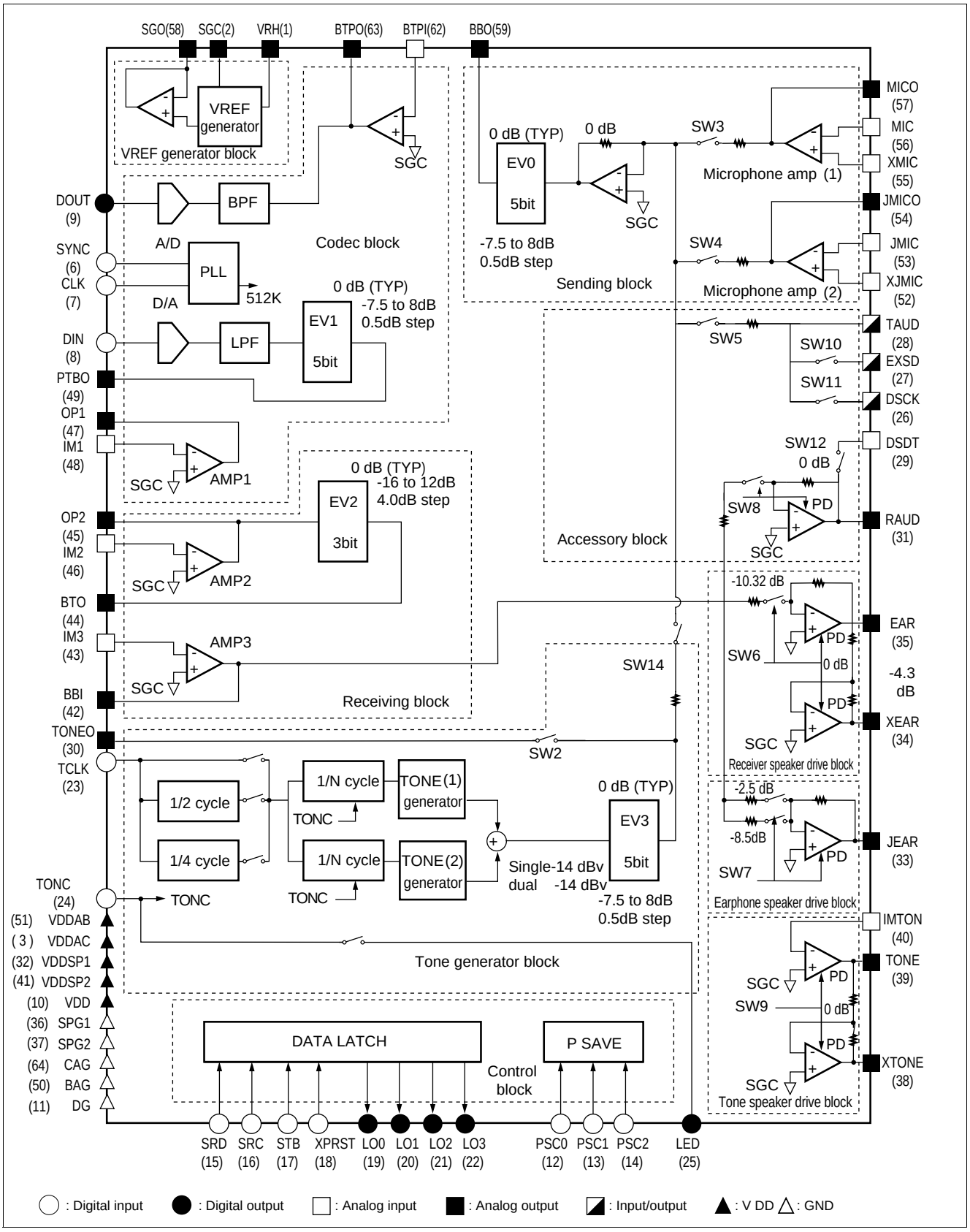
Pin No.	Symbol	I/O	A/D	Description
45	OP2	O	A	AMP2 output pin. If AMP2 is not used, IM2 should be shorted to OP2.
46	IM2	I	A	AMP2 inverted (–) signal input pin. Can form a circuit with OP2 to add sidetone or tone. Melody circuits, if used, can alsobe connected here.
47	OP1	O	A	AMP1 output pin. Can form a circuit with IM1 to include LPF or HPF in receiving block. If AMP1 is not used, IM1 should be shorted to OP1.
48	IM1	I	A	AMP1 inverted (–) signal input pin.
49	PTBO	O	A	PCM receiver output pin.
50	BAG	G	A	Analog ground pin for sending, receiving blocks. To be set to 0 V.
51	VDDAB	P	A	Analog power supply pin for sending, receiving blocks. To be set within range 2.7 to 3.6 V.
52	XJMIC	I	A	Microphone amp (2) non-inverted (+) signal input pin.
53	JMIC	I	A	Microphone amp (2) inverted (–) signal input pin.
54	JMICO	O	A	Microphone amp (2) output pin.
55	XMICI	I	A	Microphone amp (1) non-inverted (+) signal input pin.
56	MIC	I	A	Microphone amp (1) inverted (–) signal input pin.
57	MICO	O	A	Microphone amp (1) output pin.
58	SGO	O	A	Sending block signal ground potential output pin. Buffers SGC voltage.
59	BBO	O	A	Sending analog signal output pin.
62	BTPI	I	A	PCM ENCODE block input OP amp negative input pin.
63	BTPO	O	A	PCM ENCODE block input OP amp output pin.
64	CAG	G	A	Analog ground pin for codec block. To be set to 0 V.
4, 5, 60, 61	NC	—	—	Not connected. To be left open.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Register Settings

The MB86435 IC chip controls all electronic volume, switching, tone generator circuits and power-down control circuits by means of the SRD, STB and SRC data input signals.

The MB86435 uses a 9-bit serial data format consisting of a 4-bit address followed by 5 data bits. Data is picked up at the rise of the SRC signal, and latched by the STB L-level signal. The 9-bits of serial data preceding the STB signal are considered valid. These register settings are not reset at power-down. They can be reset when data is initialized by an XPRST L-level signal.

(1) Mode Settings

Control segment	Address	Data bit	Setting description	Initial data bit setting (at reset)	Remarks
	A_3 A_2 A_1 A_0	D_4 D_3 D_2 D_1 D_0		D_4 D_3 D_2 D_1 D_0	
EV0	0 0 0 1	D_4 D_3 D_2 D_1 D_0	Sending audio level adjustment. Adjusts EV0 gain.	0 1 1 1 1	*1
EV1	0 0 1 0	D_4 D_3 D_2 D_1 D_0	Sending audio level adjustment. Adjusts EV1 gain.	0 1 1 1 1	
EV2	0 0 1 1	* * D_2 D_1 D_0	Sending audio level adjustment. Adjusts EV2 gain.	* * 1 0 0	
TX-MUTE	0 1 0 0	D_4 * * * D_0	D_0: Sending audio mute SW 3, 4, 5 on/off control. Mute: 1, Unmute: 0	0 * * * 0	*2, *3
RX-MUTE			D_4: Sending audio mute SW 6, 7, 8, 9 on/off control. Mute: 1, Unmute: 0		*3, *4
SW5	0 1 0 1	D_4 * D_2 D_1 D_0	D_0: TAUD mute SW 5 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*2, *5
SW4			D_1: JMIC mute SW 4 on/off control. Mute: 1, Unmute: 0		*2
SW3			D_2: MIC mute SW 3 on/off control. Mute: 1, Unmute: 0		
SW8			D_4: RAUD mute SW 8 on/off control. Mute: 1, Unmute: 0		*3, *4, *6
SW6	0 1 1 0	D_4 * D_2 D_1 D_0	D_0: EAR, XEAR mute SW 6 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*4
SW9			D_1: TONE, XTONE mute SW 9 on/off control. Mute: 1, Unmute: 0		
SW7			D_2: JEAR mute SW 7 on/off control. Mute: 1, Unmute: 0		
ATT			D_4: JEAR attenuation level switch. 0: –2.5 dB, 1: –8.5 dB.		

(Continued)

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Control segment	Address	Data bit	Setting description	Initial data bit setting (at reset)	Remarks
	A_3 A_2 A_1 A_0	D_4 D_3 D_2 D_1 D_0		D_4 D_3 D_2 D_1 D_0	
SW10	0 1 1 1	D_4 D_3 D_2 D_1 D_0	D_0: EXSD pin selection SW 10 on/off control. On: 1, Off: 0	0 0 0 0 0	*3, *5
SW12			D_1: DSDT pin selection SW 12 on/off control. On: 1, Off: 0		*3, *6
SW11			D_2: DSCK pin selection SW 12 on/off On: 1, Off: 0		*3, *5
SW2			D_3: TONEO mute SW 2 on/off control. Mute: 1, Unmute: 0		*7
SW14			D_4: TONE sending add SW 14 on/off control. On: 1, Off: 0		
Serial/ parallel converter	1 0 0 0	* D_3 D_2 D_1 D_0	Parallel output D_3 = LO3, D_2 = LO2, D_1 = LO1, D_0 = LO0	* 0 0 0 0	*8
EV3	1 0 0 1	D_4 D_3 D_2 D_1 D_0	Tone level adjustment. Adjusts EV3 gain.	0 1 1 1 1	*1
TONE control — Frequency control	1 0 1 0	X_8 X_7 X_6 X_5 X_4	Tone (1) frequency control, set by 8-bit value X_7 to X_0. X_8 = 1 to output trapezoidal wave, X_8 = 0 to output sine wave.	0 0 0 0 0	*9, *10
	1 0 1 1	* X_3 X_2 X_1 X_0		* 0 0 1 0	
	1 1 0 0	Y_8 Y_7 Y_6 Y_5 Y_4	Tone (2) frequency control, set by 8-bit value Y_7 to Y_0. Y_8 = 1 to output trapezoidal wave, Y_8 = 0 to output sine wave.	0 0 0 0 0	
	1 1 0 1	* Y_3 Y_2 Y_1 Y_0		* 0 0 1 0	
TONE control — Output control	1 1 1 0	D_4 D_3 D_2 D_1 D_0	Tone generator control D_0: tone (2) on/off control. On: 1, off: 0 D_1: tone (1) on/off control. On: 1, off: 0 D_2: LED output on/off control. On: 1, off: 0	0 0 1 1 1	*7, *11, *12
TONE control — Master clock control			Tone CLK D_4, D_3 0 0 : TCLK1/1 frequency selected 0 1 : TCLK1/2 frequency selected 1 0 : TCLK1/4 frequency selected 1 1 : Prohibited		*9
PCM	1 1 1 1	* * * D_1 D_0	PCM control D_1, D_0 0 0 : μ-law mode selected 1 0 : A-law mode selected 0 1 : linear mode selected	* * * 0 0	*13, *14
TEST	0 0 0 0	D_4 D_3 D_2 D_1 D_0	Do not write in test mode.	0 0 0 0 0	

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*1: See (4) Electronic Volume Controls
*2: See (2) Sending Audio Mute Setting
*3: See 5. Power Saving Modes
*4: See (3) Receiving Audio Mute Settings
*5: See 2. Analog Input (2) Accessory Input
*6: See 3. Analog Output (2) Accessory Output
*7: See (5) Tone Generator Circuit • Tone Generator Control Output Level
*8: See (8) Parallel Output
*9: See (5) Tone Generator Circuit • Tone Frequency Control Registers
*10: See (5) Tone Generator Circuit • Tone Output Waveforms
*11: See (5) Tone Generator Circuit • Tone Output Controls
*12: See (5) Tone Generator Circuit • LED Output Controls
*13: See (6) Codec Input/Output
*14: See (7) The Codec SYNC Pin

(2) Sending Audio Mute Settings

Switches SW 3 to SW 5 have the following functions. Address 0100 signals have priority.

Setting										Switching setting		
Address	A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0				
	0	1	0	0	0	1	0	0				
Data bit	D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0	SW3	SW4	SW5
	—	*	*	*	1	—	*	—	—	—	○	○	○
	—	*	*	*	0	—	*	—	—	1	—	—	○
	—	*	*	*	0	—	*	—	1	—	—	○	—
	—	*	*	*	0	—	*	1	—	—	○	—	—
	—	*	*	*	0	—	*	—	—	0	—	—	×
	—	*	*	*	0	—	*	—	0	—	—	×	—
	—	*	*	*	0	—	*	0	—	—	×	—	—

○ : muted, × : unmuted, — : not determined

(3) Receiving Audio Mute Settings

Switches SW 6 to SW 9 have the following functions. Address 0100 signals have priority.

Setting														Switching setting			
Address	A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0					
	0	1	0	0	0	1	0	1	0	1	1	0					
Data bit	D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0	SW8	SW7	SW9	SW6
	1	*	*	*	—	—	*	—	—	—	—	*	—	—	—	○	○	○	○
	0	*	*	*	—	—	*	—	—	—	—	*	—	—	1	—	—	—	○
	0	*	*	*	—	—	*	—	—	—	—	*	—	1	—	—	—	○	—
	0	*	*	*	—	—	*	—	—	—	—	*	1	—	—	—	○	—	—
	0	*	*	*	—	1	*	—	—	—	—	*	—	—	—	○	—	—	—
	0	*	*	*	—	—	*	—	—	—	—	*	—	—	0	—	—	—	×
	0	*	*	*	—	—	*	—	—	—	—	*	—	0	—	—	—	×	—
	0	*	*	*	—	—	*	—	—	—	—	*	0	—	—	—	×	—	—
	0	*	*	*	—	0	*	—	—	—	—	*	—	—	—	×	—	—	—

○ : muted, × : unmuted, — : not determined

(4) Electronic Volume Controls

There are four different electronic volume controls, EV0 through EV3, with the following specifications. Electronic volume control settings are made by the SRD, SRC and STB signals, and setting values are reset by the XPRST signal. However, settings are not reset by PSC0, PSC1, PSC2 power-down mode operations.

Table 1 Relation of Volume Control Data bit Values to Gain

Step	Data bit value					EV0 sending gain adjustment	EV1 sending gain adjustment	EV2 sending gain adjustment	EV3 sending gain adjustment	Unit
	D_4	D_3	D_2	D_1	D_0	Typ.	Typ.	Typ.	Typ.	
0	0	0	0	0	0	–7.5	–7.5	–16	–7.5	dB
1	0	0	0	0	1	–7.0	–7.0	–12	–7.0	
2	0	0	0	1	0	–6.5	–6.5	–8	–6.5	
3	0	0	0	1	1	–6.0	–6.0	–4	–6.0	
4	0	0	1	0	0	–5.5	–5.5	0	–5.5	
5	0	0	1	0	1	–5.0	–5.0	4	–5.0	
6	0	0	1	1	0	–4.5	–4.5	8	–4.5	
7	0	0	1	1	1	–4.0	–4.0	12	–4.0	
8	0	1	0	0	0	–3.5	–3.5		–3.5	
9	0	1	0	0	1	–3.0	–3.0		–3.0	
10	0	1	0	1	0	–2.5	–2.5		–2.5	
11	0	1	0	1	1	–2.0	–2.0		–2.0	
12	0	1	1	0	0	–1.5	–1.5		–1.5	
13	0	1	1	0	1	–1.0	–1.0		–1.0	
14	0	1	1	1	0	–0.5	–0.5		–0.5	
15	0	1	1	1	1	0.0	0.0		0.0	
16	1	0	0	0	0	0.5	0.5		0.5	
17	1	0	0	0	1	1.0	1.0		1.0	
18	1	0	0	1	0	1.5	1.5		1.5	
19	1	0	0	1	1	2.0	2.0		2.0	
20	1	0	1	0	0	2.5	2.5		2.5	
21	1	0	1	0	1	3.0	3.0		3.0	
22	1	0	1	1	0	3.5	3.5		3.5	
23	1	0	1	1	1	4.0	4.0		4.0	
24	1	1	0	0	0	4.5	4.5		4.5	
25	1	1	0	0	1	5.0	5.0		5.0	
26	1	1	0	1	0	5.5	5.5		5.5	
27	1	1	0	1	1	6.0	6.0		6.0	
28	1	1	1	0	0	6.5	6.5		6.5	
29	1	1	1	0	1	7.0	7.0		7.0	
30	1	1	1	1	0	7.5	7.5		7.5	
31	1	1	1	1	1	8.0	8.0		8.0	

Note: Each setting value is determined in relation to the initial setting value.
Returns to initial value at reset (——— parts)
EV2 data bits D_4, D_3 are *.

Table 2 Volume Gain Deviation

Volume control No.	Condition	Min.	Typ.	Max.	Unit
EV0 EV1 EV3	Gain deviation, with respect to reference value shown in Table1 Input frequency = 1020 Hz Input level = – 20 dBv	Reference value – 0.5 dB	Reference value	Reference value + 0.5 dB	dB
EV2		Reference value – 1.0 dB	Reference value	Reference value + 1.0 dB	

(5) Tone Generator Circuit

- **Tone Frequency Control Registers**

  The tone generator uses a clock signal obtained by subdividing the TCLK clock signal input by 1/1, 1/2 or 1/4 according to the data bit in address 1110.

Table 3 Tone Clock Frequency Register Control

Address 1110		Tone generator clock signal (f_{IN})
D_4	D_3	
0	0	TCLK input clock signal
0	1	TCLK input clock signal subdivided by 1/2
1	0	TCLK input clock signal subdivided by 1/4
1	1	Prohibited

Frequency settings available through the tone frequency control register are determined by the following formula. Frequency setting $f = f_{IN}/(12*(1+n))$, n=1, 2, 3, ..., 255. (where f_{IN}: tone generator clock signal frequency). Therefore the available frequency setting range when f_{IN} = 512 kHz is between f_{min} = 167 Hz and f_{max} = 21333 Hz.

Frequency settings corresponding to each DTMF rated reference frequency are shown in the following table.

Table 4 Tone Frequency Register Control

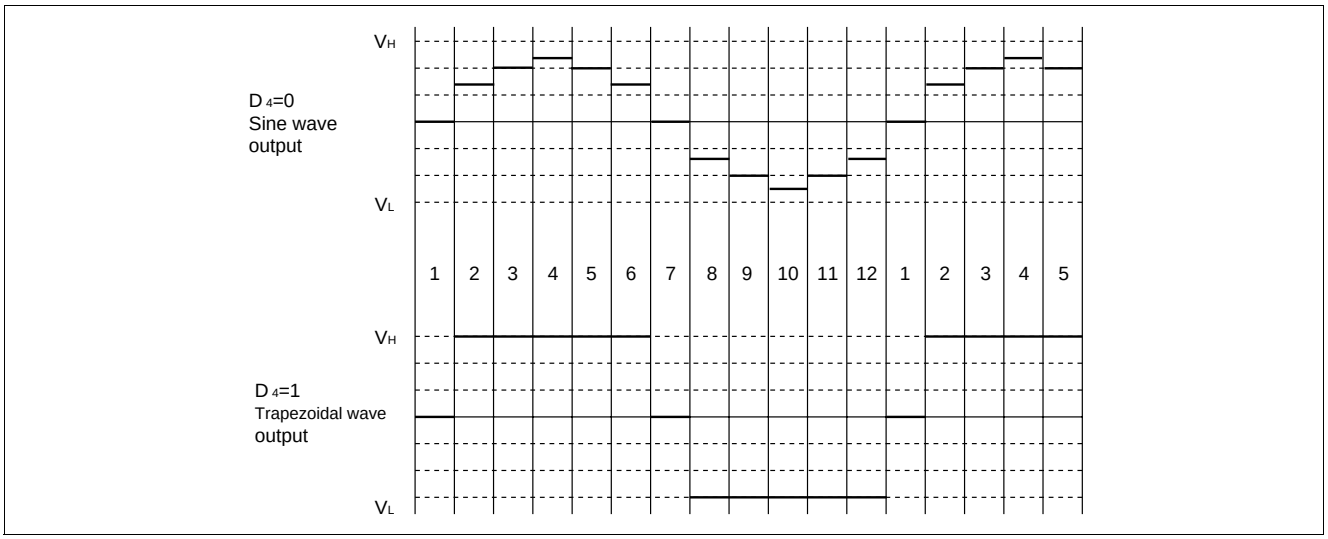
(Condition: 512 kHz)

Tone type		Rated reference frequency (generator frequency)	Frequency setting	Address 1010/1100 Data bit					Address 1011/1101 Data bit					n	Error
				D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0		
Service tone (single tone)		262 Hz	261.7 Hz	—	1	0	1	0	*	0	0	1	0	162	–0.11%
		384 Hz	384.4 Hz	—	0	1	1	0	*	1	1	1	0	110	0.10%
		400 Hz	398.7 Hz	—	0	1	1	0	*	1	0	1	0	106	–0.32%
		2000 Hz	2031.7 Hz	—	0	0	0	1	*	0	1	0	0	20	1.56%
		2600 Hz	2666.7 Hz	—	0	0	0	0	*	1	1	1	1	15	2.50%
DTMF	Low tone	697 Hz	699.4 Hz	—	0	0	1	1	*	1	1	0	0	60	0.34%
		770 Hz	775.7 Hz	—	0	0	1	1	*	0	1	1	0	54	0.74%
		852 Hz	853.3 Hz	—	0	0	1	1	*	0	0	0	1	49	0.15%
		941 Hz	948.1 Hz	—	0	0	1	0	*	1	1	0	0	44	0.75%
	High tone	1209 Hz	1219.0 Hz	—	0	0	1	0	*	0	0	1	0	34	0.82%
		1336 Hz	1333.3 Hz	—	0	0	0	1	*	1	1	1	1	31	–0.20%
		1477 Hz	1471.3 Hz	—	0	0	0	1	*	1	1	0	0	28	–0.38%
		1633 Hz	1641.0 Hz	—	0	0	0	1	*	1	0	0	1	25	0.48%

Note: • Setting values are BIN display values
• Error represents frequency setting error with respect to rated reference frequency.

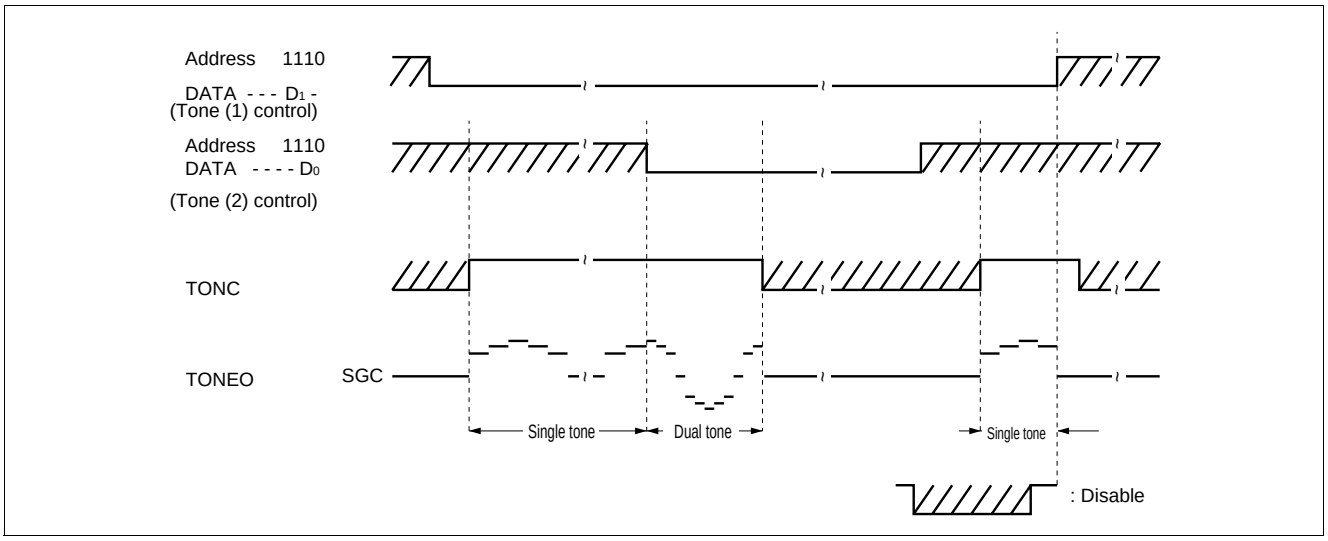
- **Tone Output Waveform**

The D4 data bit at address 1010, 1100 may be used to select either sine-wave or trapezoidal waveforms for tone output.



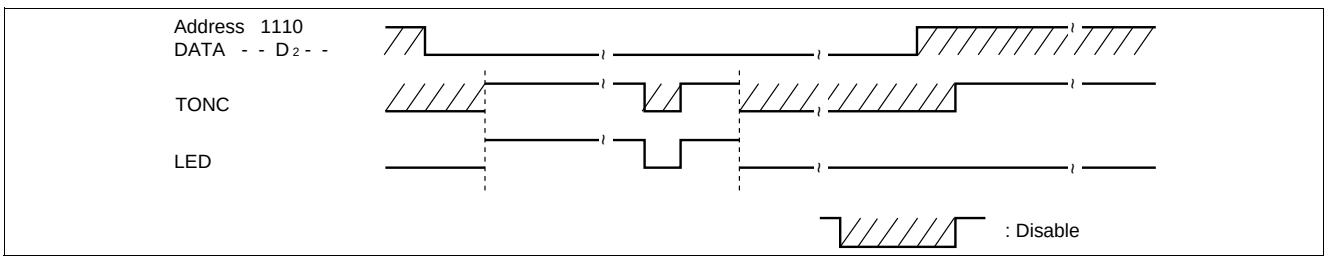
- **Tone Output Control**

Tone output may be controlled by address and through the external tone control input pin TONC. In addition, the tone control offers a choice of sine or trapezoidal waveforms.



- **LED Output Controls**

Output from the LED output pins can be controlled by the TONC signal and the address 1110 data bit D_2. When the TONC signal is H-level, and the address 1110 data bit D_2 value is L-level, the output level will be high. Output levels are CMOS levels.



- **Tone Generator Control Output Level**

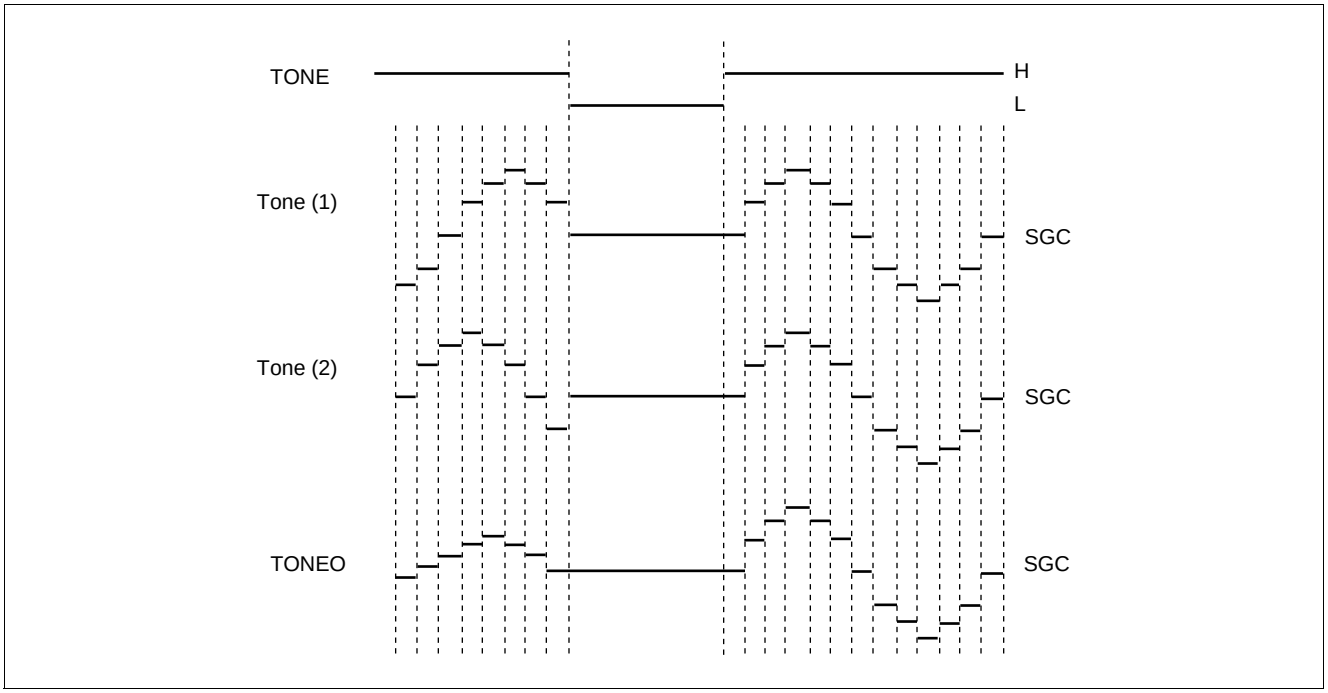
(Condition: EV3 = 0 dB)

External pins				Address 1110 data bits			Address 0111 data bits	Tone generator circuit operating mode		Output pin mode		Remarks
PSC2	PSC1	PSC0	TONC	D_2	D_1	D_0	D_3 (SW2)	Tone (1)	Tone (2)	LED	TONEO	
0	0	0	—	—	—	—	—	×	×	L	H-Z	
1	0	0	—	—	—	—	—	×	×	L	H-Z	
—	1 or 1		0	—	—	—	0	SGC	SGC	L	SGC	
—	1 or 1		0	—	—	—	1	SGC	SGC	L	H-Z	
—	1 or 1		1	1	—	—	—	—	—	L	—	
—	1 or 1		1	0	—	—	—	—	—	○	—	
—	1 or 1		1	—	1	1	0	SGC	SGC	—	SGC	
—	1 or 1		1	—	1	0	0	SGC	○	—	–14 dBv	Single tone output
—	1 or 1		1	—	0	1	0	○	SGC	—	–14 dBv	Single tone output
—	1 or 1		1	—	0	0	0	○	○	—	–14 dBv	Dual tone output

○ : Operational, × : Power down, H-Z : High-impedance, L: L-level fixed, SGC: SGC fixed

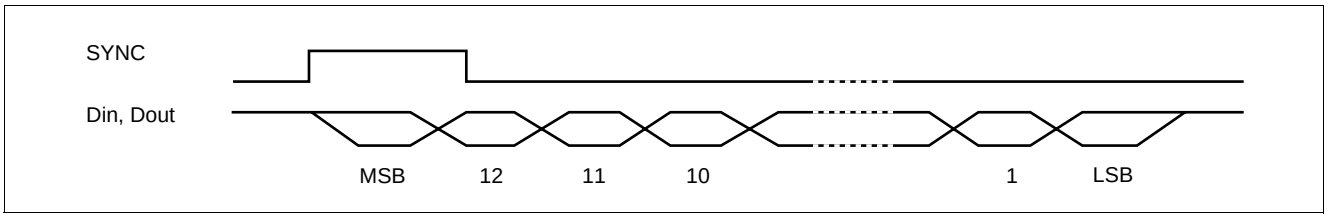
Note: When the TONC pin signal is L-level, the tone generator circuit counters will be reset. When a dual tone is generated at the time of reset, the initial phase settings for tone (1) and tone (2) will be in phase.

- **Example: When Tone (1), Tone (2) are at the same frequency:**



(6) Codec Input/Output

Both the μ-law and A-law coding/decoding conversion processes used by the MB86435 codec are compatible with CCITT Recommendation G.711. In addition, linear coding in the form of 14-bit two's complement code can be output starting with MSB values.



MSB Code LSB	PTBO reference voltage (V)
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0.7354
to	to
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1.4991
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1.5000
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1.5009
to	to
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	2.2647

(7) The Codec SYNC Pin

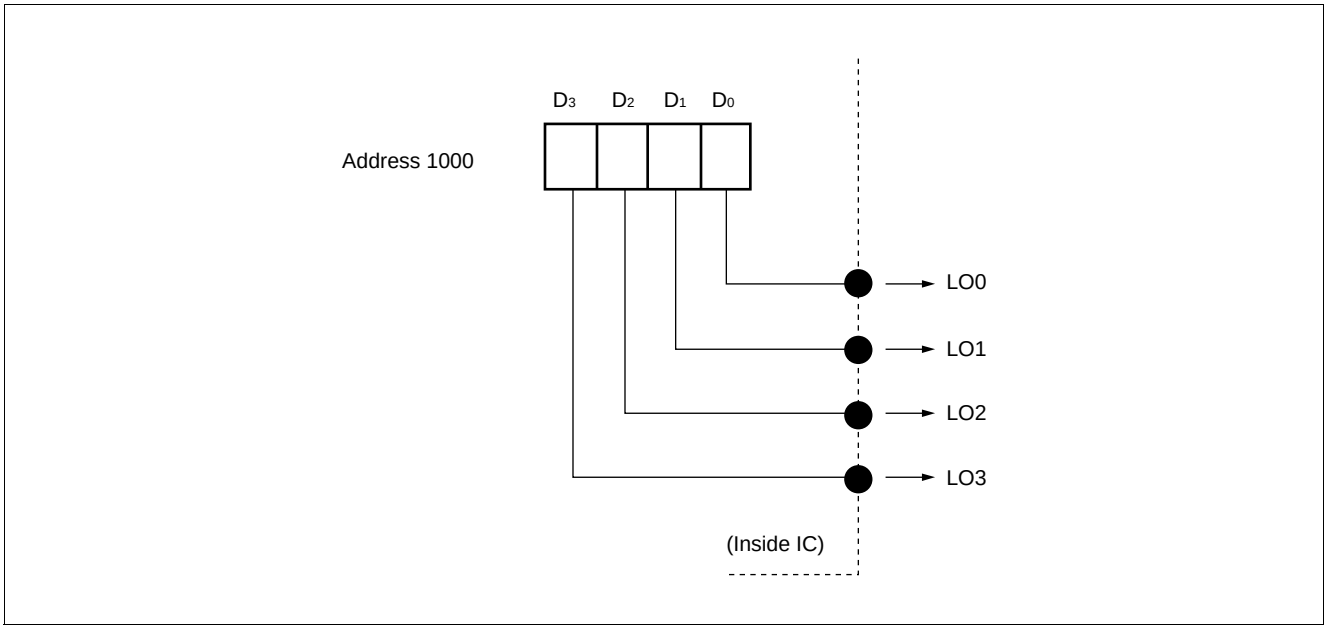
The codec block requires the input of an 8 kHz sampling clock signal at the SYNC pin, as well as a data transfer clock at the CLK pin. In order to conserve power consumption, whenever the SYNC pin or CLK pin signal is inactive, the system goes into SYNC power-down mode and stops code conversion.

Also, if either the SYNC or CLK pins encounters jitter of 5 μs or greater, the system may go into power-down mode.Table 1.10 shows the status of output pins in SYNC power-down mode.

Pin symbol	Operation
SGC	Normal operation (1.5 V)
SGO	Normal operation (1.5 V)
VRH	Normal operation (2.5 V)
DOUT	H-level fixed
PTBO	SGC
BTPO	High impedance

(8) Parallel Output

The LO0 to 3 pins carry latched output for external controls. The data written to address 1000 can be output through these pins. Output is CMOS output.



2. Analog Input

Analog input signals in the MB86435 include the two microphone inputs and the three accessory input.

(1) Microphone Amps

The microphone amps take the incoming signal from the microphones and amplify it to any desired level of gain. The microphone lines are low-noise types for use with piezoelectric-ceramic or capacitor microphones, and are capable of a wide range of amplification. All microphones and amps must be coupled with capacitors to prevent amplification of offset signals.

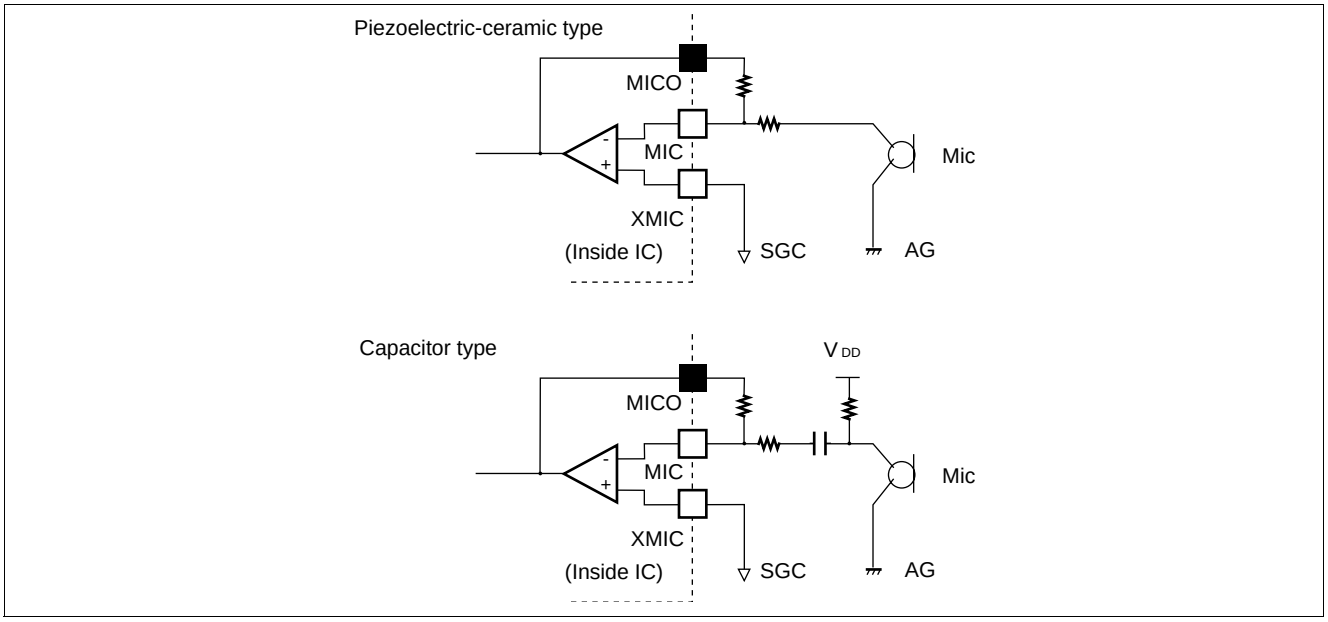


Table 5 Microphone Amp Characteristics

Parameter	Characteristics (typ)
Gain measurement range	0 to 35 dB
Minimum load level	50 kΩ
Maximum output level	0.75 V_{OP}

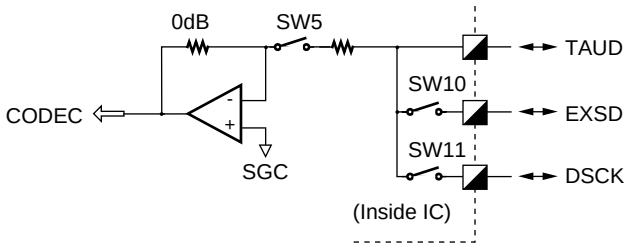
(2) Accessory Input

Direct input from the TAUD to the codec unit is possible through SW5, without passing through the microphone amp. Care must be taken with the input signal in this case, however, because input resistance is not at high-impedance level.

Microphone amp output may be added to the signal by using switching controls.

In this case, the result will be at the additional output level.

In addition, SW10 and SW11 may be used to transmit digital data from the TAUD to EXSD and DSCK, allowing the sending of fax or PC data without modification.



Note: TAUD, EXSD, and DSCK contain no digital buffers. If not used, TAUD, EXSD and DSCK should be connected to SGC.

3. Analog Output

The MB86435 has a total of four analog output circuits, including the three speaker drive circuits (receiver, earphone and tone) and the accessory output.

(1) Speaker Drive Amp

The speaker drive amps include two circuits (receiver and tone) with BTL output and one system (earphone) with single output. Because the speaker amp requires relatively high levels of power, it is connected to speaker selection switches (sw6-sw9) for power-down mode selection.

Two systems (receiver and earphone) have fixed gain levels, while the other system (tone) allows gain adjustment by means of external resistors.

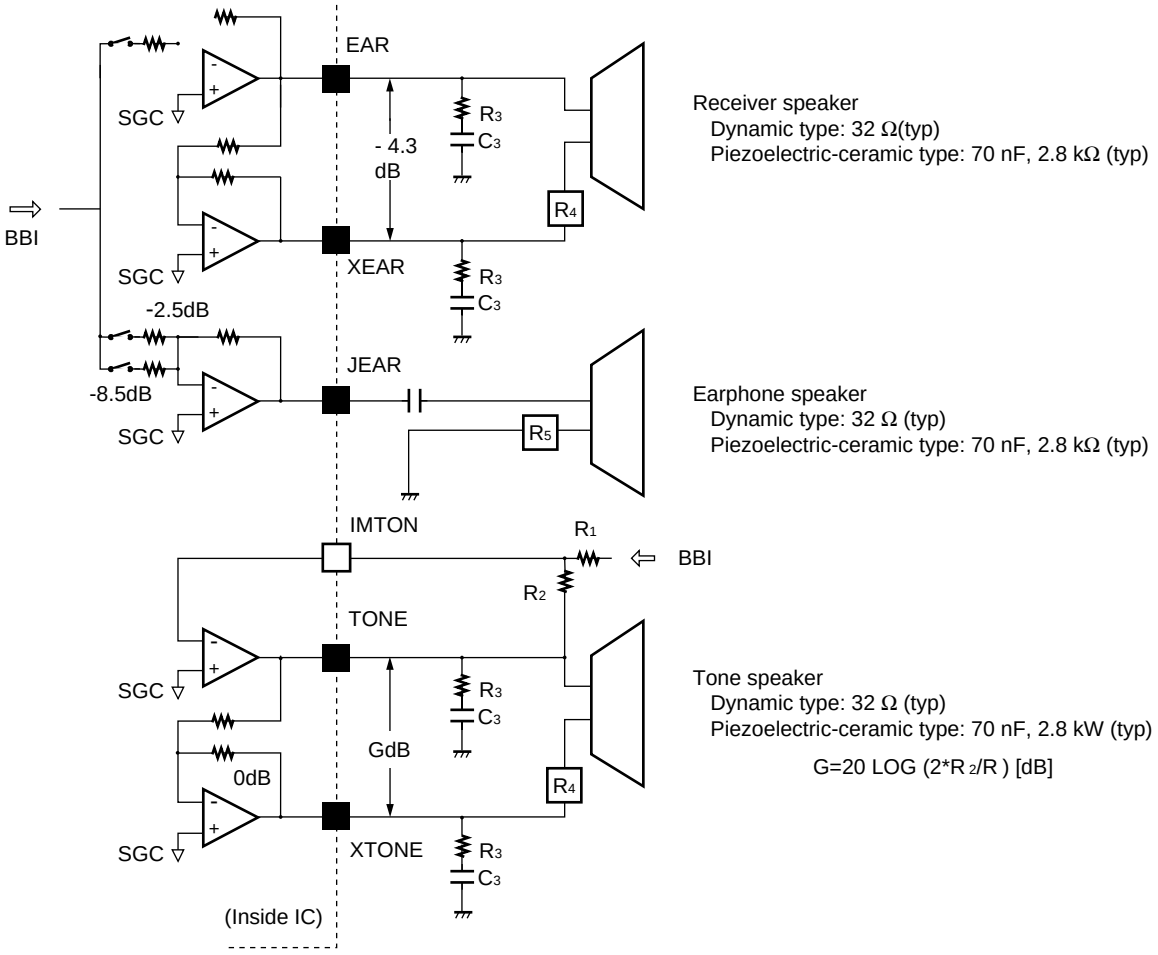
Table 6 Speaker Drive Amp Output Standards

Parameter	Receiver speaker amps (EAR, XEAR)	Earphone speaker amp (JEAR)	Tone speaker amps (TONE, XTONE)
Output type	BTL	Single	BTL
Load resistance *1	32 Ω (typ)	32 Ω (typ)	25 Ω (typ)
Load resistance *2	2.8 kΩ (typ)	2.8 kΩ (typ)	2.8 kW (typ)
Load capacity *2	70 nF	70 nF	70 nF
Final stage gain	–4.3 dB (between EAR-XEAR)	–2.5 dB/–8.5 dB (JEAR)	–5 to 20 dB (between TONE-XTONE)
Maximum output power	6.4 mW (min)	2 mW (min)	10 mW (min)

*1: Dynamic-type speaker

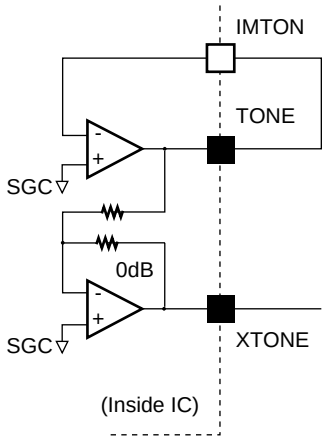
*2: Piezoelectric-ceramic type speaker

- **Analog Output Connection Example**



Note: • R_3, C_3 should be given the respective values 80Ω, 0.01 µF in order to prevent unwanted oscillation.
• If a piezoelectric-ceramic type microphone is used, R_4, R_5 should be given the respective values 20Ω, 10Ω in order to prevent unwanted oscillation.

- **Tone Speaker Amp Not Used**



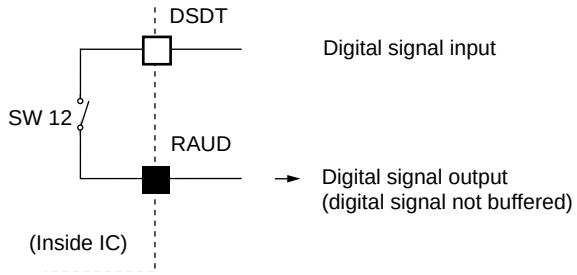
Note: When no tone speaker amp is used, the amp input IMTON and output TONE should be shorted together.

(2) Accessory Output

The accessory output (RAUD pin) can carry either digital or analog output signals, and is controlled by address 0101 data bit D_4 (SW 8), and address 0111 data bit D_1 (SW 12).

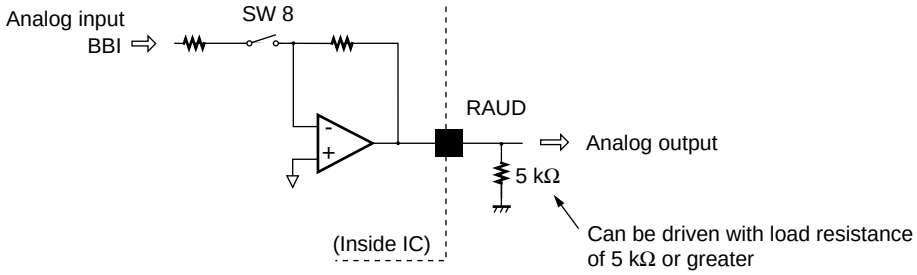
When both SW 8 and SW 12 are in off position, the accessory outputline is in H-Z (high impedance) state. Caution: never place both SW 8 and SW 12 in on position at the same time. This may cause the MB86435 to function improperly.

- **SW12 in On Position**



Address				Data bit				
A_4	A_3	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	1	1	—	—	—	1	—

- **SW8 in On Position**

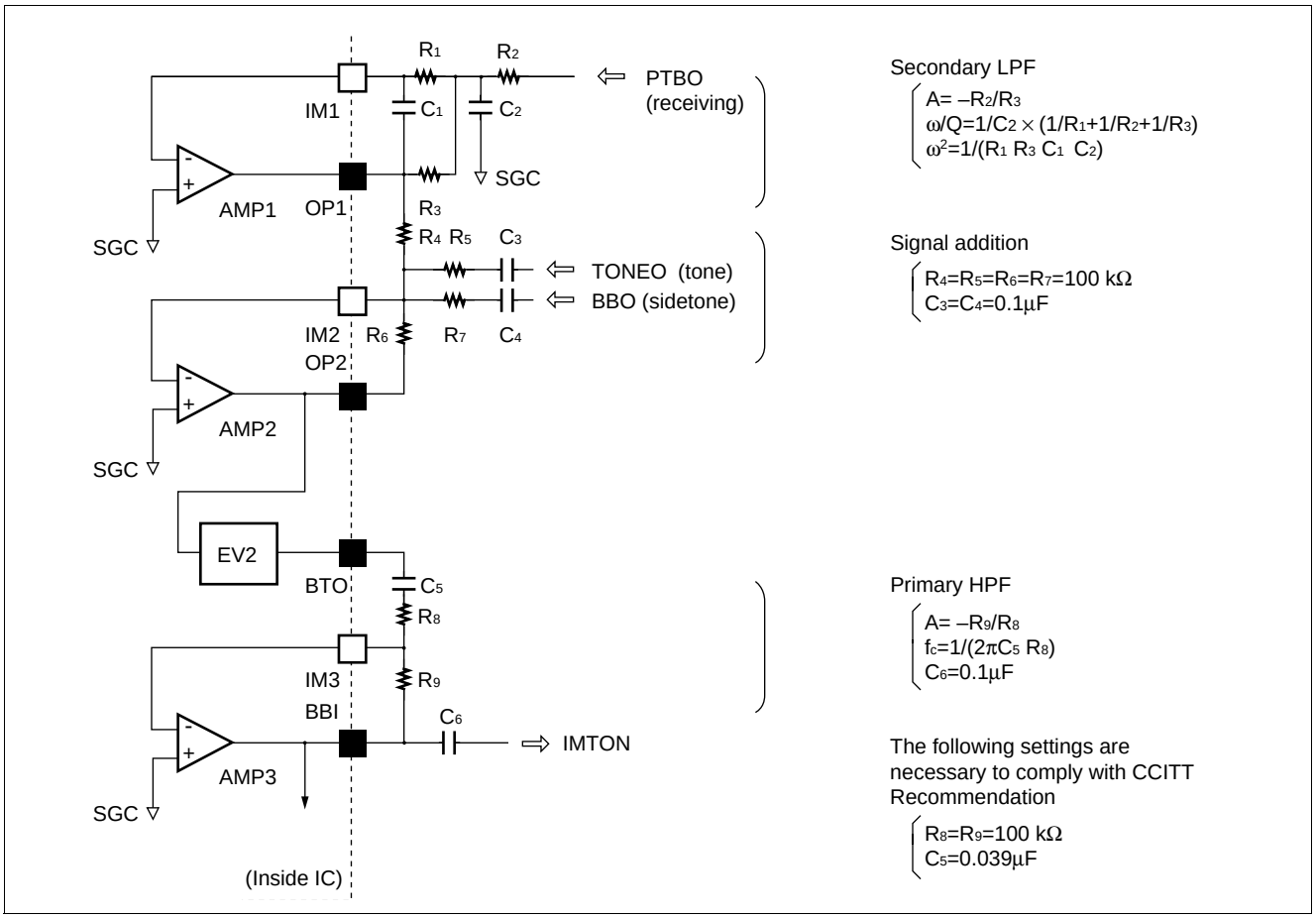


Address				Data bit				
A_4	A_3	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	*	*	*	—
0	1	0	1	0	*	—	—	—

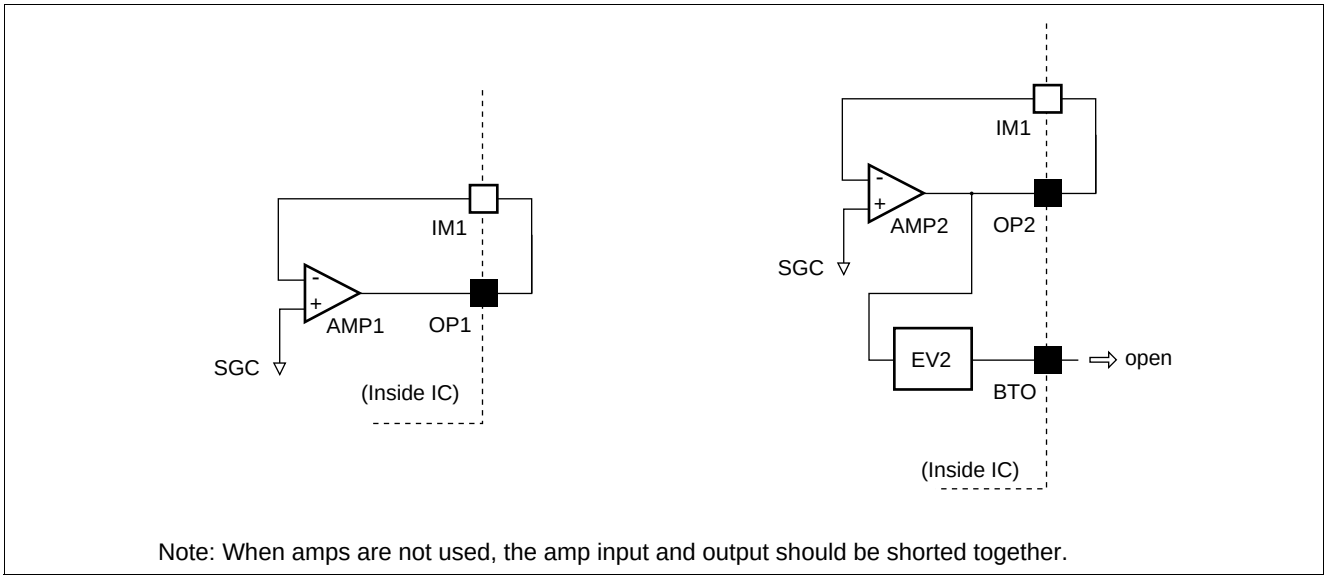
4. Receiver Connections

It is possible to add tones and adjust sidetones by using amp 1,2 and 3 and the electronic volume control. When using amp 3, however, it is necessary to include HPF to avoid interference from the speaker amp DC.

- **Tone and Sidetone Addition by Inclusion of Secondary LPF and Primary HPF.**

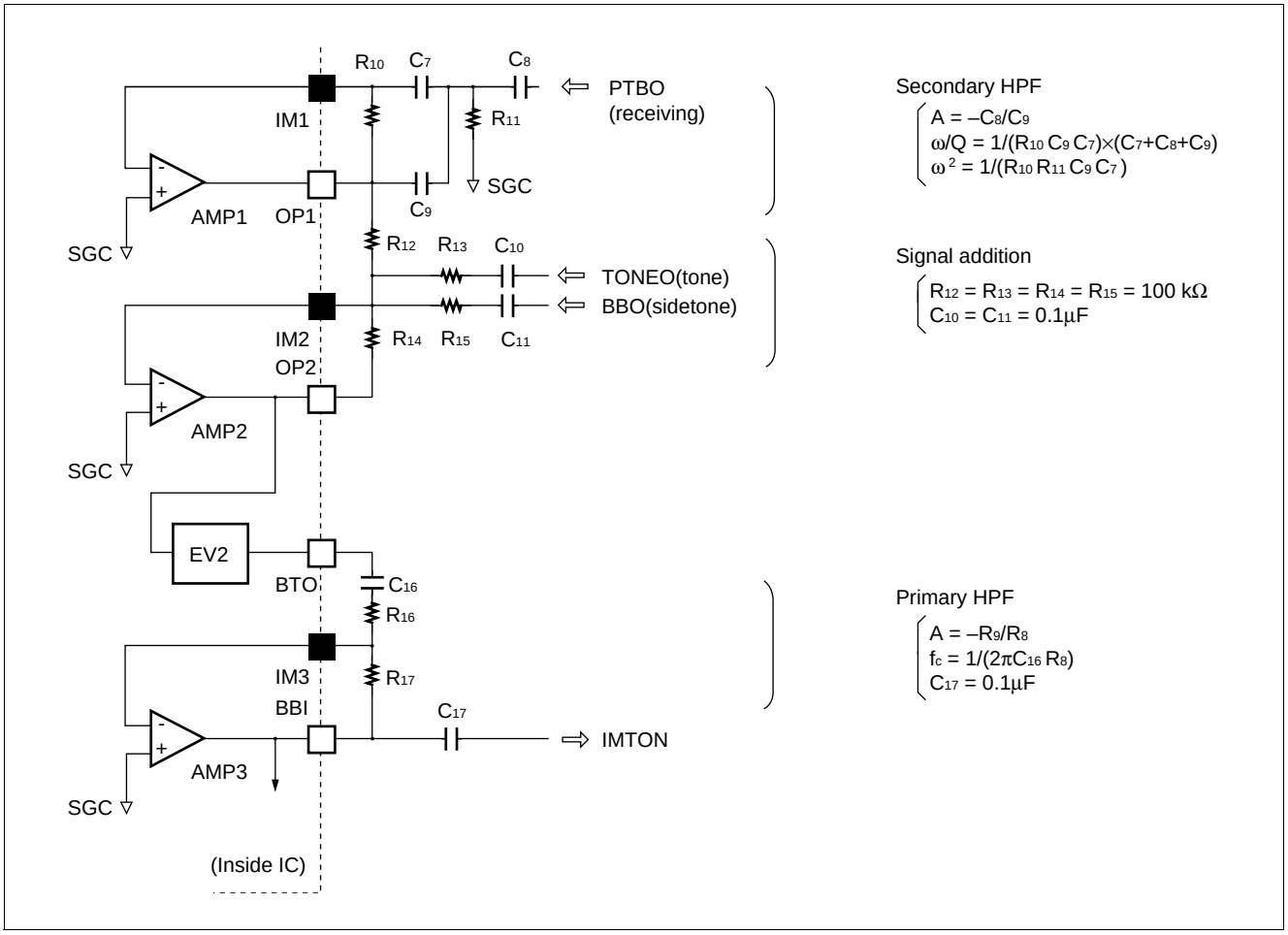


- **Amp1, Amp2 not used**



Note: When amps are not used, the amp input and output should be shorted together.

- **Tone and Sidetone Addition by Inclusion of Third-Order HPF**



5. Power Saving Modes

(1) Mode Selection

The MB86435 power saving modes can be controlled by using the external control signal lines (3 lines). It is also possible to apply power saving modes to the speaker amps with high power consumption levels by writing changes to register settings. Whenever the MB86435 changes directly from a power-down mode to normal operating mode, there is a possibility that speaker tones may be produced. The recommended sequence of coding changes to go into normal mode is (VREF mode) → (Tone mode) → (Normal mode).

Power Saving Modes

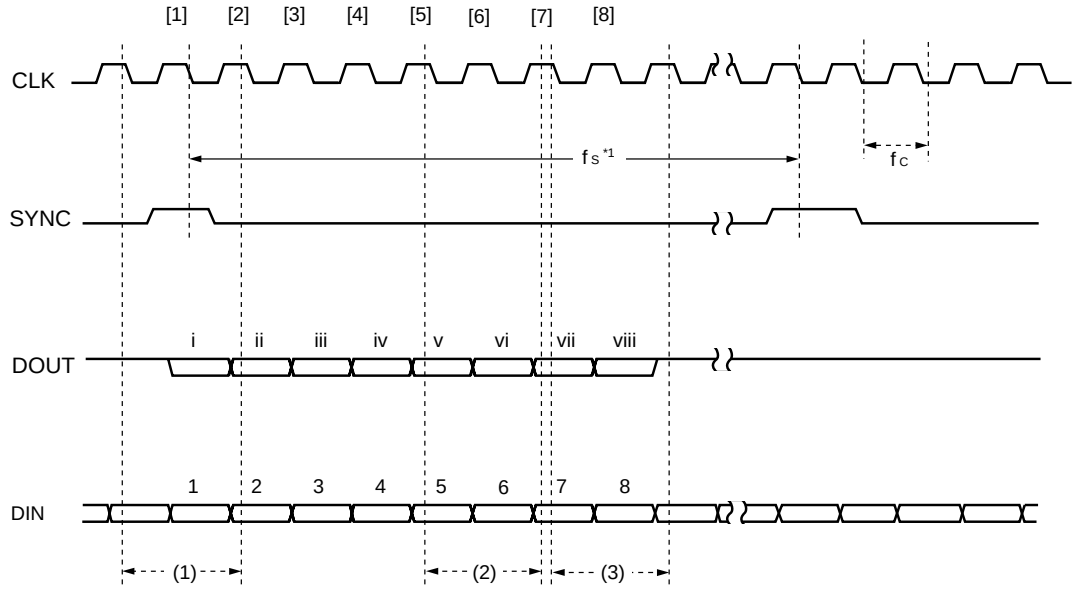
Mode	External pins			Address		Address	Address 0110			Output pin status												Operating circuit status									Power supply current (mA) (typ)
	PSC2	PSC1	PSC0	D4	D0	D	D	D	D	EAR XEAR	JEAR	TONE XTONE	RAUD	DOUT	SGC SGO	OP2 BTO	PTBO BTPO	OP1	MICO JMICO	BBO VRH	BBI	CODEC	VREF generator	TONE generator	Sending	Receiving	Receiving	Earphone	Tone	Accessory	
						SW8	SW7	SW9	SW6	SW6	SW7	SW9	SW8														SW6	SW7	SW9	SW8	
All Power-down	0	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	H-Z	ZC	H-Z	H-Z	H-Z	*	×	×	×	×	×	×	×	×	×	×	0.0005
VREF	1	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	ZC	H-Z	H-Z	H-Z	*	×	○	×	×	×	×	×	×	×	×	0.41
Tone	—	1	0	1	1	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	×	1.8
	—	1	0	0	1	0	1	1	1	ZA	H-Z	ZB	○	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	○	2.4
	—	1	0	0	1	1	0	1	1	ZA	○	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	○	×	×	4.4
	—	1	0	0	1	1	1	0	1	ZA	H-Z	○	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	○	×	6.6
	—	1	0	0	1	1	1	1	0	○	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	○	×	×	×	6.6
Normal	—	—	1	0	0	0	1	1	1	ZA	H-Z	ZB	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	○	6.0
	—	—	1	0	0	1	0	1	1	ZA	○	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	○	×	×	8.0
	—	—	1	0	0	1	1	0	1	ZA	H-Z	○	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	×	○	×	10.2
	—	—	1	0	0	1	1	1	0	○	H-Z	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	10.2
	—	—	1	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	18.2

Note: • ○ : Operational, ×: Power-down, H-Z: High impedance, H: H-level fixed
* : High impedance may not be applied, depending on status of SW6, SW7, SW8.
ZA : EAR and XEAR are floating, however high resistance connection between EAR and XEAR.
ZB : TONE and XTONE are floating, however, high resistance connection between TONE and XTONE, and between SGO and XTONE.
ZC : Floating, however high resistance connection between OP2 and BTO. Codec in [Normal] mode operates with SYNC = 8 kHz, CLK = 2048 kHz.

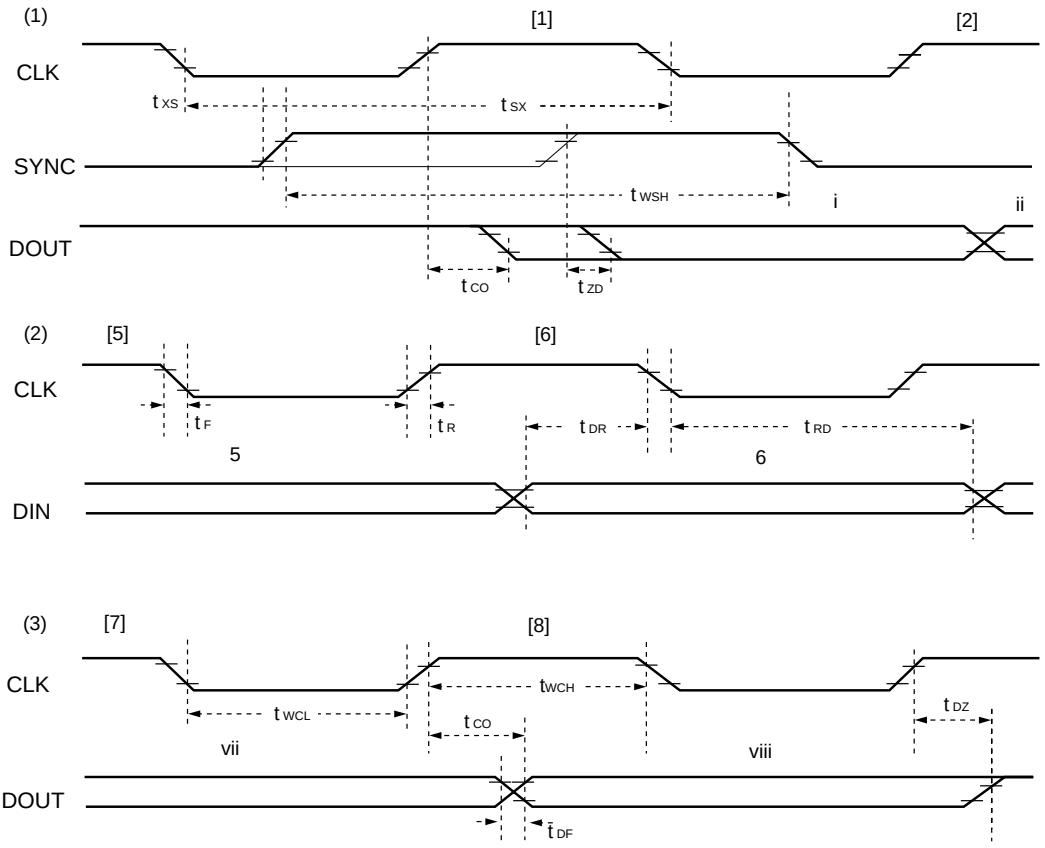
- When RAUD is operating, address 0111 data bit D1 value should be “0” (SW12 off).
- In tone mode, address 0111 data bit D3 should be “0” (SW2 on), and address 0111 data bit D4 should be “0” (SW14 off).
- When the SYNC and CLK pin signals are fixed at either L-level or H-level, part of the codec unit will go into power-down mode. At this time the PTBO signal will be SGC level, BTPO will be H-Z, and VRH output will be approximately 4.0 V.

■ TIMING CHART

• Codec-Related Signals

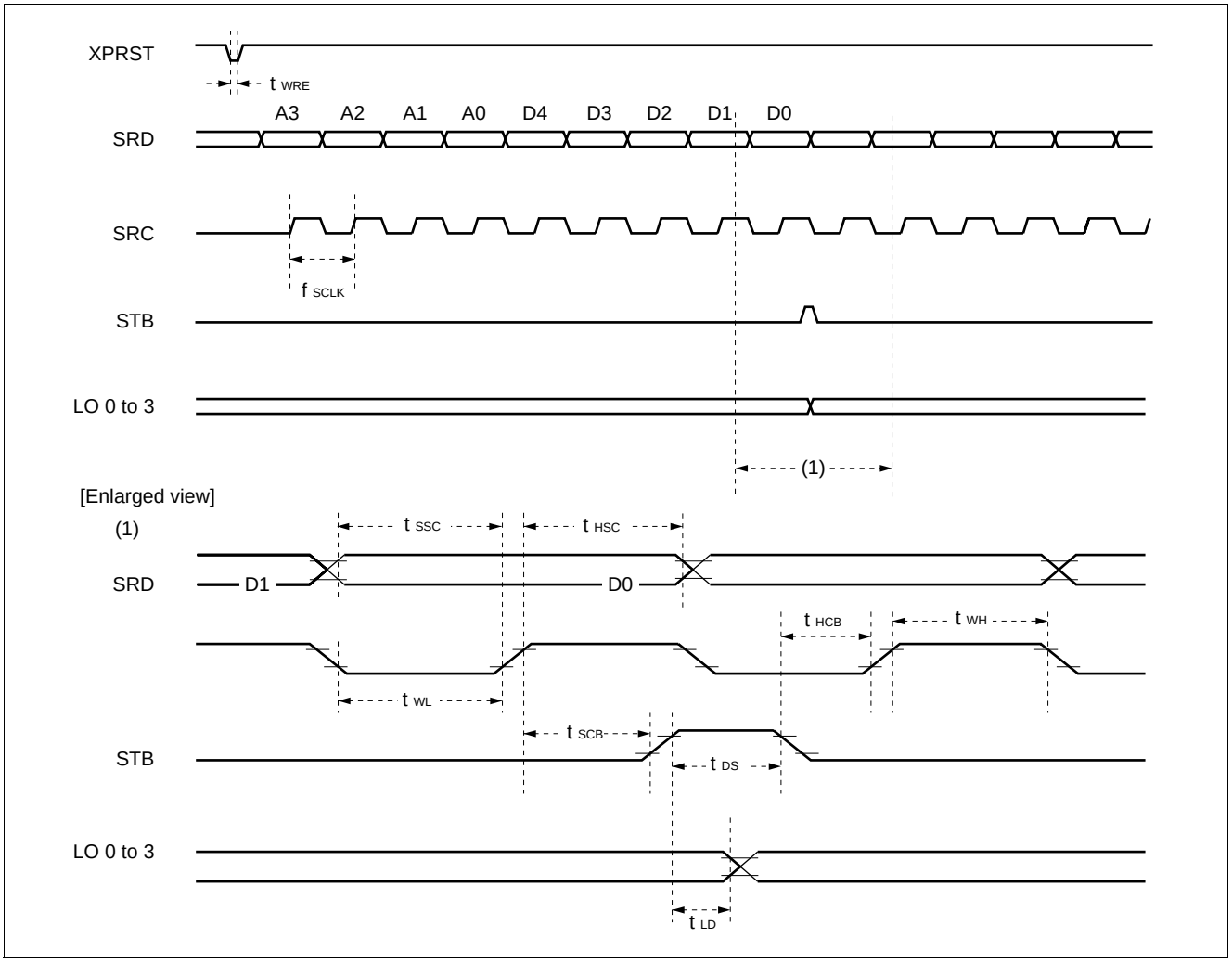


[Enlarged view]



*1 From first CLK Down to second CLK Down, SYNC = H.

• Microcomputer Data-Related Signals



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_S	–0.3	7.0	V
Analog input voltage	V_{AIN}	–0.3	$+V_S$ + 0.3	V
Digital input voltage	V_{DIN}	–0.3	$+V_S$ + 0.3	V
Storage temperature	Vstg	–55	+125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Operating temperature	Ta	—	–20	+25	+80	°C
Power supply voltage	V_S	VDD, VDDAB, VDDAC, VDDSP1 , VDDSP2	2.7	3.0	3.6	V
Digital input voltage	V_L	All digital input pins	0.0	—	V_S	V
Analog output load resistance	R_{LB}	BBO, PTBO, TONEO, BTO, BTPO	75	—	—	kΩ
Analog output load capacity	C_{LB}		—	—	20	pF
Analog output load resistance*1	R_{LE}	Between EAR-XEAR	—	32	—	Ω
Analog output load capacity*2	C_{LE}		—	—	70	nF
Analog output load resistance*1	R_{LJ}	JEAR	—	32	—	Ω
Analog output load capacity*2	C_{LJ}		—	—	70	nF
Analog output load resistance*1	R_{LT}	Between TONE-XTONE	—	25	—	Ω
Analog output load capacity*2	C_{LT}		—	—	70	nF
Analog output load resistance	R_{LM}	MICO, JMICO, SGO, BBI, OP1, OP2	50	—	—	kΩ
Analog output load capacity	C_{LM}		—	—	20	pF
Analog output load resistance*3	R_{LM}	RAUD	5	—	—	kΩ
Analog output load capacity*3	C_{LM}		—	—	20	pF
Analog output voltage	V_{AOUT}	All analog output pins	0.45	—	V_{DD}–0.45	V
Analog input voltage	V_{AIN}	All analog input pins	1.2	—	1.8	V

*1: Dynamic typ speakers
*2: Piezoelectric type speakers
*3: When SW8 = on, SW12 = off

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Pin	Conditions	Value			Unit
					Min.	Typ.	Max.	
Power supply current at full power-down mode		I_{VSST1}	All V_{DD} pins	PSC0 = 0 : PSC1 = 0 : PSC2 = 0, Ain = AG, Din = L	—	0.5	50	µA
Power supply current with VREF operating		I_{VSST2}		PSC0 = 0 : PSC1 = 0 : PSC2 = 1, Ain = SGC, Din = L	—	410	800	µA
Power supply current with TONE operating		I_{VSST3}		PSC0 = 0 : PSC1 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW8 = SW9 = off	—	1.8	3.0	mA
Power supply current for normal operation (only speaker ampmute)		I_{VSST4}		PSC0 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW9 = off	—	6.0	8.5	mA
Speaker amp power supply voltage	Receiver amps EAR, XEAR	I_{VSST5}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW6 is on/off.	—	4.8	7.0	mA
	Earphone amp JEAR	I_{VSST6}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW7 is on/off.	—	2.6	4.0	mA
	Tone amps TONE, XTONE	I_{VSST8}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW9 is on/off.	—	4.8	7.0	mA
Digital input voltage		V_{IH}	All digital input pins	—	$V_S \times 0.7$	—	V_S	V
		V_{IL}		—	0	—	$V_S \times 0.3$	V
Digital input current		I_{IH}		—	—	—	10	µA
		I_{IL}		—	—	—	10	µA
Input offset voltage		V_{FM}	Between MIC-XMIC, between JMIC-XJMIC	—	–10	—	10	mA

(Continued)

(Continued)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Output offset voltage	V_{FR}	RAUD	BBI = SGC SW8 = on, SW6 = SW7 = SW9 = SW12 = off	–15	—	15	mV
	V_{FE}	Between EAR-XEAR	BBI = SGC SW6 = on, SW7 = SW8 = SW9 = SW12 = off	–20	—	20	mV
	V_{FT}	Between TONE-XTONE	IMTON = SGC SW9 = on, SW6 = SW7 = SW8 = SW12 = off	–20	—	20	mV
	V_{FP}	PTBO	Din = ICN, EV2 = 0 dB	–100	—	100	mV
	V_{OH}	Between MIC0-BBO	EV0 = 0 dB	–100	—	100	mV
	V_{OL}	Between JMIC0-BBO					
SGC output voltage	V_{SGC}	SGC	—	1.40	1.50	1.60	V
SGO output voltage	V_{SGO}	SGO	—	1.40	1.50	1.60	V
VRH output voltage	I_{VRH}	VRH	—	—	2.5	—	V
Digital output voltage	V_{OH}	All digital output pins	I_{OH} = – 0.5 mA	$V_S \times 0.8$	—	V_S	V
Digital output voltage	V_{OL}	All digital output pins	I_{OL} = 0.5 mA	0.0	—	$V_S \times 0.2$	V
Resistance between pins TAUD and DSCK	R_{DR}	Between DSTD-RAUD	SW12 = on, SW8 = off	—	—	2	kΩ
Resistance between pins TAUD and EXSD	R_{TE}	Between TAUD-EXSD	SW10 = on, SW11 = off	—	—	2	kΩ
Resistance between pins DSTD and RAUD	R_{DE}	Between TAUD-DSCK	SW11 = on, SW10 = off	—	—	2	kΩ

Note: Measurement conditions: ■ Standard Test Circuit

2. AC Characteristics

(1) Codec-Related Signals

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Digital input rise time	t_R	$V_S \times 0.3 \rightarrow V_S \times 0.7$	—	—	50	ns
Digital input fall time	t_F		—	—	50	ns
Shift clock frequency	f_C	μ-law , A-law	64	—	3152	kHz
		Linear	256	—	3152	kHz
Shift clock pulse width (H)	t_{WCH}	$V_{IH} = V_S \times 0.7$	$1/f_C \times 0.3$	—	$1/f_C \times 0.7$	ns
Shift clock pulse width (L)	t_{WCL}	$V_{IL} = V_S \times 0.3$	$1/f_C \times 0.3$	—	$1/f_C \times 0.3$	ns
Sync frequency	f_S	—	—	8	—	kHz
Sync pulse width	t_{WSH}	—	$1/f_C$	—	62	μs
SYNC to CLK setup time	t_{SX}	—	100	—	—	ns
CLK to SYNC hold time	t_{XS}	—	50	—	—	ns
CLK to DIN hold time	t_{RD}	—	50	—	—	ns
DIN to CLK setup time	t_{DR}	—	50	—	—	ns
SYNC to DOUT delay time	t_{ZD}	BIT 1	—	—	200	ns
CLK to DOUT delay time	t_{CO}	BIT 2 to 8	—	—	200	ns
CLK to DOUT disable time	t_{DZ}	“H”	—	—	200	ns
DOUT fall time	t_{DF}	—	10	—	100	ns

(2) Microcomputer Data-Related Signals

Parameter	Symbol	Pin	Value			Unit
			Min.	Typ.	Max.	
SRC to SRD data setup time	t_{SSC}	SRD, SRC	50	—	—	ns
SRC to SRD data hold time	t_{HSC}		50	—	—	ns
SRC to STB setup time	t_{SCB}	SRC, STB	50	—	—	ns
SRC pulse width (H)	t_{WH}	SRC	200	—	—	ns
SRC pulse width (L)	t_{WL}		200	—	—	ns
STB pulse width	t_{DS}	STB	50	—	—	ns
STB to SRC hold time	t_{HCB}	STB, SRC	50	—	—	ns
LO0 to 3 delay time	t_{LD}	LO0 to 3	—	—	200	ns
Shift clock frequency	f_{SCLK}	SRC	—	—	2048	kHz
Reset pulse width	t_{WRE}	XPRST	1	—	—	μs

3. Transmission Characteristics

(1) Microphone Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between MIC0 and BBO)	G_{MB}	MICO = –20 dBv, 1020 Hz SW3 = on, SW4 = SW5 = SW14 = off EV0 = 0 dB	–1.5	—	1.5	dB
Gain (between JMIC0 and BBO)	G_{JB}	JMICO = –20 dBv, 1020 Hz SW4 = on, SW3 = SW5 = SW14 = off EV0 = 0 dB	–1.5	—	1.5	dB
Signal to noise ratio (between MIC and BBO) (between XMIC and BBO)	S_{MB}	Ain1 = –40 dBv (+20 dBgain) SW3 = on, SW4 = SW5 = SW14 = off EV0 = 0 dB, 1020 Hz C message	40	—	—	dB
Signal to noise ratio (between JMIC and BBO) (between XJMIC and BBO)	S_{JB}	Ain2 = –40 dBv (+20 dBgain) SW4 = on, SW3 = SW5 = SW14 = off EV0 = 0 dB, 1020 Hz C message	40	—	—	dB

Note: Measurement conditions: ■ Standard Test Circuit

(2) Speaker Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between EAR and XEAR)	G_{BE}	BBI = –20 dBv, 1020 Hz	—	–4.3	—	dB
Gain (between BBI and JEAR)	G_{BJ}	BBI = –20 dBv, 1020 Hz, ATT = –2.5 dB	—	–2.5	—	dB
	G_{BJ6}	BBI = –20 dBv, 1020 Hz, ATT = – 8.5 dB	—	–8.5	—	dB
Gain (between BBI and RAUD)	G_{BR}	BBI = –20 dBv, 1020 Hz SW8 = on, SW6 = SW7 = SW12 = off	—	0.0	—	dB
Output power	W_E	R = 32 Ω, between EAR-XEAR THD = 10%	6.4	—	—	mW
	W_T	R = 25 Ω, between TONE-XTONE gain = 0 dB, THD = 10%	10.0	—	—	mW
	W_J	R = 32 Ω, JEAR, ATT = –2.5 dB THD = 10%	2.0	—	—	mW

Note: Measurement conditions: ■ Standard Test Circuit

(3) TONE System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
TONE output level (TONE0)	G_{T1}	1 tone generated, SW2 = on f_1 = 948.1 kHz	—	–14.0	—	dBv
	G_{T2}	2 tone generated, SW2 = on f_1 = 948.1 kHz, f_2 = 1219.1 kHz	—	–14.0	—	dBv

Note: Measurement conditions: ■ Standard Test Circuit

(4) Electric Volume System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Volume gain error EV0 (between TAUD-BBO)	G_{E0}	SW5 = on, SW3 = SW4 = SW14 = off TAUD = –20 dBv, 1020 Hz	–0.7	—	0.7	dB
Volume gain error EV1 (between DIN-PTBO)	G_{E1}	D_{IN} = –20 dBm0, 1020 Hz	–0.8	—	0.8	dB
Volume gain error EV2 (between IM 2-BTO)	S_{E2}	IM2 = –20 dBv, 1020 Hz	–1.0	—	1.0	dB
Volume gain error EV3 (TONEO)	S_{E3}	SW2 = on 1 tone generated f_1 = 948.1 kHz	–0.5	—	0.5	dB

Note: Measurement conditions: ■ Standard test circuit

(5) Sending/Receiving System (Codec, Analog Block)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Crosstalk (send → receive)	CTX	Ain1 = 1020 Hz, – 40 dBv (20 dBgain) D_{IN} = ICN Measured at RAUD pin	—	—	–50	dB
Crosstalk (send → receive)	CTR	D_{IN} = 1020 Hz, 0 dBm0 A_{IN} = SGC Measured at DOUT pin	—	—	–50	dB
Power supply noise reduction ratio	PSRR	0 < f < 50 kHz, V_{DD} + 30 mV_{OP} C message A_{IN} = SGC, D_{IN} = ICN	—	22	—	dB

Note: Measurement conditions: ■ Standard test circuit

(6) Codec

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Gain tracking (A to D) BTPO → DOUT	GTX	1020 Hz, –10 dBm0 Reference value	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4	—	0.4	dB
			–50 to –55 dBm0	–0.8	—	0.8	dB
Gain tracking (D to A) DIN → PTBO	GTR	1020 Hz, –10 dBm0 Reference value EV1 = 0 dB	+3 to –40 dBm0	–0.4	—	0.4	dB
			–40 to –50 dBm0	–0.6	—	0.6	dB
			–50 to –55 dBm0	–1.0	—	1.0	dB
Gain tracking (A to D) (Linear) BTPO → DOUT	GTXL	1020 Hz, AFST–3 dB Reference value	AFST to AFST–43 dB	–0.2	—	0.2	dB
			AFST–43 to AFST–53 dB	–0.4	—	0.4	dB
			AFST–53 to AFST–53 dB	–0.8	—	0.8	dB
Gain tracking (D to A) (Linear) DIN → PTBO	GTRL	1020 Hz, AFST–3 dB Reference value EV1 = 0 dB	AFSR to AFSR–43 dB	–0.4	—	0.4	dB
			AFSR–43 to AFSR–53 dB	–0.6	—	0.6	dB
			AFSR–53 to AFSR–53 dB	–1.0	—	1.0	dB
Sending frequency characteristics (A to D) BTPO → DOUT	FRX	0 dBm0 (Linear : AFST–3 dB) 1020 Hz Reference value	0 to 60 Hz	24.0	—	—	dB
			60 to 300 Hz	–0.20	—	—	dB
			300 to 3000 Hz	–0.20	—	0.20	dB
			3000 to 3400 Hz	–0.20	—	0.8	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Receiving frequency characteristics (D to A) DIN → PTBO	FRR	0 dBm0 (Linear : AFSR–3 dB) 1020 Hz Reference value EV1 = 0 dB	0 to 300 Hz	–0.30	—	—	dB
			300 to 3000 Hz	–0.30	—	0.30	dB
			3000 to 3400 Hz	–0.30	—	1.10	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Sending absolute gain (A to D) BTPO → DOUT	GAX	1020 Hz, 0 dBm0 (Linear : AFST–3 dB) EV1 = 0 dB, V_S = 3.0 V, Ta = +25°C		–1.0	0	–1.0	dB
		Power supply variation		—	±0.02	—	dB
		Temperature variation		—	±0.001	—	dB/°C
Receiving absolute gain (D to A) DIN → PTBO	GAR	1020 Hz, 0 dBm0 (Linear : AFSR–3 dB) V_S = 3.0 V, Ta = +25°C		–1.20	0	1.20	dB
		Power supply variation		—	±0.04	—	dB
		Temperature variation		—	±0.002	—	dB/°C
Absolute level	VABS	Over load level μ-Law = 3.17 dB A-Law = 3.14 dB		—	0.7647	—	V_{OP}

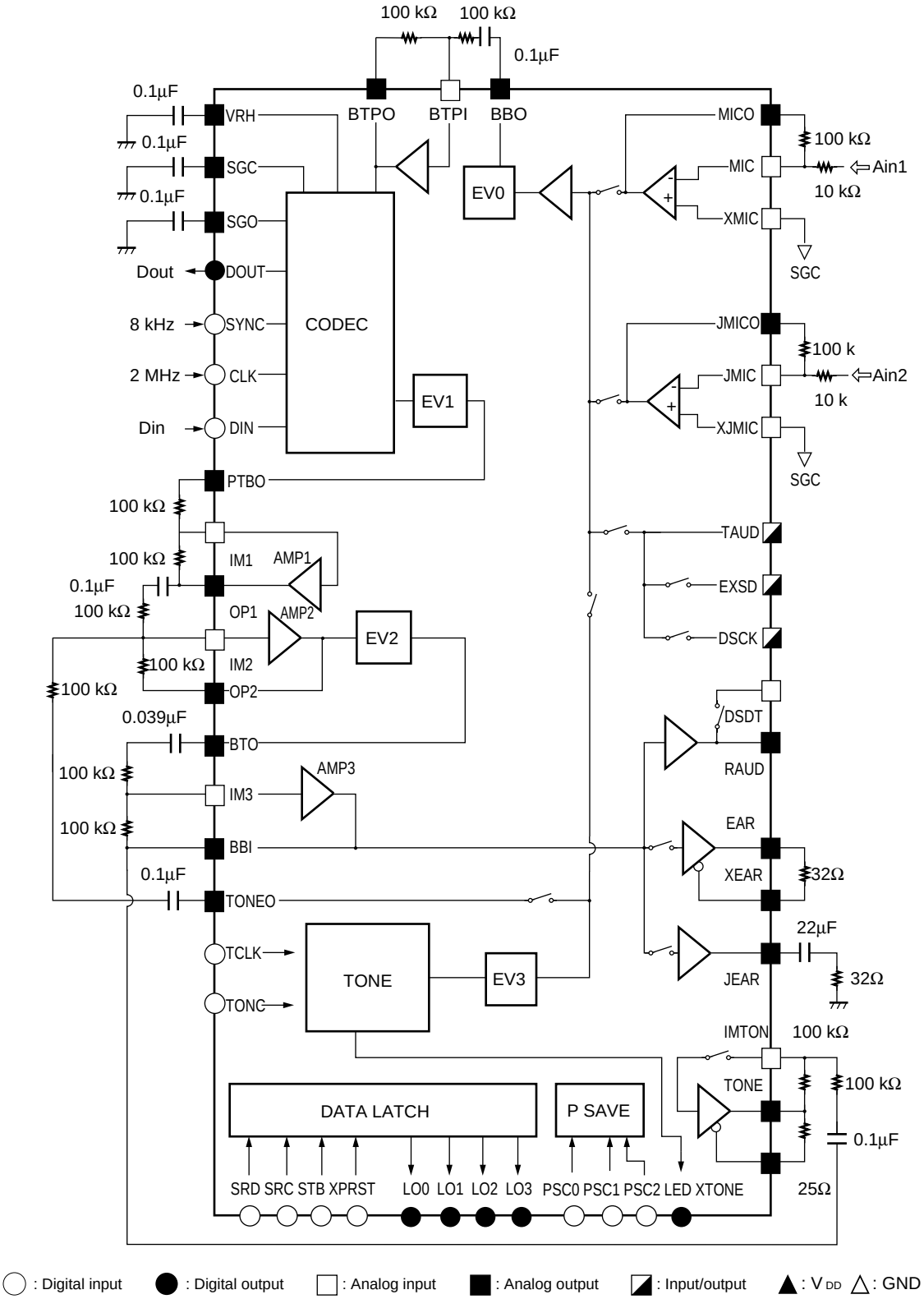
(Continued)

(Continued)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Sending signal to noise ratio BTPO → DOUT	SDX	1020 Hz C message (A to D)	0 to –30 dBm0	34.0	—	—	dB
			–40 dBm0	28.0	—	—	dB
			–45 dBm0	23.0	—	—	dB
Receiving signal to noise ratio DIN → DOUT	SDR	1020 Hz C message (D to A)	0 to –30 dBm0	34.0	—	—	dB
			–40 dBm0	28.0	—	—	dB
			–45 dBm0	23.0	—	—	dB
Sending signal to noise ratio BTPO → DOUT (Linear)	SDXL	1020 Hz C message (A to D)	AFST–3 to AFST–33 dB	34.0	—	—	dB
			AFST–43 dB	28.0	—	—	dB
			AFST–45 dB	23.0	—	—	dB
Recieving signal to noise ratio BTPO → DOUT (Linear)	SDRL	1020 Hz C message (D to A)	AFSR–3 to AFSR–33 dB	34.0	—	—	dB
			AFSR–43 dB	28.0	—	—	dB
			AFSR–45 dB	23.0	—	—	dB
Sending no-talk noise BTPO → DOUT	ICNX	C message (A to D)		—	–72	–68	dBm0C
Receiving no-talk noise DIN → PTBO	ICNR	C message (D to A)		—	–72	–68	dBm0C
Analog input level BTPO	AILU	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V μ-law		0.3290	0.3739	0.4195	Vrms
Analog output level PTBO	AOLU	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V μ-law		0.3290	0.3739	0.4195	Vrms
Analog input level BTPO	AILA	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V A-law		0.3315	0.3767	0.4227	Vrms
Analog output level PTBO	AOLA	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V A-law		0.3315	0.3767	0.4227	Vrms
Analog input fullscale level BTPO	AFST	V_S = 3.0 V, Ta = +25°C Linear		0.6729	0.7647	0.8581	V_{OP}
Analog output fullscale level PTBO	AFSR	V_S = 3.0 V, Ta = +25°C Linear		0.6729	0.7647	0.8581	V_{OP}
Overall absolute delay (BTPO → PTBO)	PDA	$F_C \geq$ 1544 kHz (DOUT-DIN short)		—	490	550	μs
Single frequency noise (BTPO → PTBO)	SFNA	BTPO = SCG (DOUT-DIN short)	0-4 kHz 4.6-200 kHz	—	—	–70 –50	dBm0 dBm0
Discrimination (BTPO → PTBO)	DISA	BTPO = 0 dBmO, 4.6-200 kHz (DOUT-DIN short)		30	—	—	dB
In-band spurious response (BTPO → PTBO)	IBSA	Second and third harmonic,BTPO = 0 dBmO 700-1100 Hz (DOUT-DIN short)		43	—	—	dB

*: $14.5 \times \{1 - \mathrm{SIN}\ \frac{\pi\ (4000 - f)}{1200}\}$

■ STANDARD TEST CIRCUIT



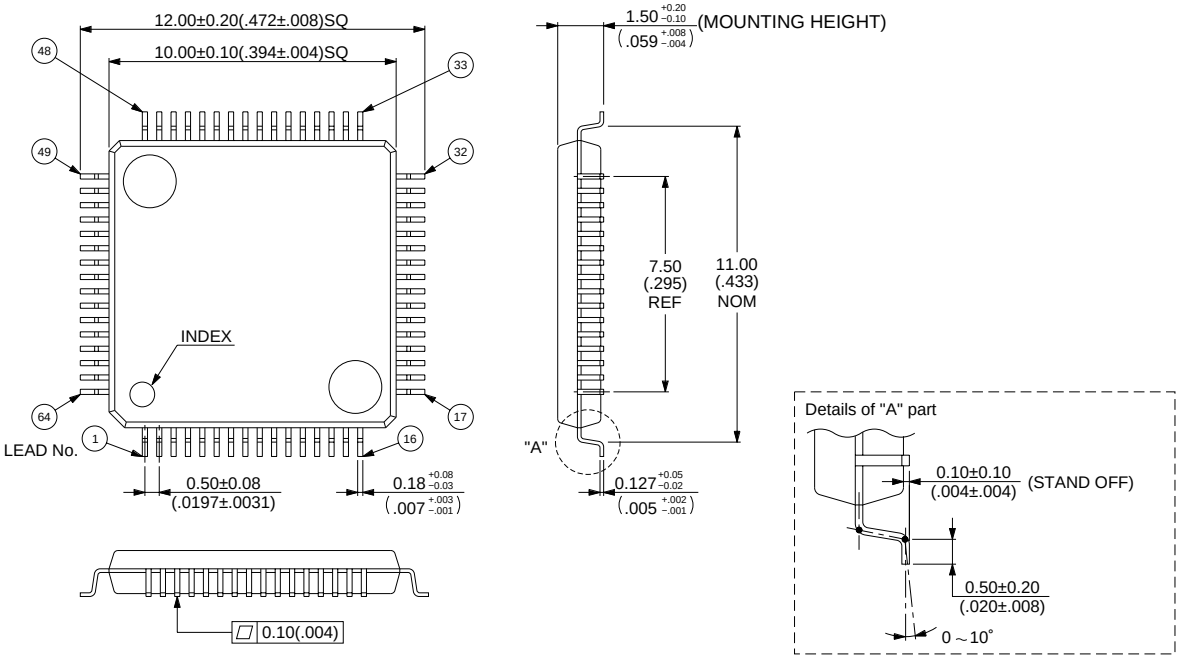
Note: Sufficient path capacitance must be placed between VDDAB–BAG, VDDAC–CAG, VDDSP1–SPG1, VDDSP2–SPG2, VDD–AG.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86435PFV	64 pins, Plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSION

64 pin Plastic LQFP
(FPT-64P-M03)



Dimensions in mm (inches)

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