C9714

100 MHz Clock Generator with SSCG and Power Management for Mobile Application

Approved Product

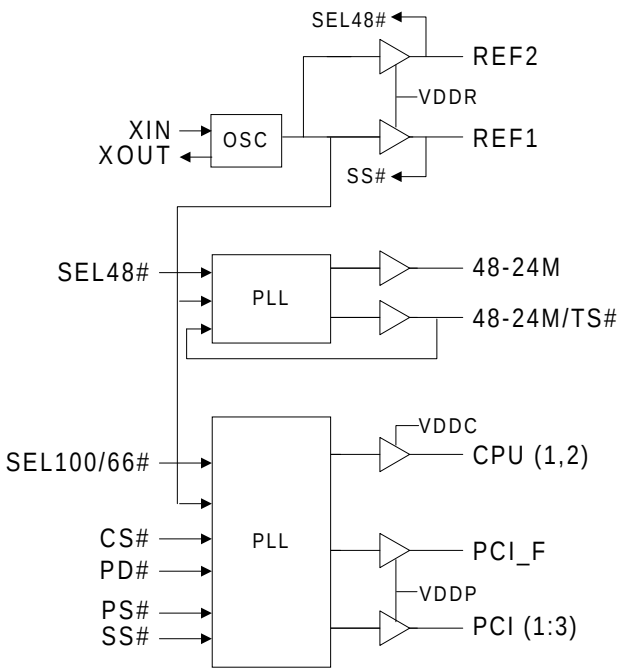
Product Features

- Supplies:
- 2 Ref clocks
  2 Host (CPU) clocks
- 1 free running and 5 PCI Clocks
- 1 48MHz fixed clock
- 1 48 or 24 MHz fixed clock
- Separate supply pins for mixed (3.3/2.5V) voltage application.
- 100 or 66 MHz CPU clock operation
- Spread Spectrum modulation for reducing EMI
- Rich Power Management Functions.
- 28-pin SSOP & TSSOP packages for minimum board space.

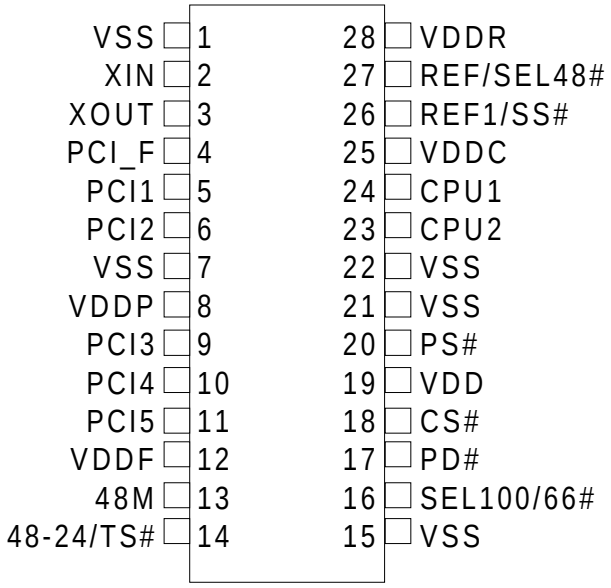
Frequency Table

SEL 100/66#	CPU Clock	PCI Clock
0	66 MHz	33 MHz
1	100 MHz	33 MHz

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
2	**XIN**	VDD	I	XTAL4	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
3	**XOUT**	VDD	O	XTAL4	O-chip reference oscillator output pin. Drives an external parallel resonant crystal (14.318 MHz) when an externally generated reference signal is used.
19	**VDD**	-	P	PWR	3.3 volt power supply for core logic.
23, 24	**CPU (1,2)**	VDDC	O	C100S	Clock outputs. CPU frequency table specified on page 1.
17	**PD#**	-	I	INP3U	Powers down device when LOW
18	**CS#**	-	I	INP3U	When signal is LOW, stops CPU clocks in low state.
16	**SEL100/66#**	-	I	INP3	Frequency select input pins. See frequency select table on page 1. NO INTERNAL PULLUP RESISTOR IS PROVIDED BY DEVICE
25	**VDDC**	-	P	PWR	2.5V power for CPU and Host clock outputs.
4	**PCI_F**	VDDP	O	P100S	Free running PCI clock 3.3V. Does not stop when PS# is at a logic LOW level
5,6,9, 10,11	**PCI(1:5)**	VDDP	O	P100S	PCI output clocks. See frequency table of page 1.
20	**PS#**	-	I	INP3U	When signal is LOW, stops all PCI clocks in low state.
8	**VDDP**	-	P	PWR	3.3 Volt power supply pins for free running PCI clock output buffer.
13	**48M**	VDDF	O	U48	Fixed 48 MHz clock.
14	**48-24M/TS#**	VDDF	I/O	U48BU	Power up selectable 48 or 24 MHz clock. If strapped LOW at powerup causes the devices outputs to be tri-stated until the next power up sequence occurs.
26	**REF1/SS#**	VDDR	I/O	U48BU	At power up this pin determines if the device's spread spectrum modulation feature is enabled or disabled. After power up this pin becomes a reference clock output. A 0 (logic low) enables SSCG and a 1 (logic high) disables SSCG.
27	**REF2/SEL48 #**	VDDR	I/O	U48BU	At power up this pin determine the frequency of the clock at pin 14. If it is LOW, the clock will be 48 MHz, if HIGH the clock will be 24 MHz. After power up this pin will become a reference clock output.
12	**VDDF**	-	P	PWR	Power for fixed clock output buffer.
1, 7, 15, 21, 22	**VSS**	-	P	PWR	Ground pins for device.
28	**VDDR**	-	P	PWR	Power for Reference Oscillator output buffer.

Notes

1. INP3U pins have internal pullup resistors that will guarantee to a logic 1 (high) level if no connection is made to the device's pin. INP3 pins do not contain this function and must be electrically connected to VDD or VSS by external circuitry to ensure a valid logic 1 or 0 is sensed.

Frequency Selection Table

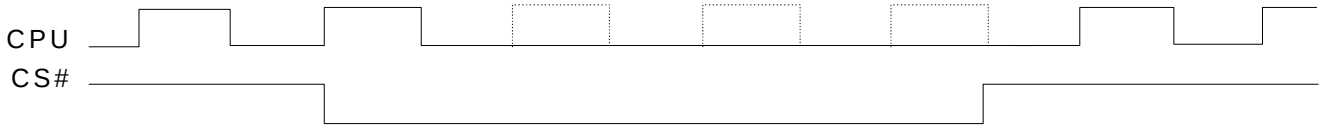
	Outputs					
Descriptions	**48-24M/TS# at Power UP**	**SEL 66/100**	**CPU**	**PCI**	**48M**	**48/24M**
All Outputs Tri-State	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
66 MHz	1	0	66 MHz	33 MHz	48 MHz	24/48 MHz
100 MHz	1	1	100 MHz	33 MHz	48 MHz	24/48 MHz

Power Management Functions

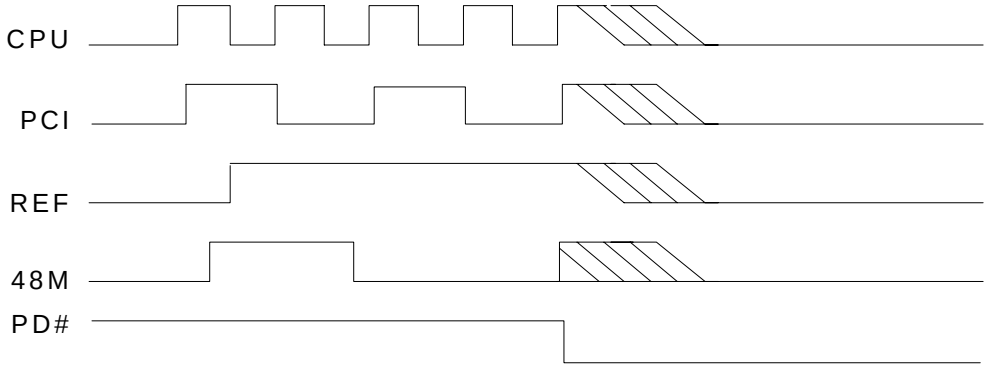
PS#	CS#	PD#	CPU	48M	PCI	PCI_F	VCOs
X	X	0	LOW	LOW	LOW	LOW	OFF
1	0	1	ON	ON	LOW	ON	ON
0	1	1	LOW	ON	ON	ON	ON
0	0	1	LOW	ON	LOW	ON	ON
1	1	1	ON	ON	ON	ON	ON

CS# is an input clock synthesizer. It is used to turn off the CPU clocks for low power operation. CS# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU Clock) and must be internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. CPU clock on latency need to be **2 or 3 CPU clocks** periods in time and CPU clock off latency needs to be **2 or 3 CPU clocks** periods in time.

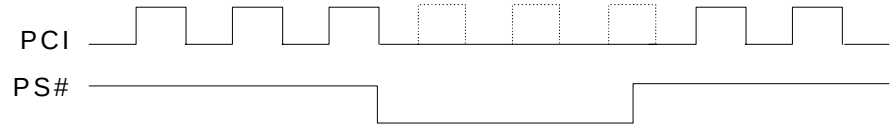
Power Management Timing



CPU STOP TIMING



POWER DOWN TIMING



PCI STOP TIMING

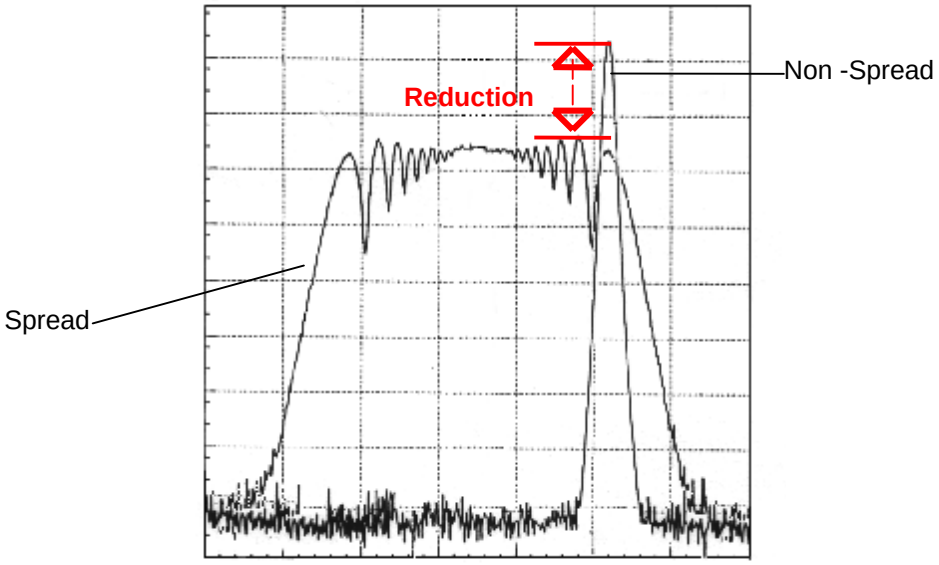
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PD# is active low, all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power-up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. AS# and CS# are considered to be don't cares during the power down operations.

Power Management Timing

		Latency
Signal	**Signal State**	**No. of rising edges of free running PCI CLOCK (PCIF)**
CS#	0 (disabled)	1
	1 (enabled)	1
PD#	1 (cold start/normal operation)	3 mS
	0 (power down)	1

NOTES:
1. Clock on/off latency is defined in the number of rising edges of free running PCI CLOCK between the clock disable goes low/high to the first valid clock comes out of the device.

Spread Spectrum Clocking

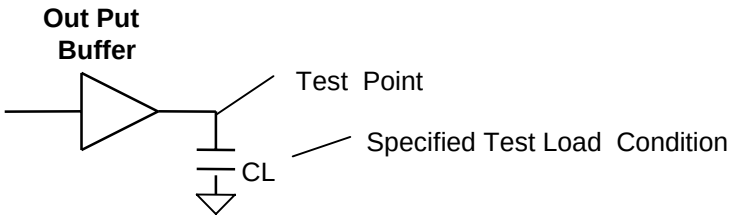


Spectrum Analysis

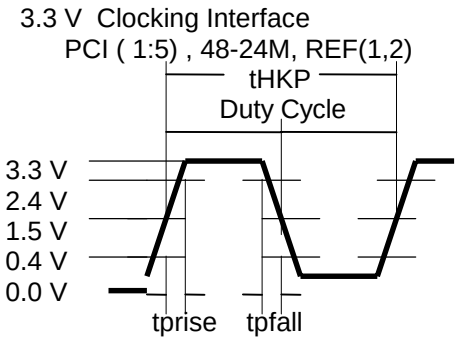
Spectrum Spreading Selection Table

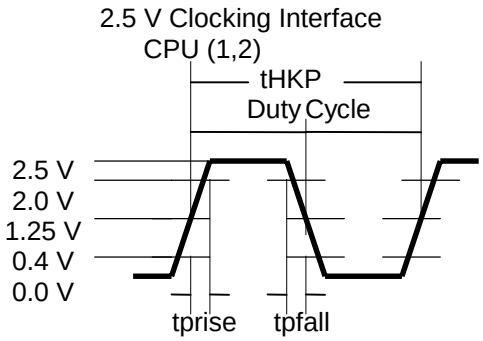
Min (MHz)	Center (MHz)	Max (MHz)	CPU Frequency	% OF FREQUENCY SPREADING	MODE
99.3	99.65	100	100	.7% (-.7% + 0%)	Down Spread
66.13	66.37	66.6	66	.7% (-.7% + 0%)	Down Spread

Test and Measurement Condition



Clock Output Wave form





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Absolute Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin should be constrained to the range:

VSS<(Vin)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0	-	-	Vdc	
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	$Idd2_{66}$	-	-	35	mA	TS# = 1, 100/66 = 0, CS# = 1
(2.5 Volt Supply)	$Idd2_{100}$	-	-	45	mA	TS# = 1, 100/66 = 0, CS# = 1
Dynamic Supply Current	$Idd3_{66}$	-	-	60	mA	TS# = 1, 100/66 = 1, CS# = 1
(3.3 Volt Supply)	$Idd3_{100}$	-	-	60	mA	TS# = 1, 100/66 = 1, CS# = 1
Power Down Mode	$I2.5_{PD}$	-	-	50	µA	PD# at logic low level
Power Down Mode	$I3.3_{PD}$	-	-	200	µA	PD# at logic low level
VDD = VDDF = VDDP=VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0°C to +70°C***						

AC Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	CPU and CPU/2 = Measured at 1.25V all others measured at 1.50V
CPU to PCI Offset	tOFF	1	-	4	ns	CPU = 20 pF load Measured at 1.25V PCI = 30 pF load Measure at 1.50V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	CPU = 20 pF load Measured at 1.25V PCI = 30 pF Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	CPU and CPU/2
ΔPeriod Adjacent Cycles	ΔP	-	-	± 500	pS	PCI Only
VDD = VDDF = VDDP =VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

AC Skew Requirements

Characteristic	Bank Skew	Cycle to Cycle Jitters	VDD	Skew, Jitters Measure Point
CPU	175pS	250pS	2.5V	1.25V
48 MHz	n/a	500pS	3.3V	1.5V
PCI, PCI_F	500pS	500pS	3.3V	1.5V
Ref	n/a	500pS	3.3V	1.5V

Offset Requirements

Characteristic	Bank Offset	Measurement Loads (lumped)	Measure Points
CPU to PCI, PCI-5	1.5-4.0nS CPU leads	CPU @ 20pF, PCI @ 30 pF	CPU @ 1.25V, PCI @ 1.5V

Buffer Characteristics for CPU Outputs

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-82	-		mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}			-67	mA	Vout = 2.375 V
Pull-Down Current Min	IOL_{min}	81	-	-	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	60	mA	Vout = 0.3 V
Rise Time Between 0.4 V and 2.4 V	TR	0.4	-	1.6	nS	20 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	1.6	nS	20 pF Load
VDD = VDDF = VDDP = VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC						

Buffer Characteristics for 48M, 48-24M and REF Outputs

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-29	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-23	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	29	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	27	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	20 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	20 pF Load
VDD = VDDP= VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0ºC to +70ºC***						

Buffer Characteristics for PCI_F, PCI (1:5)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-33	-	-	mA	Vout = 1.0 V
Pull-Up Current Max	IOH_{max}	-	-	-33	mA	Vout = 3.135 V
Pull-Down Current Min	IOL_{min}	30	-	-	mA	Vout = 1.95 V
Pull-Down Current Max	IOL_{max}	-	-	38	mA	Vout = 0.4 V
Rise Time Between 0.4 V and 2.4 V	TR	0.5	-	2.0	nS	30 pF Load
Fall Time Between 0.4 V and 2.4 V	TF	0.5	-	2.0	nS	30 pF Load
VDDP= VDDR =3.3V ±5***%, VDDC = 2.5V*** ±5***%,, TA = 0ºC to +70ºC***						

Crystal and Reference Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		5		pF	Capacitance of XIN and Xout pins
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	note 1
Effective Series resistance	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	7	pF	
X1 and X2 Load	CL		32		pF	internal crystal loading capacitors on each pin (to ground)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.

Budgeting Calculations

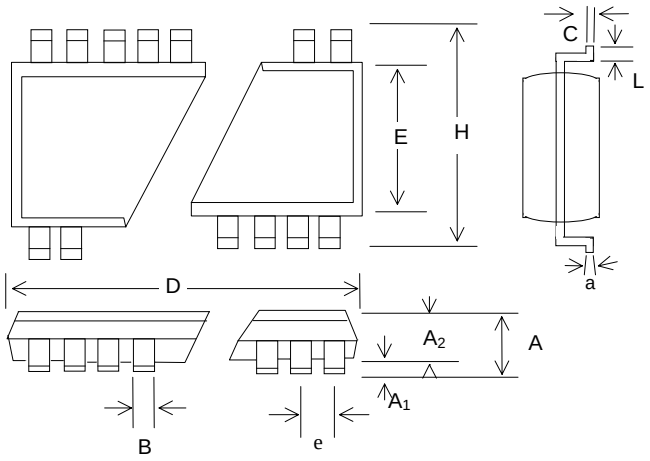
Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF

Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 18.0 pF

the total parasitic capacitance would therefore be = 20.0 pF(matching CL)

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

Package Drawing and Dimensions



28 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.079	-	-	2.0
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.065	0.069	0.073	1.65	1.75	1.85
B	0.009	-	0.015	0.22	-	0.38
C	0.004	-	0.010	0.09	-	0.25
D	0.390	0.402	0.413	6.90	7.20	7.50
E	0.197	0.209	0.220	5.00	5.30	5.60
e	0.026 BSC			0.65 BSC		
H	0.291	0.307	0.323	7.40	7.80	8.20
L	0.022	0.030	0.037	0.55	0.75	0.95
a	0º	-	8º	0º	-	8º

28 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.378	0.382	0.386	9.60	9.70	9.80
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Approved Product

Ordering Information

Part Number	Package Type	Production Flow
IMIC9714AY	28 PIN SSOP	Commercial, 0ºC to +70ºC
IMIC9714AT	28 PIN TSSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
C9714A
Date Code, Lot #

IMIC9714AY

- Package
  Y = SSOP
  T = TSSOP
- Revision
- IMI Device Number